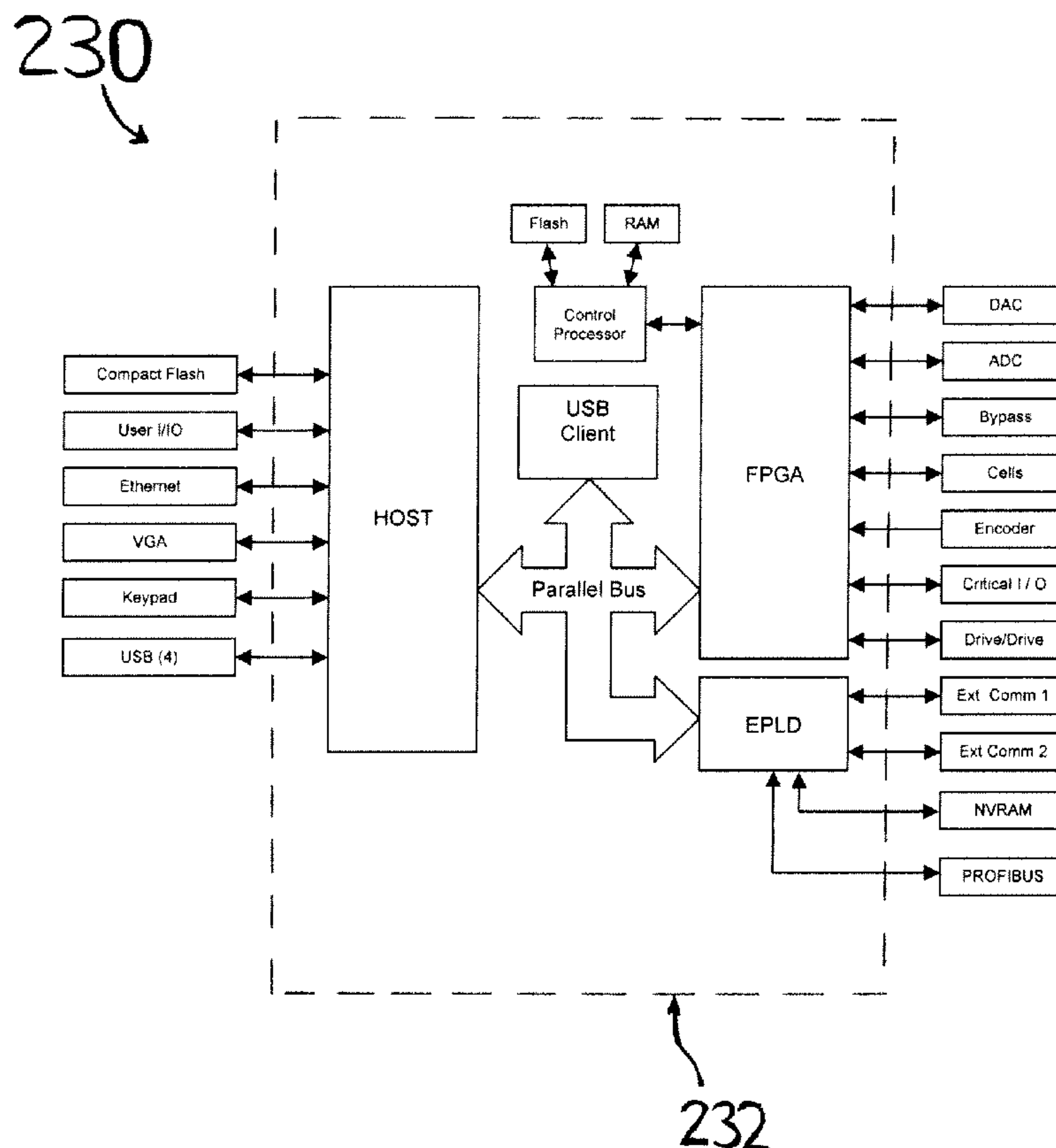




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(57) **Abrégé/Abstract:**

A power supply includes multiple power cells and a master control system in communication with each of the power cells. The master controller includes a control processor configured to receive power cell control information and a host in communication with the control processor wherein the host is configured to receive command and status information.



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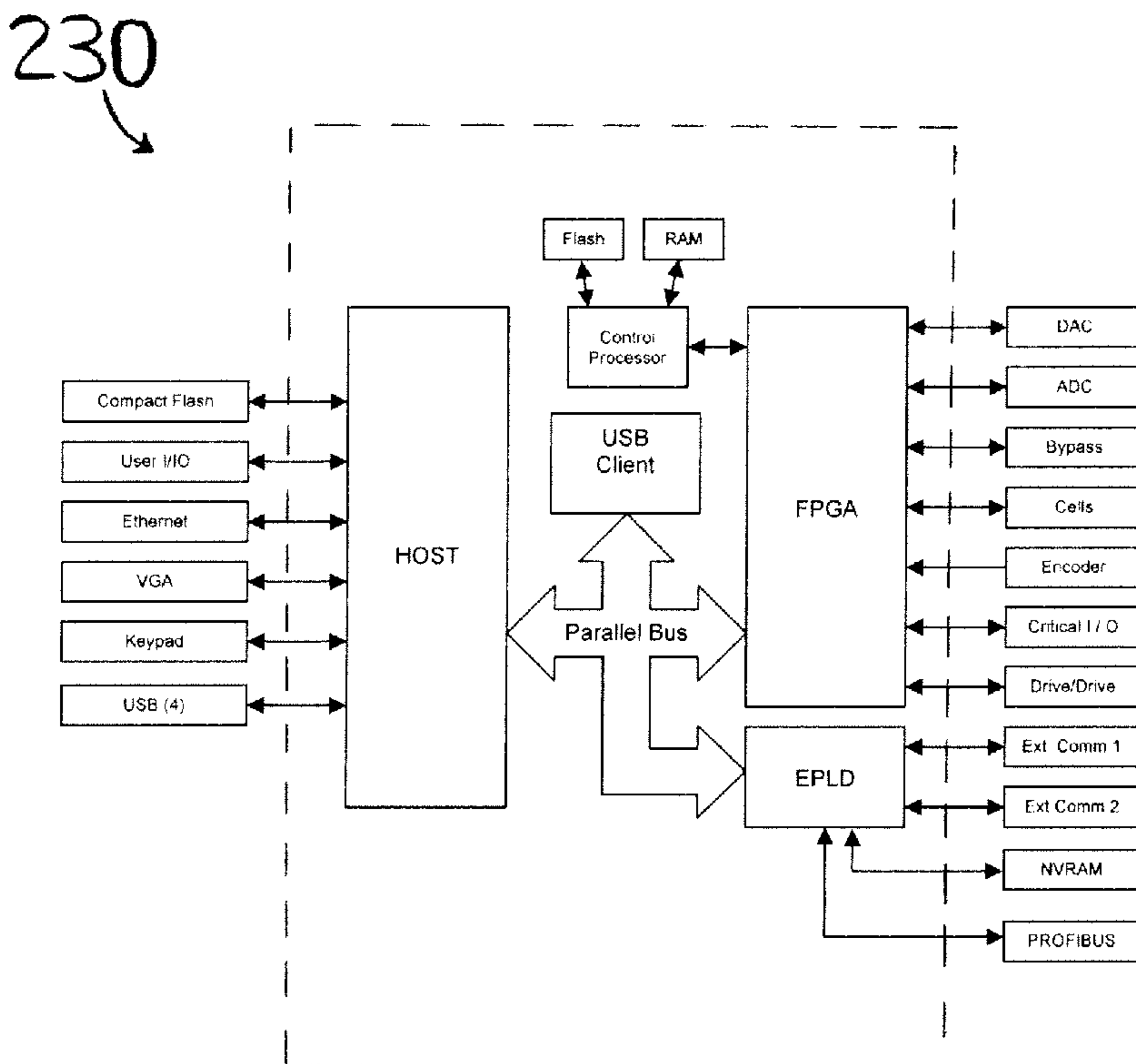


FIG. 3

232

(57) Abstract: A power supply includes multiple power cells and a master control system in communication with each of the power cells. The master controller includes a control processor configured to receive power cell control information and a host in communication with the control processor wherein the host is configured to receive command and status information.

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DUAL PROCESSOR POWER SUPPLY

[0001]

BACKGROUND

[0002] This application discloses an invention that is related, generally and in various embodiments, to a power supply having a dual processor architecture and a method of using a power supply having a dual processor architecture.

[0003] In certain applications, high voltage, high current power supplies utilize modular power cells to process power between a source and a load. Such modular power cells can be applied to a given power supply with various degrees of redundancy to improve the availability of the power supply. A control system may be incorporated to act as an interface between a user of the power supply, the power supply itself, and any load applied to the power supply. For example, FIG. 1 illustrates various embodiments of a power supply (e.g., an AC motor drive) having nine such power cells. The power cells in FIG. 1 are represented by a block having input terminals A, B, and C; and output terminals T1 and T2. In FIG. 1, a transformer or other multi-winding device 110 receives three-phase, medium-voltage power at its primary winding 112, and delivers power to a load 130 such as a three-phase AC

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motor via an array of single-phase inverters (also referred to as power cells). Each phase of the power supply output is fed by a group of series-connected power cells, called herein a “phase-group”.

[0004] The transformer 110 includes primary windings 112 that excite a number of secondary windings 114 – 122. Although primary winding 112 is illustrated as having a star configuration, a mesh configuration is also possible. Further, although secondary windings 114 – 122 are illustrated as having a delta or an extended-delta configuration, other configurations of windings may be used as described in U. S. Patent No. 5,625,545 to *Hammond*. In the example of FIG. 1 there is a separate secondary winding for each power cell. However, the number of power cells and/or secondary windings illustrated in FIG. 1 is merely exemplary, and other numbers are possible. Additional details about such a power supply are disclosed in U.S. Patent No. 5,625,545.

[0005] Any number of ranks of power cells are connected between the transformer 110 and the load 130. A “rank” in the context of FIG. 1 is considered to be a three-phase set, or a group of three power cells established across each of the three phases of the power delivery system. Referring to FIG. 1, rank 150 includes power cells 151-153, rank 160 includes power cells 161-163, and rank 170 includes power cells 171-173. A master control system 195 sends command signals to local controls and receives status/feedback information from each cell over fiber optics or another wired or wireless communications medium 190. Similarly, communications medium 192 is used by the master control system 195 for communications with a user of the power supply. Commands may be received from the user, and any status/feedback information may be transmitted back to the user. As with

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communications medium 190, communications medium 192 may be fiber optics or another wired or wireless medium. It should be noted that the number of cells per phase depicted in FIG. 1 is exemplary, and more than or less than three ranks may be possible in various embodiments.

[0006] FIG. 2 illustrates various embodiments of a power cell 210 which is representative of various embodiments of the power cells of FIG. 1. The power cell 210 includes a three-phase diode-bridge rectifier 212, one or more direct current (DC) capacitors 214, and an H-bridge inverter 216. The rectifier 212 converts the alternating current (AC) voltage received at cell input 218 (i.e., at input terminals A, B and C) to a substantially constant DC voltage that is supported by each capacitor 214 that is connected across the output of the rectifier 212. The output stage of the power cell 210 includes an H-bridge inverter 216 which includes two poles, a left pole and a right pole, each with two switching devices. The inverter 216 transforms the DC voltage across the DC capacitors 214 to an AC output at the cell output 220 (i.e., across output terminals T1 and T2) using pulse-width modulation (PWM) of the semiconductor devices in the H-bridge inverter 216.

[0007] As shown in FIG. 2, the power cell 210 may also include fuses 222 connected between the cell input 218 and the rectifier 212. The fuses 222 may operate to help protect the power cell 210 in the event of a short-circuit failure. According to other embodiments, the power cell 210 is identical to or similar to those described in U.S. Patent No. 5,986,909 and its derivative U.S. Patent No. 6,222,284 to *Hammond and Aiello*.

[0008] Returning to FIG. 1, the master control system 195 includes a single processor which receives operational information (voltage, current, etc.) associated

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with the power supply, processes the information, and based on the processed information, generates commands to control the operation of the power supply.

[0009] In many applications, users and/or owners of a given power supply utilize information associated with the power supply to control the operation of one or more systems external to the power supply, and also utilize information associated with the one or more systems to control the operation of the power supply. For such implementations, the processor receives and processes the operational information associated with the power supply, as well as the information associated with the one or more systems external to the power supply.

[0010] For some of such applications, the single processor can still provide real time control of the power supply. However, for other applications in which there is a requirement of processing and providing of more external information, the single processor is limited in the amount of data that can be processed and provided while still maintaining real time control of the power supply.

SUMMARY

[0011] In one general respect, this application discloses a power supply. The power supply includes multiple power cells and a master control system in communication with each of the power cells. The master controller includes a control processor configured to receive power cell control information and a host in communication with the control processor wherein the host is configured to receive command and status information.

[0012] In another general respect, this application discloses a method for controlling a power supply, the method including receiving drive information at a first processor of the power supply, generating a first control command based on the power

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cell control information, receiving command and status information at a second processor of the power supply, generating an instruction based on the command and status information, communicating the instruction to the first processor and generating a second control command based on the instruction.

5 **[0012a]** According to one aspect of the present invention, there is provided a power supply having a dual processor architecture, comprising: a plurality of power cells; a master control system in communication with each of the power cells, wherein the master control system comprises first and second processors, wherein the first processor comprises a control processor configured to receive power cell control information and to generate operating
10 commands; and wherein the second processor comprises a host in communication with the control processor, wherein the host is configured to receive command and status information; and a field programmable gate array in communication with the control processor, the plurality of power cells and the host, wherein the field programmable gate array is configured to receive operating information from each of the plurality of power cells and the operating
15 commands from the control processor for distribution to the plurality of power cells; a parallel bus connected to the host and field programmable gate array and an electronically programmable logic device connected to the parallel bus.

[0012b] According to another aspect of the present invention, there is provided a
20 method for controlling a power supply having a dual processor architecture, the method comprising: receiving drive information at a first processor of the power supply and transferring the drive information to a second processor of the power supply; generating by the second processor a first control command based on control information, wherein the first control command changes an operation of at least one power cell; receiving command and
25 status information related to the at least one power cell at a third processor of the power supply; generating by the third processor an instruction based on the command and status information; communicating by the third processor the instruction to the second processor; and generating by the second processor a second control command for the at least one power cell based on the instruction; and distributing, by the first processing device, the first control
30 command and the second control command to a plurality of power cells.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Various embodiments of the invention are described herein by way of example in conjunction with the following figures.

[0014] FIG. 1 illustrates various embodiments of a power supply;

[0015] FIG. 2 illustrates various embodiments of a power cell of the power supply of FIG. 1;

[0016] FIG. 3 illustrates various embodiments of a power supply having a dual processor architecture; and

[0017] FIG. 4 illustrates various embodiments of a method for controlling a power supply.

DETAILED DESCRIPTION

[0018] It is to be understood that at least some of the figures and descriptions of the invention have been simplified to focus on elements that are relevant for a clear understanding of the invention, while eliminating, for purposes of clarity, other elements that those of ordinary skill in the art will appreciate may also comprise a portion of the invention. However, because such elements are well known in the art, and because they do not necessarily facilitate a better understanding of the invention, a description of such elements is not provided herein.

[0019] FIG. 3 illustrates various embodiments relating to a master control system in a power supply **230**. The power supply **230** is similar to the multi-cell power supply of FIG. 1, but includes a different master control system **232** that overcomes the limitations of a single processor based system. As shown in FIG. 3, the master control system **232** includes a field programmable gate array (FPGA), a control processor in communication with the FPGA, an electrically programmable logic device (EPLD), and a host. The master control system **232** also includes a parallel bus, and the FPGA, the EPLD, and the host are each connected to the parallel bus.

[0020] According to various embodiments, the FPGA is RAM-based and is configured for communication with one or more digital-to-analog converters (DAC), one or more an analog-to-digital converters (ADC), a power cell bypass system (Bypass), a plurality of power cells (Cell), an encoder, one or more input/output interfaces (Critical I/O), and an internal network (Drive/Drive).

[0021] The digital-to-analog converter may be utilized to convert selected digital signals to analog signals. The one or more analog-to-digital converters may be utilized to convert various analog signals (e.g., voltage amplitudes, current amplitudes, cell temperatures, etc.) to digital signals. The power cell bypass system may be utilized to bypass one or more failed power cells of the power supply **230**. Each power cell of the power supply **230** sends operating information to the FPGA, and receives operation commands via the FPGA. The encoder is associated with a motor (e.g., a motor being driven by the power supply), converts the rotary motion or position of the motor to a code of electronic pulses, and communicates the electronic pulses to the FPGA. The one or more input/output interfaces may be embodied, for example, as switches, potentiometers, etc., and allows a user and/or owner of the

power supply 230 to define how the power supply 230 fits into a larger system. The internal network may be utilized to facilitate the interconnection of multiple power supplies.

[0022] Collectively, the information to or from the DAC, each ADC, the power cell bypass system, each power cell, the encoder, each input/output interface, and the internal network may be considered “drive” information. This drive information may include specific information related to power cell control. In operation, the FPGA performs logic operations on the received drive information, then passes the resultant information to the control processor. The control processor receives the resultant information, processes the resultant information, and based on the processed information, generates operational commands which are passed to the FPGA for distribution to the appropriate interfaces (e.g., an interface to a given ADC, an interface to a given power cell, etc.). Essentially, the FPGA handles internal housekeeping and unique communications to the appropriate interfaces. The control processor may be embodied as a digital signal processor, and together with the FPGA, provides functionality to control the load (e.g., a motor). As shown in FIG. 3, the control processor may be configured for communication with flash memory and/or random access memory (RAM).

[0023] According to various embodiments, the EPLD is in communication with one or more communication modules (e.g., Network 1, Network 2, etc.), a memory device (NVRAM), and one or more ASCII serial devices (e.g., MODBUS, PROFIBUS, etc.). The EPLD is embodied as a flash device. The communication modules may be utilized to allow the power supply to communicate using standard communication protocols. The memory device is a non-volatile memory device, and may be utilized to store information (e.g., parameters, history, etc.) which the user

and/or owner do not want to be lost when power is lost. The one or more serial interfaces allows the EPLD to communicate over a variety of different field buses.

[0024] According to various embodiments, the host includes a processor mounted to a printed circuit board. The host is configured for communication with a compact flash device, a user I/O interface, an Ethernet interface, a video graphics array (VGA) interface, a keypad interface, and one or more USB interfaces. Collectively, the respective interfaces may be considered “non-drive” interfaces. Collectively, any information received from these interfaces may be considered “non-drive” information or command and status information.

[0025] The compact flash device may be utilized to store programs executed by the host. The user I/O may allow a user to request and/or provide information to the host. Such information may include, for example, a status query, configuration of power supply parameters, log information, etc. The Ethernet interface may be embodied as, for example, an RJ45 Ethernet connector, and may be utilized to allow the host to communicate with a device connected thereto. The VGA interface may be embodied as, for example, a DB 15 video connector, and may be utilized to drive a given display connected thereto. The keypad interface may be embodied as, for example, an RS485 interface, and may be utilized to allow the host to communicate with a keypad connected thereto. The one or more USB interfaces may be utilized to allow the host to communicate with one or more devices connected thereto. For example, according to various embodiments, the host may utilize the USB interfaces to communicate with a USB mouse, a USB keyboard, a USB jump drive, etc.

[0026] In operation, the host receives and/or provides the command and status information, executes system programs, controls the non-drive interfaces, controls the modules/devices connected to the EPLD, and communicates information

to the control processor via the parallel bus and the FPGA. The information provided to the control processor may subsequently result in the control processor generating an operation command which produces a change in the operation of the power supply. Such information may include for example, an indication of the number of power cells in the power supply **230**, an indication of how many power cells can be bypassed, an instruction to change the acceleration of a motor connected to the power supply **230** when the motor reaches a particular speed, etc. In contrast to the control processor, the host does not provide motor control functionality.

[0027] According to various embodiments, as shown in FIG. 3, the master control system **232** may further include a universal serial bus (USB) client connected to the parallel bus. The USB client may be utilized to interface tools which run on a separate personal computer connected thereto. For example, a field service technician may utilize the USB client to interface diagnostic tools to the master control system **232**.

[0028] FIG. 4 illustrates various embodiments of a method **300** for controlling a power supply. For purposes of simplicity, the method **300** will be described in the context of its use with the power supply **230**.

[0029] The process begins at block **310**, where power cell control (or “drive”) information is received by the FPGA. From block **310**, the process advances to block **320**, where the FPGA performs a logic operation on the power cell control information and communicates the operated on power cell control information to the control processor. From block **320**, the process advances to block **330**, where the control processor processes the operated on power cell control information, and generates a control command based thereon. From block **330**, the process advances to block **340**, where the control command is communicated to a power cell via the

FPGA. From block 340, the process advances to block 350, where the power cell receives the control command, and changes its operation based thereon.

[0030] From block 350, the process advances to block 360, where the host receives command and status (or “non-drive”) information. From block 360, the process advances to block 370, where the host processes the command and status information, and generates an instruction based on the processed command and status information. From block 370, the process advances to block 380, where the instruction is communicated to the control processor via the parallel bus and the FPGA. From block 380, the process advances to block 330 where the same process as discussed above with respect to blocks 330, 340 and 350 repeats. A control command is generated at block 330 based upon the command and status information. According to various embodiments, the second control command may simply be a modification of the control command generated at block 330 based upon the power cell control information, or may be an entirely different control command. From block 330, the process advances to block 340, where the second control command is communicated to at least one power cell via the FPGA. From block 340, the process advances to block 350, where the at least one power cell receives the second control command, and changes its operation based thereon.

[0031] Although the method 300 is described in the context of a sequential process, it will be appreciated that the described sequence may vary, and some steps of the process may be performed concurrently and/or simultaneously. For example, when the FPGA is receiving the power cell control information at block 310, the host may also be receiving the command and status information at block 360.

[0032] Therefore, while several embodiments of the invention have been described herein by way of example, those skilled in the art will appreciate that

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various modifications, alterations, and adaptations to the described embodiments may be realized without departing from the scope of the invention defined by the appended claims.

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CLAIMS:

1. A power supply having a dual processor architecture, comprising:
a plurality of power cells;
a master control system in communication with each of the power cells,
5 wherein the master control system comprises first and second processors,
wherein the first processor comprises a control processor configured to receive
power cell control information and to generate operating commands; and
wherein the second processor comprises a host in communication with the
control processor, wherein the host is configured to receive command and status information;
10 and
a field programmable gate array in communication with the control processor,
the plurality of power cells and the host, wherein the field programmable gate array is
configured to receive operating information from each of the plurality of power cells and the
operating commands from the control processor for distribution to the plurality of power cells;
15 a parallel bus connected to the host and field programmable gate array and an
electronically programmable logic device connected to the parallel bus.
2. The power supply of claim 1, wherein the field programmable gate array is
configured to distribute the operating commands to an appropriate interface.
3. The power supply of claim 2, wherein the appropriate interface includes at
20 least one of a digital-to-analog converter, an analog-to-digital converter, a power cell bypass,
at least one power cell, an encoder, an input/output interface, and an internal network.
4. The power supply of claim 1, wherein the electronically programmable logic
device is configured to communicate with at least one of a communication module, a memory
device, and one or more serial devices.

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5. The power supply of claim 4, wherein the electronically programmable logic device is configured to communicate over a variety of different field buses via the one or more serial devices.

6. The power supply of claim 1, wherein the electronically programmable logic
5 device is configured to communicate with the host.

7. The power supply of claim 1, wherein the host is configured to communicate with at least one of a compact flash device, a user input/output interface, an Ethernet interface, a video graphics array interface, a keypad interface, and one or more universal serial bus interfaces.

10 8. A method for controlling a power supply having a dual processor architecture, the method comprising:

receiving drive information at a first processor of the power supply and transferring the drive information to a second processor of the power supply;

15 generating by the second processor a first control command based on control information, wherein the first control command changes an operation of at least one power cell;

receiving command and status information related to the at least one power cell at a third processor of the power supply;

20 generating by the third processor an instruction based on the command and status information;

communicating by the third processor the instruction to the second processor;
and

generating by the second processor a second control command for the at least one power cell based on the instruction; and

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distributing, by the first processing device, the first control command and the second control command to a plurality of power cells.

9. The method of claim 8, wherein receiving the drive information comprises receiving the control information via a field programmable gate array of the power supply.

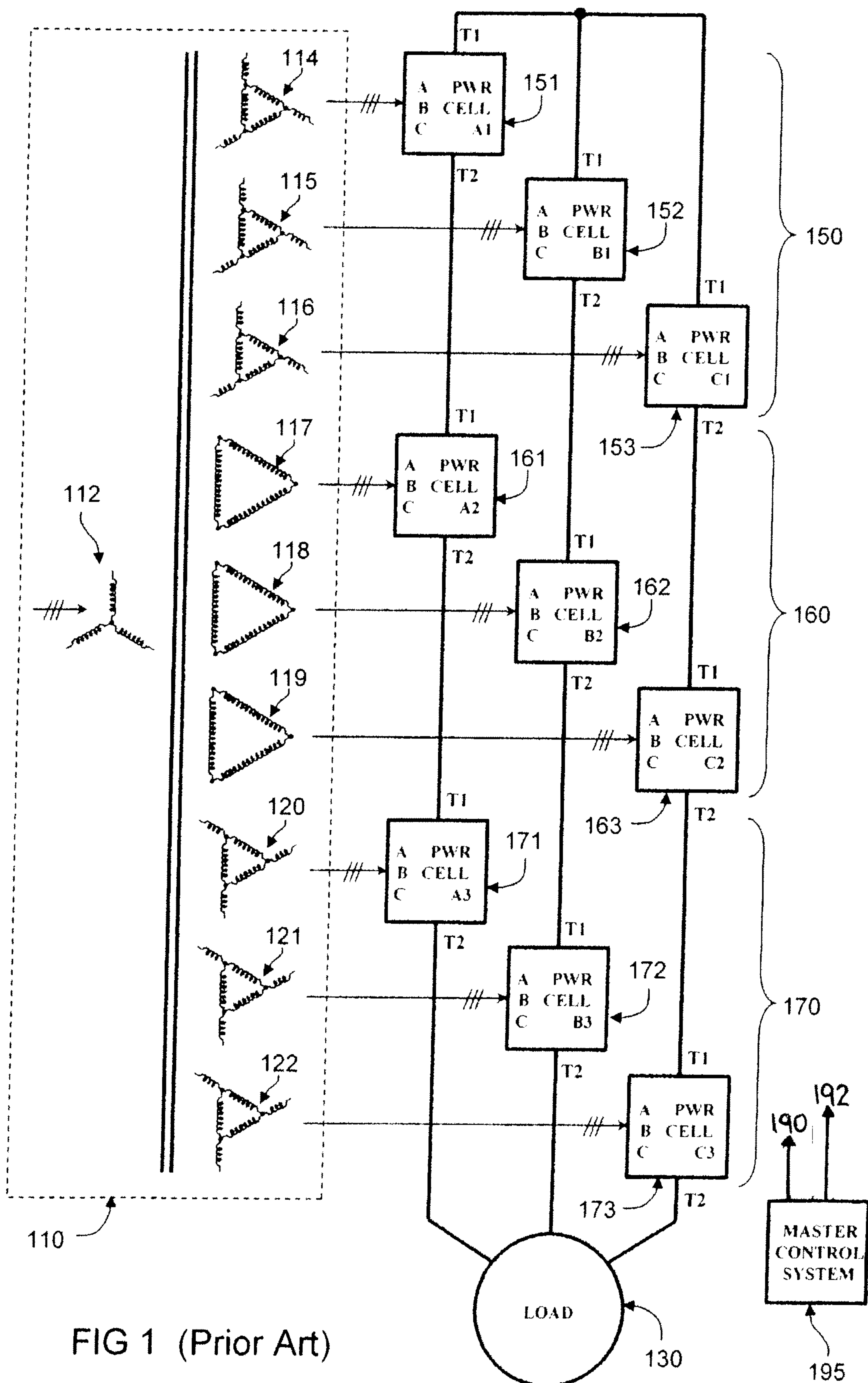
5 10. The method of claim 8, wherein communicating the instruction comprises communicating the instruction from a host processor of the power supply to a field programmable gate array of the power supply.

11. The method of claim 8, further comprising communicating at least one of the following to a power cell of the power supply:

10 the first control command generated based upon the control information; and
the second control command generated based on the received command and status information wherein the second command is at least one of an update to the first command or an entirely new command.

12. The method of claim 11, further comprising changing the operation of the
15 power cell.

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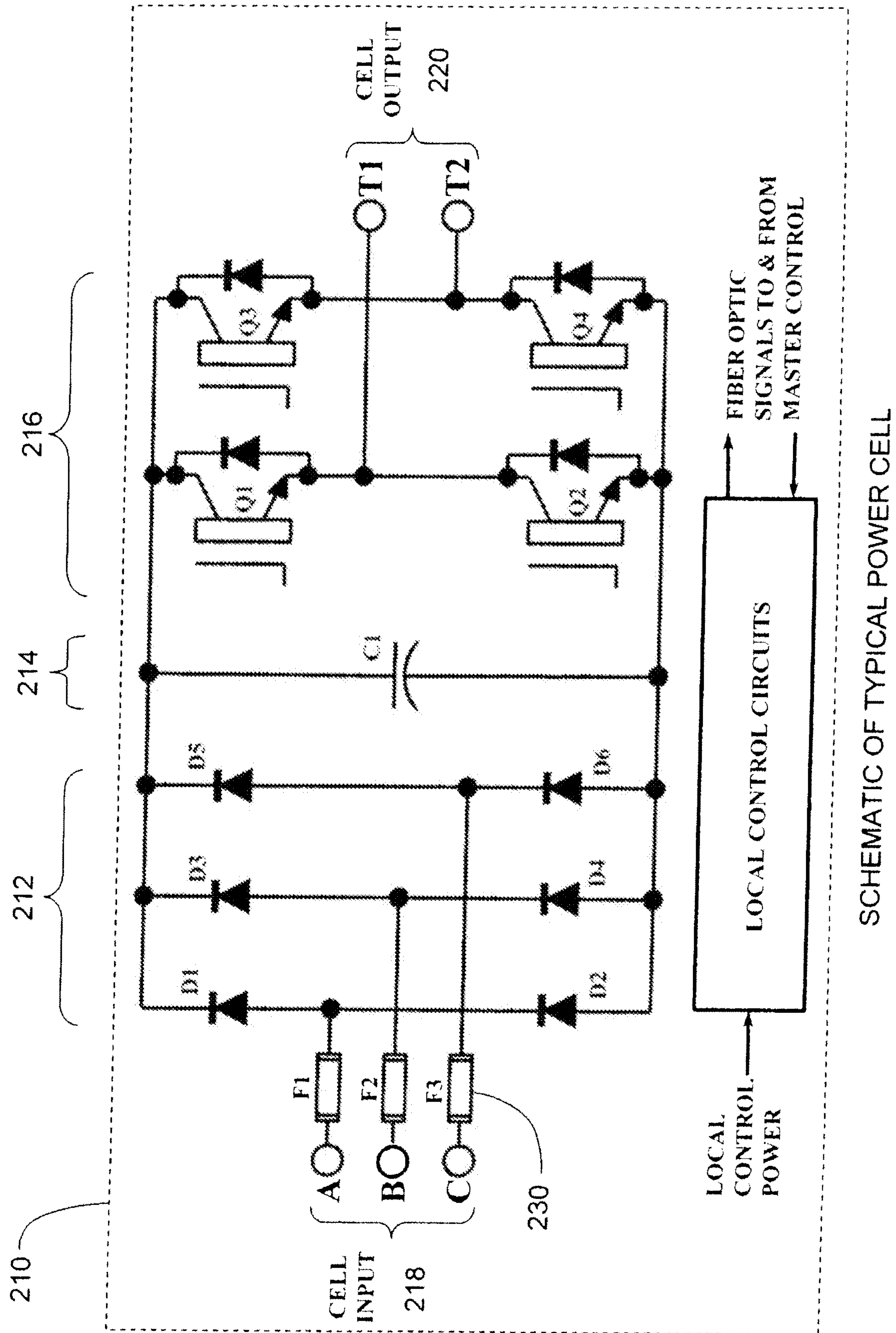


FIG 2 (Prior Art)

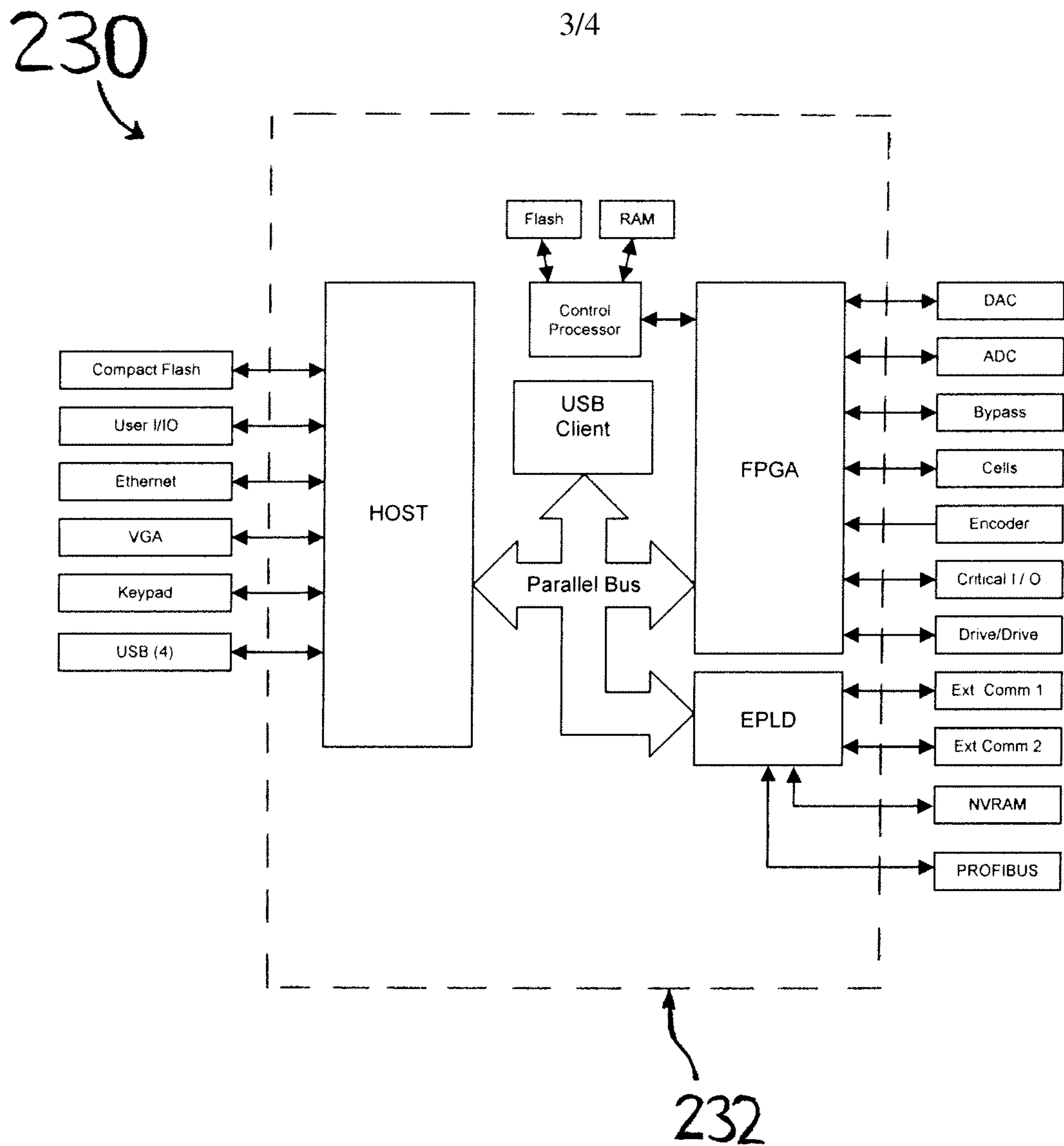
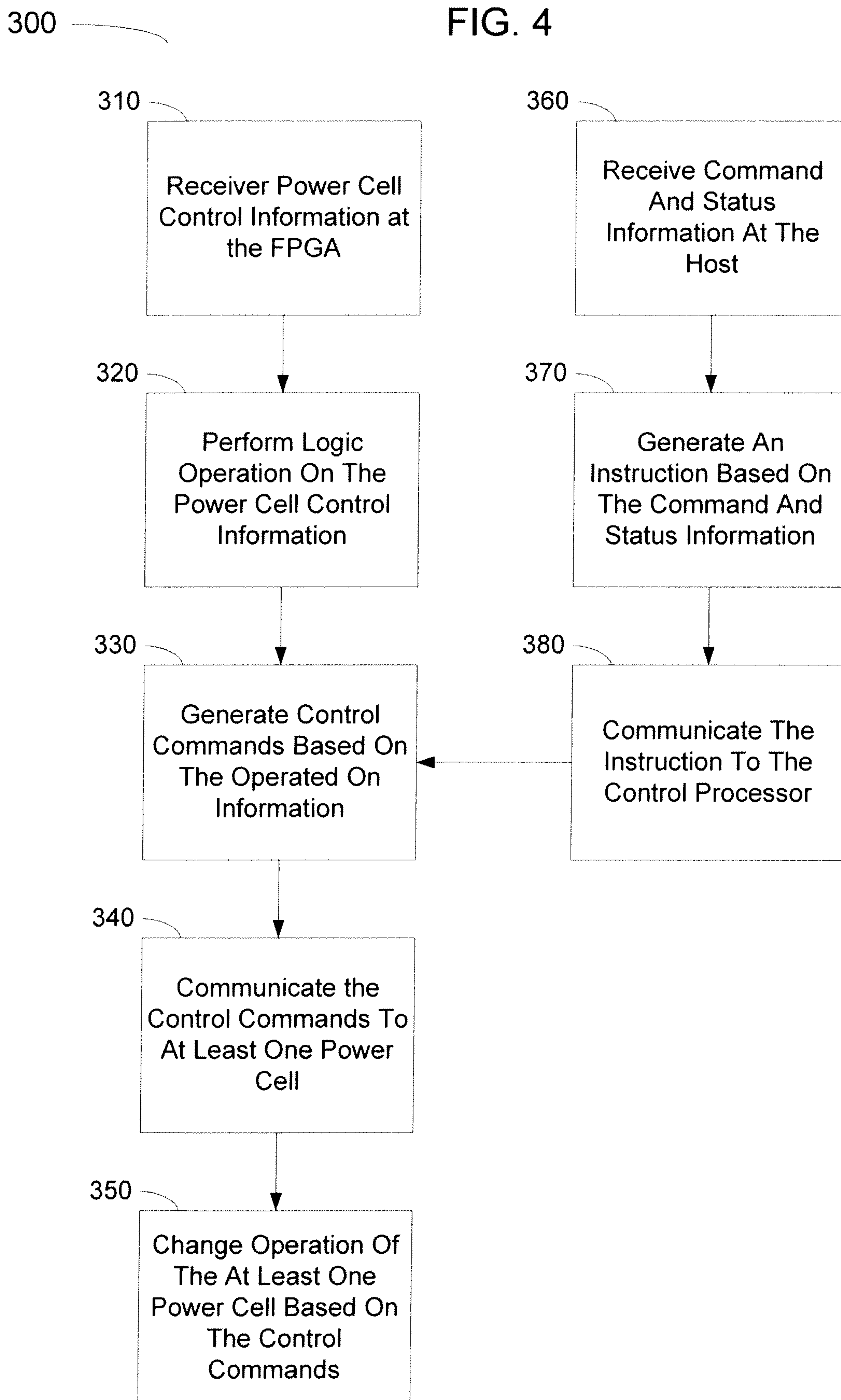


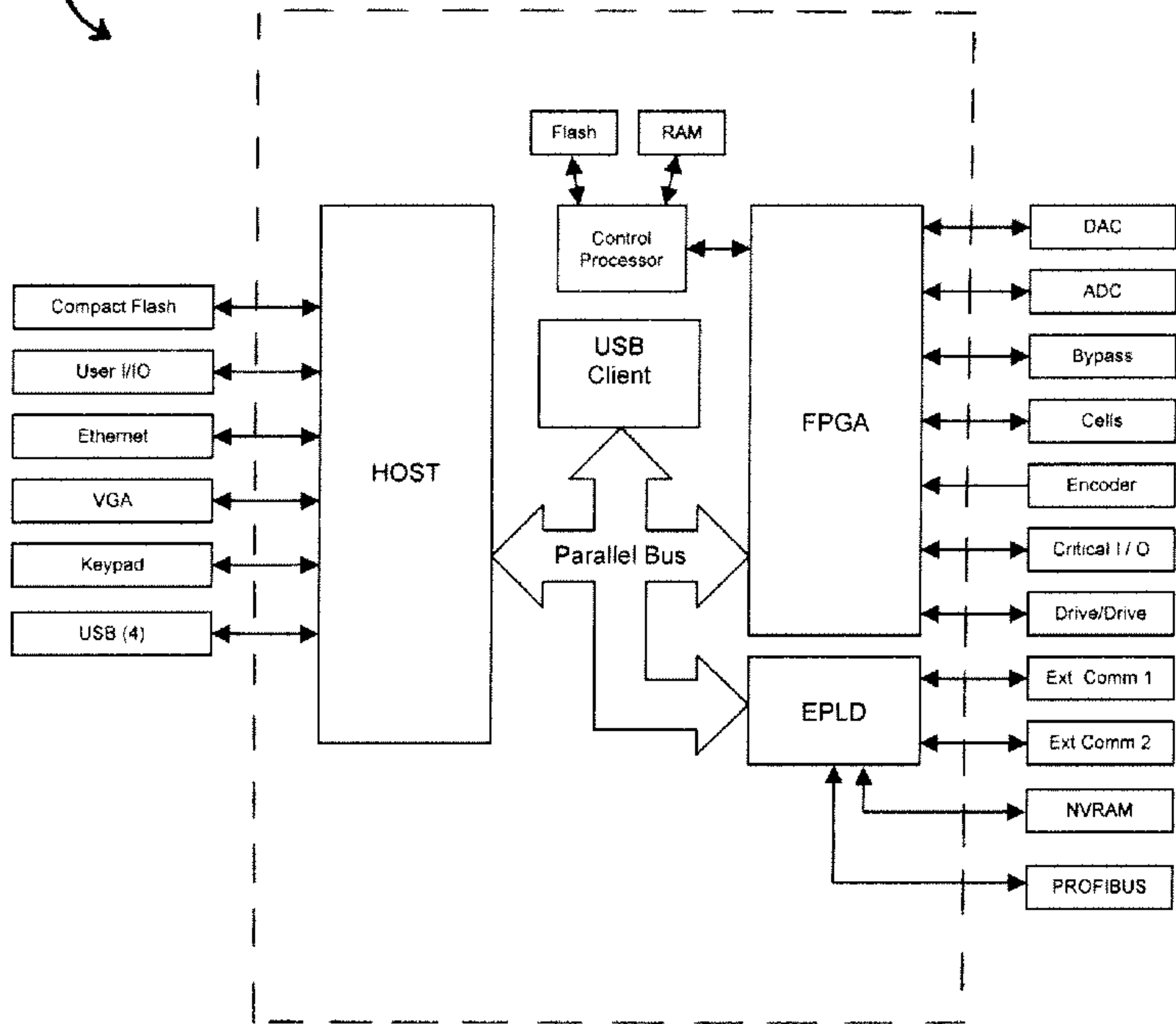
FIG. 3

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FIG. 4



230



232