United States Patent [19]

Bieszczad et al.

[11] **3,835,466**

[45] **Sept. 10, 1974**

[54] **CONTROL OF OPERATOR POSITION DISPLAY**

[75] Inventors: **Edward S. Bieszczad,** Hoffman Estates; **William R. Wedmore,** Glen Ellyn; **John S. Young,** Addison, all of Ill.

[73] Assignee: **GTE Automatic Electric Laboratories Incorporated,** Northlake, Ill.

[22] Filed: **Sept. 14, 1973**

[21] Appl. No.: **397,570**

[52] **U.S. Cl.** ..... **340/334,** 179/27 FF, 340/248 A, 340/332

[51] **Int. Cl.** **G08b 5/36**

[58] **Field of Search** ..... 340/334, 248 A, 332; 179/27 FF

[56] **References Cited**

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3,341,661	9/1967	Curtis	179/27 FF
3,341,816	9/1967	Davis et al.	340/248 A
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3,634,665	1/1972	Carter et al.	340/332 X

Primary Examiner—David L. Trafton

[57] **ABSTRACT**

A display buffer for controlling lighting of lamps and other functions at a plurality of operator positions. There is an arrangement of relay drivers and relays into what are effectively matrix circuits, with current sensors connected to relay driver ground switches using a common resistor for each bit of status codes (including reset), so that current for only one relay should flow through each resistor. The arrangement includes logic associated with the current sensors to monitor the operation and detect failures.

5 Claims, 18 Drawing Figures

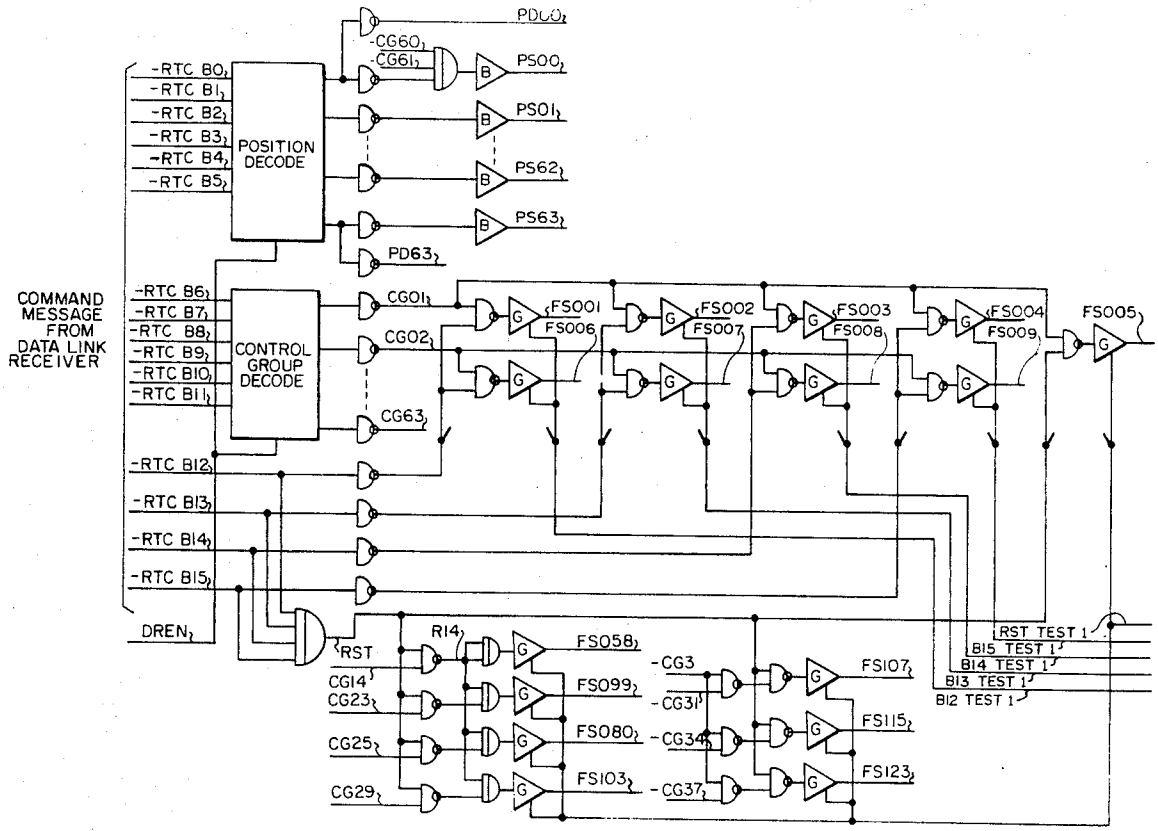
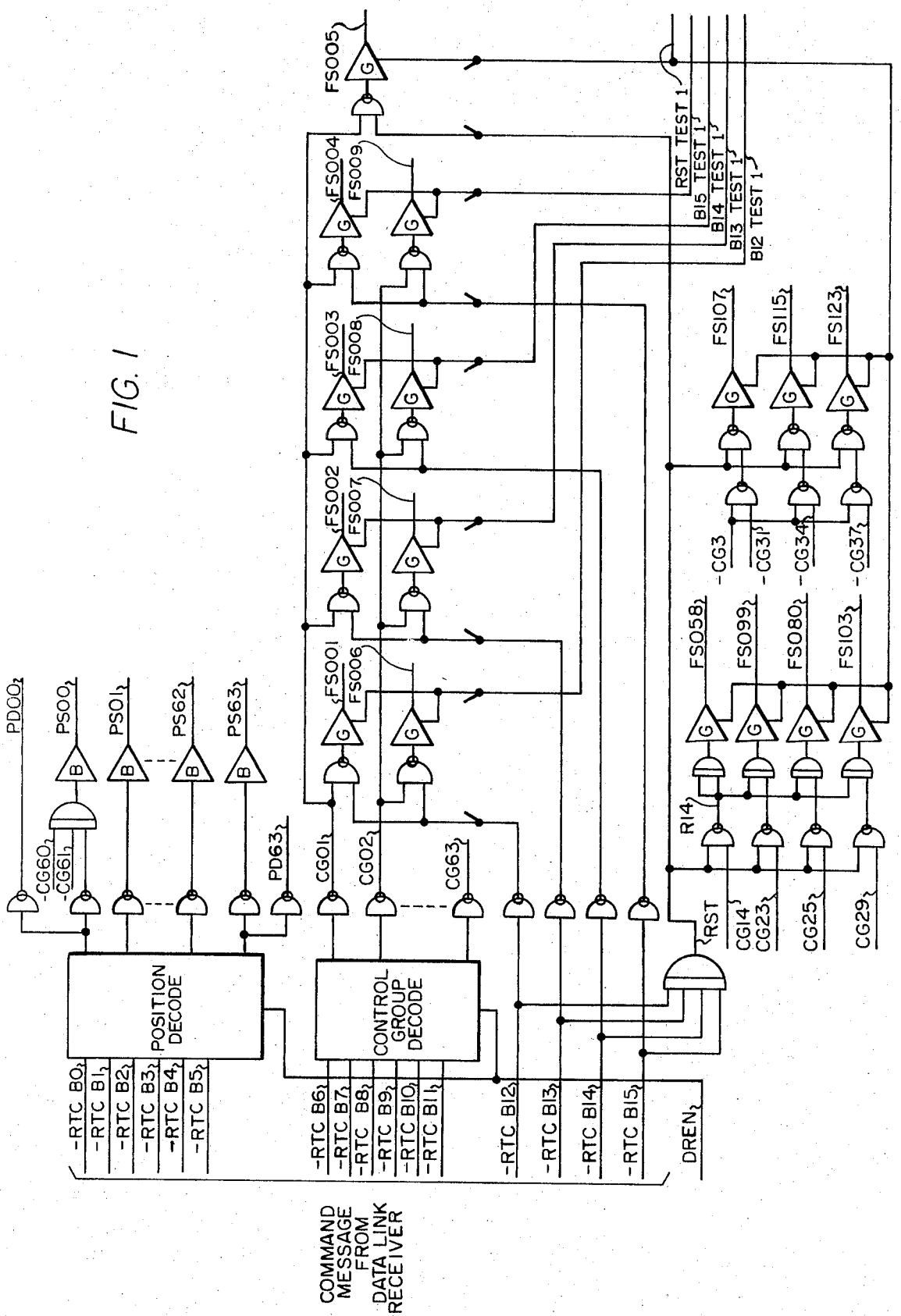


FIG. 1


COMMAND MESSAGE FROM DATA LINK RECEIVER
POSITION DECODE
CONTROL GROUP DECODE
-RTC B0
-RTC B1
-RTC B2
-RTC B3
-RTC B4
-RTC B5
-RTC B6
-RTC B7
-RTC B8
-RTC B9
-RTC B10
-RTC B11
-RTC B12
-RTC B13
-RTC B14
-RTC B15
DREN
PD00
PS00
PS01
PS62
PS63
PD63
-CG60
-CG61
CG01
CG02
CG63
FS001
FS002
FS003
FS004
FS005
FS006
FS007
FS008
FS009
RST TEST 1
BI5 TEST 1
BI4 TEST 1
BI3 TEST 1
BI2 TEST 1
FS107
FS115
FS123
-CG3
-CG31
-CG34
-CG37
FS058
FS099
FS080
FS103
R14
RST
CG14
CG23
CG25
CG29

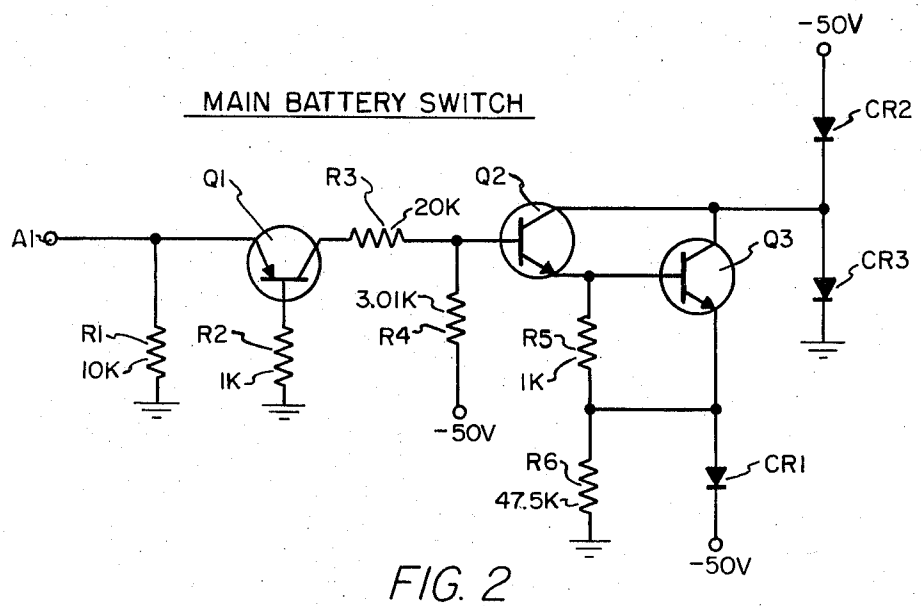

MAIN BATTERY SWITCH
-50V
CR2
Q1
R3
20K
Q2
A1
Q3
CR3
3.01K
R1
10K
R2
1K
R4
R5
1K
-50V
R6
47.5K
CR1
-50V

FIG. 2

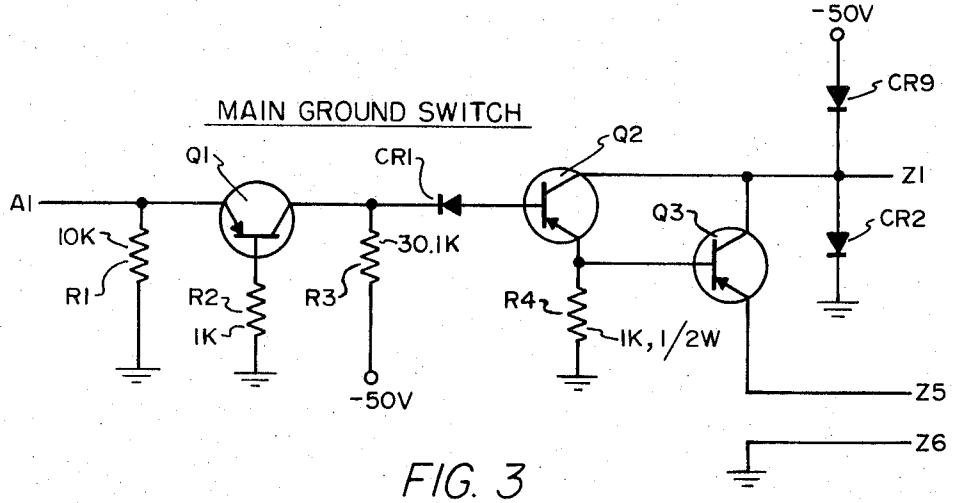

-50V
CR9
MAIN GROUND SWITCH
Q1
CR1
Q2
Z1
A1
Q3
CR2
10K
30.1K
R1
R2
R3
R4
1K, 1/2W
1K
-50V
Z5
Z6

FIG. 3

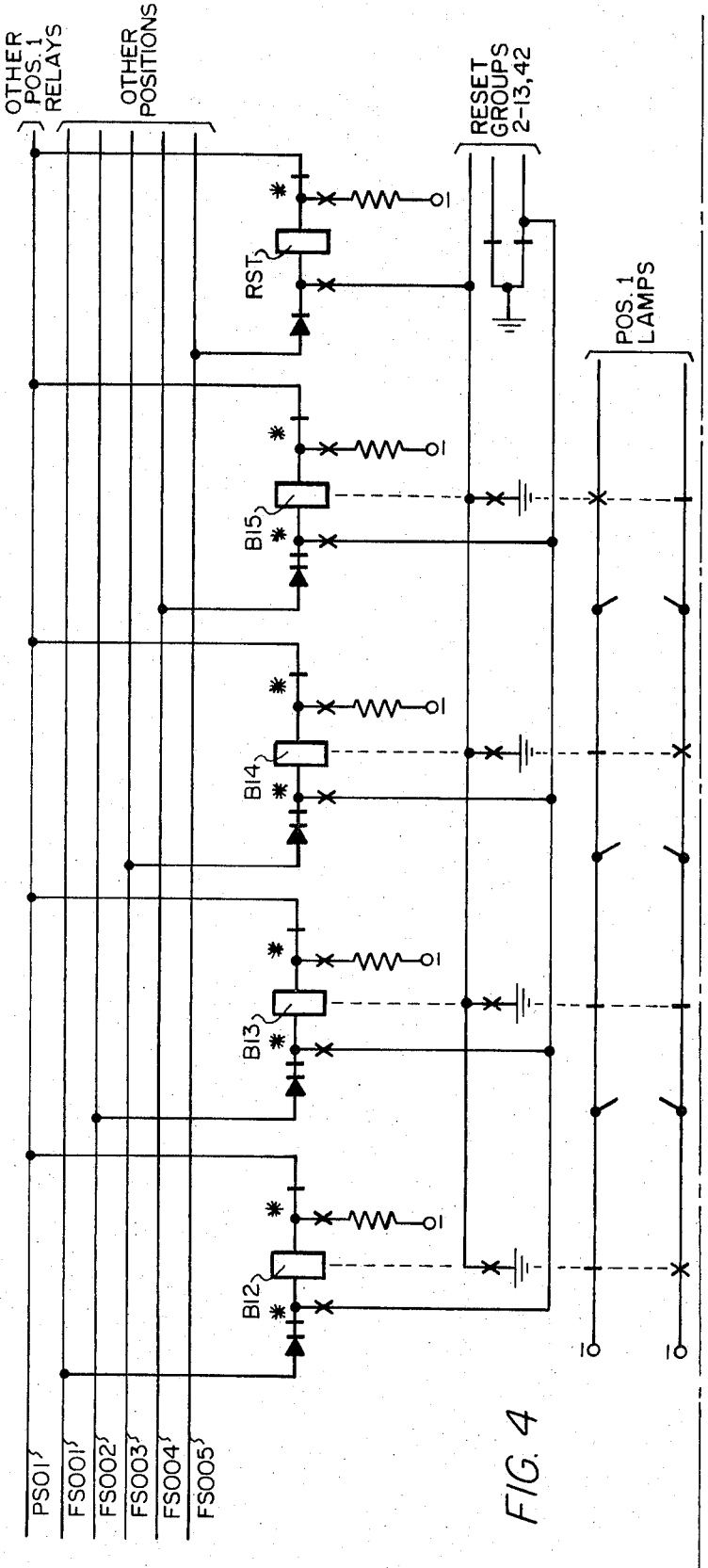

OTHER POS. 1 RELAYS
OTHER POSITIONS
RESET GROUPS 2-13,42
POS. 1 LAMPS
RST
B15
B14
B13
B12
PS01
FS001
FS002
FS003
FS004
FS005

FIG. 4

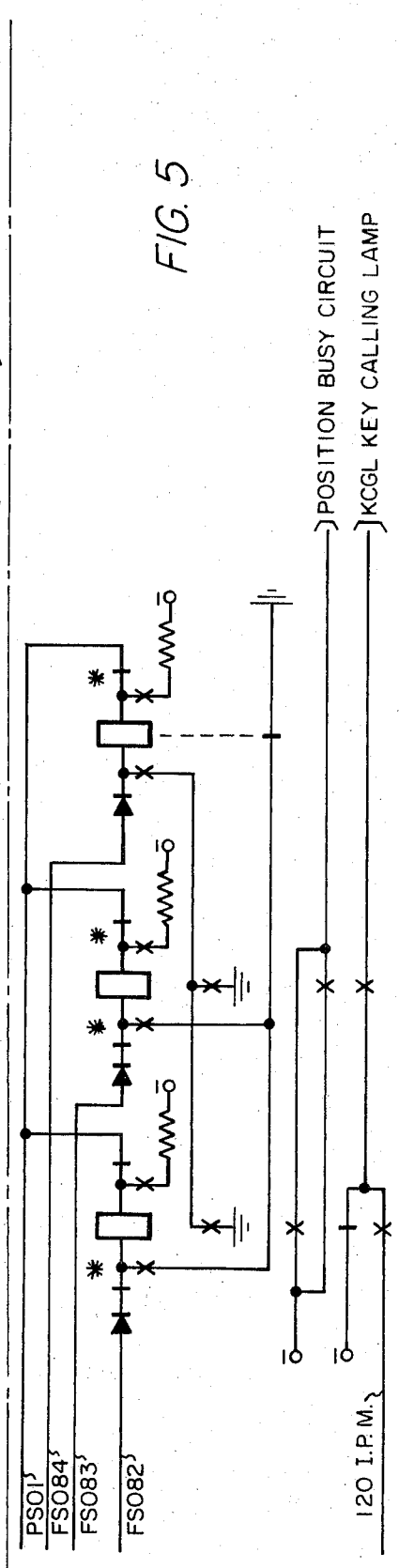

POSITION BUSY CIRCUIT
KCGL KEY CALLING LAMP
PS01
FS084
FS083
FS082
120 I.P.M.

FIG. 5

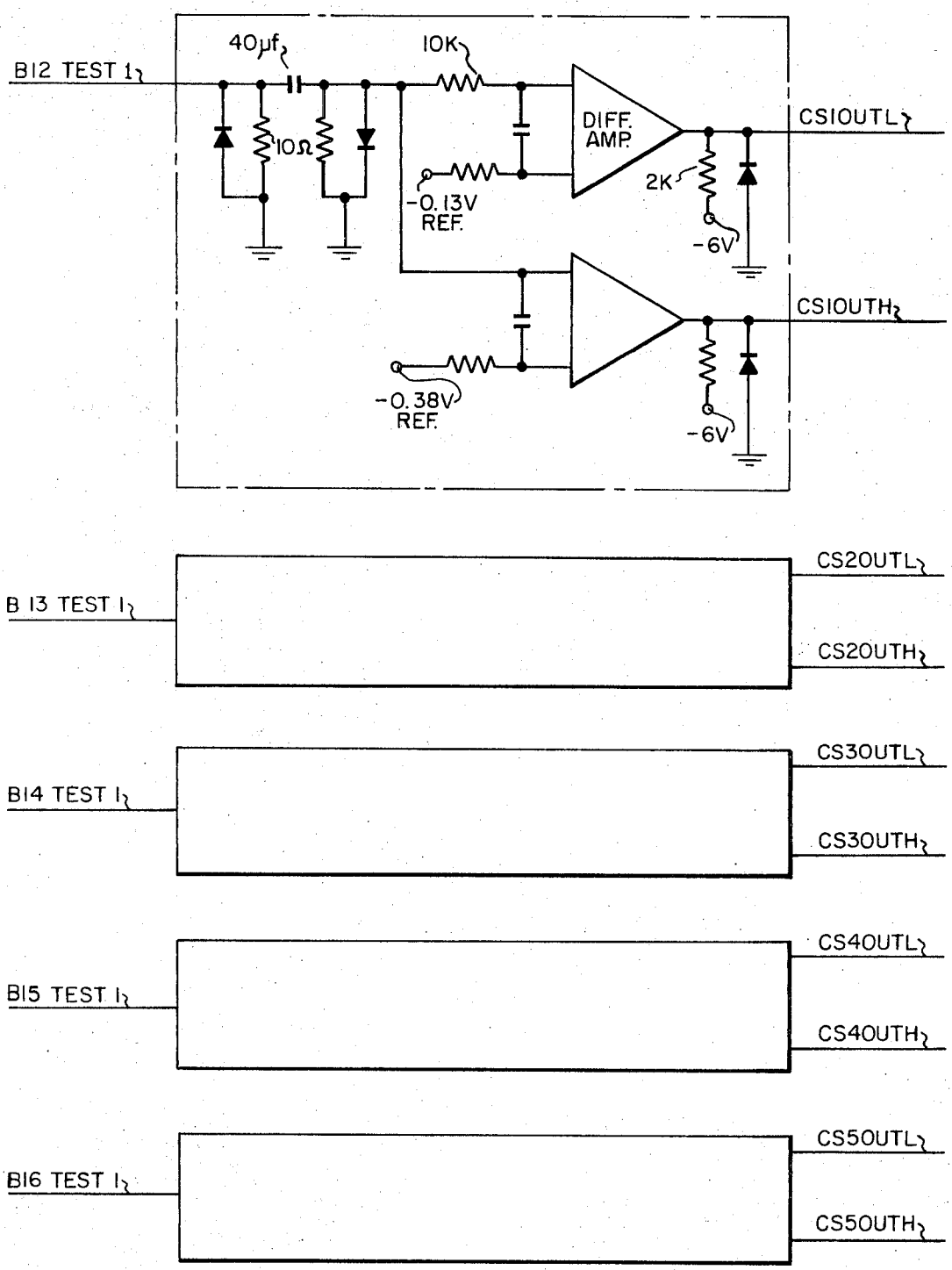
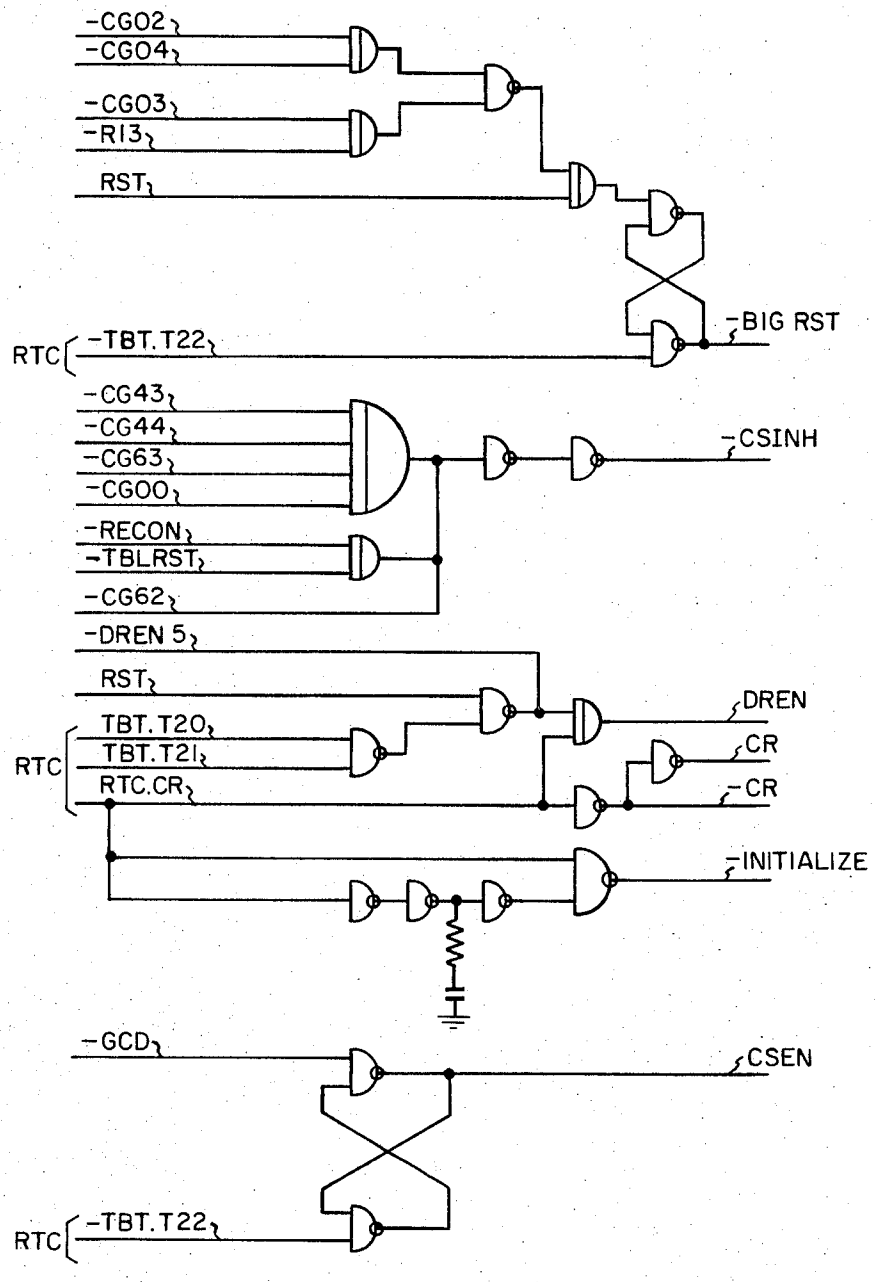

B12 TEST 1
40μf
10K
10Ω
DIFF. AMP.
2K
-0.13V REF.
-6V
CS1OUTL
CS1OUTH
-0.38V REF.
-6V
B 13 TEST 1
CS2OUTL
CS2OUTH
B14 TEST 1
CS3OUTL
CS3OUTH
B15 TEST 1
CS4OUTL
CS4OUTH
B16 TEST 1
CS5OUTL
CS5OUTH

FIG. 6

FIG. 7


-CG02
-CG04
-CG03
-RI3
RST
-BIG RST
RTC
-TBT.T22
-CG43
-CG44
-CG63
-CG00
-CSINH
-RECON
-TBLRST
-CG62
-DREN 5
RST
DREN
TBT.T20
TBT.T21
RTC
RTC.CR
CR
-CR
-INITIALIZE
-GCD
CSEN
RTC
-TBT.T22

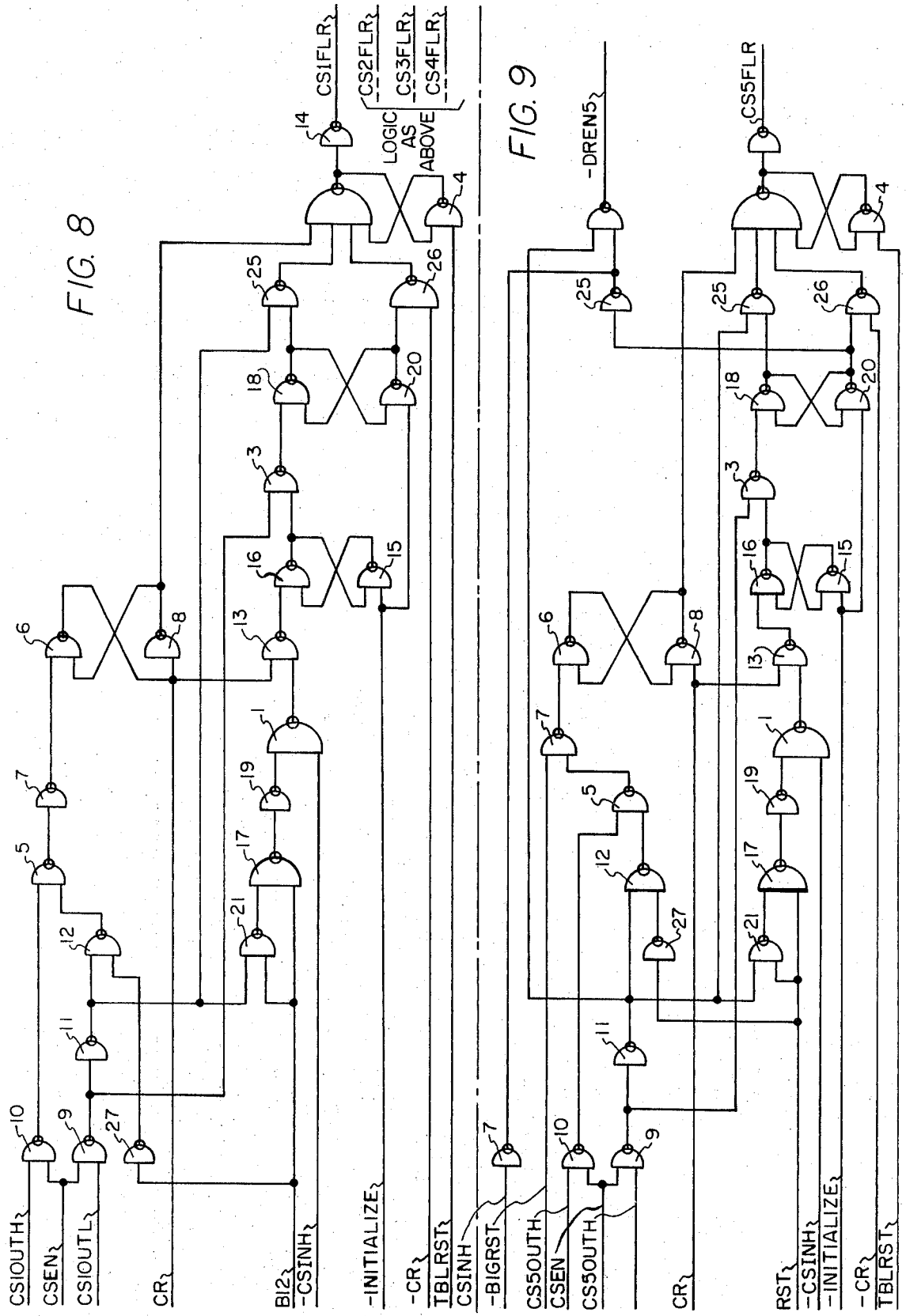

CSIOUTH
CSEN
CSIOUTL
CR
BI2
-CSINH
-INITIALIZE
-CR
TBLRST
CSINH
-BIGRST
CS5OUTH
CSEN
CS5OUTH
CR
RST
-CSINH
-INITIALIZE
-CR
TBLRST
CS1FLR
CS2FLR
CS3FLR
CS4FLR
LOGIC AS ABOVE
-DREN5
CS5FLR

FIG. 8

FIG. 9

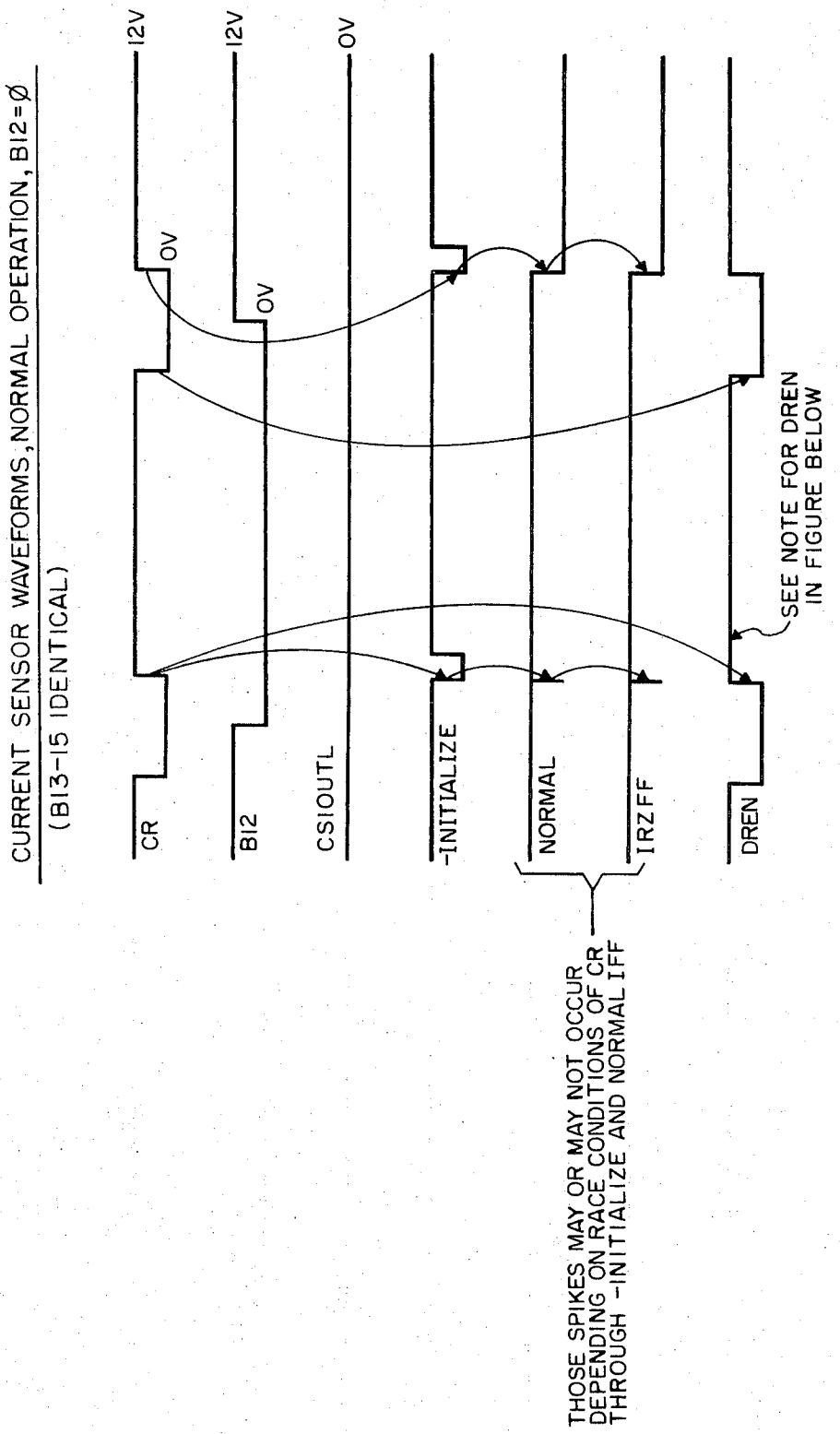

CURRENT SENSOR WAVEFORMS, NORMAL OPERATION, BI2=Ø
(BI3-I5 IDENTICAL)
I2V
0V
I2V
0V
0V
CR
BI2
CSIOUTL
-INITIALIZE
NORMAL
IRZFF
DREN
SEE NOTE FOR DREN IN FIGURE BELOW
THOSE SPIKES MAY OR MAY NOT OCCUR DEPENDING ON RACE CONDITIONS OF CR THROUGH -INITIALIZE AND NORMAL IFF

FIG. 10

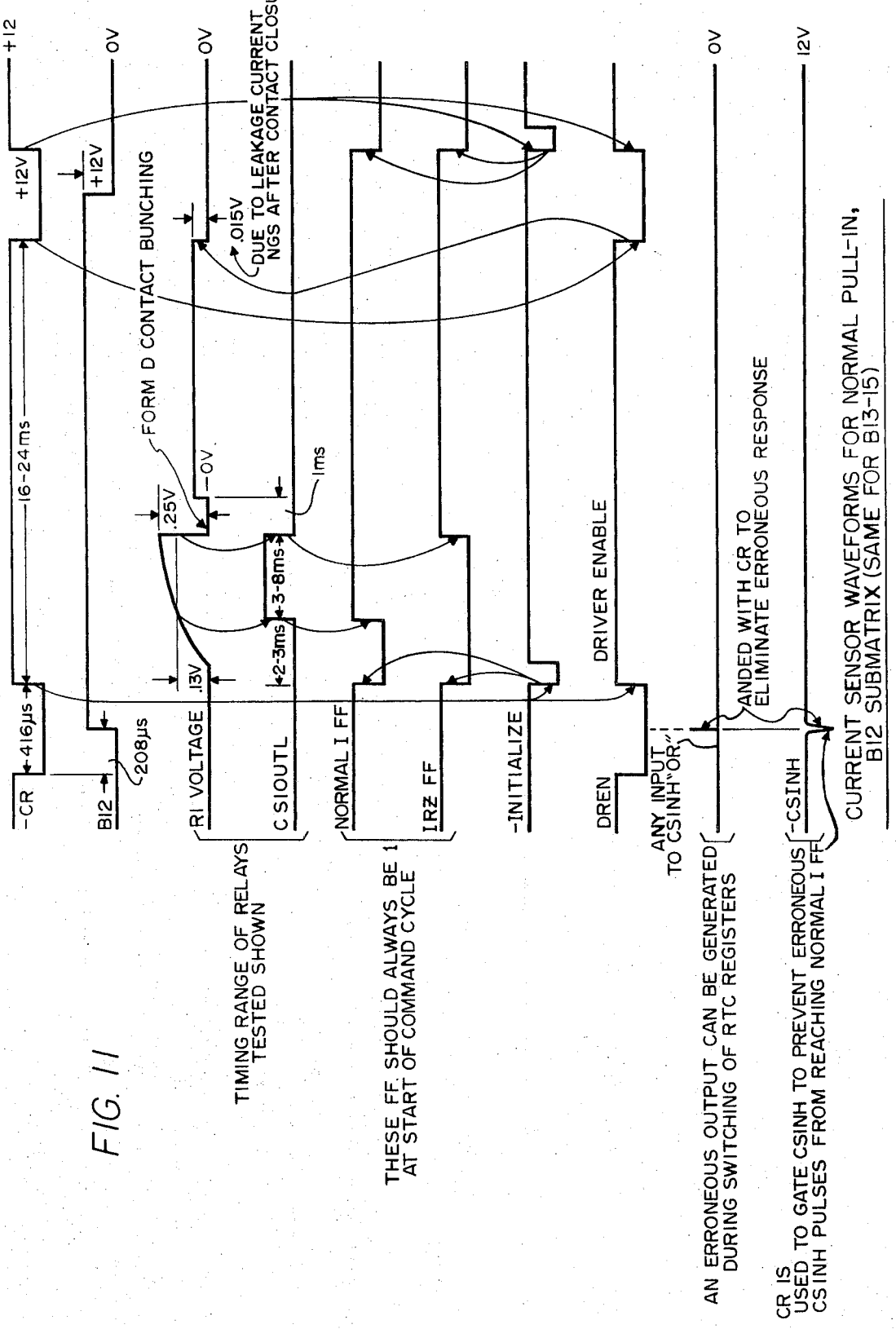

+12
0V
0V
+12V
+12V
.015V
DUE TO LEAKAGE CURRENT IN NGS AFTER CONTACT CLOSURE.
FORM D CONTACT BUNCHING
16-24ms
-CR
416μs
B12
208μs
RI VOLTAGE
.13V
.25V
0V
C SIOUTL
2-3ms
3-8ms
1ms
NORMAL I FF
IRZ FF
-INITIALIZE
DRIVER ENABLE
DREN
ANY INPUT TO CSINH "OR"
0V
ANDED WITH CR TO ELIMINATE ERRONEOUS RESPONSE
12V
-CSINH
CURRENT SENSOR WAVEFORMS FOR NORMAL PULL-IN, B12 SUBMATRIX (SAME FOR B13-15)
TIMING RANGE OF RELAYS TESTED SHOWN
THESE FF. SHOULD ALWAYS BE 1 AT START OF COMMAND CYCLE
AN ERRONEOUS OUTPUT CAN BE GENERATED DURING SWITCHING OF RTC REGISTERS
CR IS USED TO GATE CSINH TO PREVENT ERRONEOUS CSINH PULSES FROM REACHING NORMAL I FF

FIG. 11

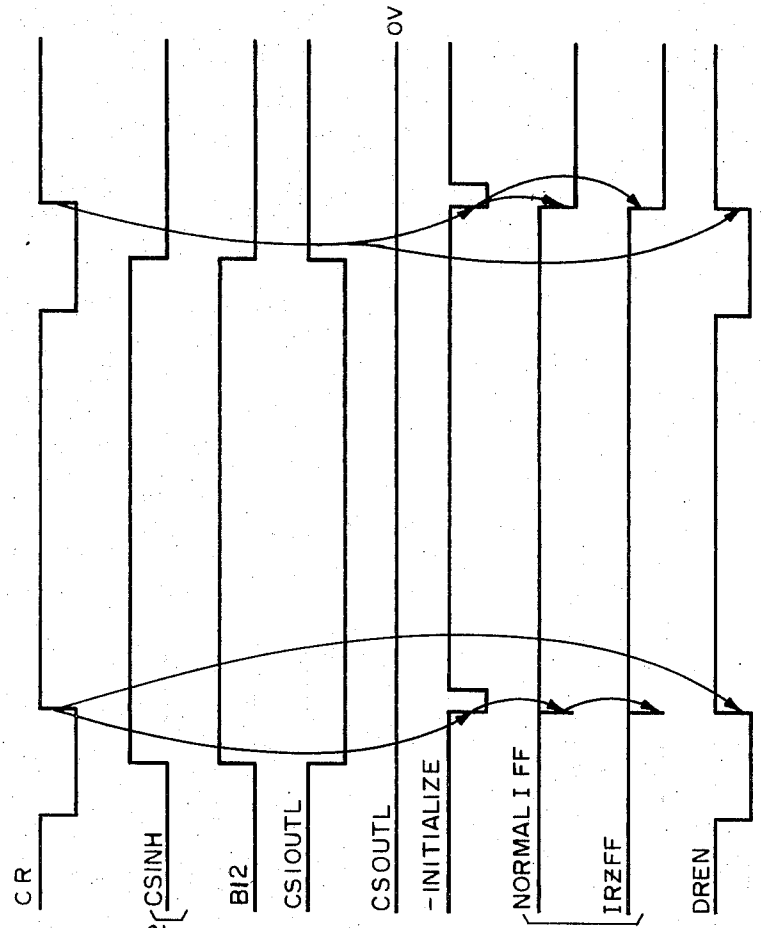


FIG. 12

CURRENT SENSOR WAVEFORMS NORMAL OPERATION, NON-RELAY PULL-IN COMMAND. (SAME FOR B13-15)

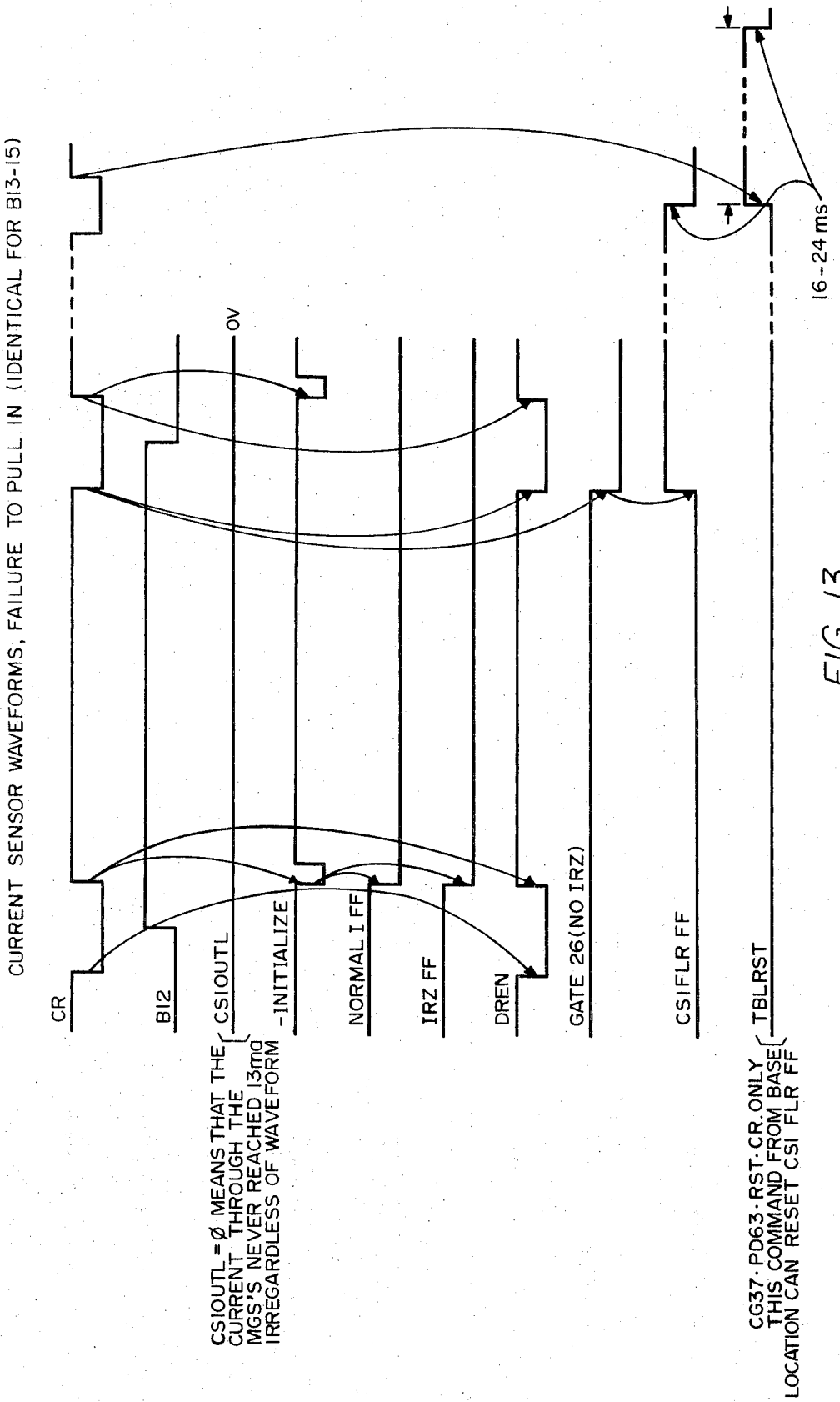

CURRENT SENSOR WAVEFORMS, FAILURE TO PULL IN (IDENTICAL FOR BI3-I5)
CR
BI2
CSIOUTL
0V
-INITIALIZE
NORMAL I FF
IRZ FF
DREN
GATE 26(NO IRZ)
CSIFLR FF
TBLRST
16-24 ms
CSIOUTL = Ø MEANS THAT THE CURRENT THROUGH THE MGS'S NEVER REACHED I3ma IRREGARDLESS OF WAVEFORM
CG37·PD63·RST·CR ONLY THIS COMMAND FROM BASE LOCATION CAN RESET CSI FLR FF

FIG. 13

A NOTCH IN WAVEFORM OCCURS WHENEVER A RELAY PULL-IN. A TWO RELAY PULL-IN. CASE IS SHOWN ALTHOUGH ANY NUMBER COULD OCCUR WITH DIGITAL WAVEFORMS BEING THE SAME. BI2 IS SHOWN=1 THUS VALID AND AN INVALID PULL-IN ARE SHOWN. A MULTIPLE PULL IN WITH BI2=Ø WOULD HAVE SAME WAVEFORMS AS FIG.15 IN VALID SINGLE PULL-IN.

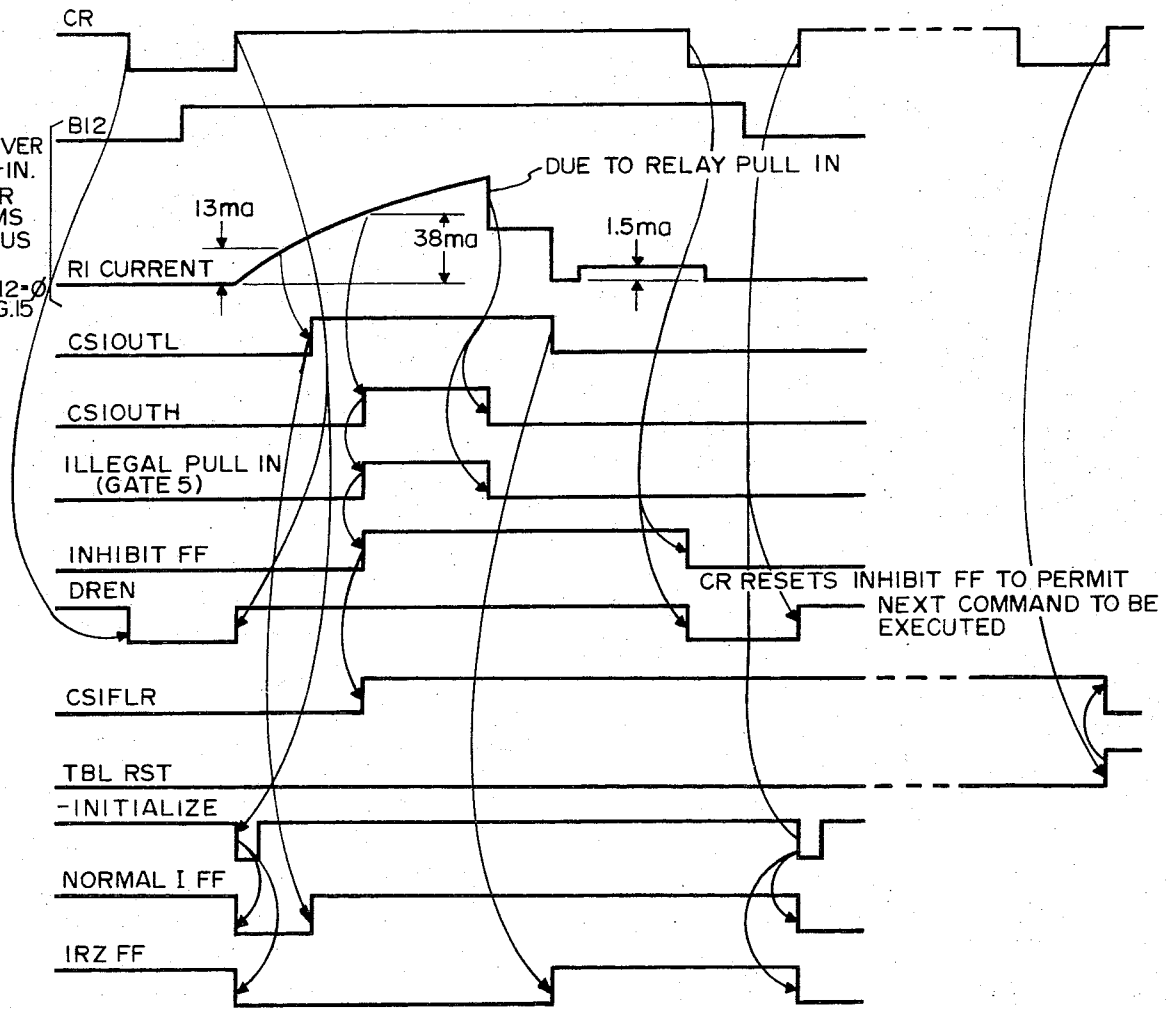
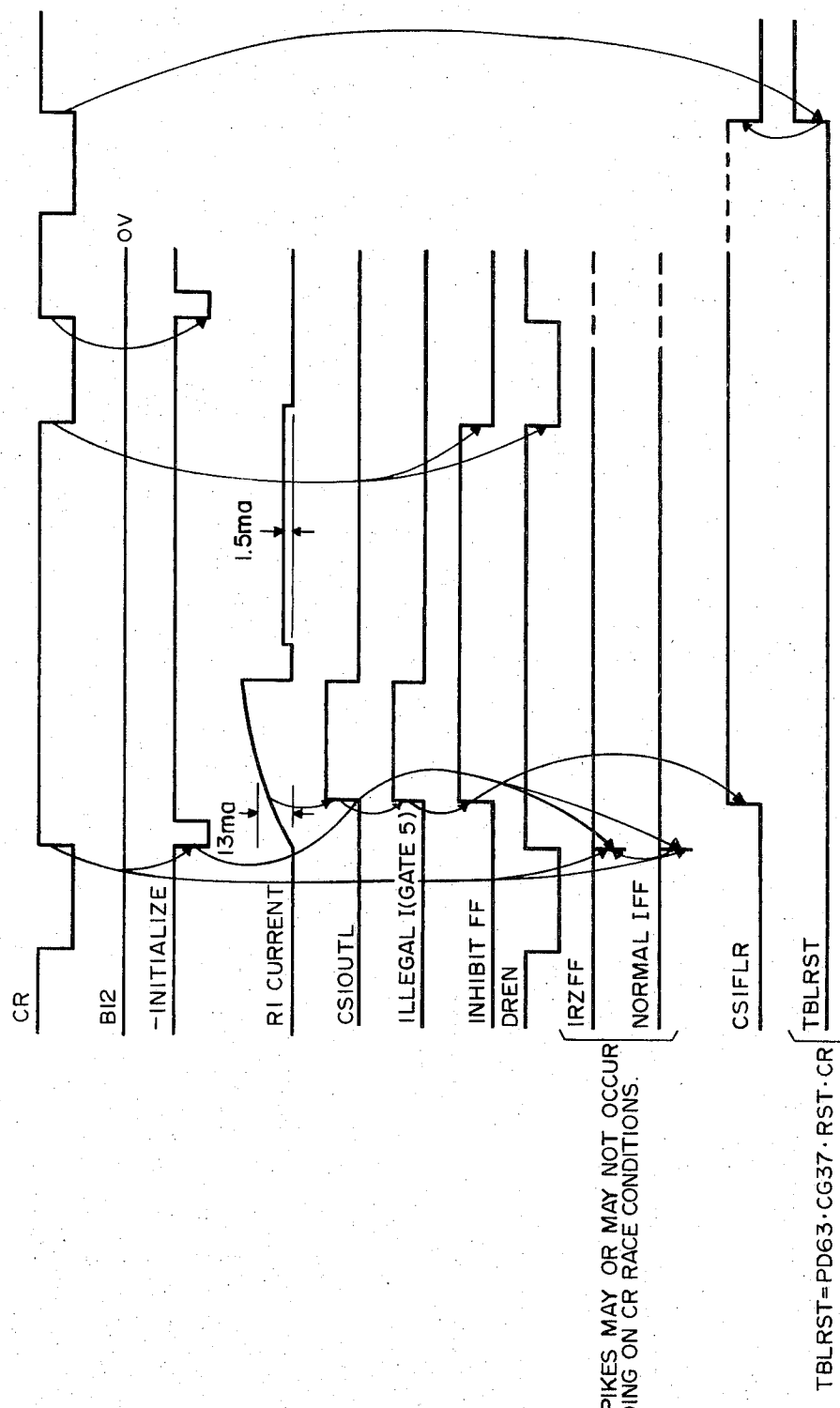


FIG. 14

BI2 CURRENT SENSOR WAVEFORMS INVALID MULTIPLE PULL-IN
(BI3-15 IDENTICAL, RST IDENTICAL IF BIGRST 0, SEE FIG.18 FOR CASE OF BIG RST=1)



BI2 CURRENT SENSOR WAVEFORMS, ILLEGAL SINGLE PULL-IN (SAME FOR BI3-15, RST)

FIG. 15

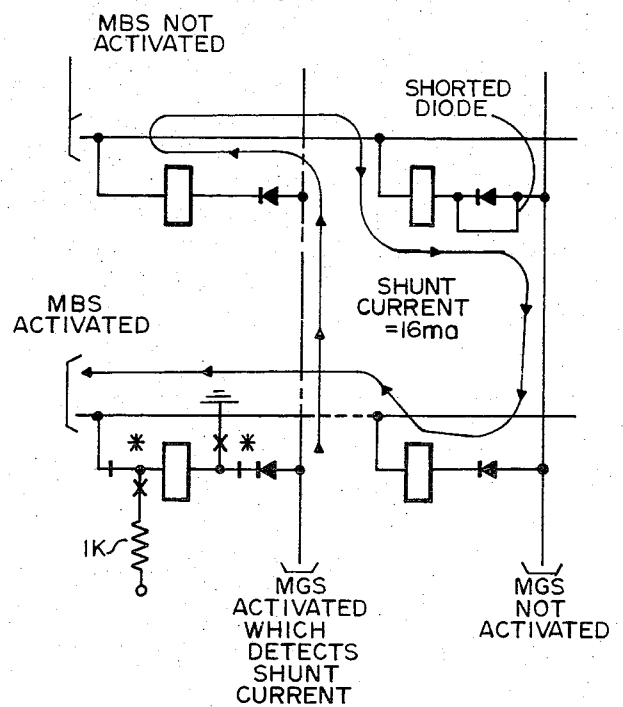
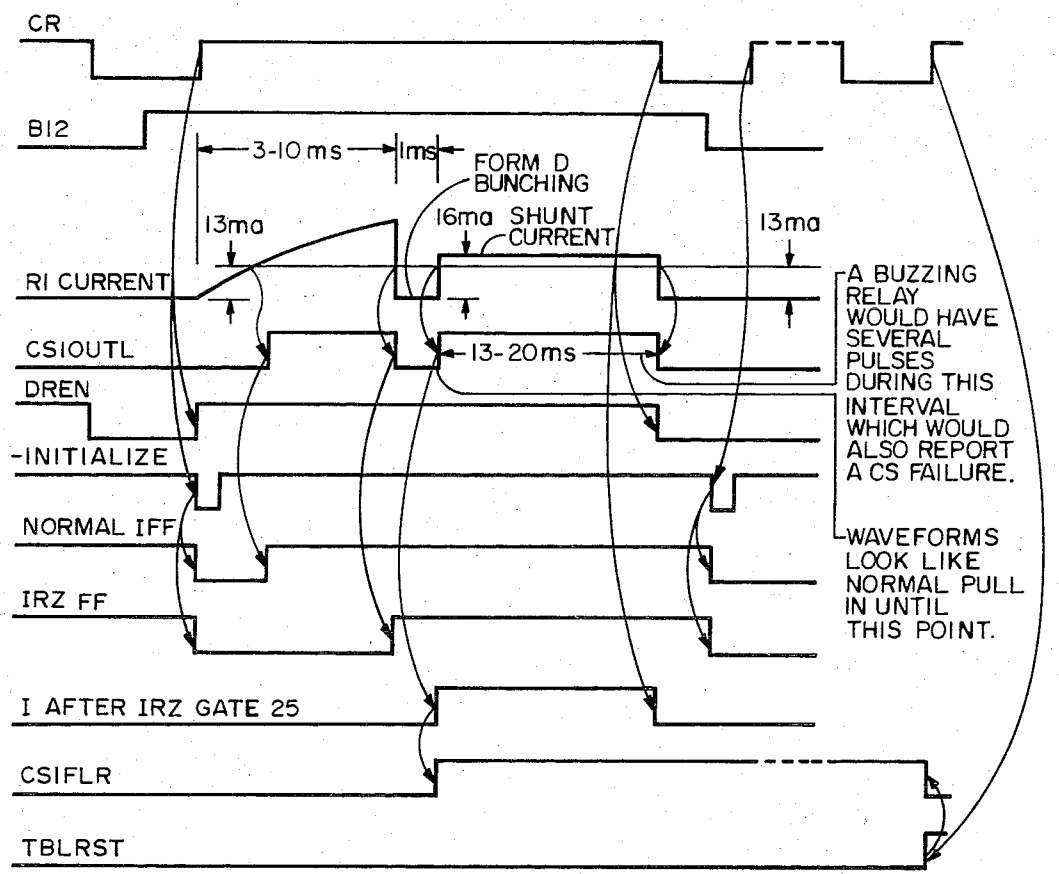
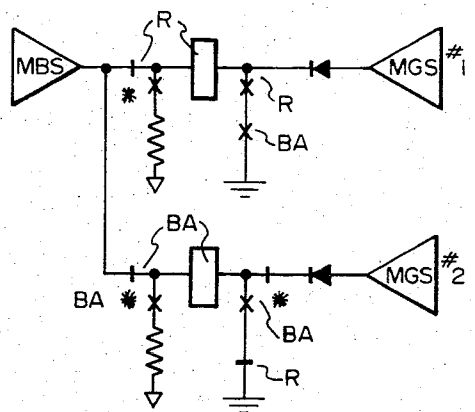


FIG. 16



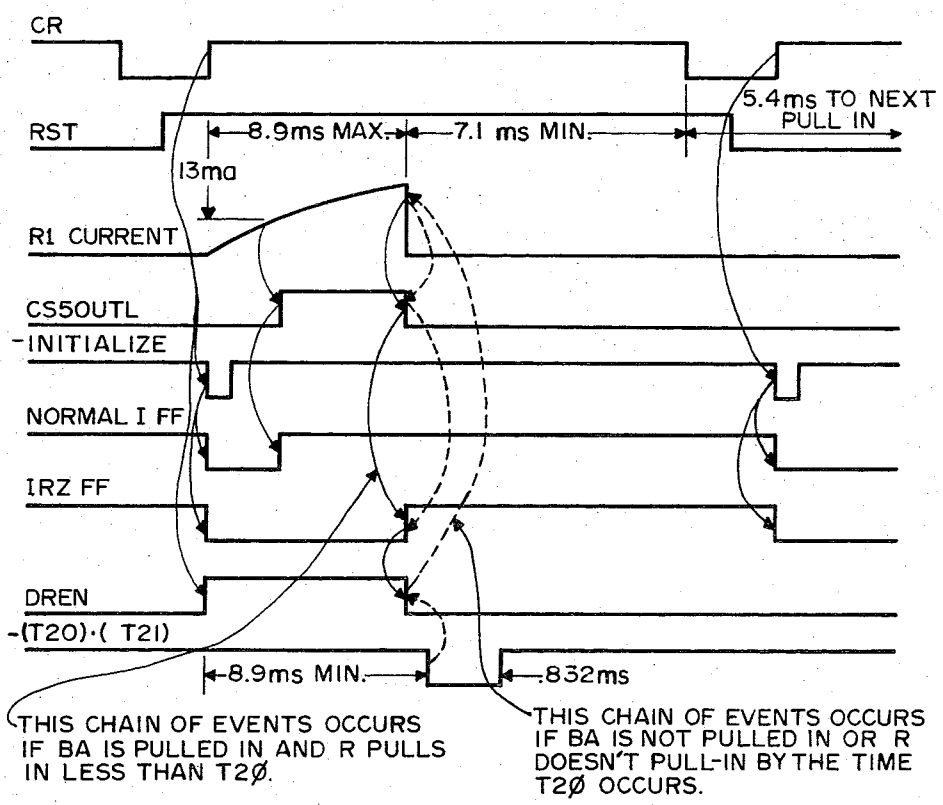
B12 CURRENT SENSOR WAVEFORMS SHORTED DIODE FAILURE
(B13-15 IDENTICAL, RST CANNO'T DETECT SHORTED DIODES)

RESET RELATED BUZZING



1) BUZZING MODE 1:
MBS AND MGS #1 ACTIVATED RELAY R CAN PULL IN IN 5ms. RELAY BA CAN THEN DROP OUT IN 6.8ms. LEAVING R TO BUZZ FOR THE REMAINDER OF THE 20ms. COMMAND INTERVAL EXCEPT THAT NC CONTACT IN MGS#1 IS NOT USED AND EITHER BA OR MGS#1 NOW PROVIDE GROUND HOLDING R UP UNTIL THE END OF COMMAND INTERVAL WITHOUT BUZZING BUT LEADING TO:

2) BUZZING MODE 2:
IF THE NEXT COMMAND ACTIVATES MGS#2 AND MBS, BA CAN PULL-IN IN 5ms. R CAN TAKE AS LONG AS 13.ms TO DROP LEAVING BA WITH NO GROUND FROM R AND CAUSING IT TO BUZZ FOR 8.3ms. ALSO SINCE BA PROVIDES BUZZING GRD. TO R, IT WILL NOT DROP IN 13.3ms AND BOTH RELAYS CAN BUZZ UNTIL COMMAND ENDS. THIS IS PREVENTED BY REMOVING DREN AS SOON AS R PULLS UP OR WHEN T20 OCCURS AS SHOWN AT RIGHT.



CURRENT SENSOR WAVEFORMS, NORMAL RST PULL-IN

FIG. 17

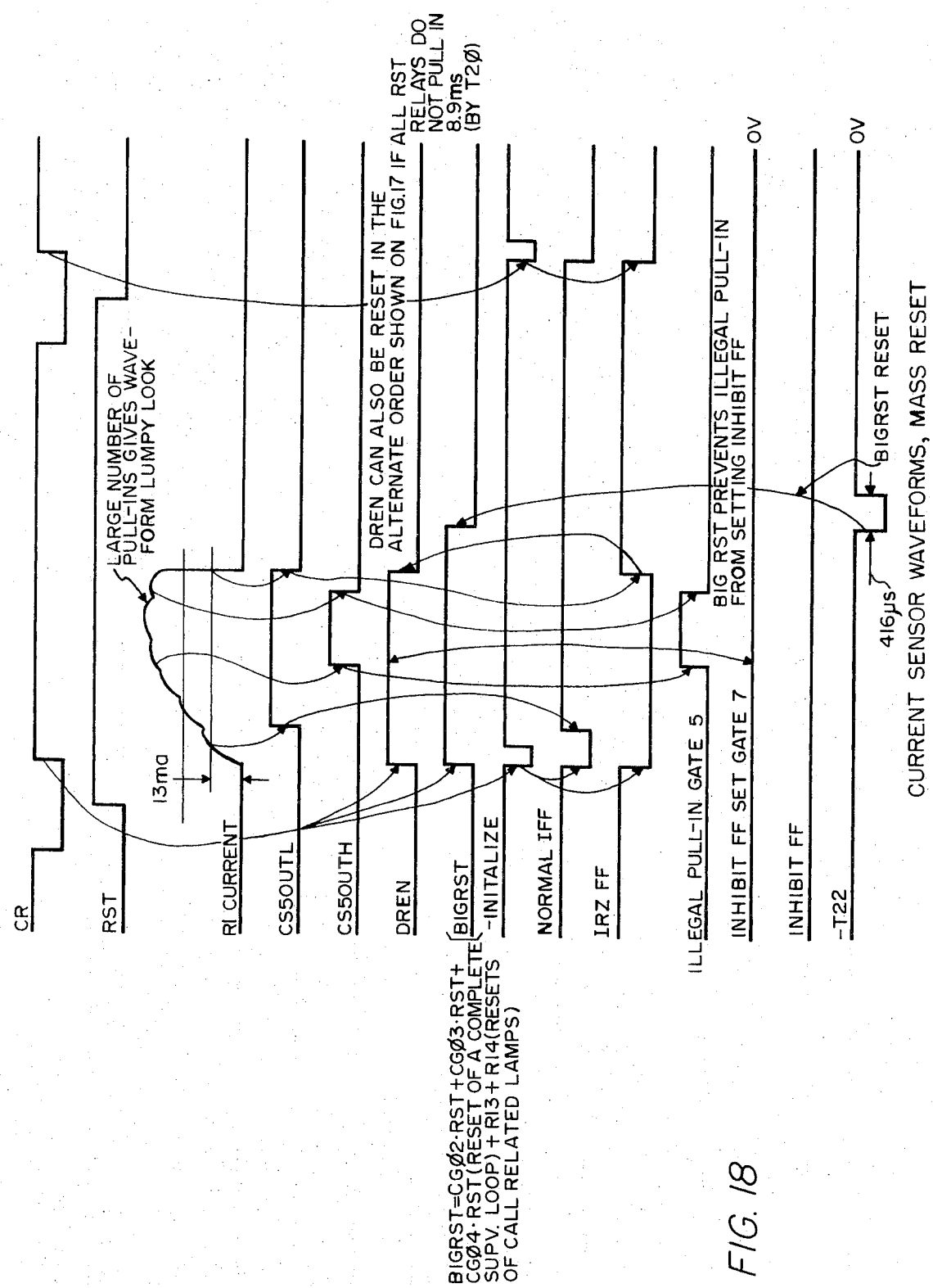

CR
RST
RI CURRENT
CS5OUTL
CS5OUTH
DREN
BIGRST
-INITALIZE
NORMAL IFF
IRZ FF
ILLEGAL PULL-IN GATE 5
INHIBIT FF SET GATE 7
INHIBIT FF
-T22
13ma
LARGE NUMBER OF PULL-INS GIVES WAVE-FORM LUMPY LOOK
DREN CAN ALSO BE RESET IN THE ALTERNATE ORDER SHOWN ON FIG.17 IF ALL RST RELAYS DO NOT PULL IN 8.9ms (BY T2Ø)
BIGRST=CGØ2·RST+CGØ3·RST+CGØ4·RST(RESET OF A COMPLETE SUPV. LOOP)+RI3+RI4(RESETS OF CALL RELATED LAMPS)
BIG RST PREVENTS ILLEGAL PULL-IN FROM SETTING INHIBIT FF
0V
0V
416μs
BIGRST RESET
CURRENT SENSOR WAVEFORMS, MASS RESET

FIG. 18

CONTROL OF OPERATOR POSITION DISPLAY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a display buffer for controlling lighting of lamps and other functions at a plurality of operator positions.

2. Description of the Prior Art

A display buffer is described in the Bell System Technical Journal, Vol. 49, No. 10, Dec. 1970, pages 2,602–2,603.

SUMMARY OF THE INVENTION

The invention relates to the arrangement of the relay drivers and relays into what are effectively matrix circuits, with current sensors connected to relay driver ground switches using a common resistor for each bit of status codes (including reset), so that current for only one relay should flow through each resistor. The arrangement includes logic associated with the current sensors to monitor the operation and detect failures.

CROSS REFERENCE TO RELATED APPLICATIONS

This invention is included in a TSPS system briefly described in the GTE Automatic Electric Technical Journal, Vol. 12, No. 7, July 1971, pages 276–285.

The central processor and peripheral controller are disclosed in a U.S. Pat. application for Control Complex for TSPS Telephone System, by E. F. Brenski et al., Ser. No. 289,718 filed Sept. 15, 1972.

The data link for communication of data between operator's positions and central control is disclosed in a U.S. application by M. Winn, W. R. Wedmore, and J. S. Young for Data Link Arrangement with Error Checking and Retransmission Control (H–1713), Ser. No. 397,454 filed the same day as this application.

DESCRIPTION OF THE DRAWING

FIG. **1** is a functional block diagram of the decoding and relay driver circuits of the buffer control circuit;

FIGS. **2** and **3** are schematic diagrams of the relay drivers for battery and ground respectively;

FIGS. **4** and **5** are diagrams of relays in the display buffer;

FIG. **6** is a schematic and functional block diagram of a current sensor;

FIGS. **7–9** are functional block logic diagrams; and

FIGS. **10–18** are wave form diagrams for operation of the current sensors and associated logic.

DETAILED DESCRIPTION

As described in the copending data link patent application, the data link has a local terminal at a base location, and a remote terminal at a traffic office which has a maximum of 62 operator positions. Messages received at the remote terminal include a command data with 15 bits **B0–B15.** A display buffer comprises relays having contacts connected to lamps of the positions. A buffer control circuit is connected between the data set and the display buffer.

The function of the Buffer Control Circuit (BCC) is to accept commands from the RTC (Remote Terminal Circuit), decode then and generate appropriate control signals as required to perform the desired Traffic Office function. In addition, maintenance circuits are provided to test for the successful completion of most commands to the T.O. The functional and maintenance circuits will be discussed separately.

FUNCTIONAL CIRCUITS

The structure of the incoming commands is basic to the understanding of the BCC. The command consists of 16 bits divided into three fields. The position field (Bits ϕ through **5**), the control group field (Bits **6** through **11**) and the status code field (Bits **12** through **15**).

The Position Field, Bϕ through **B5,** identifies the position to which the command is addressed with Bϕ as the most significant bit. These positions consists of the 62 TSPS Positions numbered 1 through 62 and two psuedo-positions numbered $\phi\phi$ and **63.** Commands to position ϕ control the MRG (Maintenance Report Generator) at present; while commands to position **63** control the displays on the administrative cabinets and perform all non-TSPS position control functions in the T.O. other than the MRG. If they should be required position $\phi\phi$ commands could perform additional T.O. control functions.

The control group field, **B6** through **B11,** usually identifies the control group addressed which is associated with the position or psuedo-position addressed in Bϕ through **B5.** A control group number is binary coded with **B6** as the most significant digit. It identifies a set of one or more devices, usually lamps, grouped together for coding efficiency because they can only take on a limited number of states. In most cases a control group consists of a set of lamps only one of which can be lit at any given time. All of the control groups and their functions are shown in Tables **1** through **3.** Table **1** shows the control group functions for position $\phi\phi$, the MRG. Table **2** shows the control groups for Traffic Service Positions, numbered **1** through **62,** and Table **3** shows the control groups for Position **63,** the Administrative Cabinet Circuit.

The remaining four bits of the command, **B12** through **B15,** the status code field, describe the state desired for the control group. The number of states which any individual control group can take varies between 1 and 13. These are listed in Tables **1** through **3** as subdivisions of the control group functions. In addition to providing for control of a traffic office with the commands listed in Tables **1** through **3** the BCC can be used as a service observation system controller. For control groups which require more than eight states all four bits of the status field are used. If only **3** bits are required then bits **B12** through **B14** are used. If two bits, then **B12** and **B13.** Two state control groups only use **B12.** In general, zeros in the status code indicates reset the control group. The only exceptions to the rule are control groups **6**ϕ and **61** in the Service Observing application.

As shown in FIG. **1,** the buffer control circuit BCC is basically a decoding device for the incoming command fields. It is implemented with HTL logic and with Main Ground Switch and Main Battery Switch Discrete Printed Circuit Boards. As can be seen in FIG. **1,** the position field is used to drive a one of **64** position decoder generating **64** PD (Position Decode) leads. Since the decoder generates an inverted signal, the PD leads are inverted before being applied to the position drivers. The position drivers are gates B (Main Battery Switches) which switch battery to the output identified

in the position field. The position decoder is enabled by DREN (Driver Enable) and if this signal is absent none of the outputs will be energized. The operation of DREN is further discussed with maintenance circuits later in this section.

The second field, the control group field, is initially handled in the same manner as the position field. **B6** through **B11,** drive a one of **64** decoder identical to the position field decoder. The decoded outputs, called CG (Control Group) leads, are then inverted.

The status code field provides a second source of inputs to the relay driver logic gates. This field again needs to be buffered. In addition, at the buffering stage all zeros in the field (Reset) is detected and brought out as a separate signal, RST. In the Traffic Office application, RST plus the individual bits, **B12** through **B15,** provide all of the inputs other than the CG leads required for the relay driver logic gates. The output of the relay driver logic gates in turn drives the FS (Function Select) relay drivers G which are (Main Ground Switches) which apply grounds at the FS outputs selected by the relays driver logic. This coincidence of battery from the position field and grounds from the remaining fields will then pull in HQA relays in the buffer. The circuits of the main battery switches B and main ground switches G are shown in FIGS. **2** and **3.** Note that the ground switch output **25** is connected via a current sensor to ground. This output is shown at the bottom of each switch G in FIG. **1.**

Almost all control functions at the T.O. are performed using the PS and FS signal coincidence as described above. There are however three other control interfaces which are different. The first of these is the TMBC control. Here the position field is used to drive MBS switches with outputs RBO through **RB5** which then store the position field in an HQA relay register. REGRST, also a battery switch, is used to reset a relay register. MON and TST which are the outputs of ground switches driven by **CG44** and **CG43** respectively to select one of two registers. The logic inputs necessary to energize the outputs are shown in Table **6.** Secondly, there is the RECON-TBLRST logic which provides switched ground on either of the two output leads to control switchover of copies of TOCF. Its logic equation is also shown in Table **6.** RCT.CR is the command relay (CR) lead from the data set indicating completion of receipt of message. Finally there are the PSF and RRF leads. Their logic equations are also shown in Table **6.** Their output is HTL logic levels. PSF (Position Status Flag) directed to the Key Scanner requests the contents of the key bus of the position identified in the position field. RRF directed to the remote terminal circuit requests retransmission of the message with sequence number in **B13** through **B15.**

DISPLAY BUFFER

FIG. **4** shows the relays of Control group No. **1** of position **1.** This group has all four function relays for bits **B12–B15** and a reset relay, with ground supplied via leads **FS001–FS005** from FIG. **1.** These leads are connected in multiple to group No. **1** of all positions. Battery potential is supplied via lead **PS01** to all five relays and also to relays of other groups for the same position. As shown in Table **2,** a digit display message may have any value from **1** to **0,** with bits **B12–B15** coded accordingly. When the decoders in FIG. **1** are activated, the selected relays operate, and make before break contacts (form D indicated by *) disconnect them from the driver leads and lock over a circuit including break contacts of the reset relay. A decoding contact tree connects battery potential for the selected lamp.

A subsequent message selects and operates the release relay, which locks itself to a path with a parallel connection via make contacts of the function relays to ground. The function relays restore, which then restores the release relay.

The release relay for this group is also used to release the function relays of groups **2–13** and **42.** The locking path for the release relay therefore has parallel connected make contacts on all the function relays of these groups. Because of the number of relays in these groups, the release relay has two break contacts for locking the function relays.

FIG. **5** shows the relays of control group **25,** position **1,** which control a key calling lamp. As shown in Table **2,** the lamp may be lit steady with bit **B13,** or flashing with bits **B12** and **B13.** For flashing, relay MA (bit **B12**) transfers the battery connection to a **120** IPM source.

BCC MAINTENANCE CIRCUITS

The BCC maintenance circuits comprise current sensors and associated logic. The function of the Current Sensor and associated logic is to determine that proper relay operation occurred in the Display Buffer Circuit, a **62** by **141** relay matrix. It accomplishes this by monitoring the current switched by the Function Select MGS circuits, the verticals of the DBCF matrix. Because it is possible for as many as four relays to pull-in at once and as few as one and because the reset relays function differently from the others, the current sensor circuits are subdivided into five separate similar subsystems. One each for the relays associated with Bits **B12** through **B15** of the command and one for reset relays. We can then conceive of the DBCF matrix as being five submatrices organized so that on any given command at most one and only one relay in each submatrix should pull-in.

System operation can be divided into Current Sensing and trouble detecting by current Sensor Logic. The current sensing circuit is shown on FIG. **6.** On an incoming command to a position the appropriate position main battery switch and one of the Function Select main ground switches are switched on. The current pulling in the relay will flow through the emitters of the main ground switches which gets ground through the 10 ohm register, **R1,** which also provides ground to the emitters of all the other **B12** main ground switches output transistors.

The voltage generated across **R1** is coupled via **C1** of FIG. **6** to a pair of differential amplifiers used as voltage comparators. The low threshold detector has Reference Voltage = 0.13 volts and its output switches from logic ϕ (= ϕ volts) to logic **1** (+12 volts) when the voltage across **R1** is greater than the reference voltage. The high threshold detector switches from logic ϕ to **1** when the voltage across **R1** is greater than the reference voltage = 0.38 volts. Minus 0.13 volts corresponds to **13MA** through **R1** while 0.38 volts means **38MA.** All five current sensor subsystems have identical current sensors.

The logic itself can be subdivided into common logic (FIG. **7**), **B12** through **B15** logic (FIG. **8**) and Reset logic (FIG. **9**). The current Sensor Logic, can best be

understood by considering the waveforms across R1 for normal operation and the various failure modes anticipated. FIG. **10** shows typical waveforms across R1 for normal pull-in in the B12 submatrix based on tests with HQA relays. The figure also shows CR (Command Ready) a nominal **20** MS pulse during which pull-in is required and all other relevant gates and FF's in the logic. The B12 Current Sensor logic FIG. **8** contains four S–R flip-flops (latches) and control gates. The flip-flops are the Inhibit FF, the Normal I FF, the IRZ FF and the CS Trouble FF. In normal operation only the Normal I and the IRZ FF are affected.

The sequence of events after a command with a B12 pull-in arrives is then as follows:

1. The initializing pulse — INITIALIZE, resets the Normal I FF and the IRZ FF at the beginning of a command sequence. The initializing pulse is generated by the HTL monostable in the CS Common Logic shown in FIG. **7** whenever Command Ready (CR) has a positive swing. It resets the Normal I FF and the IRZ FF of all five current sensors logic. Unless a failure occurred on the previous operation both of these flip-flops should be set at the beginning of a command. The waveforms for this and succeeding steps is shown in FIG. **11.**
2. The voltage across R1 begins to rise exponentially eventually reaching **130** MV and switching AMP1 output CS1OUTL to **1.**
3. CS1OUTL is buffered by the two input NANDS **9** and **11** of FIG. **9.** The buffering is necessary because the op amp will only drive **2** HTL logic loads. CS1OUTL is gated by CSEN (current sensor enable), a 2 millisecond pulse which suppresses CS1OUTL as well as all other voltage comparator outputs until switching transients have died down.
4. $\overline{\text{B12.CS1OUTL}}$ is formed at gate **21.** The function of this gate is to determine that a relay should be pulled in, B12 = 1, and that it did pull-in, CS1OUTL = 1.
5. Proper pull-in as indicated in four next drives a **3**-input "OR" formed of gates **17, 19** and **1.** The other inputs to this "OR" will be discussed subsequently as other normal modes of Current Sensor logic operation.
6. The output of the OR is next NANDED in gate **13** with Command Ready (CR) to set the NORMAL I FF, gates **16** and **15.** The Normal I FF stores the information that the voltage across R1 exceeded 130 volts, i.e., that the current drawn by the MGS's exceeded **13** MA.
7. The voltage across R1 continues to rise until the relay pulls in at 250 MV ± 50 as measured in tests with HQA relays. At pull-in the voltage across R1 drops to zero as ground comes back through the NC contact during the bunching period of the form D contact. At this time CS1OUTL drops back to zero. The output of gate **9** goes to 12 volts which when NANDED with Normal I FF in gate **3** and switches on the IRZ FF, gates **18** and **20.** IRZ is a mnemonic for Current Returned to Zero.
8. Nothing of further significance occurs through the end of $\overline{\text{CR}}$ (Command Ready) and the **416** μs period of $\overline{\text{CR}}$ until — INITIALIZE occurs at the next positive swing of Command Ready, starting another sequence. If no B12 submatrix relays are to be pulled in the waveforms will be as shown in FIG. **10.**

After the form D contact bunching period the relay is isolated from the MGS and MBS. Since the MGS is not turned off for B12 through B15 current sensors during the remainder of CR, the leakage current through the **30K** resistor in the MGS shown on FIG. **6** will draw approximately 1.5 MA. causing the 1.5 MV drop across R1. This is not enough to switch AMP1 and should have no further effect. The MGS and MBS are left on to test for shorted diodes as described later.

The other normal modes of operation are necessitated by the operation of the IRZ FF. In order to insure that pull-in occurred the IRZ FF must be set before CR drops back to zero. If it is not set gate **26** will switch to zero and set the failure flip-flop, gates **4** and A of FIG. **9** via one of the three remaining inputs to A used as a **3**-input trouble "OR." The commonest example of a command which would have this difficulty with the IRZ FF is one where B12 = ϕ as shown in FIG. **11.** In this case none of the B12 relays should pull in. The B12 input at gate **17** in this event will simulate normal I and set the NORMAL I FF when CR comes up. Since no MGS should be turned on in this case, CS1OUTL should be = ϕ and the IRZ FF should also be set immediately afterwards.

The third input which sets the Normal I FF is –C-SINH. This signal which originates in the CS Common Control logic FIG. **7** is a **7** input "OR" which indicates a message to T.O. Hardware for subsystems other than the Display buffer matrix or a dummy message. These other subsystems are the TMBC (MON or TST), the KSC (PSF or RRF) and SSC (RECON and TBLRST). Key waveforms for this case are shown in FIG. **12.**

There are four fault conditions which will set the Current Sensor Trouble FF. These are:

1. Failure to set the IRZ FF during the **20** MS.CR period as detected by gate **26.** Display Buffer Fault conditions which could cause this are:
   a. Open output in activated MGS or MBS which would never allow NORMAL I FF to be set.
   b. Open diode or winding at crosspoint relay which would also never allow NORMAL I FF to be set.
   c. Active MGS decoder stuck at **1** or Active MBS decoder stuck at ϕ which would also never allow NORMAL I FF to be set.
   d. A stuck armature on crosspoint relay with resulting failure to eventually isolate coil from MGS during Command Ready.

In any of these faults the waveforms in the Current Sensor system will be as shown in FIG. **13.**

2. The next two cases are those which set the INHIBIT FF, gates **6, 7** and **8.** This FF is set up by a two input OR formed from gates **5, 1**ϕ and **12.** The upper input to the "OR" is CS1OUTH and its primary function is to detect more than one relay pulling in. The relevant CS system waveforms are shown on FIG. **14.** The INHIBIT FF is then reset by –CR thereby providing test capability for the next Command. The fact that a failure occurred is stored in the CS1FLR FF through another input to gate A and this failure FF retains the information that a failure occurred until reset by a specific command from base location energizing TBLRST.

Failures which will set CS1OUTH are:

1. Shorted output on MGS or MBS other than the one activated.
2. Decoder output for MGS other than one activated stuck at **1** or MSB output other than that activated stuck at ϕ.
3. Shorted turns on crosspoint coil or short in wiring.

The other failure mode which sets the INHIBIT FF is CS1OUTL·$\overline{B12}$ = 1 or an attempt to pull in a relay as evidenced by R1 Current greater than **13** MA. when none should be pulled in. The "and" function is performed by gate **12.** Fault conditions which could cause this are:

1. Shorted output on an MGS.
2. Active MGS decoder output stuck at **1.**

The associated waveforms are shown on FIG. **15.**

The remaining failure mode as detected by gate **25** is I after IRZ. This is mainly intended to detect shorted diodes in the matrix. This is accomplished as can be seen in FIG. **16** by detecting the shunt current through the shorted diode during the time remaining after pull-in of the intended relay. Another fault which will cause the same output is a buzzing relay, with the current now flowing through the coil to be pulled-in and not through a shunt.

The **B13** through **B15** submatrix Current Sensor subsystem are identical to the **B12** subsystem except that the matrices themselves are smaller. The RST (Reset) submatrix is different from the previous matrices as described in Section **4,** but the difference is only in the latching mechanism as is shown on FIG. **17** and does not effect the theory of operation. The RST current sensors and their operation is also identical to that of the **B12** through **B15,** but the RST Current Sensor logic is different in two respects. First, as can be seen in the waveforms for a normal RST pull-in in FIG. **17** DREN (Driver Enable) is cut off as shown as pull-in occurs. This is accomplished by an "OR" of the INHBIT FF and the IRZ FF in gates **25** and **22.** The second difference is that the set lead to the INHIBIT FF is gated by $\overline{BIGRST}$. This signal which is generated in the C.S. Common logic is an "OR" OF all the commands which would pull in more than one Reset relay. These commands will be used at the end of a call to reset all called related displays. Since this is an additional mode of normal operation the waveforms for this case is shown in FIG. **18.** Because the drivers are turned off after pull-in, the leakage current observed in the **B12** matrix no longer occurs. For this reason also, the shunt current observed in the case of a shorted diode will not occur when pulling in crosspoints of the RST matrix. This is not a serious disability since as shown in FIG. **14** in order to detect the shunt current through the shorted diode it is necessary to pull in a crosspoint with different horizontal and vertical from the defective diode.

This can be accomplished in the **B12** through **B15** submatrices to test RST crosspoint diodes. The I after IRZ gate is still retained in the RST **CS5** logic but its sole function is to detect a buzzing RST relay.

In addition to detecting component failures, the current sensors and logic can be used to interrogate the DBCF and determine the status of crosspoints. This is done by sending a pull in message to each crosspoint immediately followed by a reset of the same crosspoint. If the crosspoint was not latched initially, both of these operations will appear normal. However, if it was latched a trouble message will be generated because CS1OUTL will never occur and the NORMAL I and consequently the IRZ FF's will never be set.

TABLE 1

CPU COMMANDS FOR POSITION ϕ (MRG)			
CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
1	$\phi\phi\phi\phi\phi$1	1$\phi\phi\phi$	Remove Alarm 1, TOCFϕ Current Sensor 1 Failure, from MRG Key bus.
		ϕ1$\phi\phi$	Remove Alarm 2, TOCFϕ Current Sensor 2 Failure, from MRG Key bus.
		$\phi\phi$1ϕ	Remove Alarm 3, TOCFϕ Current Sensor 3 Failure, from MRG Key bus.
		$\phi\phi\phi$1	Remove Alarm 4, TOCFϕ Current Sensor 4 Failure, from MRG Key bus.
2	$\phi\phi\phi\phi$1ϕ	1$\phi\phi\phi$	Remove Alarm 5, TOCFϕ Current Sensor 5 Failure, from MRG Key bus.
		ϕ1$\phi\phi$	Remove Alarm 6, TOCF1 Current Sensor 1 Failure, from MRG Key bus.
		$\phi\phi$1ϕ	Remove Alarm 7, TOCF1 Current Sensor 2 Failure from MRG Key bus.
		0001	Remove Alarm 8, TOCF1 Current Sensor 3 Failure, from MRG Key bus.
3	$\phi\phi\phi\phi$11	1$\phi\phi$ ϕ	Remove Alarm 9, TOCF1 Current Sensor 4 Failure, from MRG Key bus.
		ϕ1$\phi\phi$	Remove Alarm 10, TOCF1 Current Sensor 5 Failure, from MRG Key bus.
		$\phi\phi$1ϕ	Remove Alarm 11, Invalid BCCϕ Reconfigure message, from MRG Key bus.
		$\phi\phi\phi$1	Remove Alarm 12, Invalid BCC1 Reconfigure message, from Key bus.
4	$\phi\phi\phi$1$\phi\phi$	1$\phi\phi\phi$	Remove Alarm 13, Invalid BCCϕ and BCC1 Reconfigure message, from MRG Key bus.
		ϕ1$\phi\phi$	Remove Alarm 14, Transfer relay failure, from MRG Key bus.
		$\phi\phi$1ϕ	Remove Alarm 15, Modulator Copy ϕ Failure, from MRG Key bus.
		$\phi\phi\phi$1	Remove Alarm 16, Modulator Copy 1 Failure, from MRG Key bus.
5	$\phi\phi\phi$1ϕ1	1$\phi\phi\phi$	Remove Alarm 17, Demodulator Copy ϕ failure, from MRG Key bus.
		ϕ1$\phi\phi$	Remove Alarm 18, Demodulator Copy 1 failure, from MRG Key bus.
		$\phi\phi$1ϕ	Remove Alarm 19, TOSF major alarm, from MRG Key bus.
		$\phi\phi\phi$1	Remove Alarm 20, TOSF minor alarm, from MRG Key bus.
6	$\phi\phi\phi$11ϕ	ϕ1$\phi\phi$	Remove Alarm 22, TOCFϕ fuse alarm, from MRG Key bus.
		$\phi\phi$1ϕ	Remove Alarm 23, TOCF1 fuse alarm, from MRG Key bus.
		$\phi\phi\phi$1	Remove Alarm 24, T.O. major equipment alarm, from MRG Key bus.
7	$\phi\phi\phi$111	1$\phi\phi\phi$	Remove Alarm 25, T.O. major power alarm, from MRG Key bus.
		ϕ1$\phi\phi$	Remove Alarm 26, T.O. minor equipment alarm, from MRG Key bus.
		$\phi\phi$1ϕ	Remove alarm 27, unassigned, from MRG Key bus.
		$\phi\phi\phi$1	Remove Alarm 28, TOCFϕ request key, from MRG Key bus.

TABLE 1-Continued

CPU COMMANDS FOR POSITION ϕ (MRG)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
8	ϕϕ1ϕϕϕ	1ϕϕϕ	remove Alarm 29, TOCF1 Request Key, from MRG Key bus.
		ϕ1ϕϕ	Remove Alarm 30, TOCFϕ Power on Key, from MRG Key bus.
		ϕϕ1ϕ	Remove Alarm 31, TOCFϕ Power off Key, from MRG Key bus.
		ϕϕϕ1	Remove Alarm 32, TOCF1 Power on key, from MRG Key bus.
9	ϕϕ 1ϕϕ1	1ϕϕϕ	Remove Alarm 33, TOCF1 Power off key, from MRG Key bus.
		ϕ1ϕϕ	Remove Alarm 34, Local test key, from MRG Key bus.
		ϕϕ1ϕ	Remove Alarm 35, TOCF Transfer Key from MRG Key bus.
		ϕϕϕ1	Remove Alarm 36, Interrupter ϕ failure from MRG Key bus.
10	ϕϕ1ϕ1ϕ	1ϕϕϕ	Remove Alarm 37, Interrupter 1 failure, from MRG Key bus.
		ϕ1ϕϕ	Remove Alarm 38, unassigned, from MRG Key bus.
		ϕϕ1ϕ	Remove Alarm 39, unassigned, from MRG Key bus.
		ϕϕϕ1	Remove Alarm 40, unassigned, from MRG Key bus.
11	ϕϕ1ϕ11	1ϕϕϕ	Remove Alarm 41, unassigned, from MRG Key bus.

TABLE 1-Continued

CPU COMMANDS FOR POSITION ϕ (MRG)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B12	FUNCTION
14	ϕϕ111ϕ	ϕϕϕϕ	Restore all alarms except Alarm 21, MRG card 1 fuse alarm, and Alarm 42, MRG card 2 fuse alarm to MRG Key bus. If MRG card 1 fuse is blown then alarms 1 through 20 cannot reach MRG Key bus. If MRG card 2 fuse is blown then alarms 22 through 41 cannot reach key bus. Alarms 21 and 42 cannot be removed from MRG Key bus.
62	11111ϕ	ϕϕϕϕ	Retransmission Request for message with sequence number ϕ.
		ϕϕϕ1	Retransmission Request for message with sequence number 1.
		ϕϕ1ϕ	Retransmission Request for message with sequence number 2.
		ϕϕ11	Retransmission Request for message with sequence number 3.
		ϕ1ϕϕ	Retransmission Request for message with sequence number 4.
		ϕ1ϕ1	Retransmission Request for message with sequence number 5.
		ϕ11ϕ	Retransmission Request for message with sequence number 6.
		ϕ111	Retransmission on Request for message with sequence number 7.
63	111111	1ϕϕϕ	Return status of MRG key bus to CMC.

TABLE 2

CPU Commands for Positions 01 through 62 (In Numerical order).

CONTROL GROUP NUMBER	CONTROL GROUP IDENTIFICATION	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
1	Digit Display & Display Identification Reset	ϕϕϕϕϕ1	ϕϕϕϕ	Reset all lamps set by Control Groups 1 through 12, 13, 42.
1	Digit Display No. 1	ϕϕϕϕϕ1	ϕϕϕ1	Light number 1 on digit display.
			ϕϕ1ϕ	Light number 2 on digit display.
			ϕϕ11	Light number 3 on digit display.
			ϕ1ϕϕ	Light number 4 on digit display.
			ϕ1ϕϕ	Light number 4 on digit display.
			ϕ1ϕ1	Light Number 5 on digit display.
			ϕ11ϕ	Light number 6 on digit display.
			ϕ111	Light number 7 on digit display.
			1ϕϕϕ	Light number 8 on digit display.
			1ϕϕ1	Light number 9 on digit display.
			1ϕ1ϕ	Light number 0 on digit display.
2	Loop No. 1 Supervisory Reset	ϕϕϕϕ1ϕ	ϕϕϕϕ	Reset all lamps set by Control Groups 30, 33, 36.
2	Digit Display No. 2	ϕϕϕϕ1ϕ	ϕϕϕ1 through 1ϕ1ϕ	Same as Control Group No. 1 for digit display No. 2
3	Loop. No. 2 Supervisory Reset	ϕϕϕϕ11	ϕϕϕϕ	Reset all lamps set by Control Groups 31, 34, 47.
3	Digit Display No. 3	ϕϕϕϕ11	ϕϕϕ1 through 1ϕ1ϕ	Same as Control Group No. 1 for digit display No. 3.

TABLE 2 – Continued

CPU Commands for Positions 01 through 62 (In Numerical order).

CONTROL GROUP NUMBER	CONTROL GROUP IDENTIFICATION	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
4	Loop No. 3 Supervisory Reset	ϕϕϕ1ϕϕ	ϕϕϕϕ	Reset all lamps set by Control Groups 32, 35, 38.
4	Digit Display No. 4	ϕϕϕ1ϕϕ	ϕϕϕ1	Same as Control Group No. 1
5	do. do.	ϕϕϕ1ϕ1	↑	do.
6	do. do.	ϕϕϕ11ϕ	through	do.
7	do. do.	ϕϕϕ111	↓	do.
8	do. do.	ϕϕ1ϕϕϕ		do.
9	do. do.	ϕϕ1ϕϕ1		do.
10	do. do.	ϕϕ1ϕ1ϕ		do.
11	do. do.	ϕϕ1ϕ11		do.
12	do. No. 12	ϕϕ11ϕϕ	1ϕ1ϕ	Same as Control Group No. 1
13	Call Related Lamp Reset I	001101	0000	Reset all lamps set by Control Gps 18, 2ϕ, 21, 22, 28, 39, 41 and Reset Bit 13 Cont. Gp. 15 (Flash Class of Charge).
13	Display Identification	ϕϕ11ϕ1	ϕϕϕ1	Light Hotel Lamp Steady.
			ϕϕ1ϕ	Light Spare Lamp Steady.
			ϕ1ϕϕ	Light Minute Lamp Steady.
			ϕ1ϕ1	Light Minutes, Hours, Seconds, Lamps Steady.
			ϕ11ϕ	Light Minutes and Charges, Lamps Steady.
			111ϕ	Light Minutes and Charges, Lamps Flashing.
14	Call Related Lamp Reset II	ϕϕ111ϕ	ϕϕϕϕ	Reset Control Gps. 14, 16, 17, 23, 24, 25, 29 and Bit B12 Cont. Gp. 15 (Flash Kind of Call).
14	Kind of Call	ϕϕ111ϕ	ϕϕϕ1	Light Non-Coin Station Lamp.
			ϕϕ1ϕ	Light Non-Coin 0+ Lamp.
			ϕϕ11	Light Non-Coin 0– Lamp.
			ϕ1ϕϕ	Light Coin Station Lamp.
			ϕ1ϕ1	Light Coin 0+ Lamp.
			ϕ11ϕ	Light Coin 0– Lamp.
			ϕ111	Light Hotel Station Lamp.
			1ϕϕϕ	Light Hotel 0+ Lamp.
			1ϕϕ1	Light Hotel 0– Lamp.
15	Class of Charge Flashing Relay	ϕϕ1111	ϕ1ϕϕ	Flash Control Gp. 28.
15	Kind of Call Flashing Relay	ϕϕ1111	1ϕϕϕ	Flash Control Gp. 14.
16	Overseas	ϕ1ϕϕϕϕ	1ϕϕϕ	Light "Overseas" Lamp Steady.
17	EMG	ϕ1ϕϕϕ1	1ϕϕϕ	Light EMG Lamp Steady.
18	GST Lamp Reset	ϕ1ϕϕ1ϕ	ϕϕϕϕ	Reset Control Group 18, GST Lamp.
18	GST	ϕ1ϕϕ1ϕ	ϕϕϕϕ	Light GST Lamp Steady.
19	OGT Lamp Reset	ϕ1ϕϕ11	ϕϕϕϕ	Reset all lamps set by Control Group 19, OGT.
19	OGT	ϕ1ϕϕ11	ϕϕϕ1	Light OGT ϕ Lamp Steady
			ϕϕ1ϕ	Light OGT 1 Lamp Steady.
			ϕϕ11	Light OGT 2 Lamp Steady.
			ϕ1ϕϕ	Light OGT 3 Lamp Steady.
			1ϕϕ1	Light OGT ϕ Lamp Flashing.
			1ϕ1ϕ	Light OGT 1 Lamp Flashing.
			1ϕ11	Light OGT 2 Lamp Flashing.
			11ϕϕ	Light OGT 3 Lamp Flashing.
2ϕ	Function Control Lamp Reset	ϕ1ϕ1ϕϕ	ϕϕϕϕ	Reset all lamps set by Control Group 2ϕ.
2ϕ	Function Control	ϕ1ϕ1ϕϕ	ϕϕ1ϕ	Light Ring Back Lamp Steady.
			ϕ1ϕϕ	Light Ring FWD Lamp Steady.
			ϕ11ϕ	Light Release Back Lamp Steady.
			1ϕϕϕ	Light Release FWD Lamp Steady.
			1ϕ1ϕ	Light Coin Collect Lamp Steady.
			1ϕϕ1	Light Coin Return Lamp Steady.
21	T & C Lamp Reset	ϕ1ϕ1ϕ1	ϕϕϕϕ	Reset Control Gp. 21, T & C Lamp.
	T & C Lamp	ϕ1ϕ1ϕ1	1ϕϕϕ	Light T & C Lamp Steady.
22	PCB Lamp Reset	ϕ1ϕ11ϕ	ϕϕϕϕ	Reset Control Gp. 22, PCB Lamp.
	PCB Lamp	ϕ1ϕ11ϕ	1ϕϕϕ	Light PCB Lamp Steady.
23	NFY, Charges Due Reset	ϕ1ϕ111	ϕϕϕϕ	Reset all lamps set by Control Gps. 23 and 24.
	NFY	ϕ1ϕ111	ϕ1ϕϕ	Light NFY Lamp Steady.
			11ϕϕ	Light NFY Lamp Flashing.
24	Charges Due Lamp	ϕ11ϕϕϕ	1ϕϕϕ	Light Charges Due Lamp Steady.
25	Key Clg. Lamp Reset	ϕ11ϕϕ1	ϕϕϕϕ	Reset Control Group 25, Key Clg. Lamp.
25	Key Clg.	ϕ11ϕϕ1	ϕ1ϕϕ	Light Key Clg. Lamp Steady
			11ϕϕ	Light Key Clg. Lamp Flashing.
26	Make Busy Lamp Reset	ϕ11ϕ1ϕ	0000	Reset Control Group 26, Make Busy Lamp.

TABLE 2—Continued

CONTROL GROUP NUMBER	CONTROL GROUP IDENTIFICATION	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
	CPU Commands for Positions 01 through 62 (In Numerical order).			
26	Make Busy	ϕ11ϕ1ϕ	ϕ1ϕϕ	Light Make Busy Lamp Steady.
			11ϕϕ	Light Make Busy Lamp Flashing.
27	POS Trans. Lamp Reset	ϕ11ϕ11	ϕϕϕϕ	Reset Control Group 27, POS. Trans. Lamp.
27	Pos. Trans.	ϕ11ϕ11	1ϕϕϕ	Light Pos. Trans. Lamp Steady.
28	Class of Charge Lamps	ϕ111ϕϕ	ϕϕϕϕ	Reset all lamps set by Control Groups 28, 55 and Bit B13 of Control Gp 15.
28	Class of Charge	ϕ111ϕϕ	ϕϕϕ1	Light Station Paid Lamp.
			ϕϕ1ϕ	Light Station Collect Lamp.
			ϕϕ11	Light Station Special Clg. Lamp.
			ϕ1ϕϕ	Light Station Special Cld. Lamp.
			ϕ1ϕ1	Light Station Auto Collect Lamp.
			ϕ11ϕ	Light DDD lamp.
			ϕ111	Light Person Collect Lamp.
			1ϕϕϕ	Light Person Spl. Clg. Lamp.
			1ϕϕ1	Light Person Spl. Cld. Lamp.
			1ϕ1ϕ	Light NO ATT Lamp.
29	Timing Lamps Reset	ϕ111ϕ1	ϕϕϕϕ	Reset all lamps set by Control Group 29.
29	Timing	ϕ111ϕ1	ϕϕϕ1	Light Cancel Timing Lamp Steady.
			ϕϕ1ϕ	Light Start Timing Lamp Steady.
			ϕϕ11	Light Start Timing Lamp Steady.
			ϕ1ϕϕ	Light Record Message Lamp Steady.
			1ϕ11	Light Start Timing Lamp Flashing.
30	Loop No. 1 Hold & ACC Lamps	ϕ1111ϕ	ϕϕϕϕ	Reset all lamps set by Control Group 3ϕ.
30	Loop No. 1 Supervisory	ϕ1111ϕ	ϕ1ϕϕ	Light ACC Lamp Steady for Loop NO. 1.
			ϕ11ϕ	Light Hold Lamp Steady for Loop No. 1.
			1ϕϕϕ	Light ACC Lamp Flashing for Loop No. 1.
			111ϕ	LIght Hold Lamp Flashing for Loop No. 1.
31	Loop No. 2 Hold & ACC Lamps	ϕ11111	ϕϕϕϕ	Reset all lamps set by Control Group 31.
31	Loop No. 2 Supervisory	ϕ11111	ϕ1ϕϕ	Light ACC Lamp Steady for Loop No. 2.
			ϕ11ϕ	Light Hold Lamp Steady for Loop No. 2.
			1ϕϕϕ	Light ACC Lamp Flashing for Loop No. 2.
			111ϕ	Light Hold Lamp Flashing for Loop No. 2.
32	Loop No. 3 Hold & ACC Lamps	1ϕϕϕϕϕ	ϕϕϕϕ	Reset all lamps set by Control Group 32.
32	Loop No. 3 Supervisory	1ϕϕϕϕϕ	ϕ1ϕϕ	Light ACC Lamp Steady for Loop No. 3.
			ϕ11ϕ	Light Hold Lamp Steady for Loop No. 3.
			1ϕϕϕ	Light ACC Lamp Flashing for Loop No. 3.
			111ϕ	Light Hold Lamp Flashing for Loop No. 3.
33	Loop No. 1 Cld.	1ϕϕϕϕ1	ϕϕϕϕ	Reset all lamps set by Control Group 33.
33	Loop No. 1 Cld.	1ϕϕϕϕ1	1ϕϕϕ	Light Loop No. 1 Cld. Lamp Steady.
34	Loop No. 2 Cld.	1ϕϕϕ1ϕ	ϕϕϕϕ	Reset Control Group 34, Loop NO. 2 Cld.
34	Loop No. 2 Cld.	1ϕϕϕ1ϕ	1ϕ ϕϕ	Light Loop No. 2 Cld. Lamp Steady.
35	Loop No. 3 Cld. Lamps.	1ϕϕϕ11	ϕϕϕϕ	Reset Control Group 35, Loop No. 3 CLD.
35	Loop No. 3 Cld.	1ϕϕϕ11	1ϕϕϕ	Light Loop No. 3 Cld. Lamp Steady.
36	Loop No. 1 Clg.	1ϕϕ1ϕϕ	ϕϕϕϕ	Reset Control Group 36, Loop No. 1 Clg.
36	Loop No. 1 Clg.	1ϕϕ1ϕϕ	ϕ1ϕϕ	Light Loop No. 1 Clg. Lamp Steady.
			1ϕϕϕ	Light Loop No. 1 Clg. Lamp Flashing.
37	Loop No. 2 Clg. Lamp	1ϕϕ1ϕ1	ϕϕϕϕ	Reset Control Group 37, Loop No. 2 Clg.

TABLE 2—Continued

CPU Commands for Positions 01 through 62 (In Numerical order).

CONTROL GROUP NUMBER	CONTROL GROUP IDENTIFICATION	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
37	Loop No. 2 Clg.	1ϕϕ1ϕ1	ϕ1ϕϕ	Light Loop No. 2 Clg. Lamp Steady.
			1ϕϕϕ	Light Loop No. 2 Clg. Lamp Flashing.
38	Loop No. 3 Clg. Lamp	1ϕϕ11ϕ	ϕϕϕϕ	Reset Control Group 38. Loop No. 3 Clg.
38	Loop No. 3 Clg.	1ϕϕ11ϕ	ϕ1ϕϕ	Light Loop No. 3 Clg. Lamp Steady.
			1ϕϕϕ	Light Loop No. 3 Clg. Lamp Flashing.
39	KP Lamps	1ϕϕ111	ϕϕϕϕ	Reset all lamps set by Control Group 39.
39	KP	1ϕϕ111	ϕϕϕ1	Light KP TBL Lamp Steady.
			ϕϕ1ϕ	Light KP NFY Lamp Steady.
			ϕϕ11	Light KP BACK Lamp Steady.
			ϕ 1ϕϕ	Light KP RATE Lamp Steady.
			ϕ1ϕ1	Light KP SPL Lamp Steady.
			ϕ11ϕ	Light KP FWD Lamp Steady.
			1ϕϕ1	Light KP TBL Lamp Flashing.
			1ϕ1ϕ	Light KP NFY Lamp Flashing.
			1ϕ11	Light KP BACK Lamp Flashing
			11ϕϕ	Light KP RATE Lamp Flashing
			11ϕ1	Light KP SPL Lamp Flashing.
			111ϕ	Light KP FWD Lamp Flashing.
40	POS RLS Lamp	1ϕ1ϕϕϕ	ϕϕϕϕ	Reset Control Group 40, POS. RLS. Lamp.
40	POS RLS	1ϕ1ϕϕϕ	1ϕϕϕ	Light POS RLS Lamp Flashing.
41	ST Lamp	1ϕ1ϕϕ1	ϕϕϕϕ	Reset Control Group 41, ST Lamp.
41	ST	1ϕ1ϕϕ1	1ϕϕϕ	Light ST Lamp Steady.
42	Display Nos.	1ϕ1ϕ1ϕ	ϕ1ϕϕ	Light Clg. No. Lamp Steady.
			1ϕϕϕ	Light Cld. No. Lamp Steady.
			11ϕϕ	Light SPL. No. Lamp Steady.
43	Reset Test Register	1ϕ11ϕϕ	ϕϕϕϕ	Reset Reference Trunk Test Circuits set by Control Group 43.
43	TST	1ϕ11ϕϕ	1ϕϕϕ	Connect position addressed in Bϕ–B5 to Reference Trunk Circuit.
44	Reset Monitor Register	1ϕ1ϕ11	ϕϕϕϕ	Reset Monitoring CKTS Set by Control Group 44.
44	MON	1ϕ1ϕ11	1ϕϕϕ	Monitor position addressed on Bϕ–B5.
54	Position Not Occupied	11ϕ11ϕ	ϕϕϕϕ	Reset Control Gp. 54, Position Occupied Relay.
54	Position Occupied	11ϕ11ϕ	1ϕϕϕ	Mark Position Addressed Occupied.
55	Person Paid Lamp	11ϕ111	1ϕϕϕ	Light Person Paid Lamp Steady.
63		111111	1000	Return status of Key bus of Position identified in Bϕ–B5

TABLE 3

CPU COMMANDS FOR POSITION 63 (ACTIVE COPY)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
1	ϕϕϕϕϕ1	1ϕϕϕ	Light Exclude call type 1 lamp for controlled traffic pos. 1.
		ϕ1ϕϕ	Light Exclude call type 2 lamp for controlled traffic pos. 1.
		ϕϕ1ϕ	Light Exclude call type 3 lamp for controlled traffic pos. 1
		ϕϕϕ1	Light Exclude call type 4 lamp for controlled traffic pos. 1.
		ϕϕϕϕ	Extinguish all call exclusion lamps for controlled traffic pos. 1.
2	ϕϕϕϕ1ϕ	1ϕϕϕ	Light Exclude call type 5 lamp for controlled traffic pos. 1.

TABLE 3—Continued

CPU COMMANDS FOR POSITION 63 (ACTIVE COPY)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B16–B11	STATUS CODE B12–B15	FUNCTION
		ϕ1ϕϕ	Light Exclude call type 6 lamp for controlled traffic pos. 1.
		ϕϕ1ϕ	Light Lamp 7 in Row 1 of Admin. Cabinet.
3	ϕϕϕϕ11	1ϕϕϕ	Light Exclude call type 1 lamp for controlled traffic pos. 2.
		ϕ1ϕϕ	Light Exclude call type 2 lamp for controlled traffic pos. 2.
		ϕϕ1ϕ	Light Exclude call type 3 lamp for controlled traffic pos. 2.
		ϕϕϕ1	Light Exclude call type 4 lamp for controlled traffic pos. 2.

TABLE 3-Continued

CPU COMMANDS FOR POSITION 63 (ACTIVE COPY)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
4	ϕϕϕ1ϕϕ	1ϕϕϕ	Light Exclude call type 5 lamp for controlled traffic pos. 2.
		ϕ1ϕϕ	Light Exclude call type 6 lamp for controlled traffic pos. 2.
		ϕϕ1ϕ	Light Lamp 7 in Row 2 of Admin. Cabinet.
		ϕϕ1ϕ	Light Exclude call type 3 lamp for controlled pos. 5.
		ϕϕϕ1	Light Exclude call type 4 lamp for controlled pos. 5.
10	ϕϕ1ϕ1ϕ	1ϕϕϕ	Light Exclude call type 5 lamp for controlled pos. 5.
		ϕ1ϕϕ	Light Exclude call type 6 lamp for controlled pos. 5.
18	ϕ1ϕϕ1ϕ	ϕϕϕϕ	Extinguish all call exclusion lamps for controlled traffic pos. 2.
19	ϕ1ϕϕ11	ϕϕϕ1	Apply battery to lead S1L1 Steady.
		ϕϕ1ϕ	Apply battery to lead S1L2 Steady.
		ϕϕ11	Apply battery to lead S1L3 Steady.
		ϕ1ϕϕ	Apply battery to lead S1L4 Steady.
		ϕ1ϕ1	Apply battery to lead S1L5 Steady.
		ϕ11ϕ	Apply battery to lead S1L6 Steady.
19	ϕ1ϕϕ11	1ϕϕ1	Apply flashing battery to lead S1L1.
		1ϕ1ϕ	Apply flashing battery to lead S1L2.
		1ϕ11	Apply flashing battery to lead S1L3.
		11ϕ ϕ	Apply flashing battery to lead S1L4.
		11ϕ1	Apply flashing battery to lead S1L5.
		111ϕ	Apply flashing battery to lead S1L6.

NOTE: The above control group is spare.

20	ϕ1ϕ1ϕϕ	ϕϕϕ1	Short contact across leads RFT1.G and RFT1.S of Reference Trunk Circuit.
		ϕϕ1ϕ	Short contact across leads RFT2.G and RFT2.S of Reference Trunk Circuit.
		ϕϕ11	Short contact across leads RFT3.G and RFT3.S of Reference Trunk Circuit.
		ϕ11ϕϕ	Short contact across leads RFT4.G and RFT4.S of Reference Trunk Circuit.
		ϕ1ϕ1	Short contacts across leads RFT5.G and RFT5.S of Reference Trunk Circuit.
21	ϕ1ϕ1ϕ1	ϕϕϕϕ	Extinguish all call exclusion lamps for controlled traffic pos. 3.
22	ϕ1ϕ11ϕ	ϕϕϕϕ	Extinguish all call exclusion lamps for controlled traffic pos. 4.
23	ϕ1ϕ111	ϕϕϕ1	Light ACV Maximum lamp.
		ϕϕ1ϕ	Light ACV ON lamp.
		ϕϕ11	Light ACV ON and ACV Maximum lamps.
		ϕϕϕϕ	Extinguish all ACV lamps.
25	ϕ11ϕϕ1	1ϕϕϕ	Pull OOS Relay on TOCFϕ
		ϕ1ϕϕ	Pull OOS Relay on TOCF1
		ϕϕϕϕ	Restore both OOS Relays
27	ϕ11ϕ11	1ϕϕϕ	Enable Standby Key Scanner to collect Position Keying indications.
		ϕϕϕϕ	Disable Standby Key Scanner from collecting Position Keying indications.
28	ϕ111ϕϕ	ϕϕϕ1	Transfer Operators Audio Gp. 1 to standby audio facility.
		ϕϕ1ϕ	Transfer Operators Audio Gp. 2 to standby audio facility.
		ϕϕ11	Transfer Operators Audio Gp. 3 to standby audio facility.
		ϕ1ϕϕ	Transfer Operators Audio Gp. 4 to standby audio facility.
		ϕ1ϕ1	Transfer Operators Audio Gp. 5 to standby audio facility.
		ϕ11ϕ	Transfer Operators Audio Gp. 6 to standby audio facility.
		ϕ111	Transfer Operators Audio Gp. 7 to standby audio facility.
		1ϕϕϕ	Transfer Operators Audio Gp. 8 to standby audio facility.
		ϕϕϕϕ	Restore all operator's audio to normal facility.
29	ϕ111ϕ1	ϕϕϕϕ	Extinguish all call exclusion lamps for controlled traffic position 5.
30	ϕ1111ϕ	ϕ1ϕϕ	Apply battery to S4L1.
		ϕ11ϕ	Apply battery to S4L2.
		1ϕϕϕ	Apply battery flashing at 120 IPM to S4L1.
		1ϕ1ϕ	Apply battery flashing at 120 IPM to S4L2.
		11ϕϕ	Apply battery flashing at 30 IPM to S4L1.
		111ϕ	Apply battery flashing at 30 IPM to S4L2.
		ϕϕϕϕ	Remove power from S4L1 and S4L2.

NOTE: Control Group 30 is a spare control group.

31	ϕ11111	ϕϕϕϕ	Extinguish lamp 7 in Rows 1, 2, and 3.
32	1ϕϕϕϕϕ	ϕ1ϕϕ	Apply Battery to S5L1.
		ϕ11ϕ	Apply Battery to S5L2.
		1ϕϕϕ	Apply Battery flashing at 120 IPM to S5L1.
		1ϕ1ϕ	Apply Battery flashing at 120 IPM to S5L2.
		11ϕϕ	Apply Battery flashing to 30 IPM to S5L1.
		111ϕ	Apply Battery flashing to 30 IPM to S5L2.
		ϕϕϕϕ	Remove Power from S5L1 and S5L2.
33	1ϕϕϕϕ1	1ϕϕϕ	Energize Request Relay in CCFD.
		ϕϕϕϕ	De-energize Request Relay in CCFD.
34	1ϕϕϕϕ1	1ϕϕϕ	Light Overload Lamps.
		ϕϕϕϕ	Extinguish Overload lamps.
36	1ϕϕ1ϕ ϕ	ϕ1ϕϕ	Light Local Test lamp on TOTF Steady.
		1ϕϕϕ	Light Local Test lamp on TOTF flashing at 120 IPM.
		ϕϕϕϕ	Extinguish Local Test Lamp.
37	1ϕϕ1ϕ1	ϕ1ϕϕ	Reconfigure T.O.
38	1ϕϕ11ϕ	ϕ1ϕϕ	Activate PD1 Relay on CCFD.
		ϕϕϕϕ	DDrop PD1 Relay on CCFD.
39	1ϕϕ111	ϕϕ1ϕ	Light KPA (ACV) lamp on Admin. Cab. Steady.
		ϕ1ϕϕ	Light KPIL (EXCLUSION) lamp on Admin. Cab. Steady.
		ϕ1ϕ1	Light KPSL (Spare KP) lamp on Admin. Cab. Steady.
		1ϕ1ϕ	Light KPAL (ACV) lamp on Admin. Cab. Flashing.
		11ϕϕ	Light KPIL (EXCLUSION) lamp on Admin. Cab. Flashing.
		11ϕ1	Light KPSL (SPARE) lamp on Admin. Cab. Flashing.
4ϕ	1ϕ1ϕϕϕ	1ϕϕϕ	Light All CW (Call Waiting) lamps.
		ϕϕϕϕ	Extinguish all CW (Call Waiting) lamps.
41	1ϕ1ϕϕ1	1ϕϕϕ	Activate PDϕ Relay on CCFD.
		ϕϕϕϕ	Deactivate PDϕ Relay on CCFD.

TABLE 3-Continued

CPU COMMANDS FOR POSITION 63 (ACTIVE COPY)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
54	11ϕ11ϕ	ϕϕϕϕ	Reset SSC trouble relays and all CS fail FF's on active TOCF.
NOTE: The following CPU commands are intended for Position 63 (Standby Copy) only.			
1	ϕϕϕϕϕ1	1ϕϕϕ	Pull B12 twice pull test relay (Used to test B12 current sensors logic by pulling in the same relay twice without an intervening reset).
		ϕ1ϕϕ	Pull B13 twice pull test relay (Used to test B13 current sensor logic by pulling in the same B13 relay twice without an intervening reset).
		ϕϕ1ϕ	Pull B14 twice pull test relay (Used to test B14 current sensor logic by pulling in the same B14 relay twice without an intervening reset).
		ϕϕϕ1	Pull B15 twice test relay (Used to test B15 current sensor logic by pulling in the same B15 relay twice without an intervening reset).
		ϕϕϕϕ	Reset all B12–B15 twice pull test relays.
11	ϕϕ1ϕ11	1ϕϕϕ	Pull in two B12 test relays to test B12 current high detector and current Sensor Logic.
		ϕ1ϕϕ	Pull in two B13 test relays to test B13 Current high detector and Current Sensor Logic.
11	ϕϕ1ϕ11	ϕϕ1ϕ	Pull in two B14 test relays to test B14 Current high detector and Current Sensor Logic.
		ϕϕϕ1	Pul in two B15 test relays to test B15 Current high detector and Current Sensor Logic.
25	ϕ11ϕϕ1	ϕϕϕϕ	Reset all paired B12 to B15 test relays used for Current high tests. Reset RST twice pull test relay (Control Group 26).
26	ϕ11ϕ1ϕ	ϕϕϕϕ	Pull RST twice pull test relay (used to test RST current sensor logic by trying to pull in the same relay after first latching it up.)
27	ϕ11ϕ11	1ϕϕϕ	Enable Standby Key Scanner to collect Position Keying indications.
		ϕϕϕϕ	Disable Standby Key Scanner from collecting Position Keying indications.
35	1ϕϕϕ11	ϕϕϕϕ	Pull in two RST test relays to test RST current high detector and Current Sensor Logic.
37	1ϕϕ1ϕ1	ϕϕϕϕ	Reset RST test relay pair used for current high tests.
39	1ϕ1ϕϕ1	1ϕϕϕ	Pull in a B12 relay with three HQA relays across it to simulate a shorted diode and test B12 Current Sensor Logic.
		ϕ1ϕϕ	Pull in a B13 relay with 3 HQA relays across it to simulate a shorted diode and test B13 Current Sensor Logic.
		ϕϕ1ϕ	Pull in a B14 relay with 3 HQA relays across it to simulate a shorted diode and test B14 Current Sensor Logic.
		ϕϕϕ1	Pull in a B15 relay with 3 HQA relays across it to simulate a shorted diode and test B15 Current Sensor Logic.

TABLE 3 – Continued

CPU COMMANDS FOR POSITION 63 (ACTIVE COPY)

CONTROL GROUP NUMBER	CONTROL GROUP CODE B6–B11	STATUS CODE B12–B15	FUNCTION
54	11ϕ11ϕ	ϕϕϕϕ	Reset all Current Sensor Trouble FF's on standby TOCF.

TABLE 4

Traffic Office & Service Observation

FS No.	Equation	FS No.	Equation
1	CGϕ1·B12	24	CGϕ6·B14
2	CGϕ1·B13	25	CGϕ6·B15
3	CGϕ1·B14	26	CGϕ7·B12
4	CGϕ1·B15	27	CGϕ7·B13
5	CGϕ1·RST	28	CGϕ7·B14
6	CGϕ2·B12	29	CGϕ7·B15
7	CGϕ2·B13	3ϕ	CGϕ8·B12
8	CGϕ2·B14	31	CGϕ8·B13
9	CGϕ2·B15	32	CGϕ8·B14
1ϕ	CGϕ3·B12	33	CGϕ8·B15
11	CGϕ3·B13	34	CGϕ9·B12
12	CGϕ3·B14	35	CGϕ9·B13
13	CGϕ3·B15	36	CGϕ9·B14
14	CGϕ4·B12	37	CGϕ9·B15
15	CGϕ4·B13	38	CG1ϕ·B12
16	CGϕ4·B14	39	CG1ϕ·B13
17	CGϕ4·B15	4ϕ	CG1ϕ·B14
18	CGϕ 5·B12	41	CG1ϕ·B15
19	CGϕ5·B13	42	CG11·B12
2ϕ	CGϕ5·B14	43	CG11·B13
21	CGϕ5·B15	44	CG11·B14
22	CGϕ6·B12	45	CG11·B15
23	CGϕ6·B13	46	CG12·B12
47	CG12·B13	71	
48	CG12·B14	72	CG2ϕ·B14
49	CG12·B15	73	(CG2ϕ·RST)+R13
5ϕ	CG13·B12	74	CG21·B12
51	CG13·B13	75	(CG21·RST)+R13
52	CG13·B14	76	CG22·B12
53	CG13·B15	77	(CG23·RST)+R13
54	CG14·B12	78	CG23·B12
55	CG14·B13	79	CG23·B13
56	CG14·B14	8ϕ	(CG23·RST)+R14
57	CG14·B15	81	CG24·B12
58	CG14·RST	82	CG25·B12
59	CG15·B12	83	CG25·B13
6ϕ	CG15·B13	84	(CG25·RST)+R14
61	CG16·B12	85	CG26·B12
62	CG17·B12	86	CG26·B13
63	CG18·B12	87	CG26·RST
64	(CG18·RST)+R13	88	CG27·B12
65	CG19·B12	89	CG27·RST
66	CG19·B13	9ϕ	CG28·B12
67	CG19·B14	91	CG28·B13
68	CG19·B15	92	CG28·B14
69	CG19·RST	93	CG28·B15
7ϕ	CG2ϕ·B12	94	(CG28·RST)+R13
95	CG29·B12	119	
96	CG29·B13	12ϕ	
97	CG29·B14	121	CG37·B12
98	CG29·B15	122	CG37·B13
99	(CG29·RST)+R14	123	(CG37+CGϕ3)·RST
1ϕϕ	CG3ϕ·B12	124	CG38·B12
1ϕ1	CG3ϕ·B13	125	CG38·B13
1ϕ2	CG3ϕ·B14	126	(CG38+CGϕ4)·RST
1ϕ3	(CG3ϕ+CGϕ2)·RST	127	CG39·B12
1ϕ4	CG31·B12	128	CG39·B13
1ϕ5	CG31·B13	129	CG39·B14
1ϕ6	CG31·B14	13ϕ	CG39·B15
1ϕ7	(CG31+CGϕ3)·RST	131	(CG39·RST)+R13
1ϕ8	CG32·B12	132	CG4ϕ·B12
1ϕ9	CG32·B13	133	CG4ϕ·RST
11ϕ	CG32·B14	134	CG41·B12
111	(CG32+CGϕ4)·RST	135	(CG41·RST)+R13
112	CG33·B12	136	CG42·B12
113	(CG33+CGϕ2)·RST	137	CG42·B13
114	CG34·B12	138	CG42·B14
115	(CG34+CGϕ3)·RST	139	CG54·B12
116	CG35·B12	14ϕ	CG54·RST
117	(CG35+CGϕ4)·RST	141	CG55·B12
118	CG35·B12	142	CG2ϕ·B15

TABLE 5

FS No.	Service Observation FS Equation	FS No.	Equation
143	CG45·B12	16ϕ	CG49·B12
144	CG45·B13	161	CG49·B13
145	CG45·B14	162	CG49·B14
146	CG45·B15	163	CG49·B15
147	CG45·RST	164	CG5ϕ·B12
148	CG46·B12	165	CG5ϕ·B13
149	CG46·B13	166	CG5ϕ·B14
15ϕ	CG46·B14	167	CG5ϕ·B15
151	CG46·B15	168	CG51·B12
152	CG47·B12	169	CG51·B13
153	CG47·B13	17ϕ	CG51·B14
154	CG47·B14	171	CG51·B15
155	CG47·B15	172	CG52·RST
156	CG48·B12	173	CG52·B12
157	CG48·B13	174	CG53·RST
158	CG48·B14	175	CG53·B12
159	CG48·B15	176	CG53·B13
177	CG6ϕ·SDϕϕ	194	CG61·SDϕ3
178	CG6ϕ·SDϕ1	195	CG61·SDϕ4
179	CG6ϕ·SDϕ2	196	CG61·SDϕ5
18ϕ	CG6ϕ·SDϕ3	197	CG61·SDϕ6
181	CG6ϕ·SDϕ4	198	CG61·SDϕ7
182	CG6ϕ·SDϕ5	199	CG61·SDϕ8
183	CG6ϕ·SDϕ6	2ϕϕ	CG61·SDϕ9
184	CG6ϕ·SDϕ7	2ϕ1	CG61·SD1ϕ
185	CG6ϕ·SDϕ8	2ϕ2	CG61·SD11
186	CG6ϕ·SDϕ9	2ϕ3	CG61·SD12
187	CG6ϕ·SD1ϕ	2ϕ4	CG61·SD13
188	CG6ϕ·SD11	2ϕ5	CG59·SDϕϕ
189	CG6ϕ·SD12	2ϕ6	CG59·SDϕ1
19ϕ	CG6ϕ·SD13	2ϕ7	CG59·SDϕ2
191	CG61·SDϕϕ	2ϕ8	CG59·SDϕ3
192	CG61·SDϕ1	2ϕ9	CG59·SDϕ4
193	CG61·SDϕ2	21ϕ	CG59·SDϕ5

TABLE 6

RBϕ = Bϕ·RST (SHIFTED FROM
RB1 = B1·RST do.
RB2 = B2·RST do.
RB3 = B3·RST do.
RB4 = B4·RST do.
RB5 = B5·RST do.
REGRST = RST·(CG43+CG44) (SHIFTED FROM HTL TO MGS)
TST = CG43 (SHIFTED FROM HTL TO MGS)
MON = CG44 (SHIFTED FROM HTL TO MGS)
TBLRST = PD63·CG54·RST·(RTC·CR)(SHIFTED FROM HTL TO MGS)
RECON = PD63·CG37·(RTC·CR) (SHIFTED FROM HTL TO MGS)
BCC·PSF = CG63·(RTC·CR) (ALL HTL)
BCC·RRF = CG62·(RTC·CR) (ALL HTL)

NOTE: In the Tables:

RST	= B12·B13·B14·B15
R13	= CG13·RST
R14	= CG14·RST
CG(*n*)	= Control Group Number, Decoded Bits 6 to 11 (See Table 4)
SD(*n*)	= Status Decode Number, Decoded Bits 12 to 15 (See Table 5)
RTC·CR	= Command Ready Flag From RTC

What is claimed is:

1. A display buffer and control circuit for operating display devices and performing other functions at a plurality of positions in accordance with commands received on a set of leads, in commands having a format comprising a position field, a control group field, and a status field, each field comprising a plurality of bits with a lead for each bit in said set, there being N bits in the status field;

a position decoder having inputs from the leads for the position field and outputs of which one at a time is selected when the decoder is enabled, a plurality of first switch devices equal to the number of positions, each having an input coupled to an individual output of the position decoder, each first switch device being enabled when its position decoder output is selected to supply a first potential to an individual position select lead;

a decoding gate having inputs from all N status bit leads and an output to a reset status lead to provide a true signal condition on the reset status lead when all N of the status bits are zero;

a control group decoder having inputs from the leads for the control group field and outputs to control group leads of which one at a time is selected when the decoder is enabled;

a plurality of second switch devices, each having an enabling input, a source input, and an output to an individual function select lead, the input of each second switch device being coupled to the output of a function select gate having an input from a control group lead and an input from a status lead, organized into N + 1 status groups, all of the second switch devices in the same status group having their function select gates with an input to the same status bit lead, which for one group is the reset status lead, the source leads of all second switch devices being connected to a multiple point, with a resistor connected between the multiple point and a source of second potential, so that a second switch device when enabled supplies the second potential from the source via the resistor to its function select lead;

a decode enable lead connected to said position and control group decoders to normally enable them in response to a command ready signal;

a plurality of relays for each position organized into control groups, with at least **1** and not more than N function relays in each control group, and normally including also a reset relay, each relay having a winding and contacts, with one end of the winding coupled to a position select lead and the other end coupled via an isolation diode to a function select lead, each function relay having contacts which when the relay is operated disconnect it from the position select and function select leads and connect it to a locking path which includes break contacts of a reset relay usually in the same control group, and the reset relay having contacts which disconnect it from the position select lead and connect it to a locking path which includes make contacts in parallel for all of the function relays of the control group, so that when the reset relay is selected and operates, it releases the function relays and is then itself released when the function relays have restored, contacts of the function

relays connected to operate display devices according to a code of the status bits of each control group;

an individual current sensor for each said status group coupled to said resistor of its status group to sense the current through the resistor, each current sensor having a high output lead with means to supply a high signal thereon if the current exceeds a first threshold level, and a low output lead with means to supply a low signal thereon if the current exceeds a second lower threshold level, the normal current being as drawn by one relay being between the two threshold levels,

and logic means with connections to said output leads of the current sensors to detect and indicate various normal and abnormal conditions.

2. A circuit as claimed in claim **1,** wherein for some control groups no reset relay is provided, and the locking path for the function relays is via break contacts of the reset relay of another control group for the same position.

3. A circuit as claimed in claim **2,** wherein the reset status group of second switch devices includes some for which the function select gate is enabled in accordance with the signal condition on a plurality of control group leads.

4. A circuit as claimed in claim **3,** wherein said logic means includes means to disable certain responses to the reset current sensor for situations in which a plurality of reset relays are operated in response to the same command.

5. A circuit as claimed in claim **1,** wherein the abnormal conditions include some resulting from defective isolation diodes.

* * * * *