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Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

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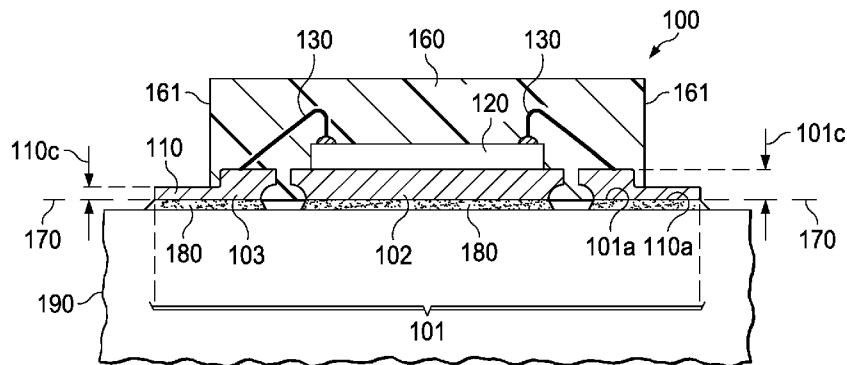


FIG. 1

(57) Abstract: In described examples, a semiconductor device (100) includes a metallic quad flat no-lead/small outline no-lead QFN/SON-type leadframe (101) with a pad (102) and multiple leads (103) with solderable surfaces (101a, 110a). At least one set of leads (103) is aligned in a row while having one surface in a common plane (170). Each lead of the set has a protrusion (110) shaped as a reduced-thickness metal sheet. A package (160) encapsulates the assembly and the leadframe (101). The package (160) material is shaped by sidewalls (161) with the row of leads (103) positioned along an edge of a sidewall (161), and the protrusions (110) extending away from the package sidewalls (161). The common plane (170) lead surfaces and the protrusions (110) remain un-encapsulated. The protruding metal sheets (110) are solder-attached along with the leads (103) to absorb thermomechanical stress.

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STRUCTURE AND METHOD OF PACKAGED SEMICONDUCTOR DEVICES
WITH QFN LEADFRAMES HAVING STRESS-ABSORBING PROTRUSIONS

[0001] This relates generally to semiconductor devices and processes, and more particularly to a structure and fabrication method of semiconductor devices with QFN/SON leadframes having extended leads.

BACKGROUND

[0002] The structure of contact pad metallizations and solder bumps for connecting integrated circuit (IC) chips to semiconductor packages or outside parts, and the thermomechanical stresses and reliability risks involved, have been described in a series of detailed publications, especially by IBM researchers (1969). During and after assembly of the IC chip to an outside part by solder reflow and then during device operation, significant temperature differences and temperature cycles appear between semiconductor chip and the substrate. The reliability of the solder joint is strongly influenced by the coefficients of thermal expansion of the semiconductor material and the substrate material. For example, more than one order of magnitude difference exists between the coefficients of thermal expansion of silicon and FR-4 and laminated boards. This difference causes thermomechanical stresses, which the solder joints have to absorb. Detailed calculations involving the optimum height and volume of the solder connection and the expected onset of fatigue and cracking proposed a number of solder design solutions.

[0003] The fabrication methods and reliability problems involving flip-chips re-appear in somewhat modified form for ball-grid array type packages and chip-scale and chip-size packages, which may be attached directly to a printed circuit board (PCB), or alternatively coupled to a second interconnection surface (such as an interposer). Attaching the ball grid array to the next interconnect is carried out by aligning the solder bumps or balls on the package to contact pads on the interconnection and then performing a solder reflow operation. During the reflow, the bumps or balls liquefy and make a bond to the next interconnect level, which has pads or traces to receive the solder. Following the solder reflow step, a polymeric underfill is often used between the package and the interposer (or PCB) to alleviate mechanical stress caused by the mismatch in the coefficients of thermal expansion (CTE) between the package, the

interposer, if any, and the PCB. Many reliability problems occur due to the stress placed on the solder bumps or balls when the assembly is cycled from hot to cool during operation.

[0004] In one method of drastically reducing the thermomechanical stress on the solder bumps, a sheet-like compliant elastomer substantially de-couples the solder bumps, affixed to the outside PCB, from the IC chip and the interposer, thereby relieving the thermal mismatch. Drawbacks of this method are assembly hurdles and cost considerations. Another method aims at absorbing part of the thermomechanical stress on the solder joints by plastic material surrounding the joints and filling the gap between chip and substrate. However, the underfilling method represents an unwelcome process step after device attachment to the motherboard.

[0005] In yet another wafer-level process, a flux-impregnated epoxy is screened on the wafer, with openings for the chip contact pads. The solder balls are placed on the pads. During the reflow process, the epoxy softens and forms a fillet, or collar, at the base of the solder ball, where stress-induced cracks typically originate. The wafer-level process with the required high temperature of solder reflow cannot be transferred to individual plastic packages.

[0006] The thermomechanical stress problems experienced at solder joints in ball-grid array devices re-appear in devices that use QFN/SON-type leadframes. The name of these leadframes (quad flat no-lead, small outline no-lead) indicates that the leads do not have cantilevered leads, but instead have flat leads, which are typically arrayed along the periphery of the packaged device. The metal of the leads is connected by solder material to the metal of respective contact pads of the external part. Even when the solder joints are formed by solder layers instead of solder balls, the nature of the thermomechanical stress at the joints derives from the mismatch of the coefficients of thermal expansion among the various materials. When plastic-packaged semiconductor devices with QFN/SON-type leadframes, attached to external parts by solder balls or solder layers, are subjected to accelerating reliability tests, such as temperature cycling, units may fail due to stress-induced microcracks through the solder joints.

SUMMARY

[0007] In described examples, a semiconductor device includes a metallic quad flat no-lead/small outline no-lead QFN/SON-type leadframe with a pad and multiple leads with solderable surfaces. At least one set of leads is aligned in a row while having one surface in a common plane. Each lead of the set has a protrusion shaped as a reduced-thickness metal sheet. A package encapsulates the assembly and the leadframe. The package material is shaped by

sidewalls with the row of leads positioned along an edge of a sidewall, and the protrusions extending away from the package sidewalls. The common-plane lead surfaces and the protrusions remain un-encapsulated. The protruding metal sheets are solder-attached along with the leads to absorb thermomechanical stress.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 illustrates a cross section of a packaged semiconductor device with a QFN/SON-type leadframe and straight lead-protrusions solder-attached to a substrate.

[0009] FIG. 2 shows a cross section of a portion of a QFN/SON-type leadframe strip with rails connecting respective leads of adjacent device sites.

[0010] FIG. 3 depicts a cross section of a portion of a leadframe strip with rails connecting respective leads and assembled semiconductor chips encapsulated in a packaging compound.

[0011] FIG. 4 illustrates a cross section of the leadframe strip of FIG. 3 during the process step of a saw blade cutting trenches into the packaging compound until reaching the rails.

[0012] FIG. 5 shows a cross section of the leadframe strip of FIG. 4 with trenches in the packaging compound cut to the rails.

[0013] FIG. 6 depicts a cross section of the leadframe strip of FIG. 5 during the process step of cleaning the trenches in the packaging compound.

[0014] FIG. 7 illustrates a cross section of a portion of the leadframe strip of FIG. 6 during the process step of cutting the rails in approximate halves, leaving a respective rail half as a protrusion attached to each lead.

[0015] FIG. 8 shows a cross section of a singulated device of the leadframe strip of FIG. 7, with the straight protrusions of the leads ready to act as stress-absorbing cantilevers in solder attachments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0016] The inventors' failure analysis of microcracks in solder joints of semiconductor devices with QFN/SON-type leadframes revealed that solder cracks typically originate in the region of high stress concentration in conjunction with small metal burrs created in the sawing or singulation processes of molded semiconductor packages. The sawing step after the packaging process uses rotating saws to form discrete devices from leadframe strips by sawing through the plastic compound and the metallic connecting rails between adjacent devices, fraying the metal into occasional burrs. Also, the inventors found that the burrs frequently hinder the forming of a

solder meniscus at the freshly exposed lead sidewalls, thereby depriving the nascent solder joint of strong fillets needed to create robust joints, which can withstand the high thermomechanical stresses during the reliability tests.

[0017] In the example embodiments, the problems of avoiding burrs and enabling robust solder meniscus are solved by a method of lead formation, which avoids burrs and enlarges the solderable area of the lead, so that strong solder fillets form automatically and solder joints with constrictions are avoided, and which also adds to the solder attachment the beneficial feature of a stress-absorbing spring-like cantilever. The method uses a leadframe strip, which has the leads of one device site, aligned in a row, connected by rails to respective leads of an adjacent site. The leads and rails of the row have solderable surfaces with one surface in a common plane. After encapsulating the strip in a packaging compound while leaving the leads and rails in the common plane un-encapsulated, a saw cuts trenches in the packaging compound between adjacent leads until the saw reaches the rails. Then, a sharp tool cuts the connecting rails in approximate halves, leaving a respective rail half as a straight metal protrusion attached to each lead. When the un-encapsulated device surface is attached to a substrate by a solder layer, the solder joints also form at the straight metal protrusions. Under thermomechanical stress, the protrusions react like absorbing springs.

[0018] Alternatively, the straight metal protrusions may be produced by other techniques, which include methods of creating trenches in package material by ablation or sputtering, and severing leadframe rails by cleaving or breaking.

[0019] FIG. 1 illustrates an example embodiment having a packaged semiconductor device 100 with a leadframe 101, which includes straight lead-protrusions 110. Device 100 including the protrusions is attached to a substrate 190 with solder 180. Metallic leadframe 101 is generally suitable for quad flat no-lead (QFN) and small outline no-lead (SON) type modules. For other devices, leadframe 101 may include other types of configurations. The leadframe includes a pad 102 and multiple leads 103. FIG. 2 indicates that the leadframe of a device 100 has at least one set of leads aligned in a row. The leadframe base metal is preferably made of copper or a copper alloy. Alternatively, the base metal may be aluminum, an iron/nickel alloy, or Kovar. One or more surfaces of the leadframe may be metallurgically prepared to facilitate solder attachment, such as by one or more layers of nickel, palladium, and gold sequentially plated onto the base metal.

[0020] Leadframe pad 102 is attached to a semiconductor chip 120, which is connected by bonding wires 130 to the leads 103. Leadframe 101, the assembled chip 120 and wires 130 are encapsulated by a package 160, which preferably employs (as package material) an epoxy-based polymeric compound suitable for transfer molding. The package material is shaped by sidewalls 161, so device 100 is preferably packaged in a housing with hexahedron shape. The one or more sets of leads aligned in rows are positioned along the edges of the package sidewalls.

[0021] The sheet of metal used for fabricating leadframe 101 is preferably planar. Consequently, surface 101a of pad 102 and leads 103 are in a common plane 170. Lead surfaces in the common plane remain un-encapsulated by package 160. The example embodiment of FIG. 1 has leads 103 positioned at the edge of package 160.

[0022] Each of these leads has as an addition formed as a protrusion 110, which is shaped as a sheet of metal extending away from the package sidewall 161. In FIG. 1, protrusion 110 has a thickness 110c smaller than thickness 101c of the leads. In other embodiments, thickness 110c may be equal to thickness 101c. The surface 110a of protrusion 110 is solderable. As FIG. 1 shows, protrusions 110 are planar and in the common plane 170. Protrusions 110 extend the area of leads 103 available for solder attachment to external parts. Due to their thinness and metallic composition, protrusions 110 are able to respond in spring-like fashion to expansions and contractions, and thereby to absorb thermomechanical stress imposed by outside forces and temperature variations.

[0023] FIG. 2 displays a strip 200 of an example metallic leadframe of the QFN/SON type, which includes multiple device sites. The leadframe portion of each device site has been designated with reference number 101. Leadframe portion 101 of each device site includes a pad 102 and multiple leads 103. At least one set of leads is aligned in a row. For a rectangular pad, four sets of leads may be arrayed in rows. As FIG. 2 shows, the leads of a row of one device site may be connected by rails 104 to respective leads of an adjacent site. Rails 104 will morph into protrusions 110 after the singulation step (see FIG. 7). The surfaces 104a of rails 104 and the surfaces 103a of aligned leads 103 are on a common plane, which has been designated with reference number 170 in FIG. 1. Also pad 102 has a surface on this common plane.

[0024] As stated above, the preferred base metal of the leadframe includes copper, but alternative metals include aluminum, iron-nickel alloys, and Kovar. Preferred thickness 101c of the leadframe base metal for the example embodiment of FIG. 1 is in a range from 0.2 mm to 0.3

mm, but other embodiments may use thicker or thinner leadframe metal. From the standpoint of low cost and batch processing, the technique preferably starts with sheet metal and fabricates the leadframe as a strip (see FIG. 2) by stamping or etching. As a consequence of the fact that the starting material is a sheet metal, leadframe pad 102, leads 103, and connecting rails 104 are in a common plane, designated with reference number 170. Preferably, the stamped leadframe is flood-plated with one or more layers of metals, which promote solder adhesion, such as nickel and palladium. A preferred metallurgy for good solder adhesion is a layer of nickel followed by a layer of palladium followed by a layer of gold. Alternatively, other metal layer may be used, such as a tin layer, in some applications in combination with other metals such a nickel. Also, for some devices, at least one surface may have a metal layer deposited to enhance thermal conductivity, such as by a plated layer of silver. The discrete devices are singulated from the leadframe strip by a trimming machine after the encapsulation process (see FIG. 7).

[0025] As the example embodiment of FIG. 2 shows, thickness 110c of the rails is preferably smaller than thickness 101c of the leads. Such reduced thickness can be obtained by an etching, planishing, or coining technique. Alternatively, in other embodiments, rails 104 may have the same thickness as leads 103.

[0026] Another embodiment includes a method of fabricating a semiconductor device using a QFN leadframe with stress-absorbing leads. The method starts by providing a metallic QFN/SON-type leadframe including multiple device sites. An example leadframe is illustrated in FIG. 2. Each site includes a pad and multiple leads with solderable surfaces. At least one set of leads is aligned in a row and connected by rails to respective leads of an adjacent site. The leads and rails of the row have a surface in a common plane.

[0027] In the fabrication flow, a semiconductor chip is attached on each pad 102 of the leadframe strip, and the chip terminals are connected to respective leads by bonding wires. Thereafter, the assembled strip is encapsulated in packages 160, preferably by a transfer molding technique using an epoxy-based polymeric molding compound. Removed from the mold, a portion of the strip may show a cross section as illustrated in FIG. 3. The sheet metal side, which was resting on the bottom mold, remains free of encapsulation compound and is therefore un-encapsulated; it is referred to as common plane.

[0028] In FIG. 4, a saw 401 is used for cutting trenches 402 between adjacent device sites by removing packaging material from the top 162 down until the connecting rails 104 are reached.

As FIG. 5 shows, the trench-cutting step creates gaps 501 between adjacent packages and sidewalls 161 of the device packages framing the connecting rails 104. FIG. 5 demonstrates that it is the process step of sawing a trench through the encapsulation material, which lays bare the rails and thereby creates the opportunity for forming the protrusions. FIG. 6 illustrates that it is preferred to employ a clean-up and deflashing step after the sawing process using a mechanical saw.

[0029] FIG. 7 depicts the process of singulating discrete device packages from the strip by cutting the connecting rails 104 between adjacent sites in approximate halves. The process uses a sharp cutting tool 701, but alternatively other cutting techniques may be used such as laser beams. The process leaves a respective rail half as a straight protrusion 110 attached to each lead.

[0030] As FIG. 8 shows, the singulation step creates discrete devices 100 with packages 160 and package sidewalls 161. Each lead 103 of the row of leads along the package periphery has an attached straight protrusion 110. The un-encapsulated surfaces of leads and protrusions are in common plane 170.

[0031] Referring to FIG. 1, as stated above, leadframe 101 preferably includes the rails between the device sites metallurgically prepared for easy solder attachment. While it may be sufficient to metallurgically prepare the un-encapsulated leadframe surface 101a, the most practical method is flood-plating of the whole leadframe after it has been stamped from the starting metal sheet. The solderable surfaces 101a and 110a are facing the solder 180. The additional solderable surface provided by the protrusion 110 extends the area of the respective lead 103 available for solder attachment to external parts, such as a printed circuit board. The inherent flexibility of the metal or alloy used as leadframe base material, combined with the reduced thickness of the protrusions, bestow compliant elastic characteristics upon the protrusions. Consequently, because of their thinness and metallic composition, protrusions 110 are able to respond in spring-like fashion to expansions and contractions during device operation, and to absorb thermomechanical stress imposed by outside forces and temperature variations.

[0032] Example embodiments are applicable to products using any type of semiconductor chip, discrete or integrated circuit, and the material of the semiconductor chip may include silicon, silicon germanium, gallium arsenide, or any other semiconductor or compound material used in integrated circuit manufacturing.

[0033] Also, example embodiments are applicable to any semiconductor device family that uses QFN/SON leadframes in strip format. The rails, which connect discrete device sites, can be singulated from the strip into discrete units, which have rail portions remaining as protrusions of the leads. These protrusions have solderable surfaces and are thereby robust enough to withstand thermomechanical stress after board attach.

[0034] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device package comprising:
 - a metallic quad flat no-lead/small outline no-lead QFN/SON-type leadframe having a pad and a plurality of leads with solderable surfaces, at least one set of leads aligned in a row while having one surface in a common plane, each lead of the set having a flat protrusion shaped as a metal sheet and one surface in the common plane;
 - a semiconductor chip assembled on the pad and connected to the leads; and
 - a package material encapsulating the assembly and the leadframe, the package material shaped by a plurality of package sidewalls with the row of leads positioned along an edge of a sidewall from the plurality of sidewalls and the flat protrusions extending away from the package sidewalls, the common-plane lead and protrusion surfaces remaining un-encapsulated.
2. The package of claim 1, wherein the sheet-like protrusions have a thickness smaller than the thickness of the leads.
3. The package of claim 1, wherein the protrusions have a thickness equal to the thickness of the leads.
4. The package of claim 1, wherein the package is shaped as a hexahedron, and the package walls are hexahedron walls.
5. A method of fabricating a semiconductor device, the method comprising:
 - providing a strip of metallic quad flat no-lead/small outline no-lead QFN/SON-type leadframes including a plurality of device sites, each site including a pad and a plurality of leads with solderable surfaces, at least one set of leads aligned in a row and connected by rails to respective leads of an adjacent site, the leads and rails of the row having a surface in a common plane, the strip with the assembled sites and connecting rails encapsulated in a packaging material, leaving the common-plane leads and rail surfaces un-encapsulated;
 - cutting trenches between adjacent sites by removing packaging material until reaching the rails, for creating sidewalls of device packages connected by rails; and
 - singulating the device packages from the strip by severing the connecting rails between adjacent sites in approximate halves, leaving a respective rail half as a straight protrusion attached to each lead.
6. The method of claim 5, wherein the cutting employs a mechanical saw.

7. The method of claim 6, wherein the singulating employs a mechanical cutting method.
8. The method of claim 5, wherein the providing further includes: for each site, providing a semiconductor device assembled on the pad and connected to respective leads.
9. The method of claim 5, wherein the package is shaped as a hexahedron, and the package sidewalls are hexahedron sidewalls.
10. The method of claim 5, wherein the rails have a thickness smaller than the thickness of the leads.
11. The method of claim 5, wherein the rails have a thickness equal to the thickness of the leads.

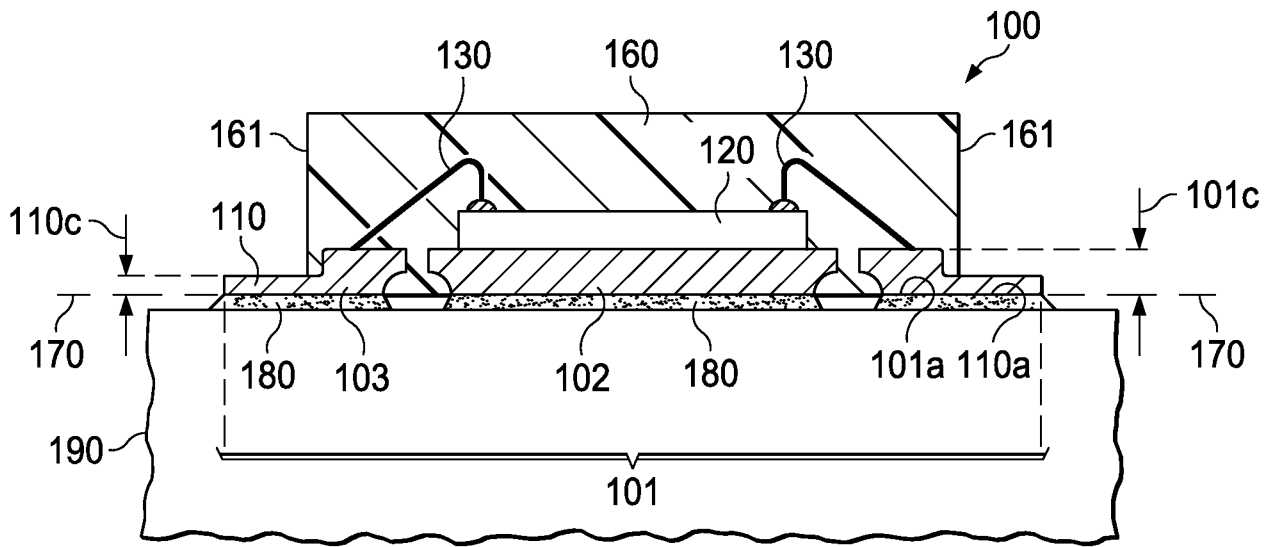


FIG. 1

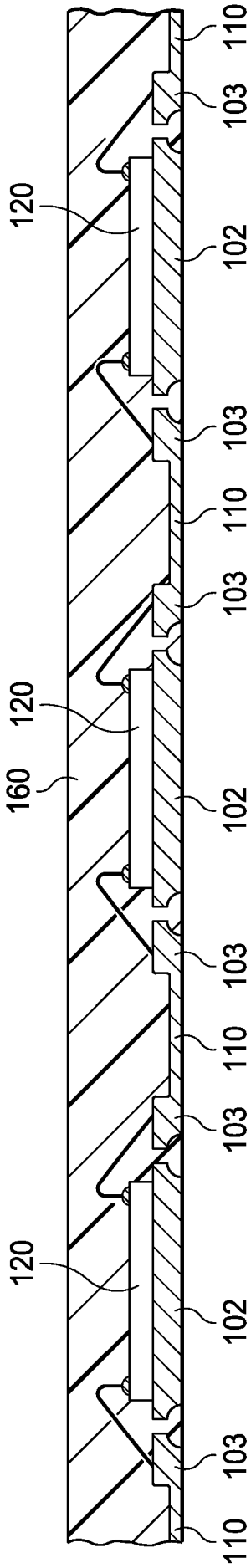


FIG. 3

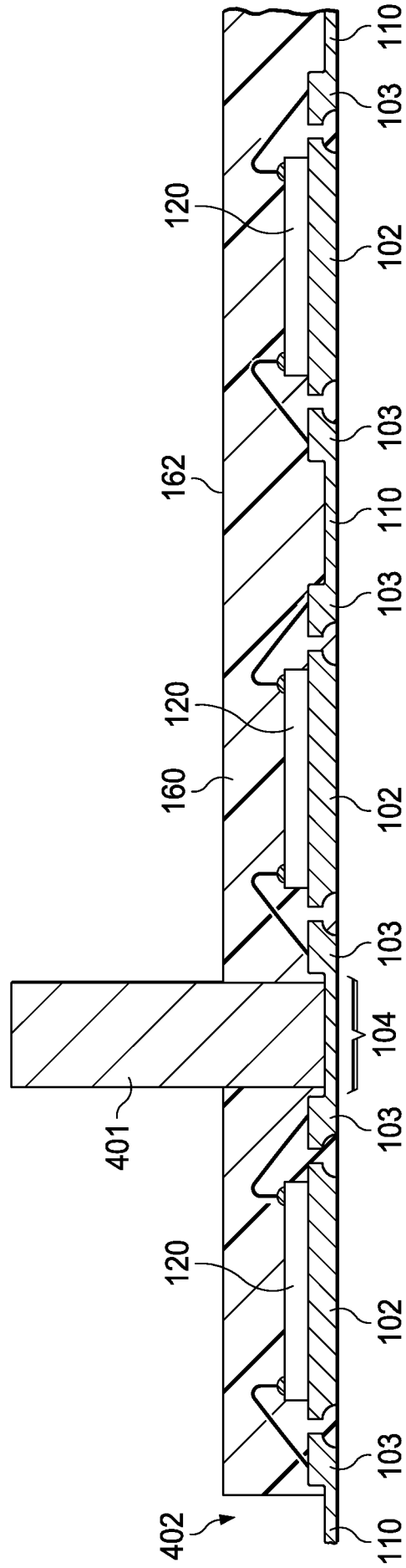


FIG. 4

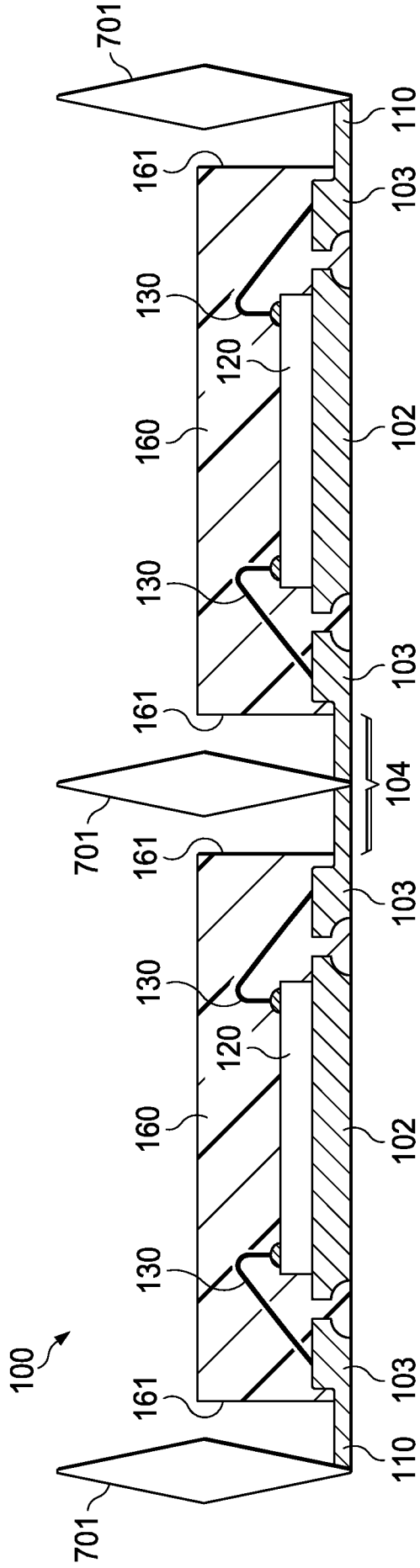


FIG. 7

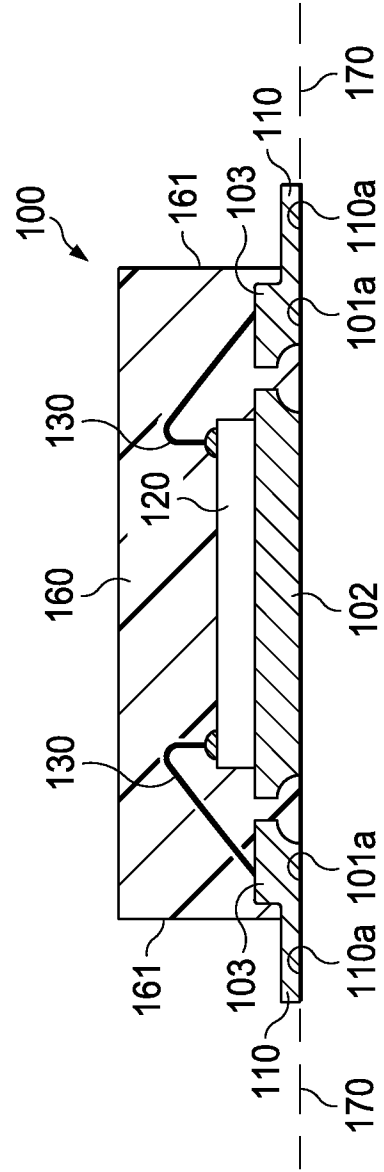


FIG. 8

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/495 (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/48-23/50, 23/28, 23/02, 21/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2001/0044169 A1 (SHOSHI YASUNAGA et al.) 22.11.2001	1-11
A	US 8242614 B2 (TEXAS INSTRUMENTS INCORPORATED) 14.08.2012	1-11
A	US 8624363 B2 (TEXAS INSTRUMENTS INCORPORATED) 07.01.2014	1-11
A	US 7608916 B2 (TEXAS INSTRUMENTS INCORPORATED) 27.10.2009	1-11
A	US 2006/0071351 A1 (TEXAS INSTRUMENTS INCORPORATED) 06.04.2006	1-11

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

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