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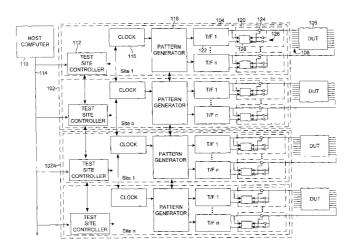
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(54) Title: STACKABLE SEMICONDUCTOR TEST SYSTEM AND METHOD FOR OPERATING SAME



(57) Abstract: A tester configured to stack with at least one other tester (102) fto provide a test system for simultaneously testing a number of devices in parallel on different testers (102), or testing a device having more pins than can be accommodated by a single tester (102). The tester (102) includes a test site (104) with a number of pin electronics channel (120), an interface (148) for interfacing with the device, and a computer for interfacing with a host computer (110) in the test system. The testers (102) can be fastened directly to one another or to a common frame. Preferably, the interface (148) enables a single device board (160) to simultaneously engage interfaces (148) on multiple testers (102). More preferably, the interface (148) extends from a top surface of the tester (102) to engage the device board (160). Vents (144,146) and front surfaces of an enclosure enables movement of air to cool components of the tester (102) without interference from testers (102) on either side or back of the enclosure.



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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

## INTERNATIONAL SEARCH REPORT

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Minimum documentation searched (classification system followed by classification symbols) U.S.: 324/158.1,73.1,760,765; 714/724,733; 165/80.3;			
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C. DOCUMENTS CONSIDERED TO BE RELEVANT			
Category *	Citation of document, with indication, where a	ppropriate, of the relevant passages	Relevant to claim No.
Α	US 4,729,246 A (MELGAARD ET AL.) 08 MARC	H 1988, See entire document.	1-43
A	US 5,650,732 A (SAKAI) 22 JULY 1997, see entire document.		1-43
	documents are listed in the continuation of Box C.	See patent family annex.	
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