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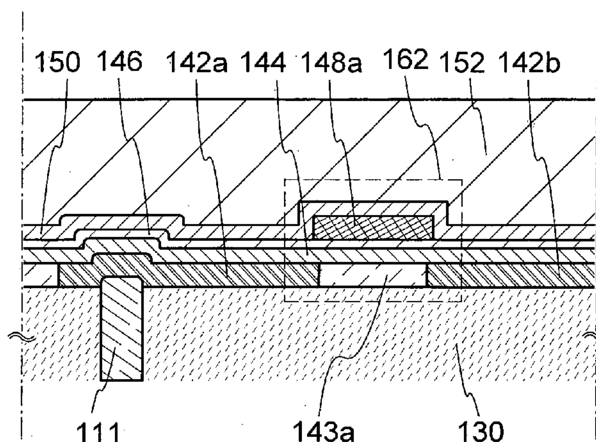
(54) Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

FIG. 1A



(57) Abstract: A semiconductor device includes a wiring embedded in an insulating layer, an oxide semiconductor layer over the insulating layer, a source electrode and a drain electrode electrically connected to the oxide semiconductor layer, a gate electrode provided to overlap with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode. The insulating layer is formed so that part of a top surface of the wiring is exposed. The part of the top surface of the wiring is positioned higher than part of a surface of the insulating layer. The wiring in a region exposed from the insulating layer is electrically connected to the source electrode or the drain electrode. The root-mean-square roughness of a region which is part of the surface of the insulating layer and in contact with the oxide semiconductor layer is 1 nm or less.

DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

5

TECHNICAL FIELD

[0001]

The technical field of the invention relates to a semiconductor device and a method for manufacturing the semiconductor device. Here, semiconductor devices
10 refer to general elements and devices which function by utilizing semiconductor characteristics.

BACKGROUND ART

[0002]

15 There are a wide variety of metal oxides and such metal oxides are used for various applications. Indium oxide is a well-known material and has been used as a material of transparent electrodes needed in liquid crystal display devices or the like.

[0003]

Some metal oxides have semiconductor characteristics. Examples of such
20 metal oxides having semiconductor characteristics are tungsten oxide, tin oxide, indium oxide, zinc oxide, and the like. A thin film transistor in which a channel formation region is formed using such a metal oxide is already known (e.g., see Patent Documents 1 to 4, Non-Patent Document 1, and the like).

[0004]

25 As metal oxides, not only single-component oxides but also multi-component oxides are known. For example, $InGaO_3(ZnO)_m$ (*m*: natural number) having a homologous series is known as a multi-component oxide semiconductor including In, Ga, and Zn (e.g., see Non-Patent Documents 2 to 4 and the like).

[0005]

30 Furthermore, it is confirmed that an oxide semiconductor including such an In-Ga-Zn-O-based oxide is applicable to a channel formation region of a thin film transistor (e.g., see Patent Document 5, Non-Patent Documents 5 and 6, and the like).

[0006]

In order to achieve high-speed operation or the like of a transistor, the transistor needs to be miniaturized. For example, Patent Document 6 discloses a thin film transistor in which the thickness of a channel layer including an oxide semiconductor is
5 approximately less than 10 nm, and Non-Patent Document 7 discloses a thin film transistor in which the length of a channel including an oxide semiconductor is 2 μm to 100 μm.

[Reference]

[Patent Document]

10 [0007]

[Patent Document 1] Japanese Published Patent Application No. S60-198861

[Patent Document 2] Japanese Published Patent Application No. H8-264794

[Patent Document 3] Japanese Translation of PCT International Application No. H11-505377

15 [Patent Document 4] Japanese Published Patent Application No. 2000-150900

[Patent Document 5] Japanese Published Patent Application No. 2004-103957

[Patent Document 6] Japanese Published Patent Application No. 2010-21170

[Non-Patent Document]

[0008]

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[Non-Patent Document 3] N. Kimizuka, M. Isobe, and M. Nakamura, "Syntheses and Single-Crystal Data of Homologous Compounds, $In_2O_3(ZnO)_m$ (m = 3, 4, and 5), $InGaO_3(ZnO)_3$, and $Ga_2O_3(ZnO)_m$ (m = 7, 8, 9, and 16) in the In_2O_3-$ZnGa_2O_4$-ZnO System", *J. Solid State Chem.*, 1995, Vol. 116, pp. 170-178

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[Non-Patent Document 7] T. Kawamura, H. Uchiyama, S. Saito, H. Wakana, T. Mine,
10 and M. Hatano, "Low-Voltage Operating Amorphous Oxide TFTs", IDW'09, pp. 1689-1692

DISCLOSURE OF INVENTION

[0009]

15 In the case where a transistor is miniaturized, a problem of a short-channel effect is caused. The short-channel effect refers to degradation of electric characteristics which becomes obvious with miniaturization of a transistor (a reduction in channel length (L)). The short-channel effect results from the effect of an electric field of a drain on a source. Specific examples of the short-channel effect are a
20 decrease in threshold voltage, an increase in subthreshold swing (S value), an increase in leakage current, and the like. In particular, since threshold voltage of a transistor including an oxide semiconductor cannot be controlled by impurity doping unlike a transistor including silicon, the short-channel effect tends to be caused easily.

[0010]

25 In the case where a transistor is miniaturized as described above, a wiring and a semiconductor element such as a transistor are formed in different layers so that a stacked-layer structure is obtained, whereby high integration of a semiconductor device can be achieved by utilizing the miniaturized transistor. However, a problem is caused in that contact resistance is increased in a contact between an electrode of the
30 miniaturized transistor and a wiring or an electrode of a semiconductor element in a different layer, resulting in an increase in the amount of heat generation or power consumption of the transistor.

[0011]

Therefore, an object of an embodiment of the disclosed invention is to provide a semiconductor device which is miniaturized with favorable characteristics maintained. Another object is to achieve three-dimensional high integration with favorable
5 characteristics of a miniaturized semiconductor device maintained.

[0012]

An embodiment of the disclosed invention is a semiconductor device including an insulating layer, a wiring embedded in the insulating layer, an oxide semiconductor layer over the insulating layer, a source electrode and a drain electrode electrically
10 connected to the oxide semiconductor layer, a gate electrode provided to overlap with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode. The insulating layer is formed so that at least part of a top surface of the wiring is exposed. The part of the top surface of the wiring is positioned higher than part of a surface of the insulating layer. The wiring in
15 the region exposed from the insulating layer is electrically connected to the source electrode or the drain electrode. The root-mean-square roughness of a region which is part of the surface of the insulating layer and is in contact with the oxide semiconductor layer is less than or equal to 1 nm.

[0013]

20 Note that in this specification and the like, a root-mean-square (RMS) roughness is obtained by three-dimensionally expanding the RMS roughness of a cross section curve so as to apply to a measurement surface. The RMS is expressed as the square root of the average value of squares of deviations from a reference surface to a specific surface, and can be obtained by the following formula.

25 [0014]

[Formula 1]

$$R_{ms} = \sqrt{\frac{1}{S_0}\int_{Y_1}^{Y_2}\int_{X_1}^{X_2}\{F(X,Y)-Z_0\}^2 dXdY}$$

[0015]

Note that the measurement surface is a surface which is shown by all the

measurement data, and is represented by the following formula.

[0016]

[Formula 2]

$$Z = F(X,Y)$$

5 [0017]

The specific surface is a surface which is an object of roughness measurement, and is a rectangular region which is surrounded by four points represented by the coordinates (X_1, Y_1), (X_1, Y_2), (X_2, Y_1), and (X_2, Y_2). The area of the specific surface is represented by S_0 when the specific surface is flat ideally. Note that S_0 is obtained

10 by the following formula.

[0018]

[Formula 3]

$$S_0 = |X_2 - X_1| \cdot |Y_2 - Y_1|$$

[0019]

15 In addition, the reference surface is a surface parallel to an X-Y plane at the average height of the specific surface. In other words, when the average value of the height of the specific surface is represented by Z_0, the height of the reference surface is also represented by Z_0. Note that Z_0 can be obtained by the following formula.

[0020]

20 [Formula 4]

$$Z_0 = \frac{1}{S_0} \int_{Y_1}^{Y_2} \int_{X_1}^{X_2} F(X,Y) dXdY$$

[0021]

Note that in this specification and the like, the root-mean-square (RMS) roughness is obtained by calculation conducted on a region of 10 nm × 10 nm,

25 preferably a region of 100 nm × 100 nm, further preferably a region of 1 μm × 1 μm, in an atomic force microscope (AFM) image obtained using an AFM.

[0022]

Another embodiment of the disclosed invention is a semiconductor device including an insulating layer, a wiring embedded in the insulating layer, an oxide semiconductor layer over the insulating layer, a source electrode and a drain electrode electrically connected to the oxide semiconductor layer, a gate electrode provided to 5 overlap with the oxide semiconductor layer, and a gate insulating layer provided between the oxide semiconductor layer and the gate electrode. The insulating layer is formed so that at least part of a top surface of the wiring is exposed. The part of the top surface of the wiring is positioned higher than part of a surface of the insulating layer. The wiring in the region exposed from the insulating layer is electrically 10 connected to the gate electrode. The root-mean-square roughness of a region which is part of the surface of the insulating layer and is in contact with the oxide semiconductor layer is less than or equal to 1 nm.

[0023]

Another embodiment of the disclosed invention is a semiconductor device 15 including a first insulating layer; a wiring embedded in the first insulating layer; a second insulating layer over the first insulating layer; a source electrode and a drain electrode embedded in the second insulating layer; an oxide semiconductor layer partly in contact with a surface of the second insulating layer, a surface of the source electrode, and a surface of the drain electrode; a gate insulating layer covering the oxide 20 semiconductor layer; and a gate electrode provided over the gate insulating layer to overlap with the oxide semiconductor layer. The first insulating layer is formed so that at least part of a top surface of the wiring is exposed. The part of the top surface of the wiring is positioned higher than part of a surface of the first insulating layer. The wiring in the region exposed from the first insulating layer is electrically connected to 25 the source electrode or the drain electrode. The root-mean-square roughness of a region which is part of the surface of the second insulating layer and is in contact with the oxide semiconductor layer is less than or equal to 1 nm.

[0024]

Note that part of a side surface of the wiring may also be exposed.

30 [0025]

Another embodiment of the disclosed invention is a semiconductor device including a first transistor, an insulating layer provided over the first transistor, and a

second transistor provided over the first transistor with the insulating layer positioned therebetween. The first transistor includes a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate electrode provided over the first gate insulating layer to overlap with the first channel formation 5 region, and a first source electrode and a first drain electrode electrically connected to the first channel formation region. The second transistor includes a second channel formation region including an oxide semiconductor layer, a second source electrode and a second drain electrode electrically connected to the second channel formation region, a second gate electrode provided to overlap with the second channel formation region, 10 and a second gate insulating layer provided between the second channel formation region and the second gate electrode. The insulating layer is formed over the first transistor so that at least part of a top surface of the first gate electrode is exposed. The part of the top surface of the first gate electrode is positioned higher than part of a surface of the insulating layer. The first gate electrode in the region exposed from the 15 insulating layer is electrically connected to the second source electrode or the second drain electrode. The root-mean-square roughness of a region which is part of the surface of the insulating layer and is in contact with the second channel formation region is less than or equal to 1 nm.

[0026]

20 Another embodiment of the disclosed invention is a semiconductor device including a first transistor, a first insulating layer provided over the first transistor, and a second transistor provided over the first transistor with the first insulating layer positioned therebetween. The first transistor includes a first channel formation region, a first gate insulating layer provided over the first channel formation region, a first gate 25 electrode provided over the first gate insulating layer to overlap with the first channel formation region, and a first source electrode and a first drain electrode electrically connected to the first channel formation region. The second transistor includes a second source electrode and a second drain electrode embedded in a second insulating layer; a second channel formation region which is partly in contact with a surface of the 30 second insulating layer, a surface of the second source electrode, and a surface of the second drain electrode and includes an oxide semiconductor layer; a second gate insulating layer covering the second channel formation region; and a second gate

electrode provided over the second gate insulating layer to overlap with the second channel formation region. The first insulating layer is formed over the first transistor so that at least part of a top surface of the first gate electrode is exposed. The part of the top surface of the first gate electrode is positioned higher than part of a surface of 5 the first insulating layer. The first gate electrode in the region exposed from the first insulating layer is electrically connected to the second source electrode or the second drain electrode. The root-mean-square roughness of a region which is part of the surface of the second insulating layer and is in contact with the second channel formation region is less than or equal to 1 nm.

10 [0027]

Note that part of a side surface of the first gate electrode may also be exposed. In addition, it is preferable that the first channel formation region and the second channel formation region include different semiconductor materials.

[0028]

15 Another embodiment of the disclosed invention is a method for manufacturing a semiconductor device, including the steps of forming a first insulating layer in which a wiring is embedded; performing planarization treatment on a surface of the first insulating layer so that the planarized first insulating layer partly has a surface with a root-mean-square roughness of less than or equal to 1 nm, at least part of a top surface 20 of the wiring is exposed, and the part of the top surface of the wiring is positioned higher than part of the surface of the first insulating layer; forming a source electrode and a drain electrode over the surfaces of the first insulating layer and the wiring so that the source electrode or the drain electrode is electrically connected to the wiring in the region exposed from the first insulating layer; forming a second insulating layer so as to 25 cover the source electrode and the drain electrode; performing planarization treatment on a surface of the second insulating layer so that the planarized second insulating layer partly has a surface with a root-mean-square roughness of less than or equal to 1 nm and at least part of top surfaces of the source electrode and the drain electrode is exposed; forming an oxide semiconductor layer partly in contact with the surface of the 30 planarized second insulating layer, a surface of the source electrode, and a surface of the drain electrode; forming a gate insulating layer covering the oxide semiconductor layer; and forming a gate electrode over the gate insulating layer so as to overlap with the

oxide semiconductor layer.

[0029]

Another embodiment of the disclosed invention is a method for manufacturing a semiconductor device, including the steps of forming a first transistor including a first channel formation region, a first gate insulating layer over the first channel formation region, a first gate electrode which is over the first gate insulating layer and overlaps with the first channel formation region, and a first source electrode and a first drain electrode electrically connected to the first channel formation region; forming a first insulating layer so as to cover the first transistor; performing planarization treatment on a surface of the first insulating layer so that the planarized first insulating layer partly has a surface with a root-mean-square roughness of less than or equal to 1 nm, at least part of a top surface of the first gate electrode is exposed, and the part of the top surface of the first gate electrode is positioned higher than part of the surface of the first insulating layer; forming a second source electrode and a second drain electrode over the surfaces of the first insulating layer and the first gate electrode so that the second source electrode or the second drain electrode is electrically connected to the first gate electrode in the region exposed from the first insulating layer; forming a second insulating layer so as to cover the second source electrode and the second drain electrode; performing planarization treatment on a surface of the second insulating layer so that the planarized second insulating layer partly has a surface with a root-mean-square roughness of less than or equal to 1 nm and at least part of top surfaces of the second source electrode and the second drain electrode is exposed; forming a second channel formation region which is partly in contact with the surface of the planarized second insulating layer, a surface of the second source electrode, and a surface of the second drain electrode and includes an oxide semiconductor layer; forming a second gate insulating layer covering the second channel formation region; and forming a second gate electrode over the second gate insulating layer so as to overlap with the second channel formation region.

[0030]

Note that the planarization treatment is preferably performed by CMP treatment.

[0031]

Note that a channel length L of the above transistor is preferably less than 2 μm, further preferably greater than or equal to 10 nm and less than or equal to 350 nm (0.35 μm). In addition, the thickness of the oxide semiconductor layer is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 2 nm and less than or equal to 20 nm, further preferably greater than or equal to 3 nm and less than or equal to 15 nm. Thus, a semiconductor device with high operation speed and low power consumption is realized. Further, a high dielectric constant material such as hafnium oxide is used for the gate insulating layer. For example, the relative permittivity of hafnium oxide is approximately 15 and the value is significantly large as compared to 3 to 4, which is the relative permittivity of silicon oxide. With the use of such a high dielectric constant material, a gate insulating layer having an equivalent oxide thickness of less than 15 nm, preferably greater than or equal to 2 nm and less than or equal to 10 nm, can be easily realized. That is, the semiconductor device can be easily miniaturized. Furthermore, a purified and intrinsic oxide semiconductor is used for the oxide semiconductor layer. Thus, the carrier density of the oxide semiconductor layer can be lower than 1×10^{12} /cm^3, preferably lower than 1.45×10^{10} /cm^3; the off-state current of the transistor can be less than or equal to 100 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A), preferably less than or equal to 10 zA/μm; and the S value of the transistor can be less than or equal to 65 mV/dec, preferably less than 63 mV/dec, for example. In the case where any of the above structures is employed, the off-state current of the transistor can be 1×10^{-24} A/μm to 1×10^{-30} A/μm in theory. The gate electrode may overlap with the source electrode and the drain electrode, or only ends of the gate electrode may overlap with an end of the source electrode and an end of the drain electrode.

[0032]

Here, semiconductor devices refer to general devices which function by utilizing semiconductor characteristics. For example, a display device, a memory device, an integrated circuit, and the like are included in the category of the semiconductor device.

[0033]

Note that in this specification and the like, the term "over" or "below" does not

necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" does not exclude the case where a component is placed between the gate insulating layer and the gate electrode.

5 [0034]

In addition, in this specification and the like, the term "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Moreover, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" is formed in an
10 integrated manner.

[0035]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flow is changed in circuit operation, for example. Therefore, the terms "source" and "drain"
15 can be replaced with each other in this specification.

[0036]

Note that in this specification and the like, the expression "electrically connected" includes the case where components are connected through an "object having any electric function". There is no particular limitation on an "object having
20 any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

25 [0037]

According to an embodiment of the disclosed invention, a channel formation region of a transistor is provided in an extremely flat region, whereby a problem such as a short-channel effect can be prevented even when the transistor is miniaturized and thus a transistor having favorable characteristics can be provided.

30 [0038]

Moreover, according to an embodiment of the disclosed invention, part of a top surface of a wiring or an electrode in a lower layer is formed in a higher position than

part of a surface of an insulating layer, whereby a reduction in the area of a portion where the wiring or the electrode in the lower layer is in contact with an electrode of a transistor in an upper layer can be prevented and thus the contact resistance between the wiring or the electrode in the lower layer and the electrode of the transistor in the upper
5 layer can be reduced. Accordingly, the amount of heat generation or power consumption of the transistor in the upper layer which is electrically connected to the wiring or the electrode in the lower layer can be reduced; therefore, the wiring or the electrode in the lower layer and the transistor in the upper layer can be stacked with the amount of heat generation or power consumption of the transistor in the upper layer
10 suppressed. Consequently, by forming a stacked-layer structure with the use of the miniaturized transistor and the wiring or the electrode, three-dimensional high integration of a semiconductor device can be achieved with favorable transistor characteristics maintained.

15 BRIEF DESCRIPTION OF DRAWINGS

[0039]

In the accompanying drawings:

FIGS. 1A and 1B are cross-sectional views illustrating examples of a structure of a semiconductor device;

20 FIGS. 2A and 2B are cross-sectional views illustrating examples of a structure of a semiconductor device;

FIGS. 3A to 3E are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 4A to 4C are cross-sectional views illustrating a manufacturing process
25 of a semiconductor device;

FIGS. 5A to 5C are a cross-sectional view, a plan view, and a circuit diagram, respectively, illustrating an example of a structure of a semiconductor device;

FIGS. 6A to 6C are a cross-sectional view, a plan view, and a circuit diagram, respectively, illustrating an example of a structure of a semiconductor device;

30 FIGS. 7A to 7D are cross-sectional views illustrating a manufacturing process of a semiconductor device;

FIGS. 8A to 8C are cross-sectional views illustrating a manufacturing process

of a semiconductor device;

FIGS. 9A to 9C are diagrams illustrating application examples of a semiconductor device;

FIGS. 10A and 10B are diagrams illustrating application examples of a semiconductor device;

FIGS. 11A to 11C are diagrams illustrating application examples of a semiconductor device;

FIGS. 12A to 12D are diagrams illustrating an application example of a semiconductor device;

FIG. 13 is a diagram illustrating an application example of a semiconductor device;

FIGS. 14A and 14B are diagrams illustrating an application example of a semiconductor device; and

FIGS. 15A to 15F are diagrams each illustrating an electronic device including a semiconductor device.

BEST MODE FOR CARRYING OUT THE INVENTION

[0040]

Examples of embodiments of the present invention will be described below with reference to the drawings. Note that the present invention is not limited to the following description and it will be easily understood by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not construed as being limited to the description in the following embodiments.

[0041]

Note that the position, the size, the range, or the like of each component illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, the size, the range, or the like disclosed in the drawings and the like.

[0042]

In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not

limit the components numerically.

[0043]

(Embodiment 1)

In this embodiment, a structure and a manufacturing method of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 1A and 1B, FIGS. 2A and 2B, FIGS. 3A to 3E, and FIGS. 4A to 4C.

[0044]

<Example of Structure of Semiconductor Device>

FIG. 1A illustrates an example of a structure of a semiconductor device including a transistor 162 which is formed over an insulating layer 130 where a wiring 111 is embedded and which is electrically connected to the wiring 111 via a source electrode 142a.

[0045]

The transistor 162 illustrated in FIG. 1A includes an insulating layer 143a formed over the insulating layer 130 where the wiring 111 is embedded; the source electrode 142a and a drain electrode 142b embedded in an insulating layer including the insulating layer 143a; an oxide semiconductor layer 144 partly in contact with a top surface of the insulating layer 143a, a top surface of the source electrode 142a, and a top surface of the drain electrode 142b; a gate insulating layer 146 covering the oxide semiconductor layer 144; and a gate electrode 148a over the gate insulating layer 146. Further, an insulating layer 150 and an insulating layer 152 may be formed over the transistor 162 so as to cover the gate insulating layer 146, the gate electrode 148a, and the like.

[0046]

The insulating layer 130 is formed so that at least part of a top surface of the wiring 111 is exposed. The part of the top surface of the wiring 111 is positioned higher than part of a surface of the insulating layer 130, and the wiring 111 in the region exposed from the insulating layer 130 is electrically connected to the source electrode 142a (drain electrode in some cases). Here, the insulating layer 130 and the wiring 111 are formed over a surface where a layer is formed, such as a surface of a substrate or the like, and part of the surface of the insulating layer 130 and the part of the top surface of

the wiring 111 have favorable planarity. The root-mean-square (RMS) roughness of the part of the surface of the insulating layer 130 is preferably less than or equal to 1 nm. The root-mean-square (RMS) roughness of the part of the top surface of the wiring 111 is preferably less than or equal to 2 nm. Note that in this specification, the part of the top surface of the wiring 111 refers to a region which is in the top surface of the wiring 111 and parallel to the surface where a layer is formed. In this specification, the part of the surface of the insulating layer 130 refers to a region which is in the surface of the insulating layer 130 and parallel to the surface where a layer is formed.

[0047]

In addition, the difference in height between the part of the top surface of the wiring 111 and the part of the surface of the insulating layer 130 is preferably 0.1 times to 5 times as large as the thickness of the gate insulating layer 146.

[0048]

By forming the part of the top surface of the wiring 111 in a higher position than the part of the surface of the insulating layer 130, a reduction in the area of a portion where the wiring 111 is in contact with the source electrode 142a can be prevented. For example, if the part of the top surface of the wiring 111 is formed in a lower position than the part of the surface of the insulating layer 130 as illustrated in FIG. 1B, a region which is in the top surface of the wiring 111 exposed from the insulating layer 130 and is not in contact with the source electrode 142a is easily formed. On the other hand, when the part of the top surface of the wiring 111 is formed in a higher position than the part of the surface of the insulating layer 130 as illustrated in FIG. 1A, the wiring 111 can be in contact with the source electrode 142a in the entire area of the top surface of the wiring 111 exposed from the insulating layer 130. Note that in the case where part of a side surface of the wiring 111 is also exposed from the insulating layer 130, the wiring 111 can also be in contact with the source electrode 142a in the part of the side surface of the wiring 111.

[0049]

Thus, by forming the part of the top surface of the wiring 111 in a higher position than the part of the surface of the insulating layer 130, a reduction in the area of a portion where the wiring 111 is in contact with the source electrode 142a can be prevented; accordingly, the contact resistance between the wiring 111 and the source

electrode 142a can be reduced. Moreover, since the part of the top surface of the wiring 111 has favorable planarity, adhesion between the wiring 111 and the source electrode 142a is favorable and thus the contact resistance can be further reduced. Consequently, the amount of heat generation or power consumption of the transistor 162 5 whose source electrode 142a is electrically connected to the wiring 111 can be reduced.

[0050]

Further, when the part of the top surface of the wiring 111 is exposed by CMP treatment or the like, an edge portion of the top surface of the wiring 111 can be polished and the edge portion of the top surface of the wiring 111 can have a smooth 10 shape, preferably a shape having a surface curved smoothly from the surface of the insulating layer 130 to a top end portion of the projecting wiring 111. By providing such a smooth curved surface on the top end portion of the wiring 111 which projects from the insulating layer 130, the wiring 111 and the source electrode 142a can be in close contact with each other without a space therebetween. Accordingly, the contact 15 resistance between the wiring 111 and the source electrode 142a can be further reduced. Furthermore, even when the thickness of the source electrode 142a is reduced, disconnection of the source electrode 142a in an intersection with the wiring 111 can be prevented.

[0051]

20 By forming the part of the top surface of the wiring 111 in a higher position than the part of the surface of the insulating layer 130, an interface between the wiring 111 and the source electrode 142a becomes not two-dimensional but three-dimensional; thus, adhesion between the wiring 111 and the source electrode 142a can be improved and the physical strength in attachment of the wiring 111 and the source electrode 142a 25 can be improved.

[0052]

By using an oxide semiconductor in an active layer of the transistor as illustrated in FIG. 1A, favorable characteristics can be obtained. For example, the S value of the transistor can be less than or equal to 65 mV/dec, preferably less than 63 30 mV/dec. In addition, as illustrated in FIG. 1A, a cross-sectional shape of a portion corresponding to a channel formation region of the oxide semiconductor layer which is used as the active layer of the transistor is preferably a flat shape.

[0053]

It is preferable that the root-mean-square (RMS) roughness of a region which is part of the top surface of the insulating layer 143a (the part particularly refers to a region parallel to a surface where a layer is formed) and in contact with the oxide semiconductor layer be less than or equal to 1 nm. It is preferable that the difference in height between an upper end portion of the insulating layer 143a and an upper end portion of the source electrode 142a, which are in contact with each other, or the difference in height between another upper end portion of the insulating layer 143a and an upper end portion of the drain electrode 142b, which are in contact with each other, be less than 5 nm.

[0054]

As described above, by providing the channel formation region of the transistor 162 in an extremely flat region whose root-mean-square (RMS) roughness is less than or equal to 1 nm, a problem such as a short-channel effect can be prevented even when the transistor 162 is miniaturized and thus the transistor 162 having favorable characteristics can be provided.

[0055]

Further, by increasing the planarity of the insulating layer 130, variation in the thickness of the oxide semiconductor layer 144 can be reduced and characteristics of the transistor 162 can be improved. Furthermore, degradation of coverage due to a large difference in height can be suppressed and disconnection (wiring disconnection) or a connection defect of the oxide semiconductor layer 144 can be prevented.

[0056]

Here, the oxide semiconductor layer 144 is preferably a purified oxide semiconductor layer obtained by sufficiently removing impurities such as hydrogen or sufficiently supplying oxygen. Specifically, the hydrogen concentration of the oxide semiconductor layer 144 is lower than or equal to 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, further preferably lower than or equal to 5×10^{17} atoms/cm^3, for example. Note that the hydrogen concentration of the oxide semiconductor layer 144 is measured by secondary ion mass spectrometry (SIMS). Thus, in the oxide semiconductor layer 144 in which the hydrogen concentration is

sufficiently reduced so that the oxide semiconductor layer is purified and defect levels in the energy gap due to oxygen deficiency are reduced by sufficient supply of oxygen, the density of carriers due to a donor such as hydrogen is lower than 1×10^{12} /cm^3, preferably lower than 1×10^{11} /cm^3, further preferably lower than 1.45×10^{10} /cm^3.
5 For example, the off-state current (here, current per micrometer (μm) of channel width) at room temperature (25 °C) is less than or equal to 100 zA (1 zA (zeptoampere) is 1×10^{-21} A), preferably less than or equal to 10 zA. In this manner, by using an i-type (intrinsic) or substantially i-type oxide semiconductor, the transistor 162 which has extremely favorable off-state current characteristics can be obtained. Further, by using
10 the i-type (intrinsic) or substantially i-type oxide semiconductor, a problem of the transistor caused owing to the thickness of the oxide semiconductor layer can be suppressed.

[0057]

Note that as disclosed in Non-Patent Document 7 or the like, a transistor
15 having a relatively large size of a channel length of 2 μm to 100 μm, for example, can be realized with the use of an n-type oxide semiconductor having a high carrier density of 2×10^{19} /cm^3; however, if such a material is used for a transistor which is miniaturized (to have a channel length of less than 2 μm), the threshold voltage thereof is largely shifted to a minus side and thus it is extremely difficult to realize a
20 normally-off transistor. In other words, a transistor which is manufactured using such a material and has a channel length of less than 2 μm is not suitable for practical use. In contrast, the carrier density of an oxide semiconductor that is purified and made intrinsic or substantially intrinsic is lower than 1×10^{14} /cm^3 at most, and the above-described problem in that the transistor is normally on does not occur;
25 accordingly, a transistor having a channel length of less than 2 μm can be easily realized.

[0058]

Note that the structure of a semiconductor device according to an embodiment of the disclosed invention is not limited to the structure of the semiconductor device
30 illustrated in FIG. 1A. Although the semiconductor device illustrated in FIG. 1A includes the transistor 162 which is electrically connected to the wiring 111 via the

source electrode 142a, a semiconductor device illustrated in FIG. 2A including the transistor 162 whose gate electrode 148a is electrically connected to the wiring 111 may be employed, for example. In the semiconductor device illustrated in FIG. 2A, the same reference numerals are used for portions common to those of the semiconductor
5 device illustrated in FIG. 1A.

[0059]

The semiconductor device illustrated in FIG. 2A includes the source electrode 142a electrically connected to the wiring 111; the drain electrode 142b; an electrode 156a which is formed in an opening provided in the oxide semiconductor layer 144, the
10 gate insulating layer 146, the insulating layer 150, and the insulating layer 152 and electrically connected to the source electrode 142a; a wiring 158 which is formed over the insulating layer 152 and electrically connected to the electrode 156a; and an electrode 156b which is formed in an opening provided in the insulating layer 150 and the insulating layer 152 and electrically connected to the wiring 158 and the gate
15 electrode 148a. Note that the other portions of the semiconductor device illustrated in FIG. 2A are similar to those of the semiconductor device illustrated in FIG. 1A. By employing such a structure, the semiconductor device can have a structure in which the gate electrode 148a of the transistor 162 and the wiring 111 formed in the lower layer are electrically connected to each other.

20 [0060]

In addition, although the semiconductor device illustrated in FIG. 1A has a structure in which the source electrode 142a and the drain electrode 142b are embedded in the insulating layer including the insulating layer 143a, the source electrode 142a and the drain electrode 142b may be formed over the insulating layer 130 without being
25 embedded in the insulating layer as illustrated in FIG. 2B, for example. In the semiconductor device illustrated in FIG. 2B, the same reference numerals are used for portions common to those of the semiconductor device illustrated in FIG. 1A.

[0061]

The semiconductor device illustrated in FIG. 2B has almost the same structure
30 as the semiconductor device illustrated in FIG. 1A, and includes the oxide semiconductor layer 144 formed over the insulating layer 130 where the wiring 111 is embedded, the source electrode 142a and the drain electrode 142b electrically connected

to the oxide semiconductor layer 144, the gate electrode 148a provided to overlap with the oxide semiconductor layer 144, and the gate insulating layer 146 provided between the oxide semiconductor layer 144 and the gate electrode 148a. Further, the insulating layer 150 and the insulating layer 152 may be formed over the transistor 162 so as to
5 cover the gate insulating layer 146, the gate electrode 148a, and the like. The insulating layer 130 is formed so that at least part of a top surface of the wiring 111 is exposed. The part of the top surface of the wiring 111 is positioned higher than part of a surface of the insulating layer 130, and the wiring 111 in the region exposed from the insulating layer 130 is electrically connected to the source electrode 142a or the drain
10 electrode 142b.

[0062]

Note that since the oxide semiconductor layer 144 is formed over and in contact with the insulating layer 130 in the semiconductor device illustrated in FIG. 2B, it is preferable that the root-mean-square (RMS) roughness of a region which is part of
15 the surface of the insulating layer 130 (the part particularly refers to a region parallel to a surface where a layer is formed) and in contact with the oxide semiconductor layer 144 be less than or equal to 1 nm.

[0063]

As illustrated in FIG. 2B, the source electrode 142a and the drain electrode
20 142b may be tapered in the transistor 162. The taper angle can be greater than or equal to 30° and less than or equal to 60°, for example. Note that the taper angle refers to an inclination angle formed with a side surface and a bottom surface of a layer having a tapered shape (e.g., the source electrode 142a or the drain electrode 142b) in the case where the layer is observed from a direction perpendicular to a cross section (a plane
25 perpendicular to the surface of the insulating layer 130).

[0064]

By applying a structure similar to that of the semiconductor device illustrated in FIG. 2A to the semiconductor device illustrated in FIG. 2B, the semiconductor device can have a structure in which the wiring 111 and the gate electrode 148a are electrically
30 connected to each other.

[0065]

<Example of Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the above semiconductor device will be described with reference to FIGS. 3A to 3E and FIGS. 4A to 4C. Here, FIGS. 3A to 3E and FIGS. 4A to 4C illustrate an example of a method for manufacturing the transistor 162 in FIG. 1A which is formed over the insulating layer 5 130 where the wiring 111 is embedded and electrically connected to the wiring 111 via the source electrode 142a.

[0066]

FIGS. 3A to 3E and FIGS. 4A to 4C will be described below. First, over a substrate having a surface where a layer is formed, the insulating layer 130 and the 10 wiring 111 embedded in the insulating layer 130 are formed (see FIG. 3A).

[0067]

Although there is no particular limitation on a substrate which can be used as the substrate having a surface where a layer is formed, it is necessary that the substrate have at least heat resistance enough to withstand heat treatment performed later. For 15 example, a substrate such as a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate can be used as a base. As long as the substrate has an insulating surface, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like; a compound semiconductor substrate of silicon germanium or the like; an SOI substrate; or the like can be used as the base. 20 Further, a structure in which a semiconductor element is provided over the substrate may be employed as the base. A base film may be formed over the substrate having a surface where a layer is formed.

[0068]

Note that it is preferable that the surface where a layer is formed of the 25 substrate be sufficiently flat. For example, a surface whose root-mean-square (RMS) roughness is less than or equal to 1 nm (preferably less than or equal to 0.5 nm) is employed as the surface where a layer is formed. By forming the transistor 162 over such a surface, characteristics thereof can be sufficiently improved. In the case where the planarity of the surface where a layer is formed of the substrate is insufficient, the 30 surface is preferably subjected to chemical mechanical polishing (CMP) treatment, etching treatment, or the like so as to have planarity that satisfies the above condition. For details of the CMP treatment, description of CMP treatment performed on an

insulating layer 143 later can be referred to.

[0069]

Here, the wiring 111 can be formed in such a manner that a conductive layer is formed over the surface where a layer is formed of the substrate and the conductive layer is selectively etched. The conductive layer can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. As a material of the conductive layer, an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, and tungsten; an alloy including any of these elements as a component; or the like can be used. A material including one of manganese, magnesium, zirconium, beryllium, neodymium, and scandium or a combination of any of these may be used. In addition, the conductive layer may have a single-layer structure or a stacked-layer structure including two or more layers.

[0070]

The insulating layer 130 is formed so as to cover the wiring 111. The insulating layer 130 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, or aluminum oxide. In particular, the insulating layer 130 is preferably formed using a low dielectric constant (low-k) material, whereby capacitance caused by an overlap of electrodes or wirings can be sufficiently reduced. Note that a porous insulating layer including any of these materials may be used for the insulating layer 130. Since the porous insulating layer has low dielectric constant as compared to a dense insulating layer, capacitance due to electrodes or wirings can be further reduced. Moreover, the insulating layer 130 can be formed using an organic insulating material such as polyimide or acrylic. Note that the insulating layer 130 has a single-layer structure in this embodiment; however, an embodiment of the disclosed invention is not limited to this. The insulating layer 130 may have a stacked-layer structure including two or more layers. For example, the insulating layer 130 may have a structure in which silicon oxynitride is stacked over silicon oxide. Only an inorganic insulating material including a large amount of oxygen, such as silicon oxynitride or silicon oxide, is used for the insulating layer 130, whereby CMP treatment can be easily performed on the insulating layer 130 in a later step.

[0071]

Note that in this specification, "silicon oxynitride" refers to a substance that includes more oxygen than nitrogen, and "silicon nitride oxide" refers to a substance that includes more nitrogen than oxygen.

[0072]

5 Next, planarization treatment is performed on a surface of the insulating layer 130; thus, the insulating layer 130 partly has a surface with a root-mean-square (RMS) roughness of less than or equal to 1 nm, at least part of a top surface of the wiring 111 is exposed, and the part of the top surface of the wiring 111 is formed in a higher position than part of the surface of the insulating layer 130 (see FIG. 3B). As the planarization 10 treatment for the insulating layer 130, chemical mechanical polishing (CMP) treatment is performed.

[0073]

Here, the CMP treatment is a method of planarizing a surface of an object to be processed by a combination of chemical and mechanical actions with the use of the 15 surface as a reference. In general, the CMP treatment is a method in which a polishing cloth is attached to a polishing stage, the polishing stage and the object to be processed are each rotated or swung while a slurry (an abrasive) is supplied between the object to be processed and the polishing cloth, and the surface of the object to be processed is polished by chemical reaction between the slurry and the surface of the object to be 20 processed and by action of mechanical polishing of the object to be processed with the polishing cloth.

[0074]

The CMP treatment may be performed once or plural times. When the CMP treatment is performed plural times, it is preferable that first polishing with a high 25 polishing rate be performed and then final polishing with a low polishing rate be performed. By combining polishing with different polishing rates in this manner, the planarity of the surface of the insulating layer 130 can be further improved.

[0075]

By the above CMP treatment, the root-mean-square (RMS) roughness of at 30 least part of the surface of the insulating layer 130 is preferably made to be less than or equal to 1 nm. The root-mean-square (RMS) roughness of the part of the top surface of the wiring 111 is preferably less than or equal to 2 nm.

[0076]

At this time, the surface of the insulating layer 130 is planarized, at least part of the top surface of the wiring 111 is exposed, and the part of the top surface of the wiring 111 is formed in a higher position than the part of the surface of the insulating layer 130. Here, the difference in height between the part of the top surface of the wiring 111 and the part of the surface of the insulating layer 130 is preferably 0.1 times to 5 times as large as the thickness of the gate insulating layer 146.

[0077]

Further, when the part of the top surface of the wiring 111 is exposed by the CMP treatment, an edge portion of the top surface of the wiring 111 can be polished and the edge portion of the top surface of the wiring 111 can have a smooth shape, preferably a shape having a surface curved smoothly from the surface of the insulating layer 130 to a top end portion of the projecting wiring 111. By providing such a smooth curved surface on the top end portion of the wiring 111 which projects from the insulating layer 130, the wiring 111 and the source electrode 142a can be in close contact with each other without a space therebetween. Accordingly, the contact resistance between the wiring 111 and the source electrode 142a can be further reduced. Furthermore, even when the thickness of the source electrode 142a is reduced, disconnection in an intersection with the wiring 111 can be prevented.

[0078]

Next, the source electrode 142a and the drain electrode 142b are formed over the surface of the insulating layer 130 so that the source electrode 142a or the drain electrode 142b is electrically connected to the wiring 111 in a region where the wiring 111 is exposed from the insulating layer 130 (see FIG. 3C).

[0079]

The source electrode 142a and the drain electrode 142b can be formed in such as manner that a conductive layer is formed over the insulating layer 130 so as to be in contact with the wiring 111 and the conductive layer is selectively etched.

[0080]

The above conductive layer can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. As a material of the conductive layer, an element selected from aluminum, chromium, copper, tantalum,

titanium, molybdenum, and tungsten; an alloy including any of these elements as a component; or the like can be used. A material including one of manganese, magnesium, zirconium, beryllium, neodymium, and scandium or a combination of any of these may be used.

5 [0081]

The conductive layer may have a single-layer structure or a stacked-layer structure including two or more layers. For example, a single-layer structure of a titanium film or a titanium nitride film, a single-layer structure of an aluminum film including silicon, a two-layer structure in which a titanium film is stacked over an

10 aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked, and the like can be given. Note that in the case where the conductive layer has a single-layer structure of a titanium film or a titanium nitride film, there is an advantage in that the conductive layer is easily processed into the source

15 electrode 142a and the drain electrode 142b having tapered shapes.

[0082]

Alternatively, the conductive layer may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an indium oxide-tin oxide alloy (In_2O_3-SnO_2, which is abbreviated to ITO

20 in some cases), an indium oxide-zinc oxide alloy (In_2O_3-ZnO), or any of these metal oxide materials including silicon or silicon oxide can be used.

[0083]

Note that the conductive layer may be etched either by dry etching or wet etching; however, dry etching is preferable for miniaturization because its controllability

25 is favorable. Further, the etching may be performed so that the source electrode 142a and the drain electrode 142b are tapered. The taper angle can be greater than or equal to 30° and less than or equal to 60°, for example.

[0084]

The channel length (L) of the transistor 162 is determined by a distance

30 between an upper end portion of the source electrode 142a and an upper end portion of the drain electrode 142b. Note that for light exposure for forming a mask used in the case where a transistor with a channel length (L) of less than 25 nm is formed, it is

preferable to use extreme ultraviolet rays whose wavelength is as short as several nanometers to several tens of nanometers. In the light exposure with extreme ultraviolet rays, the resolution is high and the focus depth is large. For these reasons, the channel length (L) of the transistor formed later can be less than 2 μm, preferably greater than or equal to 10 nm and less than or equal to 350 nm (0.35 μm), and the circuit can operate at higher speed. Moreover, miniaturization can lead to low power consumption of the semiconductor device.

[0085]

As described above, by forming the part of the top surface of the wiring 111 in a higher position than the part of the surface of the insulating layer 130, a reduction in the area of a portion where the wiring 111 is in contact with the source electrode 142a can be prevented; thus, the contact resistance between the wiring 111 and the source electrode 142a can be reduced. Moreover, since the part of the top surface of the wiring 111 has favorable planarity, adhesion between the wiring 111 and the source electrode 142a is favorable; accordingly, the contact resistance can be further reduced. Consequently, the amount of heat generation or power consumption of the transistor 162 whose source electrode 142a is electrically connected to the wiring 111 can be reduced.

[0086]

When the part of the top surface of the wiring 111 is formed in a higher position than the part of the surface of the insulating layer 130, a region of the source electrode 142a, which overlaps with the wiring 111, projects as illustrated in FIG. 3C; this portion can be removed by CMP treatment or the like so that a top surface of the source electrode 142a is planarized. By this treatment, the contact resistance between the oxide semiconductor layer 144 formed in a later step and the source electrode 142a can be reduced; therefore, the amount of heat generation or power consumption of the transistor 162 can be reduced and the mobility of the transistor 162 can be improved. Moreover, it is possible to prevent disconnection (wiring disconnection) or the like of the oxide semiconductor layer 144 or the gate insulating layer 146 due to a difference in height.

[0087]

Next, the insulating layer 143 is formed so as to cover the source electrode

142a and the drain electrode 142b (see FIG. 3D).

[0088]

The insulating layer 143 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, or aluminum oxide. It is particularly preferable that the insulating layer 143 be formed using silicon oxide because the insulating layer 143 is in contact with the oxide semiconductor layer 144 later. There is no particular limitation on a formation method of the insulating layer 143; in consideration of the fact that the insulating layer 143 is in contact with the oxide semiconductor layer 144, a method in which hydrogen is sufficiently reduced is preferably employed. An example of such a method is a sputtering method. Needless to say, another film formation method, typically a plasma CVD method, may be employed.

[0089]

Next, the insulating layer 143 is planarized by chemical mechanical polishing (CMP) treatment, so that the insulating layer 143a is formed (see FIG. 3E). Here, the CMP treatment is performed under the condition where at least part of surfaces of the source electrode 142a and the drain electrode 142b is exposed. In addition, the CMP treatment is performed under the condition where the root-mean-square (RMS) roughness of a surface of the insulating layer 143a is less than or equal to 1 nm (preferably less than or equal to 0.5 nm). By performing the CMP treatment under such conditions, the planarity of a surface where the oxide semiconductor layer 144 is formed later is improved and characteristics of the transistor 162 can be improved.

[0090]

Note that the CMP treatment may be performed only once or plural times. When the CMP treatment is performed plural times, it is preferable that first polishing with a high polishing rate be performed and then final polishing with a low polishing rate be performed. By combining polishing with different polishing rates in this manner, the planarity of the surface of the insulating layer 143a can be further improved.

[0091]

By the above CMP treatment, the difference in height between an upper end portion of the insulating layer 143a and an upper end portion of the source electrode

142a, which are in contact with each other, or the difference in height between another upper end portion of the insulating layer 143a and an upper end portion of the drain electrode 142b, which are in contact with each other, can be less than 5 nm.

[0092]

5 Note that a high stress is applied to an interface between the source electrode 142a and the wiring 111 in the CMP treatment in some cases. However, the interface between the wiring 111 and the source electrode 142a has a three-dimensional structure, whereby adhesion between the wiring 111 and the source electrode 142a is improved and the physical strength in attachment of the wiring 111 and the source electrode 142a 10 is improved. Therefore, the CMP treatment can be performed without peeling of the source electrode 142a.

[0093]

Next, the oxide semiconductor layer 144 is formed so as to be partly in contact with a top surface of the source electrode 142a, a top surface of the drain electrode 142b, 15 and a top surface of the insulating layer 143a, and then the gate insulating layer 146 is formed so as to cover the oxide semiconductor layer 144 (see FIG. 4A).

[0094]

The oxide semiconductor layer 144 can be formed using an In-Sn-Ga-Zn-O-based material which is a four-component metal oxide; an 20 In-Ga-Zn-O-based material, an In-Sn-Zn-O-based material, an In-Al-Zn-O-based material, a Sn-Ga-Zn-O-based material, an Al-Ga-Zn-O-based material, or a Sn-Al-Zn-O-based material which is a three-component metal oxide; an In-Zn-O-based material, a Sn-Zn-O-based material, an Al-Zn-O-based material, a Zn-Mg-O-based material, a Sn-Mg-O-based material, or an In-Mg-O-based material which is a 25 two-component metal oxide; an In-O-based material, a Sn-O-based material, or a Zn-O-based material which is a one-component metal oxide; or the like.

[0095]

In particular, an In-Ga-Zn-O-based oxide semiconductor material has a sufficiently high resistance when there is no electric field and thus a sufficiently low 30 off-state current can be obtained. In addition, having high field-effect mobility, the In-Ga-Zn-O-based oxide semiconductor material is suitable for a semiconductor device.

[0096]

As a typical example of the In-Ga-Zn-O-based oxide semiconductor material, one represented by $InGaO_3(ZnO)_m$ ($m > 0$) is given. Moreover, there is an oxide semiconductor material represented by $InMO_3(ZnO)_m$ ($m > 0$), using M instead of Ga. Here, M denotes one or more metal elements selected from gallium (Ga), aluminum
5 (Al), iron (Fe), nickel (Ni), manganese (Mn), cobalt (Co), and the like. For example, M can be Ga, Ga and Al, Ga and Fe, Ga and Ni, Ga and Mn, Ga and Co, or the like. Note that the above compositions are derived from the crystal structures that the oxide semiconductor material can have and are only examples.

[0097]

10 In the case where an In-Zn-O-based material is used as the oxide semiconductor, the composition ratio of a target used is In: Zn = 50:1 to 1:2 in an atomic ratio (In_2O_3: ZnO = 25:1 to 1:4 in a molar ratio), preferably In: Zn = 20:1 to 1:1 in an atomic ratio (In_2O_3: ZnO = 10:1 to 1:2 in a molar ratio), further preferably In: Zn = 15:1 to 1.5:1 in an atomic ratio (In_2O_3: ZnO = 15:2 to 3:4 in a molar ratio). For example, in
15 a target used for formation of an In-Zn-O-based oxide semiconductor which has an atomic ratio of In:Zn:O = X:Y:Z, the relation of $Z > 1.5X+Y$ is satisfied.

[0098]

As a target for forming the oxide semiconductor layer 144 by a sputtering method, it is preferable to use a target that is represented by a composition ratio of
20 In:Ga:Zn = 1:x:y (x is greater than or equal to 0, and y is greater than or equal to 0.5 and less than or equal to 5). For example, a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:2 [molar ratio] (x = 1, y = 1) or the like can be used. Alternatively, a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1 [molar ratio] (x = 1, y = 0.5), a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:4
25 [molar ratio] (x = 1, y = 2), or a target having a composition ratio of In_2O_3:Ga_2O_3:ZnO = 1:0:2 [molar ratio] (x = 0, y = 1) can be used.

[0099]

In this embodiment, the oxide semiconductor layer 144 having an amorphous structure is formed by a sputtering method using a target for forming an
30 In-Ga-Zn-O-based oxide semiconductor. In addition, the thickness thereof is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to

2 nm and less than or equal to 20 nm, further preferably greater than or equal to 3 nm and less than or equal to 15 nm.

[0100]

The relative density of a metal oxide in the target for forming an oxide semiconductor is 80 % or higher, preferably 95 % or higher, further preferably 99.9 % or higher. With the use of a target for forming an oxide semiconductor with high relative density, an oxide semiconductor layer having a dense structure can be formed.

[0101]

The atmosphere in which the oxide semiconductor layer 144 is formed is preferably a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere including a rare gas (typically argon) and oxygen. Specifically, it is preferable to use, for example, an atmosphere of a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or hydride is removed so that the concentration is 1 ppm or lower (preferably the concentration is 10 ppb or lower).

[0102]

In forming the oxide semiconductor layer 144, for example, an object to be processed is held in a treatment chamber kept under reduced pressure and the object to be processed is heated to a temperature of higher than or equal to 100 °C and lower than 550 °C, preferably higher than or equal to 200 °C and lower than or equal to 400 °C. Alternatively, the temperature of the object to be processed in the formation of the oxide semiconductor layer 144 may be room temperature (25 °C ± 10 °C). Then, moisture in the treatment chamber is removed, a sputtering gas from which hydrogen, water, and the like are removed is introduced, and the above target is used, so that the oxide semiconductor layer 144 is formed. By forming the oxide semiconductor layer 144 while heating the object to be processed, impurities in the oxide semiconductor layer 144 can be reduced. In addition, damage on the oxide semiconductor layer 144 due to sputtering can be reduced. In order to remove moisture in the treatment chamber, an entrapment vacuum pump is preferably used. For example, a cryopump, an ion pump, a titanium sublimation pump, or the like can be used. A turbo pump provided with a cold trap may be used. By evacuation with a cryopump or the like, hydrogen, water, and the like can be removed from the treatment chamber; thus, the impurity

concentration of the oxide semiconductor layer can be reduced.

[0103]

The oxide semiconductor layer 144 can be formed under the following conditions, for example: the distance between the object to be processed and the target is 170 mm, the pressure is 0.4 Pa, the direct current (DC) power is 0.5 kW, and the atmosphere is an oxygen (oxygen: 100 %) atmosphere, an argon (argon: 100 %) atmosphere, or a mixed atmosphere including oxygen and argon. Note that a pulsed direct current (DC) power source is preferably used because powder substances (also referred to as particles or dust) generated in film formation can be reduced and variation in thickness can be reduced. The thickness of the oxide semiconductor layer 144 is greater than or equal to 1 nm and less than or equal to 50 nm, preferably greater than or equal to 2 nm and less than or equal to 20 nm, further preferably greater than or equal to 3 nm and less than or equal to 15 nm. With the structure according to the disclosed invention, a short-channel effect due to miniaturization can be suppressed even when the oxide semiconductor layer 144 has such a thickness. Note that the appropriate thickness differs depending on the oxide semiconductor material to be used, the intended use of the semiconductor device, or the like; therefore, the thickness may be determined in accordance with the material, the intended use, or the like. By forming the insulating layer 143a in the above manner, a surface where a portion corresponding to a channel formation region of the oxide semiconductor layer 144 is formed can be sufficiently planarized; accordingly, even an oxide semiconductor layer having a small thickness can be favorably formed. In addition, as illustrated in FIG. 4A, a cross-sectional shape of the portion corresponding to the channel formation region of the oxide semiconductor layer 144 is preferably a flat shape. By making the cross-sectional shape of the portion corresponding to the channel formation region of the oxide semiconductor layer 144 flat, leakage current can be reduced as compared to the case where the cross-sectional shape of the oxide semiconductor layer 144 is not flat.

[0104]

Note that before the oxide semiconductor layer 144 is formed by a sputtering method, a substance attached to a surface where the oxide semiconductor layer 144 is formed (e.g., the surface of the insulating layer 143a) may be removed by reverse

sputtering in which an argon gas is introduced and plasma is generated. Here, the reverse sputtering is a method in which ions collide with a surface to be processed so that the surface is modified, in contrast to normal sputtering in which ions collide with a sputtering target. An example of a method for making ions collide with a surface to be
5 processed is a method in which high-frequency voltage is applied to the surface to be processed side in an argon atmosphere so that plasma is generated in the vicinity of the object to be processed. Note that a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used instead of an argon atmosphere.

[0105]

10 After the formation of the oxide semiconductor layer 144, heat treatment (first heat treatment) is preferably performed on the oxide semiconductor layer 144. Excessive hydrogen (including water and a hydroxyl group) in the oxide semiconductor layer 144 can be removed by the first heat treatment, so that the structure of the oxide semiconductor layer 144 can be ordered and defect levels in the energy gap can be
15 reduced. The temperature of the first heat treatment is, for example, higher than or equal to 300 °C and lower than 550 °C, preferably higher than or equal to 400 °C and lower than or equal to 500 °C.

[0106]

The heat treatment can be performed in such a manner that, for example, an
20 object to be processed is introduced into an electric furnace in which a resistance heating element or the like is used and heated at 450 °C for 1 hour in a nitrogen atmosphere. During the heat treatment, the oxide semiconductor layer is not exposed to the air to prevent the entry of water and hydrogen.

[0107]

25 The heat treatment apparatus is not limited to the electric furnace and may be an apparatus for heating an object to be processed by thermal conduction or thermal radiation from a medium such as a heated gas. For example, a rapid thermal annealing (RTA) apparatus such as a lamp rapid thermal annealing (LRTA) apparatus or a gas rapid thermal annealing (GRTA) apparatus can be used. An LRTA apparatus is an
30 apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc

lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. A GRTA apparatus is an apparatus for performing heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, such as nitrogen or a rare gas such as argon, is used.

5 [0108]

For example, as the first heat treatment, GRTA treatment may be performed in the following manner. The object to be processed is put in an inert gas atmosphere that has been heated, heated for several minutes, and taken out of the inert gas atmosphere. The GRTA treatment enables high-temperature heat treatment in a short time.
10 Moreover, GRTA treatment can be employed even when the temperature exceeds the upper temperature limit of the object to be processed. Note that the inert gas may be switched to a gas including oxygen during the treatment. This is because defect levels in the energy gap due to oxygen deficiency can be reduced by performing the first heat treatment in an atmosphere including oxygen.

15 [0109]

Note that as the inert gas atmosphere, an atmosphere that includes nitrogen or a rare gas (such as helium, neon, or argon) as a main component and does not include water, hydrogen, or the like is preferably used. For example, the purity of nitrogen or a rare gas such as helium, neon, or argon introduced into the heat treatment apparatus is
20 higher than or equal to 6N (99.9999 %), preferably higher than or equal to 7N (99.99999 %) (i.e., the impurity concentration is 1 ppm or lower, preferably 0.1 ppm or lower).

[0110]

In any case, an i-type (intrinsic) or substantially i-type oxide semiconductor
25 layer in which impurities are reduced by the first heat treatment is formed, which enables a transistor having extremely excellent characteristics to be realized. Further, by forming the i-type (intrinsic) or substantially i-type oxide semiconductor layer, a problem of a transistor caused owing to the thickness of the oxide semiconductor layer can be suppressed.

30 [0111]

The above heat treatment (first heat treatment) has an effect of removing

hydrogen, water, and the like and thus can also be referred to as dehydration treatment, dehydrogenation treatment, or the like. The dehydration treatment or the dehydrogenation treatment can also be performed at any of the following timings: after the formation of the oxide semiconductor layer 144, after the formation of the gate 5 insulating layer 146, after the formation of the gate electrode, and the like. Such dehydration treatment or dehydrogenation treatment may be performed once or plural times.

[0112]

After the formation of the oxide semiconductor layer 144, the oxide 10 semiconductor layer 144 may be processed into an island-shaped oxide semiconductor layer. The oxide semiconductor layer can be processed into an island shape by etching, for example. The etching may be performed either before or after the above heat treatment. In addition, dry etching is preferable in terms of miniaturization of an element, though wet etching may be employed. An etching gas and an etchant can be 15 selected as appropriate in accordance with a material to be etched.

[0113]

The gate insulating layer 146 can be formed by a CVD method, a sputtering method, or the like. The gate insulating layer 146 is preferably formed so as to include silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, tantalum oxide, 20 hafnium oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x > 0, y > 0$)) to which nitrogen is added, or the like. The gate insulating layer 146 may have a single-layer structure or a stacked-layer structure. There is no particular limitation on the thickness of the gate insulating layer 146; in the case where the semiconductor 25 device is miniaturized, the gate insulating layer 146 is preferably thin in order to secure operation of the transistor. For example, in the case of using silicon oxide, the thickness can be greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0114]

30 When the gate insulating layer is thin as in the above description, a problem of gate leakage due to a tunneling effect or the like is caused. In order to solve the problem of gate leakage, it is preferable that the gate insulating layer 146 be formed

using a high dielectric constant (high-k) material such as hafnium oxide, tantalum oxide, yttrium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)) to which nitrogen is added, or hafnium aluminate ($HfAl_xO_y$ ($x > 0, y > 0$)) to which nitrogen is added. By using a high-k material for the gate insulating layer 146, the thickness thereof can be increased for suppression of gate leakage with the electric characteristics maintained in a good condition. For example, the relative permittivity of hafnium oxide is approximately 15 and the value is significantly large as compared to 3 to 4, which is the relative permittivity of silicon oxide. With the use of such a high dielectric constant material, a gate insulating layer having an equivalent oxide thickness of less than 15 nm, preferably greater than or equal to 2 nm and less than or equal to 10 nm, can be easily realized. Note that a stacked-layer structure of a film including a high-k material and a film including any of silicon oxide, silicon nitride, silicon oxynitride, silicon nitride oxide, aluminum oxide, and the like may also be employed.

[0115]

After the gate insulating layer 146 is formed, second heat treatment is preferably performed in an inert gas atmosphere or an oxygen atmosphere. The temperature of the heat treatment is higher than or equal to 200 °C and lower than or equal to 450 °C, preferably higher than or equal to 250 °C and lower than or equal to 350 °C. For example, the heat treatment may be performed at 250 °C for 1 hour in a nitrogen atmosphere. The second heat treatment can reduce variation in electric characteristics of the transistor. Moreover, in the case where the gate insulating layer 146 includes oxygen, oxygen is supplied to the oxide semiconductor layer 144 to compensate for oxygen deficiency in the oxide semiconductor layer 144, whereby an i-type (intrinsic) or substantially i-type oxide semiconductor layer can be formed.

[0116]

Note that the second heat treatment is performed after the gate insulating layer 146 is formed in this embodiment; however, the timing of the second heat treatment is not limited to this. For example, the second heat treatment may be performed after the gate electrode is formed. Furthermore, the first heat treatment and the second heat treatment may be successively performed, the first heat treatment may also serve as the second heat treatment, or the second heat treatment may also serve as the first heat

treatment.

[0117]

As described above, at least one of the first heat treatment and the second heat treatment is performed, whereby the oxide semiconductor layer 144 can be purified so
5 that impurities other than main components are included as little as possible.

[0118]

Next, the gate electrode 148a is formed over the gate insulating layer 146 (see FIG. 4B).

[0119]

10 The gate electrode 148a can be formed in such a manner that a conductive layer is formed over the gate insulating layer 146 and then selectively etched. The conductive layer to be the gate electrode 148a can be formed by a PVD method typified by a sputtering method or a CVD method such as a plasma CVD method. The details are similar to those of the source electrode 142a, the drain electrode 142b, or the like;
15 thus, description thereof can be referred to. Note that a structure in which part of the gate electrode 148a overlaps with the source electrode 142a and the drain electrode 142b is employed in this embodiment; however, the disclosed invention is not limited to this. A structure in which one end of the gate electrode 148a overlaps with an end of the source electrode 142a and the other end of the gate electrode 148a overlaps with an
20 end of the drain electrode 142b can also be employed.

[0120]

Next, the insulating layer 150 and the insulating layer 152 are formed so as to cover the gate insulating layer 146, the gate electrode 148a, and the like (see FIG. 4C). The insulating layer 150 and the insulating layer 152 can be formed by a PVD method,
25 a CVD method, or the like. The insulating layer 150 and the insulating layer 152 can be formed using a material including an inorganic insulating material such as silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, or aluminum oxide.

[0121]

Note that a low dielectric constant material or a structure having a low
30 dielectric constant (such as a porous structure) is preferably employed for the insulating layer 150 and the insulating layer 152 because when the insulating layer 150 and the insulating layer 152 each have a low dielectric constant, capacitance generated between

wirings, electrodes, or the like can be reduced and high-speed operation can be achieved.

[0122]

Note that a stacked-layer structure of the insulating layer 150 and the insulating layer 152 is employed in this embodiment; however, an embodiment of the disclosed invention is not limited this. A single-layer structure or a stacked-layer structure including three or more layers may be employed. Moreover, it is possible to employ a structure in which the insulating layers are not provided.

[0123]

Note that the insulating layer 152 is preferably formed so as to have a planarized surface. By forming the insulating layer 152 so as to have a planarized surface, an electrode, a wiring, or the like can be favorably formed over the insulating layer 152 even in the case where the semiconductor device is miniaturized, for example. The insulating layer 152 can be planarized using a method such as chemical mechanical polishing (CMP).

[0124]

Through the above steps, the transistor 162 including the purified oxide semiconductor layer 144 is completed (see FIG. 4C).

[0125]

Note that after the above steps, a variety of wirings, electrodes, and the like may be formed. The wiring and the electrode can be formed by a method such as a so-called damascene method or dual damascene method.

[0126]

In the above-described manner, the channel formation region of the transistor 162 can be provided in an extremely flat region whose root-mean-square (RMS) roughness is less than or equal to 1 nm (preferably less than or equal to 0.5 nm). Accordingly, even when the transistor 162 is miniaturized, a problem such as a short-channel effect can be prevented and thus the transistor 162 can have favorable characteristics.

[0127]

Further, in the transistor 162 described in this embodiment, the oxide semiconductor layer 144 is purified and thus the hydrogen concentration thereof is

lower than or equal to 5×10^{19} atoms/cm^3, preferably lower than or equal to 5×10^{18} atoms/cm^3, further preferably lower than or equal to 5×10^{17} atoms/cm^3. In addition, the value of the density of carriers due to a donor such as hydrogen in the oxide semiconductor layer 144 is sufficiently small (e.g., lower than 1×10^{12} /cm^3, preferably
5 lower than 1.45×10^{10} /cm^3) as compared with the carrier density of a general silicon wafer (approximately 1×10^{14} /cm^3). Thus, the off-state current of the transistor 162 is sufficiently small. For example, the off-state current (here, current per micrometer (μm) of channel width) of the transistor 162 at room temperature (25 °C) is less than or equal to 100 zA (1 zA (zeptoampere) is 1×10^{-21} A), preferably less than or equal to 10
10 zA. In the case where the above structure is employed, the off-state current of the transistor can be 1×10^{-24} A/μm to 1×10^{-30} A/μm in theory.

[0128]

With the use of the purified and intrinsic oxide semiconductor layer 144, a sufficient reduction in the off-state current of the transistor can be easily achieved.

15 [0129]

Moreover, by forming the part of the top surface of the wiring 111 in a higher position than the part of the surface of the insulating layer 130, a reduction in the area of a portion where the wiring 111 is in contact with the source electrode 142a can be prevented; thus the contact resistance between the wiring 111 and the source electrode
20 142a can be reduced. As a result, the amount of heat generation or power consumption of the transistor 162 which is electrically connected to the wiring 111 in the lower layer can be reduced; accordingly, the wiring and the transistor can be stacked with the amount of heat generation or power consumption of the transistor suppressed. Consequently, by forming a stacked-layer structure with the use of the miniaturized
25 transistor and the wiring, three-dimensional high integration of the semiconductor device can be achieved with favorable transistor characteristics maintained.

[0130]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in
30 the other embodiments.

[0131]

(Embodiment 2)

In this embodiment, a structure and a manufacturing method of a semiconductor device according to another embodiment of the disclosed invention will be described with reference to FIGS. 5A to 5C, FIGS. 6A to 6C, FIGS. 7A to 7D, and 5 FIGS. 8A to 8C.

[0132]

<Example of Structure of Semiconductor Device>

FIGS. 5A to 5C illustrate an example of a structure of a semiconductor device. FIGS. 5A to 5C illustrate a cross-sectional view, a plan view, and a circuit configuration 10 of the semiconductor device, respectively. Note that operation of the semiconductor device will be described in detail in the following embodiment; in this embodiment, the structure of the semiconductor device will be mainly described. Note that the semiconductor device illustrated in FIGS. 5A to 5C is an example of a semiconductor device having a predetermined function and does not exhaustively represent the 15 semiconductor device of the disclosed invention. The semiconductor device according to the disclosed invention can have another function by changing connection of an electrode or the like as appropriate.

[0133]

FIG. 5A corresponds to a cross section along line A1-A2 and line B1-B2 in FIG. 20 5B. The semiconductor device illustrated in FIGS. 5A and 5B includes a transistor 160 below the transistor 162 described in the above embodiment and a capacitor 164, in addition to the transistor 162. Although the wiring 111 and the source electrode 142a are electrically connected to each other in FIG. 1A of the above embodiment, a gate electrode 110 of the transistor 160 is electrically connected to the source electrode 142a 25 of the transistor 162 in this embodiment.

[0134]

Here, it is preferable that a semiconductor material of the transistor 162 and a semiconductor material of the transistor 160 be different materials. For example, an oxide semiconductor can be used as the semiconductor material of the transistor 162, 30 and a semiconductor material (such as silicon) other than an oxide semiconductor can be used for the transistor 160. A transistor including an oxide semiconductor can hold charge for a long time owing to its characteristics. On the other hand, a transistor

including a material other than an oxide semiconductor can operate at high speed easily.

[0135]

The transistor 160 in FIGS. 5A to 5C includes a channel formation region 116 provided in a substrate 100 including a semiconductor material (e.g., silicon), impurity regions 120 provided with the channel formation region 116 positioned therebetween, metal compound regions 124 in contact with the impurity regions 120, a gate insulating layer 108 provided over the channel formation region 116, and the gate electrode 110 provided over the gate insulating layer 108. Note that a transistor whose source electrode and drain electrode are not illustrated in the drawing may be referred to as a transistor for the sake of convenience. Further, in such a case, in description of connection of a transistor, a source region and a source electrode are collectively referred to as a "source electrode", and a drain region and a drain electrode are collectively referred to as a "drain electrode". In other words, in this specification, the term "source electrode" may include a source region and the term "drain electrode" may include a drain region.

[0136]

Further, an element isolation insulating layer 106 is provided over the substrate 100 so as to surround the transistor 160, and the insulating layer 130 is provided so as to cover the transistor 160. Note that in order to realize high integration, it is preferable that the transistor 160 do not have a sidewall insulating layer as illustrated in FIGS. 5A to 5C. On the other hand, in the case where characteristics of the transistor 160 are emphasized, a sidewall insulating layer may be provided on a side surface of the gate electrode 110 and the impurity regions 120 may include a region having a different impurity concentration.

[0137]

The insulating layer 130 is formed over the transistor 160 so that at least part of a top surface of the gate electrode 110 is exposed. The part of the top surface of the gate electrode 110 is positioned higher than part of a surface of the insulating layer 130, and the gate electrode 110 in the region exposed from the insulating layer 130 is electrically connected to the source electrode 142a (drain electrode in some cases). Here, part of the surface of the insulating layer 130 and the part of the top surface of the gate electrode 110 have favorable planarity. The root-mean-square (RMS) roughness

of the part of the surface of the insulating layer 130 is preferably less than or equal to 1 nm. The root-mean-square (RMS) roughness of the part of the top surface of the gate electrode 110 is preferably less than or equal to 2 nm. Note that in this specification, the part of the top surface of the gate electrode 110 refers to a region which is in the top surface of the gate electrode 110 and parallel to a surface where a layer is formed.

[0138]

In addition, the difference in height between the part of the top surface of the gate electrode 110 and the part of the surface of the insulating layer 130 is preferably 0.1 times to 5 times as large as the thickness of the gate insulating layer 146.

[0139]

The structure of the transistor 162 in FIGS. 5A to 5C is similar to the structure of the transistor 162 in the above embodiment. Note that in this embodiment, the gate electrode 110 of the transistor 160 is provided instead of the wiring 111 and the source electrode 142a (drain electrode in some cases) of the transistor 162 is connected to the gate electrode 110 of the transistor 160.

[0140]

As described in the above embodiment, by providing a channel formation region of the transistor 162 in an extremely flat region whose root-mean-square (RMS) roughness is less than or equal to 1 nm, a problem such as a short-channel effect can be prevented even when the transistor 162 is miniaturized and thus the transistor 162 having favorable characteristics can be provided.

[0141]

By employing the above structure and forming the part of the top surface of the gate electrode 110 in a higher position than the part of the surface of the insulating layer 130, a reduction in the area of a portion where the gate electrode 110 is in contact with the source electrode 142a can be prevented; thus the contact resistance between the gate electrode 110 and the source electrode 142a can be reduced. Moreover, since the part of the top surface of the gate electrode 110 has favorable planarity, adhesion between the gate electrode 110 and the source electrode 142a is favorable; accordingly, the contact resistance can be further reduced. Consequently, the amount of heat generation or power consumption of the transistor 162 whose source electrode 142a is electrically connected to the gate electrode 110 can be reduced.

[0142]

Further, when the part of the top surface of the gate electrode 110 is exposed by CMP treatment or the like, an edge portion of the top surface of the gate electrode 110 can be polished and the edge portion of the top surface of the gate electrode 110 can have a smooth shape, preferably a shape having a surface curved smoothly from the surface of the insulating layer 130 to a top end portion of the projecting gate electrode 110. By providing such a smooth curved surface on the top end portion of the gate electrode 110 which projects from the insulating layer 130, the gate electrode 110 and the source electrode 142a can be in close contact with each other without a space therebetween. Accordingly, the contact resistance between the gate electrode 110 and the source electrode 142a can be further reduced. Furthermore, even when the thickness of the source electrode 142a is reduced, disconnection in an intersection with the gate electrode 110 can be prevented.

[0143]

The capacitor 164 in FIGS. 5A to 5C includes the source electrode 142a (drain electrode in some cases), the oxide semiconductor layer 144, the gate insulating layer 146, and an electrode 148b. That is, the source electrode 142a functions as one electrode of the capacitor 164, and the electrode 148b functions as the other electrode of the capacitor 164. Note that the electrode 148b is formed through steps similar to those of the gate electrode 148a of the transistor 162.

[0144]

Note that in the capacitor 164 in FIGS. 5A to 5C, insulation between the source electrode 142a and the electrode 148b can be adequately secured by stacking the oxide semiconductor layer 144 and the gate insulating layer 146. Needless to say, the capacitor 164 may have a structure without the oxide semiconductor layer 144 in order to secure sufficient capacitance. In the case where a capacitor is not needed, it is possible to employ a structure without the capacitor 164.

[0145]

In this embodiment, the transistor 162 and the capacitor 164 are provided so as to overlap with the transistor 160. By employing such a planar layout, high integration is possible. For example, given that the minimum feature size is F, the area occupied by the above semiconductor device can be $15F^2$ to $25F^2$.

[0146]

Note that the structure of a semiconductor device according to the disclosed invention is not limited to the structure illustrated in FIGS. 5A to 5C. Since the technical spirit of an embodiment of the disclosed invention is formation of a
5 stacked-layer structure using an oxide semiconductor and a material other than an oxide semiconductor, details such as connection of an electrode or the like can be modified as appropriate.

[0147]

In addition, although the semiconductor device illustrated in FIGS. 5A to 5C
10 has a structure in which the source electrode 142a and the drain electrode 142b are embedded in an insulating layer including the insulating layer 143a, the source electrode 142a and the drain electrode 142b may be formed over the insulating layer 130 without being embedded in the insulating layer as illustrated in FIGS. 6A to 6C, for example. Here, FIGS. 6A to 6C illustrate a cross-sectional view, a plan view, and a circuit
15 configuration of a semiconductor device, respectively. In addition, in the semiconductor device illustrated in FIGS. 6A to 6C, the same reference numerals are used for portions common to those of the semiconductor device illustrated in FIGS. 5A to 5C.

[0148]

20 The semiconductor device illustrated in FIGS. 6A to 6C has almost the same structure as the semiconductor device illustrated in FIGS. 5A to 5C. The transistor 162 includes the oxide semiconductor layer 144 formed over the insulating layer 130, the source electrode 142a and the drain electrode 142b electrically connected to the oxide semiconductor layer 144, the gate electrode 148a provided to overlap with the oxide
25 semiconductor layer 144, and the gate insulating layer 146 provided between the oxide semiconductor layer 144 and the gate electrode 148a. Further, the insulating layer 150 and the insulating layer 152 may be formed over the transistor 162 so as to cover the gate insulating layer 146, the gate electrode 148a, and the like. The insulating layer 130 is formed over the transistor 160 so that at least part of a top surface of the gate
30 electrode 110 of the transistor 160 is exposed. The part of the top surface of the gate electrode 110 is positioned higher than part of a surface of the insulating layer 130, and the gate electrode 110 in the region exposed from the insulating layer 130 is electrically

connected to the source electrode 142a or the drain electrode 142b. In addition, the transistor 160 and the capacitor 164 of the semiconductor device illustrated in FIGS. 6A to 6C have almost the same structures as those of the semiconductor device illustrated in FIGS. 5A to 5C.

5 [0149]

Note that since the oxide semiconductor layer 144 is formed over and in contact with the insulating layer 130 in the semiconductor device illustrated in FIGS. 6A to 6C, it is preferable that the root-mean-square (RMS) roughness of a region which is part of the surface of the insulating layer 130 (the part particularly refers to a region
10 parallel to a surface where a layer is formed) and in contact with the oxide semiconductor layer 144 be less than or equal to 1 nm.

[0150]

As illustrated in FIGS. 6A to 6C, the source electrode 142a and the drain electrode 142b may be tapered in the transistor 162. The taper angle can be greater
15 than or equal to 30° and less than or equal to 60°, for example. Note that the taper angle refers to an inclination angle formed with a side surface and a bottom surface of a layer having a tapered shape (e.g., the source electrode 142a or the drain electrode 142b) in the case where the layer is observed from a direction perpendicular to a cross section (a plane perpendicular to the surface of the insulating layer 130).

20 [0151]

<Method for Manufacturing Semiconductor Device>

Next, an example of a method for manufacturing the above semiconductor device will be described with reference to FIGS. 7A to 7D and FIGS. 8A to 8C. Note that FIGS. 7A to 7D and FIGS. 8A to 8C correspond to cross sections along line A1-A2
25 and line B1-B2 in FIG. 5B. A method for manufacturing the transistor 162 is similar to that in the above embodiment; therefore, a method for manufacturing the transistor 160 will be mainly described in this embodiment.

[0152]

First, the substrate 100 including a semiconductor material is prepared (see FIG.
30 7A). As the substrate 100 including a semiconductor material, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like; a compound semiconductor substrate of silicon germanium or the

like; an SOI substrate; or the like can be used. Here, an example of using a single crystal silicon substrate as the substrate 100 including a semiconductor material is described. Note that in general, the term "SOI substrate" means a substrate where a silicon semiconductor layer is provided on an insulating surface. In this specification and the like, the term "SOI substrate" also includes a substrate where a semiconductor layer formed using a material other than silicon is provided on an insulating surface in its category. That is, a semiconductor layer included in the "SOI substrate" is not limited to a silicon semiconductor layer. Moreover, the SOI substrate can be a substrate having a structure in which a semiconductor layer is provided over an insulating substrate such as a glass substrate, with an insulating layer positioned therebetween.

[0153]

It is particularly preferable that a single crystal semiconductor substrate of silicon or the like be used as the substrate 100 including a semiconductor material because high-speed reading operation in the semiconductor device is possible.

[0154]

Note that in order to control threshold voltage of the transistor, an impurity element may be added to a region which serves as the channel formation region 116 of the transistor 160 later. Here, an impurity element imparting conductivity with which the transistor 160 has positive threshold voltage is added. In the case where the semiconductor material is silicon, examples of the impurity imparting the conductivity include boron, aluminum, and gallium. After the addition of the impurity element, heat treatment is preferably performed so that the impurity element is activated and defects generated at the time of the addition of the impurity element are repaired, for example.

[0155]

Next, a protective layer 102 which serves as a mask for forming an element isolation insulating layer is formed over the substrate 100 (see FIG. 7A). As the protective layer 102, an insulating layer formed using silicon oxide, silicon nitride, silicon oxynitride, or the like can be used, for example.

[0156]

Next, part of the substrate 100 in a region that is not covered with the

protective layer 102 (in an exposed region) is removed by etching using the protective layer 102 as a mask. Thus, a semiconductor region 104 isolated from the other semiconductor regions is formed (see FIG. 7B). As the etching, dry etching is preferably performed, but wet etching may be performed. An etching gas and an
5 etchant can be selected as appropriate in accordance with a material to be etched.

[0157]

Then, an insulating layer is formed so as to cover the semiconductor region 104, and the insulating layer in a region overlapping with the semiconductor region 104 is selectively removed, so that the element isolation insulating layer 106 is formed (see
10 FIG. 7C). The insulating layer is formed using silicon oxide, silicon nitride, silicon oxynitride, or the like. As a method for removing the insulating layer, there are etching treatment and polishing treatment such as chemical mechanical polishing (CMP) treatment, and any of them may be employed. Note that the protective layer 102 is removed after the formation of the semiconductor region 104 or after the
15 formation of the element isolation insulating layer 106.

[0158]

Next, an insulating layer is formed over a surface of the semiconductor region 104, and a layer including a conductive material is formed over the insulating layer.

[0159]

20 The insulating layer is to be a gate insulating layer later and can be formed by performing heat treatment (such as thermal oxidation treatment or thermal nitridation treatment) on the surface of the semiconductor region 104, for example. Instead of heat treatment, high-density plasma treatment may be employed. The high-density plasma treatment can be performed using, for example, a mixed gas of a rare gas such as
25 He, Ar, Kr, or Xe and oxygen, nitrogen oxide, ammonia, nitrogen, hydrogen, or the like. Needless to say, the insulating layer may be formed using a CVD method, a sputtering method, or the like. The insulating layer preferably has a single-layer structure or a stacked-layer structure including any of silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, tantalum oxide, yttrium oxide, hafnium silicate
30 ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, hafnium aluminate ($HfAl_xO_y$ ($x > 0$, $y > 0$)) to which nitrogen is added, and the

like. The thickness of the insulating layer can be, for example, greater than or equal to 1 nm and less than or equal to 100 nm, preferably greater than or equal to 10 nm and less than or equal to 50 nm.

[0160]

5 The layer including a conductive material can be formed using a metal material such as aluminum, copper, titanium, tantalum, or tungsten. The layer including a conductive material may be formed using a semiconductor material such as polycrystalline silicon. There is no particular limitation on the method for forming the layer including a conductive material, and a variety of film formation methods such as 10 an evaporation method, a CVD method, a sputtering method, and a spin coating method can be employed. Note that an example of the case where the layer including a conductive material is formed using a metal material is described in this embodiment.

[0161]

After that, the insulating layer and the layer including a conductive material are 15 selectively etched, so that the gate insulating layer 108 and the gate electrode 110 are formed (see FIG. 7C).

[0162]

Next, phosphorus (P), arsenic (As), or the like is added to the semiconductor region 104, so that the channel formation region 116 and the impurity regions 120 are 20 formed (see FIG. 7D). Note that phosphorus or arsenic is added here in order to form an n-channel transistor; an impurity element such as boron (B) or aluminum (Al) may be added in the case of forming a p-channel transistor. Here, the concentration of the impurity added can be set as appropriate; the concentration is preferably increased in the case where the semiconductor element is highly miniaturized.

25 [0163]

Note that a sidewall insulating layer may be formed in the periphery of the gate electrode 110 so that an impurity region to which an impurity element is added at a different concentration is formed.

[0164]

30 Next, a metal layer 122 is formed so as to cover the gate electrode 110, the impurity regions 120, and the like (see FIG. 8A). A variety of film formation methods such as a vacuum evaporation method, a sputtering method, and a spin coating method

can be employed for forming the metal layer 122. The metal layer 122 is preferably formed using a metal material that reacts with a semiconductor material included in the semiconductor region 104 to be a low-resistance metal compound. Examples of such a metal material include titanium, tantalum, tungsten, nickel, cobalt, and platinum.

5 [0165]

Next, heat treatment is performed so that the metal layer 122 reacts with the semiconductor material. Thus, the metal compound regions 124 that are in contact with the impurity regions 120 are formed (see FIG. 8A). Note that when the gate electrode 110 is formed using polycrystalline silicon or the like, a metal compound

10 region is also formed in a region of the gate electrode 110 in contact with the metal layer 122.

[0166]

As the heat treatment, irradiation with a flash lamp can be employed, for example. Although it is needless to say that another heat treatment method may be

15 used, a method by which heat treatment in an extremely short time can be achieved is preferably used in order to improve the controllability of chemical reaction in formation of the metal compound. Note that the metal compound regions are formed by reaction of the metal material and the semiconductor material and have sufficiently high conductivity. The formation of the metal compound regions can sufficiently reduce

20 the electric resistance and improve element characteristics. Note that the metal layer 122 is removed after the metal compound regions 124 are formed.

[0167]

Next, the insulating layer 130 is formed so as to cover the components formed in the above steps (see FIG. 8B). The insulating layer 130 can be formed using a

25 material and a structure similar to those of the above embodiment; therefore, the above embodiment can be referred to for details thereof.

[0168]

Through the above steps, the transistor 160 using the substrate 100 including a semiconductor material is formed (see FIG. 8B). The transistor 160 is capable of

30 high-speed operation. Therefore, when the transistor is used as a reading transistor, data can be read at high speed.

[0169]

Next, planarization treatment is performed on a surface of the insulating layer 130; thus, the insulating layer 130 partly has a surface with a root-mean-square (RMS) roughness of less than or equal to 1 nm, at least part of a top surface of the gate electrode 110 is exposed, and the part of the top surface of the gate electrode 110 is
5 formed in a higher position than part of the surface of the insulating layer 130 (see FIG. 8C). As the planarization treatment for the insulating layer 130, chemical mechanical polishing (CMP) treatment is performed. Note that the CMP treatment can be performed by a method similar to that described in the above embodiment; therefore, the above embodiment can be referred to for details thereof.
10 [0170]

By the above CMP treatment, the root-mean-square (RMS) roughness of at least part of the surface of the insulating layer 130 is preferably made to be less than or equal to 1 nm. The root-mean-square (RMS) roughness of the part of the top surface of the gate electrode 110 is preferably less than or equal to 2 nm.
15 [0171]

At this time, the surface of the insulating layer 130 is planarized, at least part of the top surface of the gate electrode 110 is exposed, and the part of the top surface of the gate electrode 110 is formed in a higher position than the part of the surface of the insulating layer 130. Here, the difference in height between the part of the top surface
20 of the gate electrode 110 and the part of the surface of the insulating layer 130 is preferably 0.1 times to 5 times as large as the thickness of the gate insulating layer 146.
[0172]

Further, when the part of the top surface of the gate electrode 110 is exposed by CMP treatment, an edge portion of the top surface of the gate electrode 110 can be
25 polished and the edge portion of the top surface of the gate electrode 110 can have a smooth shape, preferably a shape having a surface curved smoothly from the surface of the insulating layer 130 to a top end portion of the projecting gate electrode 110. By providing such a smooth curved surface on the top end portion of the gate electrode 110 which projects from the insulating layer 130, the gate electrode 110 and the source
30 electrode 142a can be in close contact with each other without a space therebetween. Accordingly, the contact resistance between the gate electrode 110 and the source electrode 142a can be further reduced. Furthermore, even when the thickness of the

source electrode 142a is reduced, disconnection in an intersection with the gate electrode 110 can be prevented.

[0173]

Note that before or after any of the above steps, a step of forming an additional electrode, wiring, semiconductor layer, insulating layer, or the like may be performed. For example, a multilayer wiring structure in which an insulating layer and a conductive layer are stacked is employed as a structure of a wiring, whereby a highly-integrated semiconductor device can be realized.

[0174]

In subsequent steps, the transistor 162 can be manufactured by a method similar to the method described in the above embodiment with reference to FIGS. 3C to 3E and FIGS. 4A to 4C. Therefore, the above embodiment can be referred to for details of the subsequent steps. The capacitor 164 can be manufactured in such a manner that the electrode 148b is formed so as to overlap with the source electrode 142a in the formation of the gate electrode 148a described with reference to FIG. 4B.

[0175]

In the above-described manner, the channel formation region of the transistor 162 can be provided in an extremely flat region whose root-mean-square (RMS) roughness is less than or equal to 1 nm (preferably less than or equal to 0.5 nm). Accordingly, even when the transistor 162 is miniaturized, a problem such as a short-channel effect can be prevented and thus the transistor 162 can have favorable characteristics.

[0176]

Moreover, by forming the part of the top surface of the gate electrode 110 in a higher position than the part of the surface of the insulating layer 130, a reduction in the area of a portion where the gate electrode 110 is in contact with the source electrode 142a can be prevented; thus the contact resistance between the gate electrode 110 and the source electrode 142a can be reduced. As a result, the amount of heat generation or power consumption of the transistor 162 which is electrically connected to the transistor 160 can be reduced; accordingly, the transistors can be stacked with the amount of heat generation or power consumption of the transistor suppressed. Consequently, by forming a stacked-layer structure of the miniaturized transistors,

three-dimensional high integration of the semiconductor device can be achieved with favorable transistor characteristics maintained.

[0177]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0178]

(Embodiment 3)

In this embodiment, an application example of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 9A to 9C. Here, an example of a memory device will be described. Note that in circuit diagrams, "OS" may be written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

[0179]

In the semiconductor device illustrated in FIG. 9A, which can be used as a memory device, a first wiring (1st Line) is electrically connected to a source electrode of a transistor 1000, and a second wiring (2nd Line) is electrically connected to a drain electrode of the transistor 1000. A gate electrode of the transistor 1000 and one of a source electrode and a drain electrode of a transistor 1010 are electrically connected to one electrode of a capacitor 1020. A third wiring (3rd Line) and the other of the source electrode and the drain electrode of the transistor 1010 are electrically connected to each other, and a fourth wiring (4th Line) and a gate electrode of the transistor 1010 are electrically connected to each other. Further, a fifth wiring (5th Line) is electrically connected to the other electrode of the capacitor 1020.

[0180]

Here, a transistor including an oxide semiconductor is used as the transistor 1010. Here, as the transistor including an oxide semiconductor, for example, the transistor described in the above embodiment can be used. A transistor including an oxide semiconductor has a characteristic of extremely small off-state current. Therefore, when the transistor 1010 is turned off, the potential of the gate electrode of the transistor 1000 can be held for an extremely long time. Moreover, by using the transistor described in the above embodiment, a short-channel effect of the transistor

1010 can be suppressed and miniaturization thereof can be achieved. By providing the capacitor 1020, holding of charge given to the gate electrode of the transistor 1000 and reading of stored data can be easily performed. Here, as the capacitor 1020, for example, the capacitor described in the above embodiment can be used.

5 [0181]

Further, a transistor including a semiconductor material other than an oxide semiconductor is used as the transistor 1000. The semiconductor material other than an oxide semiconductor can be silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like, for example, and is preferably a single crystal

10 semiconductor. Alternatively, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material can easily operate at high speed. Here, as the transistor including a semiconductor material other than an oxide semiconductor, for example, the transistor described in the above embodiment can be used.

15 [0182]

Here, the gate electrode of the transistor 1000 and the source electrode (drain electrode in some cases) of the transistor 1010 are electrically connected to each other to have a structure similar to that described in the above embodiment, whereby the amount of heat generation or power consumption of the transistor 1010 which is electrically

20 connected to the transistor 1000 can be reduced; accordingly, the transistors can be stacked with the amount of heat generation or power consumption of the transistor suppressed. Consequently, by forming a stacked-layer structure of the miniaturized transistors, three-dimensional high integration of the semiconductor device can be achieved with favorable transistor characteristics maintained.

25 [0183]

Further, as illustrated in FIG. 9C, a structure in which the capacitor 1020 is not provided may also be employed.

[0184]

In the semiconductor device illustrated in FIG. 9A, writing, storing, and reading

30 of data can be performed in the following manner, utilizing the advantage in that the potential of the gate electrode of the transistor 1000 can be held.

[0185]

Firstly, writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 1010 is turned on, so that the transistor 1010 is turned on. Accordingly, the potential of the third wiring is supplied to the gate electrode of the transistor 1000 and the capacitor 1020. That is, 5 predetermined charge is given to the gate electrode of the transistor 1000 (writing). Here, one of charges for supply of two different potentials (hereinafter, charge for supply of a low potential is referred to as charge Q_L and charge for supply of a high potential is referred to as charge Q_H) is given. Note that charges giving three or more different potentials may be applied to increase storage capacity. After that, the 10 potential of the fourth wiring is set to a potential at which the transistor 1010 is turned off, so that the transistor 1010 is turned off. Thus, the charge given to the gate electrode of the transistor 1000 is held (storing).

[0186]

Since the off-state current of the transistor 1010 is extremely small, the charge 15 of the gate electrode of the transistor 1000 is held for a long time.

[0187]

Secondly, reading of data will be described. By supplying an appropriate potential (reading potential) to the fifth wiring when a predetermined potential (constant potential) is supplied to the first wiring, the potential of the second wiring varies 20 depending on the amount of charge held in the gate electrode of the transistor 1000. This is because in general, when the transistor 1000 is an n-channel transistor, apparent threshold voltage V_{th_H} in the case where Q_H is given to the gate electrode of the transistor 1000 is lower than apparent threshold voltage V_{th_L} in the case where Q_L is given to the gate electrode of the transistor 1000. Here, apparent threshold voltage 25 refers to the potential of the fifth wiring, which is needed to turn on the transistor 1000. Thus, the potential of the fifth wiring is set to a potential V_0 intermediate between V_{th_H} and V_{th_L}, whereby charge given to the gate electrode of the transistor 1000 can be determined. For example, in the case where Q_H is given in writing, when the potential of the fifth wiring is set to V_0 ($> V_{th_H}$), the transistor 1000 is turned on. In the case 30 where Q_L is given in writing, even when the potential of the fifth wiring is set to V_0 ($< V_{th_L}$), the transistor 1000 remains in an off state. Therefore, the stored data can be

read by measuring the potential of the second wiring.

[0188]

Note that in the case where memory cells are arrayed to be used, only data of desired memory cells need to be read. Thus, in the case where data of predetermined memory cells is read and data of the other memory cells is not read, a potential at which the transistor 1000 is turned off regardless of the state of the gate electrode, that is, a potential lower than V_{th_H} may be supplied to fifth wirings of the memory cells whose data is not to be read. Alternatively, a potential at which the transistor 1000 is turned on regardless of the state of the gate electrode, that is, a potential higher than V_{th_L} may be supplied to the fifth wirings.

[0189]

Thirdly, rewriting of data will be described. Rewriting of data is performed in a manner similar to that of the writing and storing of data. Specifically, the potential of the fourth wiring is set to a potential at which the transistor 1010 is turned on, so that the transistor 1010 is turned on. Accordingly, the potential of the third wiring (potential for new data) is supplied to the gate electrode of the transistor 1000 and the capacitor 1020. After that, the potential of the fourth wiring is set to a potential at which the transistor 1010 is turned off, so that the transistor 1010 is turned off. Accordingly, charge for new data is given to the gate electrode of the transistor 1000.

[0190]

In the semiconductor device according to the disclosed invention, data can be directly rewritten by another writing of data as described above. Therefore, extracting of charge from a floating gate with the use of high voltage, which is needed in a flash memory or the like, is not necessary and thus a reduction in operation speed, which is attributed to erasing operation, can be suppressed. In other words, high-speed operation of the semiconductor device is realized.

[0191]

Note that the source electrode or the drain electrode of the transistor 1010 is electrically connected to the gate electrode of the transistor 1000, thereby having an effect similar to that of a floating gate of a floating gate transistor used for a nonvolatile memory element. Therefore, a portion in the drawing where the source electrode or

the drain electrode of the transistor 1010 is electrically connected to the gate electrode of the transistor 1000 is called a floating gate portion FG in some cases. When the transistor 1010 is off, the floating gate portion FG can be regarded as being embedded in an insulator and thus charge is held in the floating gate portion FG. The amount of off-state current of the transistor 1010 including an oxide semiconductor is less than or equal to one hundred thousandth of the amount of off-state current of a transistor including a silicon semiconductor or the like; thus, loss of charge accumulated in the floating gate portion FG due to leakage current of the transistor 1010 is negligible. That is, with the transistor 1010 including an oxide semiconductor, a nonvolatile memory device which can store data without being supplied with power can be realized.

[0192]

For example, when the off-state current of the transistor 1010 at room temperature is less than or equal to 10 zA/μm (1 zA (zeptoampere) is 1×10^{-21} A) and the capacitance of the capacitor 1020 is approximately 10 fF, data can be stored for 10^4 seconds or longer. Needless to say, the storage time depends on transistor characteristics and the capacitance.

[0193]

Further, in that case, the problem of deterioration of a gate insulating film (tunnel insulating film), which is pointed out in a conventional floating gate transistor, does not exist. That is to say, the deterioration of a gate insulating film due to injection of an electron into a floating gate, which has been conventionally regarded as a problem, can be neglected. This means that there is no limit on the number of times of writing in principle. Furthermore, high voltage needed for writing or erasing in a conventional floating gate transistor is not necessary.

[0194]

The components such as transistors in the semiconductor device in FIG. 9A can be regarded as including a resistor and a capacitor as illustrated in FIG. 9B. That is, in FIG. 9B, the transistor 1000 and the capacitor 1020 are each regarded as including a resistor and a capacitor. R1 and C1 denote the resistance and the capacitance of the capacitor 1020, respectively. The resistance R1 corresponds to the resistance of an insulating layer included in the capacitor 1020. R2 and C2 denote the resistance and the capacitance of the transistor 1000, respectively. The resistance R2 corresponds to

the resistance of a gate insulating layer at the time when the transistor 1000 is on. The capacitance C2 corresponds to so-called gate capacitance (capacitance formed between the gate electrode and the source or drain electrode, and capacitance formed between the gate electrode and a channel formation region).

5 [0195]

The resistance (also referred to as effective resistance) between the source electrode and the drain electrode in the case where the transistor 1010 is off is denoted by ROS. When R1 and R2 satisfy the relations of R1 ≥ ROS and R2 ≥ ROS under the condition where gate leakage of the transistor 1010 is sufficiently small, a charge 10 holding period (also referred to as a data storage period) is determined mainly by the off-state current of the transistor 1010.

[0196]

On the other hand, when the conditions are not satisfied, it is difficult to sufficiently secure the holding period even if the off-state current of the transistor 1010 15 is small enough. This is because leakage current other than the off-state current of the transistor 1010 (e.g., leakage current generated between the source electrode and the gate electrode) is large. Thus, it can be said that the semiconductor device disclosed in this embodiment preferably satisfies the above relations.

[0197]

20 It is preferable that C1 ≥ C2 be satisfied. This is because when C1 is large, the potential of the fifth wiring can be supplied to the floating gate portion FG efficiently at the time of controlling the potential of the floating gate portion FG by the fifth wiring, and a difference between potentials (e.g., the reading potential and a non-reading potential) supplied to the fifth wiring can be reduced.

25 [0198]

When the above relation is satisfied, a more favorable semiconductor device can be realized. Note that R1 and R2 are controlled by the gate insulating layer of the transistor 1000 and the insulating layer of the capacitor 1020. The same relation is applied to C1 and C2. Therefore, it is preferable that the material, the thickness, and 30 the like of the gate insulating layer be set as appropriate to satisfy the above relation.

[0199]

In the semiconductor device described in this embodiment, the floating gate portion FG has an effect similar to that of a floating gate of a floating gate transistor of a flash memory or the like, but the floating gate portion FG of this embodiment has a feature which is essentially different from that of the floating gate of the flash memory or the like. In the case of a flash memory, since voltage applied to a control gate is high, it is necessary to keep a proper distance between cells in order to prevent the potential from affecting a floating gate of the adjacent cell. This is one of factors inhibiting high integration of the semiconductor device. The factor is attributed to a basic principle of a flash memory, in which tunneling current is generated by application of a high electric field.

[0200]

Further, because of the above principle of a flash memory, deterioration of an insulating film proceeds and thus another problem of the limit on the number of times of rewriting (approximately 10^4 times to 10^5 times) occurs.

[0201]

The semiconductor device according to the disclosed invention is operated by switching of a transistor including an oxide semiconductor and does not use the above-described principle of charge injection by tunneling current. That is, a high electric field for charge injection is not necessary unlike a flash memory. Accordingly, it is not necessary to consider an influence of a high electric field from a control gate on an adjacent cell, which facilitates high integration.

[0202]

Further, charge injection by tunneling current is not utilized, which means that there are no causes for deterioration of a memory cell. In other words, the semiconductor device according to the disclosed invention has higher durability and reliability than a flash memory.

[0203]

In addition, the semiconductor device according to the disclosed invention is advantageous over a flash memory in that a high electric field is not necessary and a large peripheral circuit (such as a booster circuit) is not necessary.

[0204]

In the case where the relative permittivity εr1 of the insulating layer included in

the capacitor 1020 is different from the relative permittivity $\varepsilon r2$ of the insulating layer included in the transistor 1000, it is easy to satisfy $C1 \geq C2$ while $2 \cdot S2 \geq S1$ (preferably $S2 \geq S1$) is satisfied where S1 is the area of the insulating layer included in the capacitor 1020 and S2 is the area of the insulating layer included in the gate capacitor of the
5 transistor 1000. In other words, $C1 \geq C2$ can be easily satisfied while the area of the insulating layer included in the capacitor 1020 is small. Specifically, for example, a film formed of a high-k material such as hafnium oxide or a stack of a film formed of a high-k material such as hafnium oxide and a film formed of an oxide semiconductor is used for the insulating layer included in the capacitor 1020 so that $\varepsilon r1$ can be 10 or more,
10 preferably 15 or more, and silicon oxide is used for the insulating layer included in the gate capacitor so that $\varepsilon r2$ can be 3 to 4.

[0205]

Combination of such structures enables higher integration of the semiconductor device according to the disclosed invention.

15 [0206]

Note that an n-channel transistor in which electrons are majority carriers is used in the above description; needless to say, a p-channel transistor in which holes are majority carriers can be used instead of the n-channel transistor.

[0207]

20 As described above, the semiconductor device according to an embodiment of the disclosed invention has a nonvolatile memory cell which includes a writing transistor where leakage current (off-state current) between a source and a drain in an off state is small, a reading transistor including a semiconductor material different from that of the writing transistor, and a capacitor.

25 [0208]

In the case of using a general silicon semiconductor, it is difficult to reduce the leakage current (off-state current) at a temperature at which a transistor is used (e.g., 25 °C) to approximately less than 100 zA (1×10^{-19} A); however, the above characteristic can be obtained in a transistor manufactured by processing an oxide semiconductor
30 under appropriate conditions. Therefore, a transistor including an oxide semiconductor is preferably used as the writing transistor.

[0209]

In addition, a transistor including an oxide semiconductor has a small subthreshold swing (S value); thus, the switching rate can be sufficiently high even if mobility is comparatively low. Therefore, by using the transistor as the writing 5 transistor, rising of a writing pulse given to the floating gate portion FG can be very sharp. Further, the off-state current is small and thus the amount of charge held in the floating gate portion FG can be reduced. That is, by using the transistor including an oxide semiconductor as the writing transistor, rewriting of data can be performed at high speed.

10 [0210]

As for the reading transistor, although there is no limitation on off-state current, it is preferable to use a transistor which operates at high speed in order to increase the reading rate. For example, a transistor with a switching rate of 1 nanosecond or lower is preferably used as the reading transistor.

15 [0211]

In this manner, when a transistor including an oxide semiconductor is used as a writing transistor and a transistor including a semiconductor material other than an oxide semiconductor is used as a reading transistor, a semiconductor device capable of storing data for a long time and reading data at high speed, which can be used as a 20 memory device, can be obtained.

[0212]

Moreover, by using the transistor described in the above embodiment as the writing transistor, a short-channel effect of the writing transistor can be suppressed and miniaturization thereof can be achieved. Accordingly, high integration of the 25 semiconductor device which can be used as a memory device can be achieved.

[0213]

Further, the gate electrode of the reading transistor and the source electrode of the writing transistor are electrically connected to each other to have a structure similar to that described in the above embodiment, whereby the amount of heat generation or 30 power consumption of the writing transistor which is electrically connected to the reading transistor can be reduced; accordingly, the transistors can be stacked with the amount of heat generation or power consumption of the transistor suppressed.

Consequently, by forming a stacked-layer structure of the miniaturized transistors, three-dimensional high integration of the semiconductor device can be achieved with favorable transistor characteristics maintained.

[0214]

5 The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0215]

(Embodiment 4)

10 In this embodiment, an application example of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 10A and 10B and FIGS. 11A to 11C. Here, an example of a memory device will be described. Note that in circuit diagrams, "OS" may be written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

15 [0216]

FIGS. 10A and 10B are circuit diagrams of semiconductor devices each of which includes a plurality of semiconductor devices (hereinafter also referred to as memory cells 1050) illustrated in FIG. 9A and can be used as a memory device. FIG. 10A is a circuit diagram of a so-called NAND semiconductor device in which the 20 memory cells 1050 are connected in series, and FIG. 10B is a circuit diagram of a so-called NOR semiconductor device in which the memory cells 1050 are connected in parallel.

[0217]

The semiconductor device in FIG. 10A includes a source line SL, a bit line BL, 25 a first signal line S1, a plurality of second signal lines S2, a plurality of word lines WL, and a plurality of memory cells 1050. In FIG. 10A, one source line SL and one bit line BL are provided; however, an embodiment of the disclosed invention is not limited to this. A plurality of source lines SL and a plurality of bit lines BL may be provided.

[0218]

30 In each of the memory cells 1050, a gate electrode of the transistor 1000, one of a source electrode and a drain electrode of the transistor 1010, and one electrode of the capacitor 1020 are electrically connected to one another. The first signal line S1

and the other of the source electrode and the drain electrode of the transistor 1010 are electrically connected to each other, and the second signal line S2 and a gate electrode of the transistor 1010 are electrically connected to each other. The word line WL and the other electrode of the capacitor 1020 are electrically connected to each other.

5 [0219]

Further, a source electrode of the transistor 1000 included in the memory cell 1050 is electrically connected to a drain electrode of the transistor 1000 in the adjacent memory cell 1050. The drain electrode of the transistor 1000 included in the memory cell 1050 is electrically connected to the source electrode of the transistor 1000 in the 10 adjacent memory cell 1050. Note that the drain electrode of the transistor 1000 included in the memory cell 1050 of the plurality of memory cells connected in series, which is provided at one end, is electrically connected to the bit line. The source electrode of the transistor 1000 included in the memory cell 1050 of the plurality of memory cells connected in series, which is provided at the other end, is electrically 15 connected to the source line.

[0220]

In the semiconductor device in FIG. 10A, writing operation and reading operation are performed for each row. The writing operation is performed as follows. A potential at which the transistor 1010 is turned on is supplied to the second signal line 20 S2 in a row where writing is performed, so that the transistor 1010 in the row where writing is performed is turned on. Accordingly, the potential of the first signal line S1 is supplied to the gate electrode of the transistor 1000 of the specified row, whereby predetermined charge is given to the gate electrode. Thus, data can be written to the memory cell of the specified row.

25 [0221]

Further, the reading operation is performed as follows. First, a potential at which the transistor 1000 is turned on regardless of charge given to the gate electrode of the transistor 1000 is supplied to the word lines WL of rows other than a row where reading is performed, whereby the transistors 1000 of the rows other than the row where 30 reading is performed are turned on. Then, a potential (reading potential) at which an on state or an off state of the transistor 1000 is determined depending on charge in the gate electrode of the transistor 1000 is supplied to the word line WL of the row where

reading is performed. After that, a constant potential is supplied to the source line SL so that a reading circuit (not shown) connected to the bit line BL is operated. Here, the plurality of transistors 1000 between the source line SL and the bit line BL are on except the transistor 1000 of the row where reading is performed; therefore, conductance between the source line SL and the bit line BL is determined by the state (an on state or an off state) of the transistor 1000 of the row where reading is performed. The conductance of the transistor 1000 of the row where reading is performed depends on charge in the gate electrode thereof. Thus, the potential of the bit line BL varies accordingly. By reading the potential of the bit line with the reading circuit, data can be read from the memory cell of the specified row.

[0222]

The semiconductor device in FIG. 10B includes a plurality of source lines SL, a plurality of bit lines BL, a plurality of first signal lines S1, a plurality of second signal lines S2, a plurality of word lines WL, and a plurality of memory cells 1050. A gate electrode of the transistor 1000, one of a source electrode and a drain electrode of the transistor 1010, and one electrode of the capacitor 1020 are electrically connected to one another. The source line SL and a source electrode of the transistor 1000 are electrically connected to each other. The bit line BL and a drain electrode of the transistor 1000 are electrically connected to each other. The first signal line S1 and the other of the source electrode and the drain electrode of the transistor 1010 are electrically connected to each other, and the second signal line S2 and a gate electrode of the transistor 1010 are electrically connected to each other. The word line WL and the other electrode of the capacitor 1020 are electrically connected to each other.

[0223]

In the semiconductor device in FIG. 10B, writing operation and reading operation are performed for each row. The writing operation is performed in a manner similar to that of the semiconductor device in FIG. 10A. The reading operation is performed as follows. First, a potential at which the transistor 1000 is turned off regardless of charge given to the gate electrode of the transistor 1000 is supplied to the word lines WL of rows other than a row where reading is performed, so that the transistors 1000 of the rows other than the row where reading is performed are turned off. Then, a potential (reading potential) at which an on state or an off state of the

transistor 1000 is determined depending on charge in the gate electrode of the transistor 1000 is supplied to the word line WL of the row where reading is performed. After that, a constant potential is supplied to the source lines SL so that a reading circuit (not shown) connected to the bit lines BL is operated. Here, conductance between the source line SL and the bit line BL is determined by the state of the transistor 1000 of the row where reading is performed. That is, the potential of the bit line BL varies depending on charge in the gate electrode of the transistor 1000 of the row where reading is performed. By reading the potential of the bit lines with the reading circuit, data can be read from the memory cells of the specified row.

[0224]

Although the amount of data which can be stored in each of the memory cells 1050 is one bit in the above description, the structure of the semiconductor device of this embodiment is not limited to this. The amount of data which is stored in each of the memory cells 1050 may be increased by preparing three or more potentials to be supplied to the gate electrode of the transistor 1000. For example, in the case where the number of potentials to be supplied to the gate electrode of the transistor 1000 is four, data of two bits can be stored in each of the memory cells.

[0225]

Next, an example of a reading circuit which can be used for the semiconductor devices in FIGS. 10A and 10B, or the like will be described with reference to FIGS. 11A to 11C.

[0226]

FIG. 11A illustrates an outline of a reading circuit. The reading circuit includes a transistor and a sense amplifier circuit.

[0227]

At the time of reading data, a terminal A is connected to a bit line to which a memory cell from which data is read is connected. Further, a bias potential Vbias is applied to a gate electrode of the transistor so that a potential of the terminal A is controlled.

[0228]

The resistance of the memory cell 1050 varies depending on stored data. Specifically, when the transistor 1000 in the selected memory cell 1050 is on, the

memory cell has low resistance, whereas when the transistor 1000 in the selected memory cell 1050 is off, the memory cell has high resistance.

[0229]

When the memory cell has high resistance, a potential of the terminal A is higher than a reference potential Vref and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A. On the other hand, when the memory cell has low resistance, the potential of the terminal A is lower than the reference potential Vref and the sense amplifier circuit outputs a potential corresponding to the potential of the terminal A.

[0230]

Thus, by using the reading circuit, data can be read from the memory cell. Note that the reading circuit of this embodiment is an example. Another circuit may be used. The reading circuit may further include a precharge circuit. Instead of the reference potential Vref, a reference bit line may be connected to the sense amplifier circuit.

[0231]

FIG. 11B illustrates a differential sense amplifier which is an example of sense amplifier circuits. The differential sense amplifier has input terminals Vin (+) and Vin (−) and an output terminal Vout and amplifies the potential difference between Vin (+) and Vin (−). If the potential of Vin (+) is higher than the potential of Vin (−), Vout outputs a signal High, whereas if the potential of Vin (+) is lower than the potential of Vin (−), Vout outputs a signal Low. In the case where the differential sense amplifier is used for the reading circuit, one of Vin (+) and Vin (−) is connected to the terminal A, and the reference potential Vref is supplied to the other of Vin (+) and Vin (−).

[0232]

FIG. 11C illustrates a latch sense amplifier which is an example of sense amplifier circuits. The latch sense amplifier has input/output terminals V1 and V2 and input terminals of control signals Sp and Sn. First, the signal Sp is set high and the signal Sn is set low, and a power supply potential (Vdd) is interrupted. Next, a potential to be compared is supplied to each of V1 and V2. After that, when the power supply potential (Vdd) is supplied by setting the signal Sp low and the signal Sn high.

An output of V1 is High and an output of V2 is Low when the potential of V1 is higher than the potential of V2. The output of V1 is Low and the output of V2 is High when the potential of V1 is lower than the potential of V2. By utilizing such a relation, the potential difference between V1 and V2 can be amplified. In the case where the latch sense amplifier is used for the reading circuit, one of V1 and V2 is connected to the terminal A and the output terminal through a switch, and the reference potential Vref is supplied to the other of V1 and V2.

[0233]

In the semiconductor device described above, which can be used as a memory device, the transistor described in the above embodiment is used as the writing transistor of a memory cell, whereby a short-channel effect of the writing transistor can be suppressed and miniaturization thereof can be achieved. Accordingly, high integration of the semiconductor device which can be used as a memory device can be achieved.

[0234]

Further, the gate electrode of the reading transistor and the source electrode of the writing transistor are electrically connected to each other to have a structure similar to that described in the above embodiment, whereby the amount of heat generation or power consumption of the writing transistor which is electrically connected to the reading transistor can be reduced; accordingly, the transistors can be stacked with the amount of heat generation or power consumption of the transistor suppressed. Consequently, by forming a stacked-layer structure of the miniaturized transistors, three-dimensional high integration of the semiconductor device which can be used as a memory device can be achieved with favorable transistor characteristics maintained.

[0235]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0236]

(Embodiment 5)

In this embodiment, a structure of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIGS. 12A to

12D.

[0237]

<Planar Structure and Circuit Configuration of Semiconductor Device>

FIGS. 12A to 12C are specific examples of plan views of a memory cell included the semiconductor device described in the above embodiment. FIG. 12D illustrates a circuit configuration of the memory cell. FIGS. 12A to 12C are plan views illustrating three stages of a manufacturing process in order.

[0238]

The plan view of FIG. 12A illustrates the metal compound region 124 and the gate electrode 110 which are included in the transistor 160. Note that a channel formation region and a gate insulating layer over the channel formation region are provided below the gate electrode 110. The element isolation insulating layer 106 is provided so as to surround the transistor 160.

[0239]

The plan view of FIG. 12B illustrates the source electrode 142a, the drain electrode 142b, the oxide semiconductor layer 144, and the gate electrode 148a, which are included in the transistor 162; a signal line S1 (142b); a signal line S2 (148a); a word line WL (148b); and the electrode 148b included in the capacitor 164, in addition to the components illustrated in the plan view of FIG. 12A. The source electrode 142a and the drain electrode 142b included in the transistor 162 are formed using the same conductive layer as the signal line S1. Further, the gate electrode 148a included in the transistor 162, the electrode 148b included in the capacitor 164, the signal line S2, and the word line WL are formed using the same conductive layer. Note that in the capacitor 164, the source electrode 142a functions as one electrode and the electrode 148b functions as the other electrode.

[0240]

The plan view of FIG. 12C illustrates a bit line BL, a source line SL, an opening 130a formed between the bit line BL and the metal compound region 124, and an opening 130b formed between the source line SL and the metal compound region 124, in addition to the components illustrated in the plan view of FIG. 12B.

[0241]

In the case where the manufacturing method described in Embodiment 2 is

employed, FIG. 5A can be referred to for a cross-sectional structure along line C1-C2 and line D1-D2 in FIG. 12C.

[0242]

FIG. 12D illustrates a circuit configuration of the memory cell, corresponding to the plan views of FIGS. 12A to 12C. The memory cell illustrated in FIG. 12D includes the bit line (BL), the first signal line (S1), the source line (SL), the word line (WL), and the second signal line (S2).

[0243]

A conductive layer used for forming the source electrode and the drain electrode can be planarized by a CMP process. In the case of performing CMP treatment, the thickness of the conductive layer can be set as appropriate because the surface condition (the planarity of a surface) is hardly influenced by the thickness of the conductive layer. For example, by forming the conductive layer to have a large thickness (e.g., 150 nm to 500 nm), the conductive layer can have lower resistance and can be used for a wiring.

[0244]

Note that in the case where a CMP process is not performed on the conductive layer used for forming the source electrode and the drain electrode, a structure in which the conductive layer is tapered and the thickness of the conductive layer is reduced so that an oxide semiconductor layer favorably covers the conductive layer can be considered. In that case, the conductive layer has high resistance and thus is not favorable for use as a wiring. Furthermore, the tapered source electrode and drain electrode hinder miniaturization of the transistor 162. In contrast, according to a method for manufacturing a semiconductor device of an embodiment of the present invention, the conductive layer used for forming the source electrode layer and the drain electrode layer is planarized by a CMP process, whereby the source electrode and the drain electrode of the transistor 162 do not need to be tapered and the thickness of the conductive layer can be increased. Accordingly, the transistor 162 can be effectively miniaturized, and the wiring resistance can be reduced by increasing the thickness of the conductive layer.

[0245]

The plan views of FIGS. 12A to 12C are an example in which the conductive

layer used for forming the source electrode 142a is also used as the first signal line (S1). With such a structure, an opening for connection between the first signal line (S1) and the source electrode or the drain electrode is unnecessary and the area of the memory cell can be reduced as compared to the case where the first signal line is formed using another conductive layer. Moreover, the first signal line (S1) and the bit line (BL) are formed using different conductive layers, whereby these wirings can overlap with each other and thus the area can be reduced. Accordingly, by employing such a planar layout, high integration of the semiconductor device is possible.

[0246]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0247]

(Embodiment 6)

In this embodiment, an application example of a semiconductor device according to an embodiment of the disclosed invention will be described with reference to FIG. 13. In this embodiment, a central processing unit (CPU) will be described.

[0248]

FIG. 13 is an example of a block diagram of a CPU. A CPU 1101 illustrated in FIG. 13 includes a timing control circuit 1102, an instruction decoder 1103, a register array 1104, an address logic and buffer circuit 1105, a data bus interface 1106, an ALU (arithmetic logic unit) 1107, an instruction register 1108, and the like.

[0249]

These circuits are manufactured using the transistor described in the above embodiment, an inverter circuit, a resistor, a capacitor, and the like. Since the off-state current of the transistor described in the above embodiment can be extremely small, lower power consumption of the CPU 1101 can be realized. Moreover, by using the transistor described in the above embodiment, a short-channel effect of the transistor can be suppressed and miniaturization thereof can be achieved.

[0250]

Each of the circuits included in the CPU 1101 will be briefly described below. The timing control circuit 1102 receives an instruction from the outside, converts the

instruction into data for the inside, and sends the data to another block. In addition, the timing control circuit 1102 gives directions such as reading and writing of memory data to the outside in accordance with internal operation. The instruction decoder 1103 has a function of converting an instruction from the outside into an instruction for the inside.
5 The register array 1104 has a function of temporarily storing data. The address logic and buffer circuit 1105 has a function of specifying the address of an external memory. The data bus interface 1106 has a function of taking data in and out of an external memory or a device such as a printer. The ALU 1107 has a function of performing an operation. The instruction register 1108 has a function of temporarily storing an
10 instruction. The CPU includes a combination of such circuits.

[0251]

By using the transistor described in the above embodiment in at least part of the CPU 1101, a short-channel effect of the transistor can be suppressed and miniaturization thereof can be achieved; accordingly, high integration of the CPU 1101
15 can be achieved.

[0252]

Moreover, when a circuit element, a wiring, or the like included in each block of the CPU 1101 is formed by being stacked, the miniaturized transistor is connected to an electrode or a wiring of the circuit element in a manner similar to that described in
20 the above embodiment, whereby the amount of heat generation or power consumption of the miniaturized transistor can be reduced. Consequently, by forming a stacked-layer structure including the miniaturized transistor, three-dimensional high integration of the CPU 1101 can be achieved with favorable transistor characteristics maintained.

25 [0253]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0254]

30 (Embodiment 7)

In this embodiment, an application example of a semiconductor device according to an embodiment of the disclosed invention will be described with reference

to FIGS. 14A and 14B. Here, an example of a semiconductor device having an image sensor function of reading information of an object will be described. Note that in a circuit diagram, "OS" may be written beside a transistor in order to indicate that the transistor includes an oxide semiconductor.

5 [0255]

FIG. 14A illustrates an example of the semiconductor device having an image sensor function. FIG. 14A illustrates an equivalent circuit of a photosensor, and FIG. 14B is a cross-sectional view illustrating part of the photosensor.

[0256]

10 One electrode of a photodiode 1202 is electrically connected to a photodiode reset signal line 1212, and the other electrode of the photodiode 1202 is electrically connected to a gate of a transistor 1204. One of a source electrode and a drain electrode of the transistor 1204 is electrically connected to a photosensor reference signal line 1218, and the other of the source electrode and the drain electrode of the 15 transistor 1204 is electrically connected to one of a source electrode and a drain electrode of a transistor 1206. A gate electrode of the transistor 1206 is electrically connected to a gate signal line 1214, and the other of the source electrode and the drain electrode of the transistor 1206 is electrically connected to a photosensor output signal line 1216.

20 [0257]

Here, a transistor including an oxide semiconductor is used as the transistors 1204 and 1206 illustrated in FIG. 14A. As the transistor including an oxide semiconductor, the transistor described in the above embodiment can be used. In the transistor described in the above embodiment, leakage current in an off state can be 25 extremely small; therefore, the photodetection accuracy of the photosensor can be improved. Moreover, by using the transistor described in the above embodiment, a short-channel effect of the transistor can be suppressed and miniaturization thereof can be achieved; accordingly, the area of the photodiode can be increased and the photodetection accuracy of the photosensor can be improved.

30 [0258]

FIG. 14B is a cross-sectional view illustrating the photodiode 1202 and the transistor 1204 in the photosensor. An insulating layer 1248 where a wiring 1246 is

embedded is formed over a substrate 1222 (TFT substrate) having an insulating surface, and the photodiode 1202 functioning as a sensor and the transistor 1204 are provided over the insulating layer 1248. A substrate 1224 is provided over the photodiode 1202 and the transistor 1204 with the use of an adhesive layer 1228. Further, an insulating
5 layer 1234, an interlayer insulating layer 1236, and an interlayer insulating layer 1238 are provided over the transistor 1204.

[0259]

Here, the wiring 1246 is connected to the source electrode or the drain electrode of the transistor 1204 in a manner similar to that described in the above
10 embodiment, whereby the amount of heat generation or power consumption of the miniaturized transistor 1204 can be reduced. Consequently, by forming a stacked-layer structure including the miniaturized transistor, three-dimensional high integration of the photosensor can be achieved with favorable transistor characteristics maintained.

15 [0260]

Further, a gate electrode layer 1240 is provided in the same layer as the gate electrode of the transistor 1204 so as to be electrically connected to the gate electrode. The gate electrode layer 1240 is electrically connected to an electrode layer 1242 over the interlayer insulating layer 1236 through an opening provided in the insulating layer
20 1234 and the interlayer insulating layer 1236. Since the photodiode 1202 is formed over the electrode layer 1242, the photodiode 1202 and the transistor 1204 are electrically connected to each other through the gate electrode layer 1240 and the electrode layer 1242.

[0261]

25 The photodiode 1202 has a structure in which a first semiconductor layer 1226a, a second semiconductor layer 1226b, and a third semiconductor layer 1226c are sequentially stacked over the electrode layer 1242. In other words, the photodiode 1202 is electrically connected to the electrode layer 1242 through the first semiconductor layer 1226a. In addition, the photodiode 1202 is electrically connected
30 to an electrode layer 1244 over the interlayer insulating layer 1238 through the third semiconductor layer 1226c.

[0262]

Here, a pin photodiode in which a semiconductor layer having n-type conductivity as the first semiconductor layer 1226a, a high-resistance semiconductor layer (i-type semiconductor layer) as the second semiconductor layer 1226b, and a semiconductor layer having p-type conductivity as the third semiconductor layer 1226c
5 are stacked is illustrated as an example.

[0263]

The first semiconductor layer 1226a is an n-type semiconductor layer and is formed using an amorphous silicon film including an impurity element imparting n-type conductivity. The first semiconductor layer 1226a is formed by a plasma CVD method
10 using a semiconductor material gas including an impurity element belonging to Group 15 (e.g., phosphorus (P)). As the semiconductor material gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. Further alternatively, an amorphous silicon film which does not include an impurity element may be formed, and then an impurity element may be introduced into the
15 amorphous silicon film by a diffusion method or an ion implantation method. Heating or the like is preferably performed after introduction of the impurity element by an ion implantation method or the like in order to diffuse the impurity element. In this case, as a method for forming the amorphous silicon film, an LPCVD method, a chemical vapor deposition method, a sputtering method, or the like may be used. The first
20 semiconductor layer 1226a is preferably formed to have a thickness of greater than or equal to 20 nm and less than or equal to 200 nm.

[0264]

The second semiconductor layer 1226b is an i-type semiconductor layer (intrinsic semiconductor layer) and is formed using an amorphous silicon film. As for
25 formation of the second semiconductor layer 1226b, an amorphous silicon film is formed by a plasma CVD method using a semiconductor material gas. As the semiconductor material gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. The second semiconductor layer 1226b may be formed by an LPCVD method, a chemical vapor deposition method, a
30 sputtering method, or the like. The second semiconductor layer 1226b is preferably formed to have a thickness of greater than or equal to 200 nm and less than or equal to 1000 nm.

[0265]

The third semiconductor layer 1226c is a p-type semiconductor layer and can be formed using an amorphous silicon film including an impurity element imparting p-type conductivity. The third semiconductor layer 1226c is formed by a plasma CVD method using a semiconductor material gas including an impurity element belonging to Group 13 (e.g., boron (B)). As the semiconductor material gas, silane (SiH_4) may be used. Alternatively, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like may be used. Further alternatively, an amorphous silicon film which does not include an impurity element may be formed, and then an impurity element may be introduced into the amorphous silicon film by a diffusion method or an ion implantation method. Heating or the like is preferably performed after introduction of the impurity element by an ion implantation method or the like in order to diffuse the impurity element. In this case, as a method for forming the amorphous silicon film, an LPCVD method, a chemical vapor deposition method, a sputtering method, or the like may be used. The third semiconductor layer 1226c is preferably formed to have a thickness of greater than or equal to 10 nm and less than or equal to 50 nm.

[0266]

The first semiconductor layer 1226a, the second semiconductor layer 1226b, and the third semiconductor layer 1226c are not necessarily formed using an amorphous semiconductor, and they may be formed using a polycrystalline semiconductor or a microcrystalline semiconductor (semi-amorphous semiconductor (SAS)).

[0267]

Considering Gibbs free energy, the microcrystalline semiconductor is in a metastable state that is intermediate between an amorphous state and a single crystal state. That is, the microcrystalline semiconductor is a semiconductor having a third state which is stable in terms of free energy and has a short range order and lattice distortion. Columnar-like or needle-like crystals grow in a normal direction with respect to a substrate surface. The Raman spectrum of microcrystalline silicon, which is a typical example of a microcrystalline semiconductor, is shifted to a lower wavenumber side than 520 cm^{-1}, which represents single crystal silicon. That is, the peak of the Raman spectrum of the microcrystalline silicon exists between 520 cm^{-1}

which represents single crystal silicon and 480 cm^{-1} which represents amorphous silicon. In addition, microcrystalline silicon includes hydrogen or halogen at least 1 atomic% or more in order to terminate a dangling bond. Moreover, microcrystalline silicon includes a rare gas element such as helium, argon, krypton, or neon to further
5 promote lattice distortion, so that stability is increased and a favorable microcrystalline semiconductor can be obtained.

[0268]

This microcrystalline semiconductor film can be formed by a high-frequency plasma CVD method with a frequency of several tens of megahertz to several hundreds
10 of megahertz, or a microwave plasma CVD apparatus with a frequency of 1 GHz or higher. Typically, the microcrystalline semiconductor film can be formed by using a gas obtained by diluting silicon hydride such as SiH_4, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, or SiF_4, with hydrogen. Alternatively, the microcrystalline semiconductor film can be formed by using a gas including silicon hydride and hydrogen which is diluted with one
15 or more rare gas elements selected from helium, argon, krypton, and neon. In this case, the flow rate of hydrogen is set greater than or equal to 5 times and less than or equal to 200 times, preferably greater than or equal to 50 times and less than or equal to 150 times, further preferably 100 times, as high as that of silicon hydride. Further, a carbide gas such as CH_4 or C_2H_6, a germanium gas such as GeH_4 or GeF_4, F_2, or the like
20 may be mixed into the gas including silicon.

[0269]

In addition, since the mobility of holes generated by the photoelectric effect is lower than that of electrons, a pin photodiode has better characteristics when a surface on the p-type semiconductor layer side is used as a light-receiving plane. An example
25 in which the photodiode 1202 receives incident light 1230 from the substrate 1224 side and converts it into an electric signal is described here. Further, light from the semiconductor layer side, which has a conductivity type opposite to that of the semiconductor layer on the light-receiving plane side, is disturbance light; therefore, the electrode layer 1242 is preferably formed using a light-blocking conductive film. A
30 surface on the n-type semiconductor layer side can alternatively be used as the light-receiving plane.

[0270]

The incident light 1230 enters from the substrate 1224 side, whereby an oxide semiconductor layer of the transistor 1204 can be shielded from the incident light 1230 by the gate electrode of the transistor 1204.

5 [0271]

With the use of an insulating material, the insulating layer 1234, the interlayer insulating layer 1236, and the interlayer insulating layer 1238 can be formed, depending on the material, by a method such as a sputtering method, an SOG method, spin coating, dip coating, spray coating, or a droplet discharge method (such as an ink-jet method, 10 screen printing, or offset printing), or a tool (equipment) such as a doctor knife, a roll coater, a curtain coater, or a knife coater.

[0272]

As an inorganic insulating material of the insulating layer 1234, a single layer or a stack of any of oxide insulating layers and nitride insulating layers such as a silicon 15 oxide layer, a silicon oxynitride layer, a silicon nitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum oxynitride layer, an aluminum nitride layer, and an aluminum nitride oxide layer can be used. High-density plasma CVD using microwaves (2.45 GHz) is preferably employed because formation of a dense and high-quality insulating layer having high withstand voltage is possible.

20 [0273]

For reduction of surface roughness, an insulating layer functioning as a planarization insulating film is preferably used as the interlayer insulating layer 1236 and the interlayer insulating layer 1238. The interlayer insulating layer 1236 and the interlayer insulating layer 1238 can be formed using an organic insulating material 25 having heat resistance such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy, for example. Other than such organic insulating materials, it is possible to use a single layer or a stack of a low-dielectric constant material (a low-k material), a siloxane-based resin, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like.

30 [0274]

The photodiode 1202 can read information of an object by detecting the incident light 1230. Note that a light source such as a backlight can be used at the time

of reading information of an object.

[0275]

In the photosensor described above, the transistor described in the above embodiment can be used as the transistor including an oxide semiconductor. In the transistor described in the above embodiment, leakage current in an off state can be extremely small; therefore, the photodetection accuracy of the photosensor can be improved. Moreover, by using the transistor described in the above embodiment, a short-channel effect of the transistor can be suppressed and miniaturization thereof can be achieved; accordingly, the area of the photodiode can be increased and the photodetection accuracy of the photosensor can be improved.

[0276]

Further, a wiring is connected to a source electrode or a drain electrode of the transistor including an oxide semiconductor in a manner similar to that described in the above embodiment, whereby the amount of heat generation or power consumption of the miniaturized transistor can be reduced. Consequently, by forming a stacked-layer structure including the miniaturized transistor, three-dimensional high integration of the photosensor can be achieved with favorable transistor characteristics maintained.

[0277]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the structures, methods, and the like described in the other embodiments.

[0278]

(Embodiment 8)

In this embodiment, the cases where the semiconductor device described in any of the above embodiments is applied to an electronic device will be described with reference to FIGS. 15A to 15F. In this embodiment, the case where the above semiconductor device is applied to an electronic device such as a computer, a mobile phone (also referred to as a cellular phone or a mobile telephone device), a portable information terminal (including a portable game machine, an audio reproducing device, and the like), a digital camera, a digital video camera, electronic paper, or a television device (also referred to as a television or a television receiver).

[0279]

FIG. 15A illustrates a laptop computer including a housing 701, a housing 702, a display portion 703, a keyboard 704, and the like. The semiconductor device described in any of the above embodiments is provided in at least one of the housing 701 and the housing 702. Therefore, the laptop computer can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

[0280]

FIG. 15B illustrates a portable information terminal (personal digital assistance (PDA)). A main body 711 is provided with a display portion 713, an external interface 715, operation buttons 714, and the like. Further, a stylus 712 for operating the portable information terminal or the like is provided. The semiconductor device described in any of the above embodiments is provided in the main body 711. Therefore, the portable information terminal can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

[0281]

FIG. 15C illustrates an electronic book reader 720 mounting electronic paper. The electronic book reader has two housings of a housing 721 and a housing 723. The housing 721 and the housing 723 are provided with a display portion 725 and a display portion 727, respectively. The housing 721 and the housing 723 are connected by a hinge 737 and can be opened and closed with the hinge 737 as an axis. Further, the housing 721 is provided with a power switch 731, operation keys 733, a speaker 735, and the like. At least one of the housing 721 and the housing 723 is provided with the semiconductor device described in any of the above embodiments. Therefore, the electronic book reader can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

[0282]

FIG. 15D illustrates a mobile phone including two housings of a housing 740 and a housing 741. Further, the housing 740 and the housing 741 in a state where they are developed as illustrated in FIG. 15D can shift by sliding so that one is lapped over the other; therefore, the size of the mobile phone can be reduced, which makes the mobile phone suitable for being carried. The housing 741 is provided with a display panel 742, a speaker 743, a microphone 744, an operation key 745, a pointing device

746, a camera lens 747, an external connection terminal 748, and the like. The housing 740 is provided with a solar cell 749 that charges the mobile phone, an external memory slot 750, and the like. Further, an antenna is incorporated in the housing 741. At least one of the housing 740 and the housing 741 is provided with the semiconductor
5 device described in any of the above embodiments. Therefore, the mobile phone can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

[0283]

FIG. 15E illustrates a digital camera including a main body 761, a display
10 portion 767, an eyepiece 763, an operation switch 764, a display portion 765, a battery 766, and the like. The semiconductor device described in any of the above embodiments is provided in the main body 761. Therefore, the digital camera can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

15 [0284]

FIG. 15F illustrates a television device 770 including a housing 771, a display portion 773, a stand 775, and the like. The television device 770 can be operated by a switch of the housing 771 or a remote controller 780. The semiconductor devices described in any of the above embodiments are provided for the housing 771 and the
20 remote controller 780. Therefore, the television device can perform writing and reading of data at high speed, store data for a long time, and have sufficiently low power consumption.

[0285]

Thus, the semiconductor devices according to any of the above embodiments
25 are provided for the electronic devices described in this embodiment. Accordingly, electronic devices with low power consumption can be realized.

This application is based on Japanese Patent Application serial no. 2010-056758 filed with Japan Patent Office on March 12, 2010, the entire contents of
30 which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

an insulating layer;

5 a wiring embedded in the insulating layer;

an oxide semiconductor layer over the insulating layer;

a source electrode and a drain electrode electrically connected to the oxide semiconductor layer;

a gate electrode provided to overlap with the oxide semiconductor layer; and

10 a gate insulating layer provided between the oxide semiconductor layer and the gate electrode,

wherein at least a part of a top surface of the wiring is projected from the insulating layer,

wherein the part of the top surface of the wiring is positioned higher than a part

15 of a surface of the insulating layer,

wherein the wiring in a region projected from the insulating layer is electrically connected to the source electrode or the drain electrode.

2. The semiconductor device according to claim 1,

20 wherein a part of a side surface of the wiring is exposed.

3. A semiconductor device comprising:

an insulating layer;

a wiring embedded in the insulating layer;

25 an oxide semiconductor layer over the insulating layer;

a source electrode and a drain electrode electrically connected to the oxide semiconductor layer;

a gate electrode provided to overlap with the oxide semiconductor layer; and

a gate insulating layer provided between the oxide semiconductor layer and the

30 gate electrode,

wherein the insulating layer is formed so that at least a part of a top surface of the wiring is exposed,

wherein the part of the top surface of the wiring is positioned higher than a part of a surface of the insulating layer,

wherein the wiring in a region exposed from the insulating layer is electrically connected to the source electrode or the drain electrode, and

5 wherein a root-mean-square roughness of a region which is a part of the surface of the insulating layer and is in contact with the oxide semiconductor layer is less than or equal to 1 nm.

4. The semiconductor device according to claim 3,

10 wherein a part of a side surface of the wiring is exposed.

5. A semiconductor device comprising:

an insulating layer;

a wiring embedded in the insulating layer;

15 an oxide semiconductor layer over the insulating layer;

a source electrode and a drain electrode electrically connected to the oxide semiconductor layer;

a gate electrode provided to overlap with the oxide semiconductor layer; and

a gate insulating layer provided between the oxide semiconductor layer and the

20 gate electrode,

wherein the insulating layer is formed so that at least a part of a top surface of the wiring is exposed,

wherein the part of the top surface of the wiring is positioned higher than a part of a surface of the insulating layer,

25 wherein the wiring in a region exposed from the insulating layer is electrically connected to the gate electrode, and

wherein a root-mean-square roughness of a region which is a part of the surface of the insulating layer and is in contact with the oxide semiconductor layer is less than or equal to 1 nm.

30

6. The semiconductor device according to claim 5,

wherein a part of a side surface of the wiring is exposed.

7. A semiconductor device comprising:

a first insulating layer;

a wiring embedded in the first insulating layer;

5 a second insulating layer over the first insulating layer;

a source electrode and a drain electrode embedded in the second insulating layer;

an oxide semiconductor layer partly in contact with a surface of the second insulating layer, a surface of the source electrode, and a surface of the drain electrode;

10 a gate insulating layer covering the oxide semiconductor layer; and

a gate electrode provided over the gate insulating layer to overlap with the oxide semiconductor layer,

wherein the first insulating layer is formed so that at least a part of a top surface of the wiring is exposed,

15 wherein the part of the top surface of the wiring is positioned higher than a part of a surface of the first insulating layer,

wherein the wiring in a region exposed from the first insulating layer is electrically connected to the source electrode or the drain electrode, and

wherein a root-mean-square roughness of a region which is a part of the surface 20 of the second insulating layer and is in contact with the oxide semiconductor layer is less than or equal to 1 nm.

8. The semiconductor device according to claim 7,

wherein a part of a side surface of the wiring is exposed.

25

9. A semiconductor device comprising:

a first transistor;

an insulating layer provided over the first transistor; and

a second transistor provided over the first transistor with the insulating layer 30 positioned therebetween,

wherein the first transistor comprises:

a first channel formation region;

a first gate insulating layer provided over the first channel formation region;

a first gate electrode provided over the first gate insulating layer to overlap with the first channel formation region; and

a first source electrode and a first drain electrode electrically connected to the first channel formation region,

wherein the second transistor comprises:

a second channel formation region comprising an oxide semiconductor layer;

a second source electrode and a second drain electrode electrically connected to the second channel formation region;

a second gate electrode provided to overlap with the second channel formation region; and

a second gate insulating layer provided between the second channel formation region and the second gate electrode,

wherein the insulating layer is formed over the first transistor so that at least a part of a top surface of the first gate electrode is exposed,

wherein the part of the top surface of the first gate electrode is positioned higher than a part of a surface of the insulating layer,

wherein the first gate electrode in a region exposed from the insulating layer is electrically connected to the second source electrode or the second drain electrode, and

wherein a root-mean-square roughness of a region which is a part of the surface of the insulating layer and is in contact with the second channel formation region is less than or equal to 1 nm.

10. The semiconductor device according to claim 9,

wherein part of a side surface of the first gate electrode is exposed.

11. The semiconductor device according to claim 9,

wherein the first channel formation region and the second channel formation region comprise different semiconductor materials.

12. A semiconductor device comprising:

a first transistor;

a first insulating layer provided over the first transistor; and

a second transistor provided over the first transistor with the first insulating
5 layer positioned therebetween,

wherein the first transistor comprises:

a first channel formation region;

a first gate insulating layer provided over the first channel formation region;

10 a first gate electrode provided over the first gate insulating layer to overlap with the first channel formation region; and

a first source electrode and a first drain electrode electrically connected to the first channel formation region,

wherein the second transistor comprises:

15 a second source electrode and a second drain electrode embedded in a second insulating layer;

a second channel formation region which is partly in contact with a surface of the second insulating layer, a surface of the second source electrode, and a surface of the second drain electrode and comprises an oxide semiconductor layer;

20 a second gate insulating layer covering the second channel formation region; and

a second gate electrode provided over the second gate insulating layer to overlap with the second channel formation region,

wherein the first insulating layer is formed over the first transistor so that at
25 least a part of a top surface of the first gate electrode is exposed,

wherein the part of the top surface of the first gate electrode is positioned higher than a part of a surface of the first insulating layer,

wherein the first gate electrode in a region exposed from the first insulating layer is electrically connected to the second source electrode or the second drain
30 electrode, and

wherein a root-mean-square roughness of a region which is a part of the surface of the second insulating layer and is in contact with the second channel formation

region is less than or equal to 1 nm.

13. The semiconductor device according to claim 12,

wherein a part of a side surface of the first gate electrode is exposed.

5

14. The semiconductor device according to claim 12,

wherein the first channel formation region and the second channel formation region comprise different semiconductor materials.

10 15. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first insulating layer in which a wiring is embedded;

performing planarization treatment on a surface of the first insulating layer so that the planarized first insulating layer partly comprises a surface with a
15 root-mean-square roughness of less than or equal to 1 nm, at least a part of a top surface of the wiring is exposed, and the part of the top surface of the wiring is positioned higher than a part of the surface of the first insulating layer;

forming a source electrode and a drain electrode over the surfaces of the first insulating layer and the wiring so that the source electrode or the drain electrode is
20 electrically connected to the wiring in a region exposed from the first insulating layer;

forming a second insulating layer so as to cover the source electrode and the drain electrode;

performing planarization treatment on a surface of the second insulating layer so that the planarized second insulating layer partly comprises a surface with a
25 root-mean-square roughness of less than or equal to 1 nm and at least a part of top surfaces of the source electrode and the drain electrode is exposed;

forming an oxide semiconductor layer partly in contact with the surface of the planarized second insulating layer, a surface of the source electrode, and a surface of the drain electrode;

30 forming a gate insulating layer covering the oxide semiconductor layer; and

forming a gate electrode over the gate insulating layer so as to overlap with the oxide semiconductor layer.

16. The method for manufacturing a semiconductor device, according to claim 15,

wherein the planarization treatment is performed by CMP treatment.

5

17. A method for manufacturing a semiconductor device, comprising the steps of:

forming a first transistor comprising a first channel formation region, a first gate insulating layer over the first channel formation region, a first gate electrode which
10 is over the first gate insulating layer and overlaps with the first channel formation region, and a first source electrode and a first drain electrode electrically connected to the first channel formation region;

forming a first insulating layer so as to cover the first transistor;

performing planarization treatment on a surface of the first insulating layer so
15 that the planarized first insulating layer partly comprises a surface with a root-mean-square roughness of less than or equal to 1 nm, at least a part of a top surface of the first gate electrode is exposed, and the part of the top surface of the first gate electrode is positioned higher than a part of the surface of the first insulating layer;

forming a second source electrode and a second drain electrode over the
20 surfaces of the first insulating layer and the first gate electrode so that the second source electrode or the second drain electrode is electrically connected to the first gate electrode in a region exposed from the first insulating layer;

forming a second insulating layer so as to cover the second source electrode and the second drain electrode;

25 performing planarization treatment on a surface of the second insulating layer so that the planarized second insulating layer partly comprises a surface with a root-mean-square roughness of less than or equal to 1 nm and at least a part of top surfaces of the second source electrode and the second drain electrode is exposed;

forming a second channel formation region which is partly in contact with the
30 surface of the planarized second insulating layer, a surface of the second source electrode, and a surface of the second drain electrode and comprises an oxide semiconductor layer;

forming a second gate insulating layer covering the second channel formation region; and

forming a second gate electrode over the second gate insulating layer so as to overlap with the second channel formation region.

5

18. The method for manufacturing a semiconductor device, according to claim 17,

wherein the planarization treatment is performed by CMP treatment.

FIG. 1A

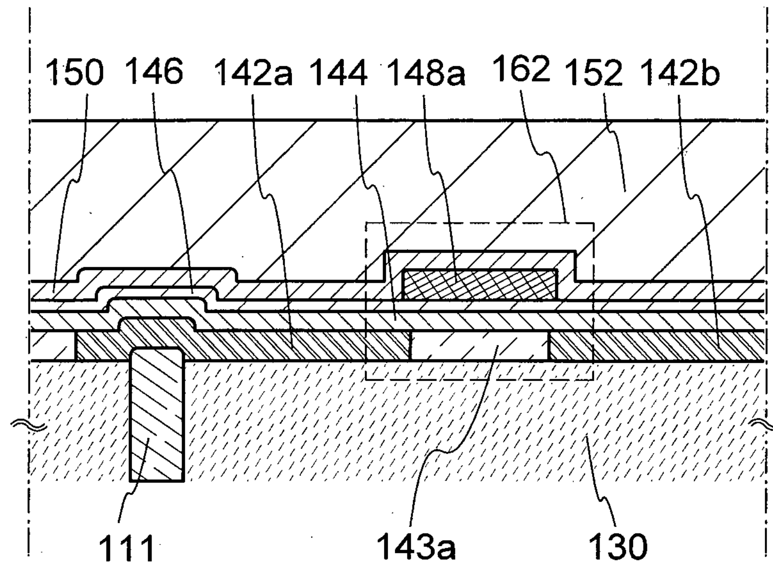


FIG. 1B

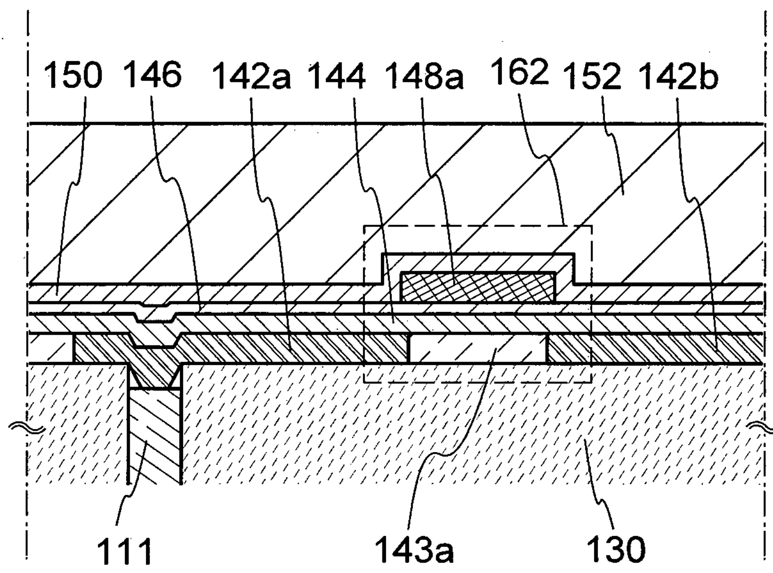


FIG. 2A

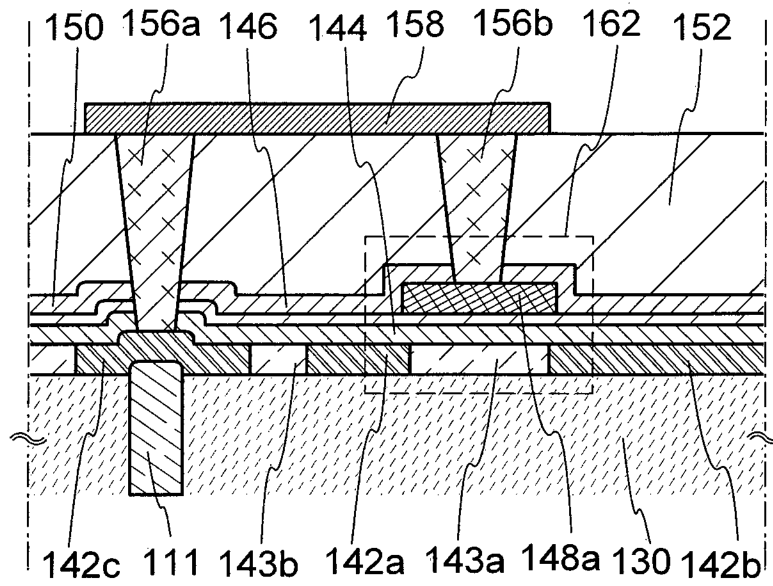


FIG. 2B

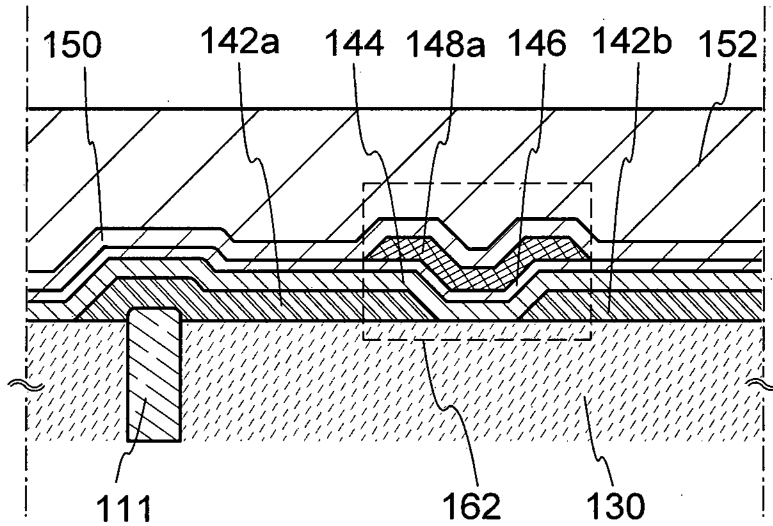


FIG. 3A

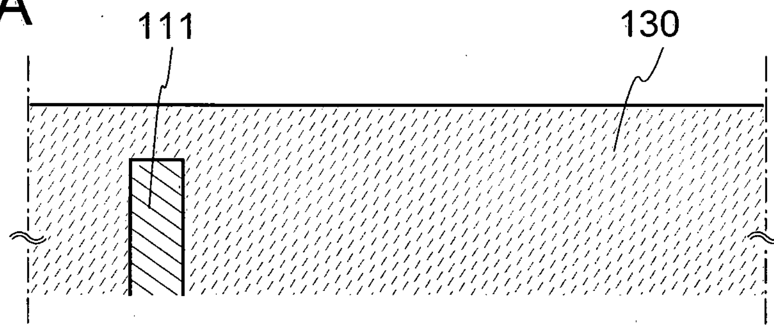


FIG. 3B

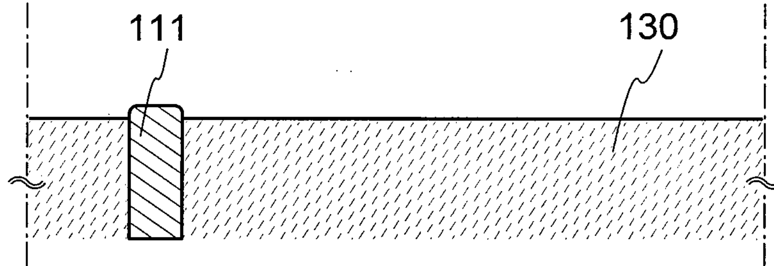


FIG. 3C

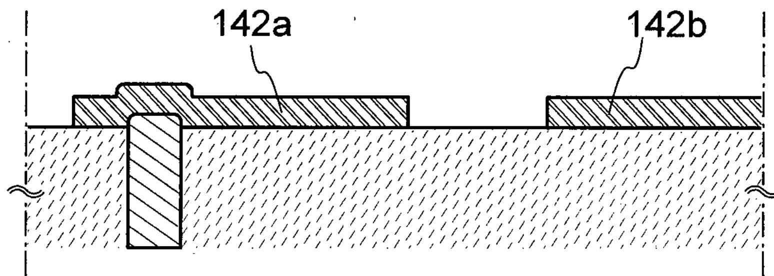


FIG. 3D

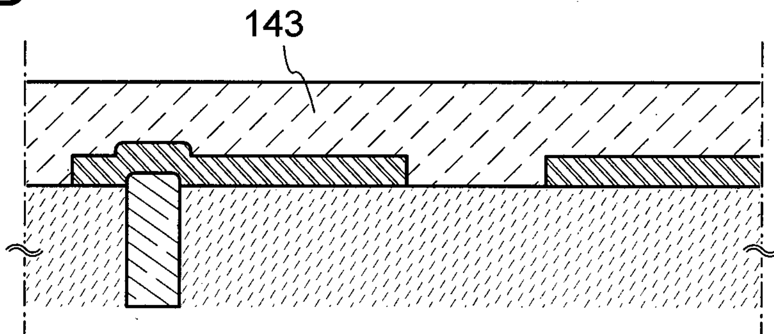


FIG. 3E

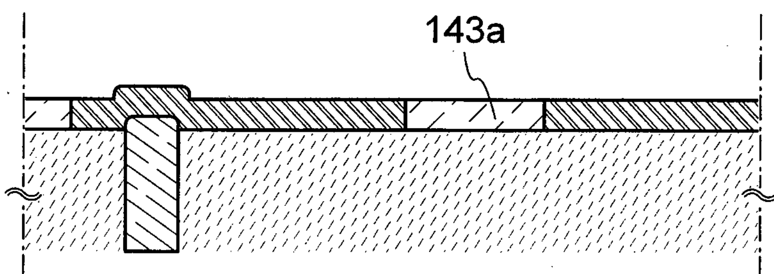


FIG. 4A

FIG. 4B

FIG. 4C

FIG. 5A

FIG. 5B

FIG. 5C

FIG. 6A

FIG. 6B

FIG. 6C

FIG. 7A

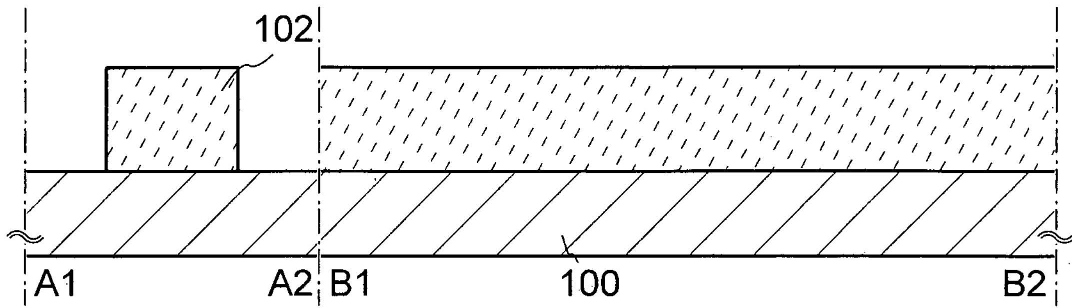


FIG. 7B

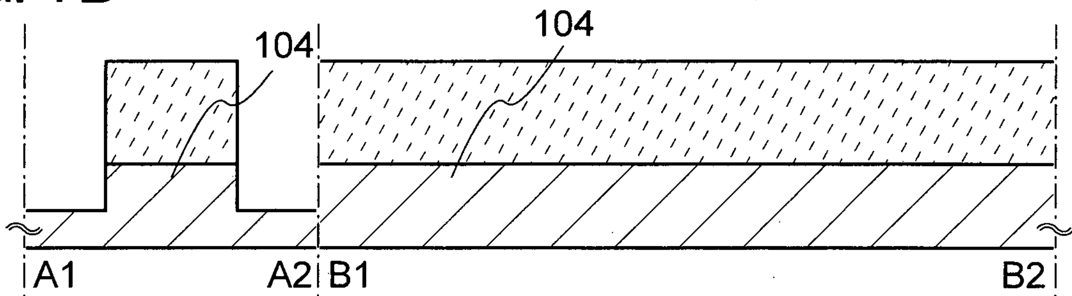


FIG. 7C

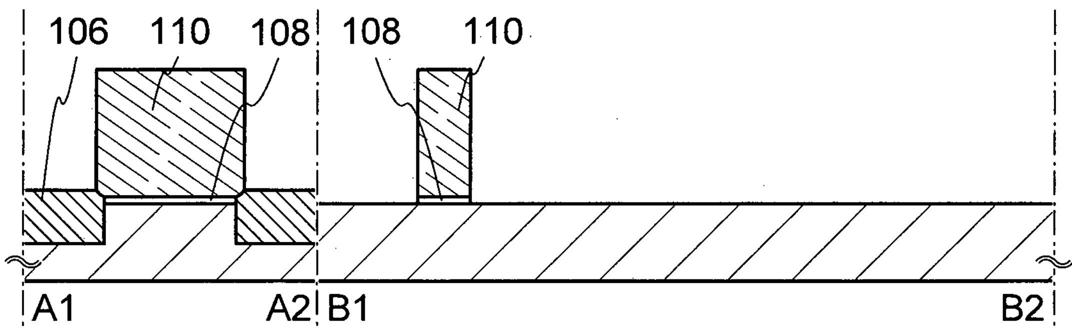


FIG. 7D

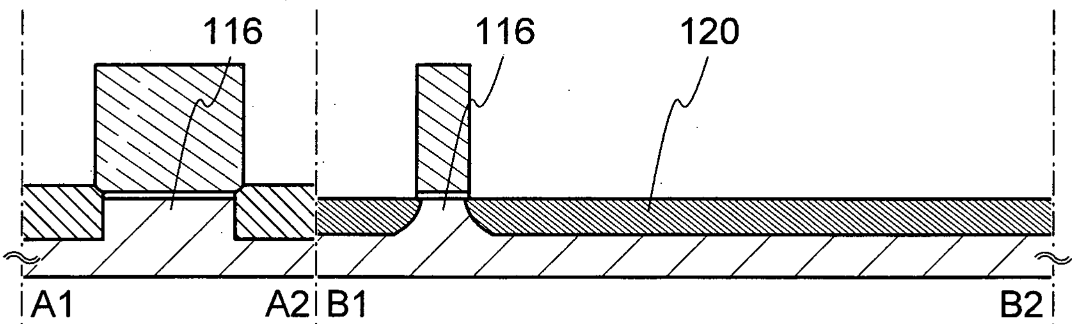


FIG. 8A

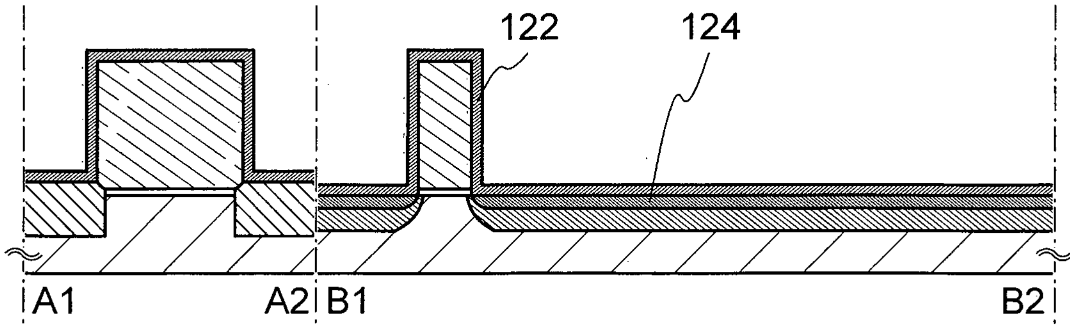


FIG. 8B

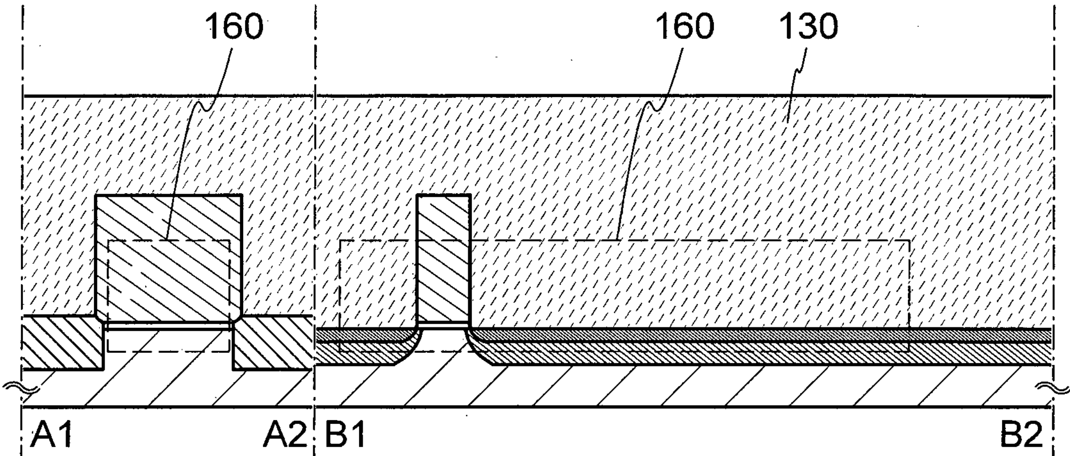


FIG. 8C

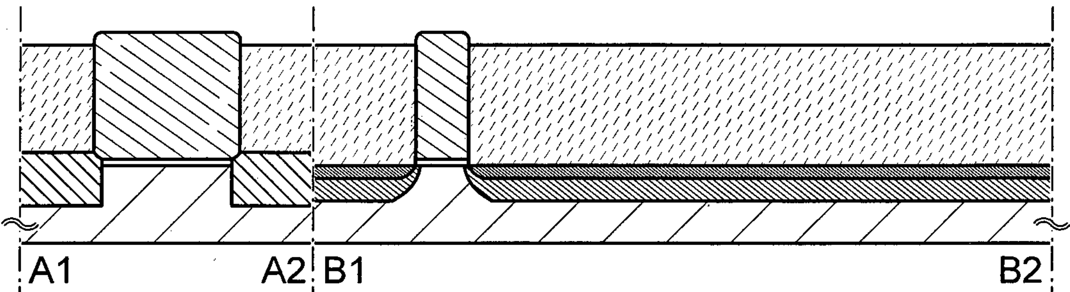


FIG. 9A

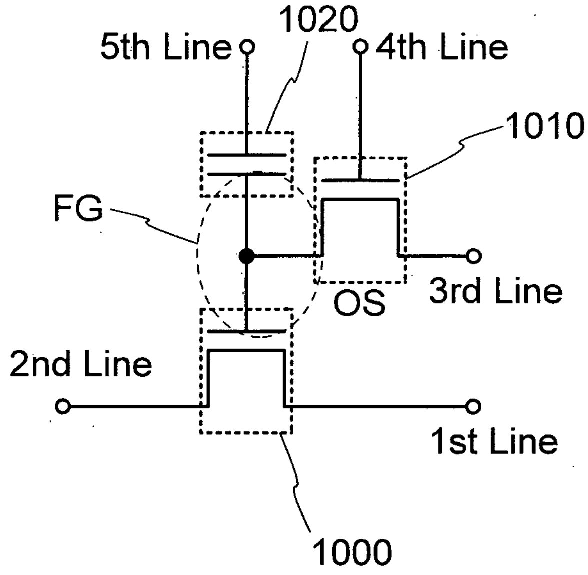


FIG. 9C

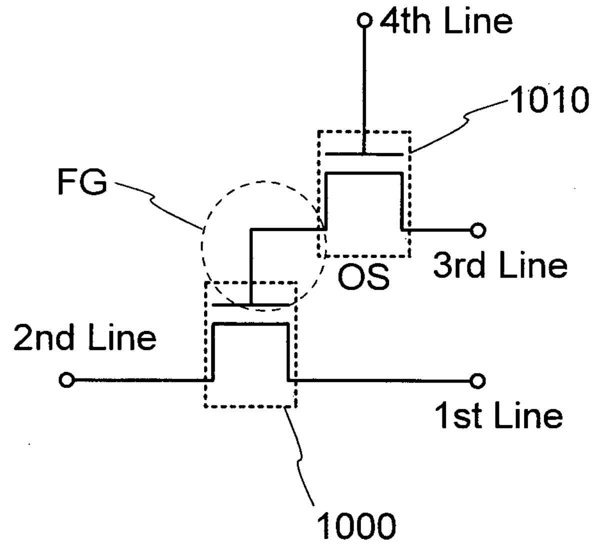


FIG. 9B

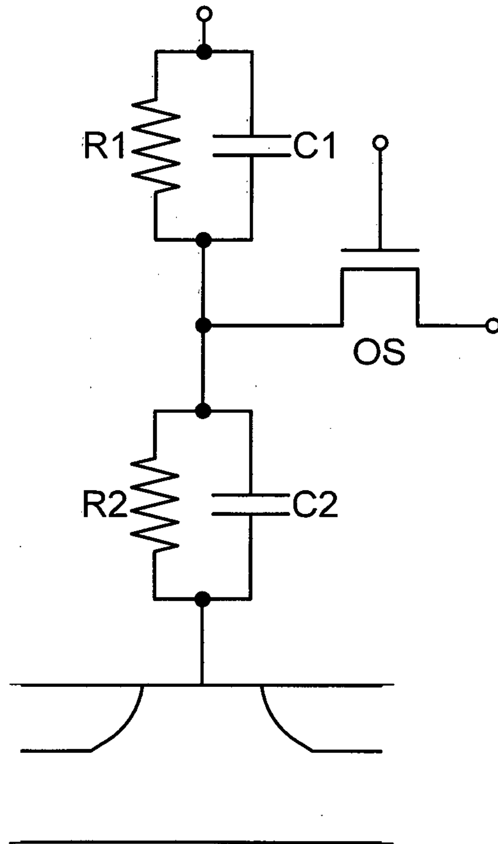


FIG. 10A

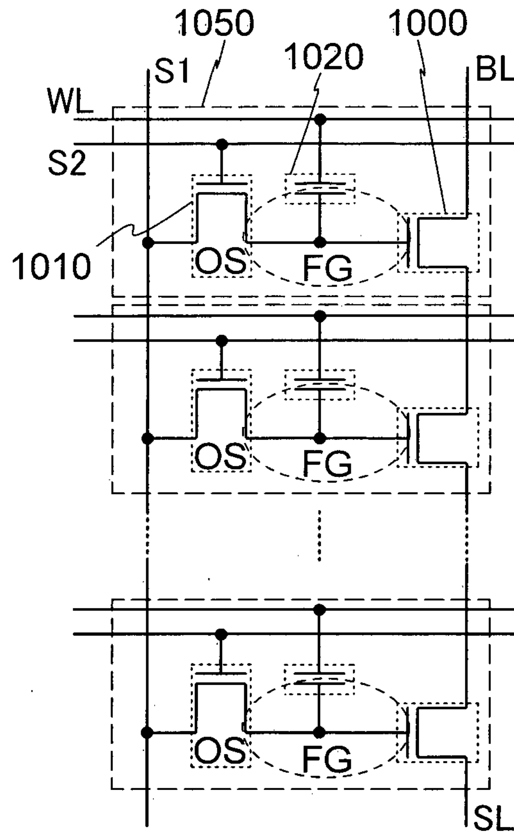


FIG. 10B

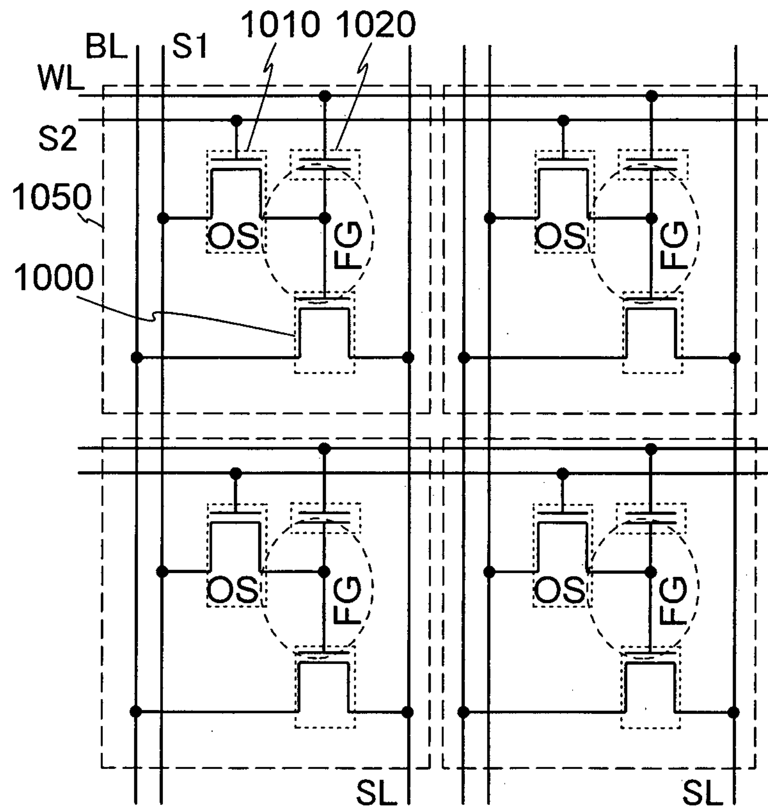


FIG. 11A

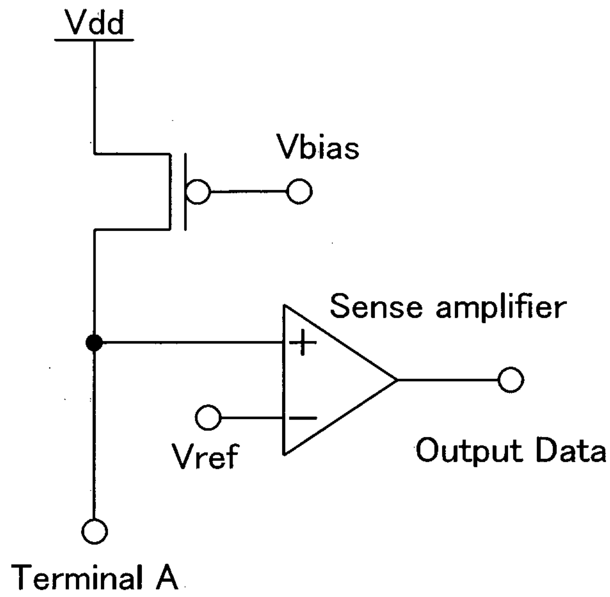


FIG. 11B

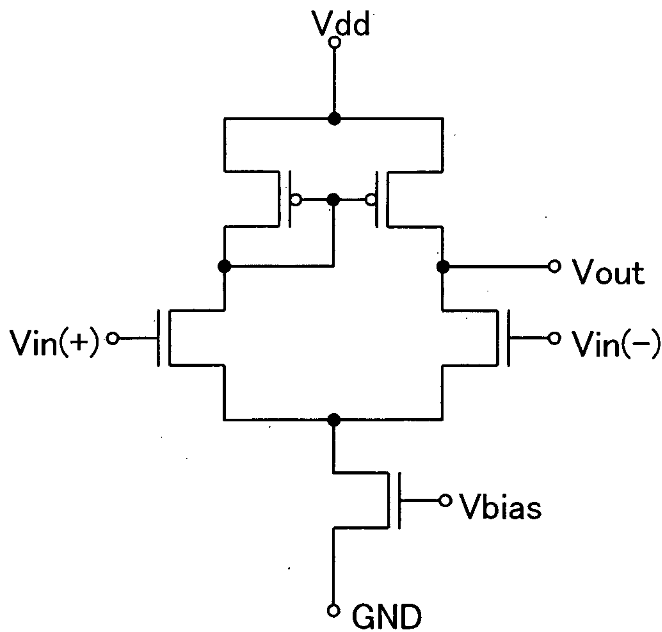


FIG. 11C

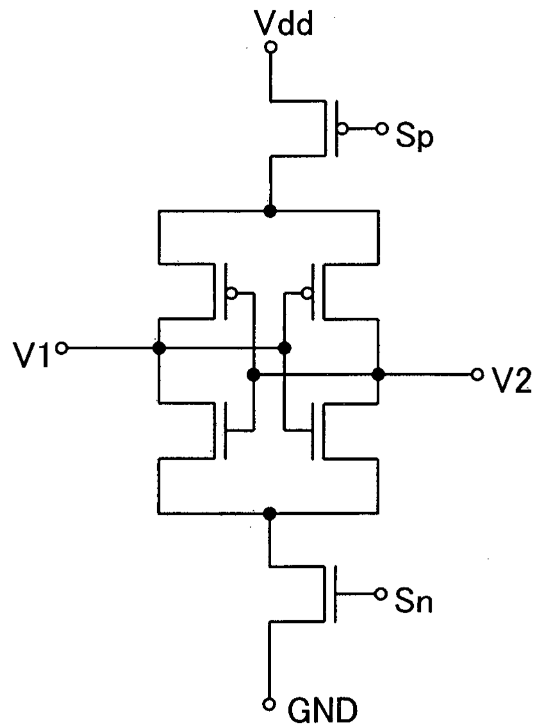


FIG. 12A

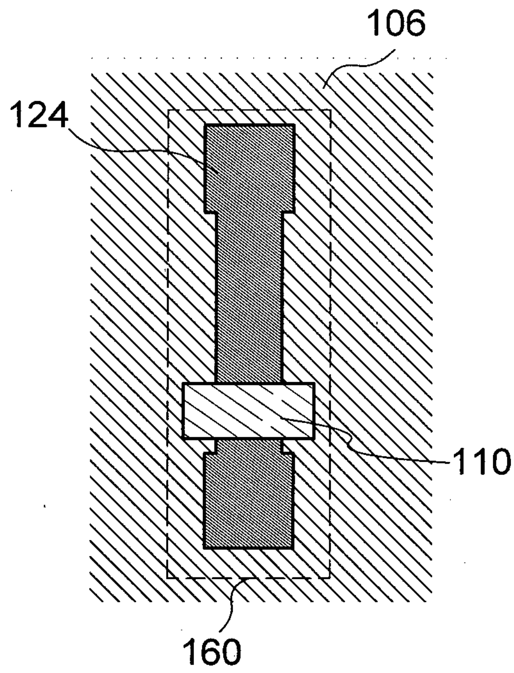


FIG. 12B

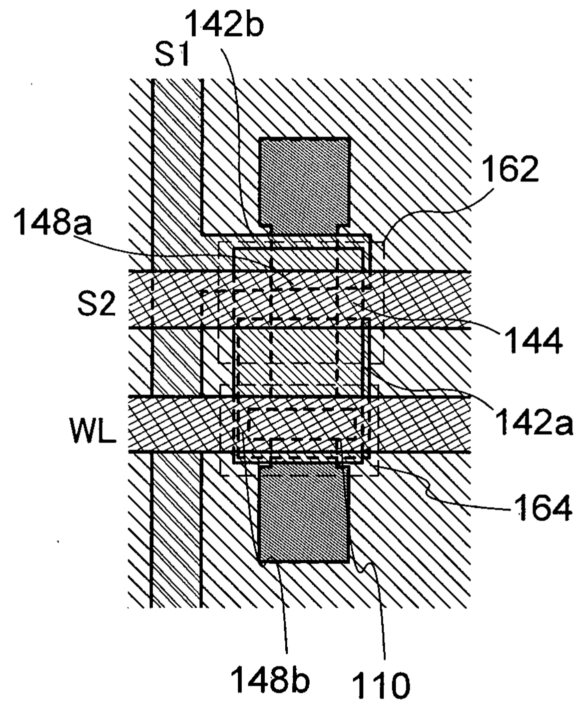


FIG. 12C

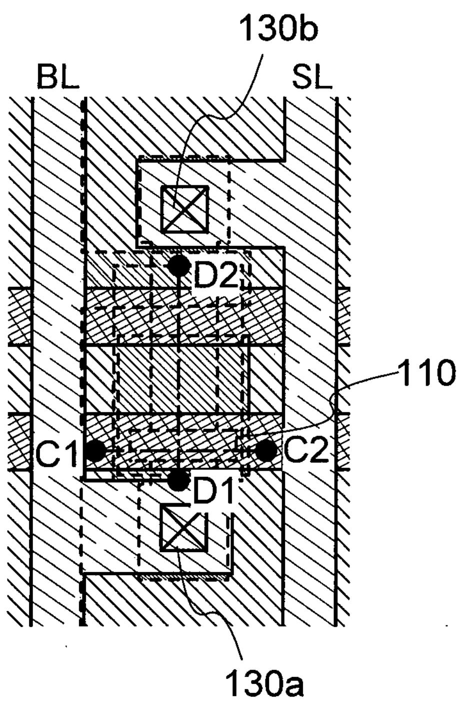
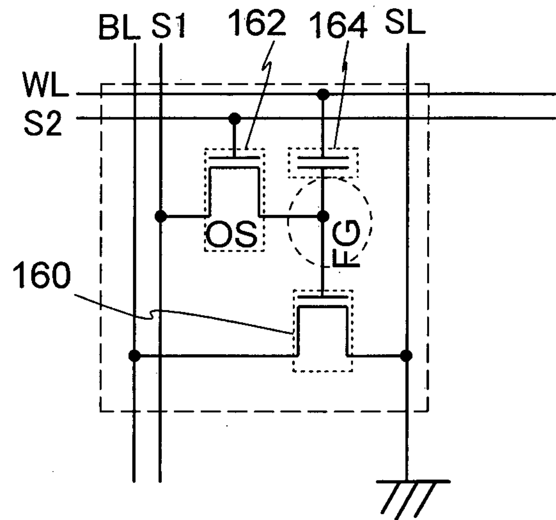


FIG. 12D



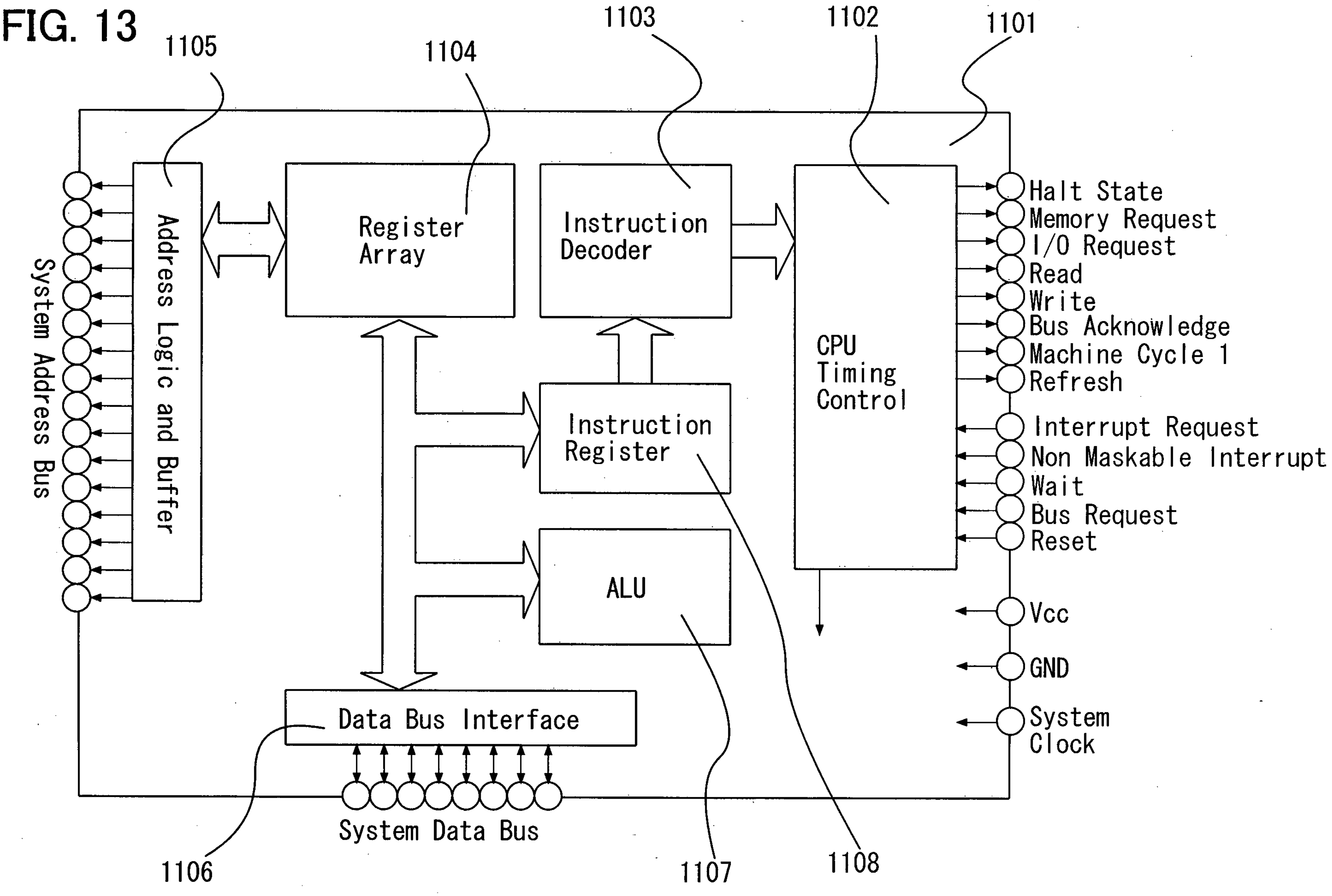


FIG. 13
1105
1104
1103
1102
1101
Register Array
Instruction Decoder
CPU Timing Control
Halt State
Memory Request
I/O Request
Read
Write
Bus Acknowledge
Machine Cycle 1
Refresh
Interrupt Request
Non Maskable Interrupt
Wait
Bus Request
Reset
Vcc
GND
System Clock
System Address Bus
Address Logic and Buffer
Instruction Register
ALU
Data Bus Interface
System Data Bus
1106
1107
1108

FIG. 14A

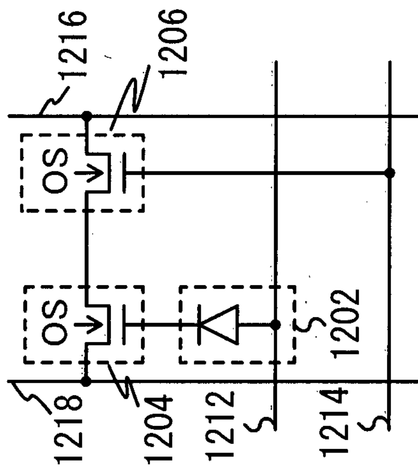


FIG. 14B

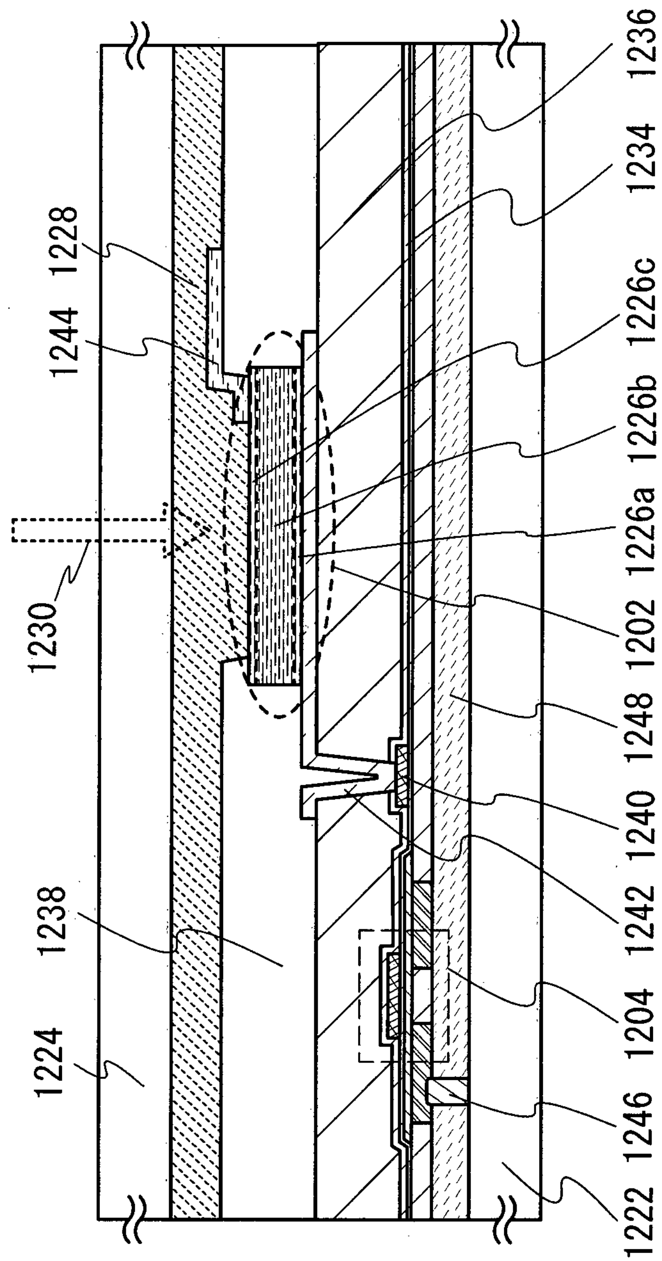


FIG. 15A

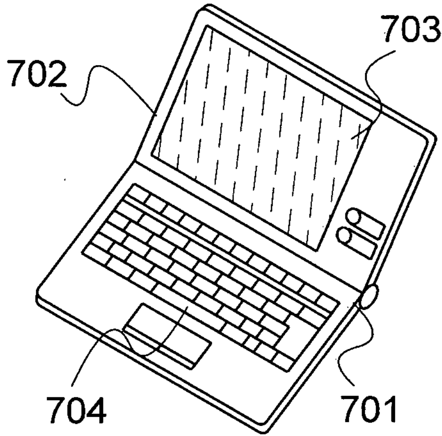


FIG. 15D

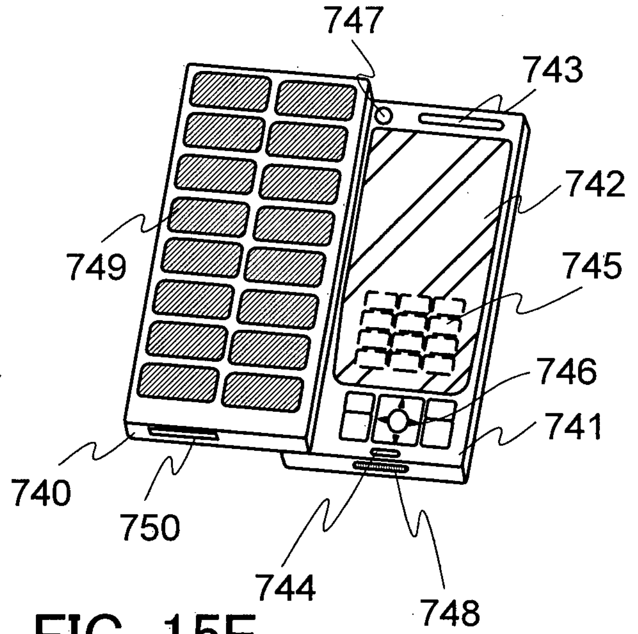


FIG. 15B

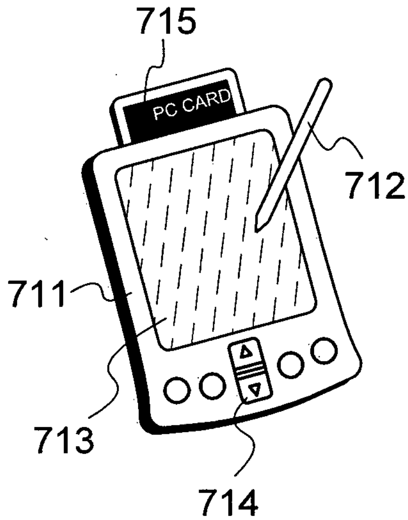


FIG. 15E

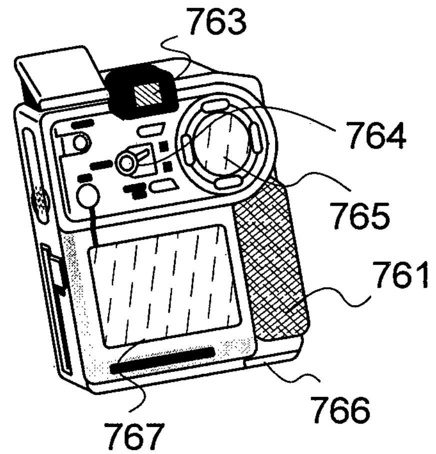


FIG. 15C

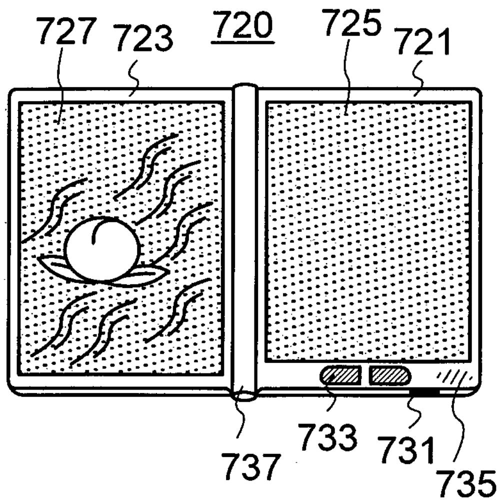
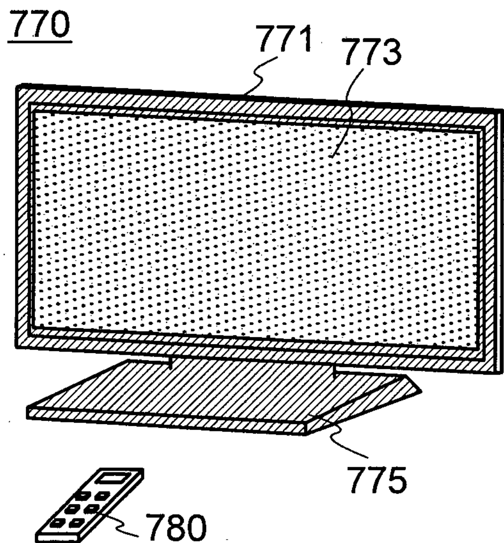


FIG. 15F



EXPLANATION OF REFERENCE

100: substrate, 102: protective layer, 104: semiconductor region, 106: element isolation insulating layer, 108: gate insulating layer, 110: gate electrode, 111: wiring, 116: channel formation region, 120: impurity region, 122: metal layer, 124: metal compound region, 130: insulating layer, 130a: opening, 130b: opening, 142a: source electrode, 142b: drain electrode, 143: insulating layer, 143a: insulating layer, 144: oxide semiconductor layer, 146: gate insulating layer, 148a: gate electrode, 148b: electrode, 150: insulating layer, 152: insulating layer, 156a: electrode, 156b: electrode, 158: wiring, 160: transistor, 162: transistor, 164: capacitor, 701: housing, 702: housing, 703: display portion, 704: keyboard, 711: main body, 712: stylus, 713: display portion, 714: operation button, 715: external interface, 720: electronic book reader, 721: housing, 723: housing, 725: display portion, 727: display portion, 731: power switch, 733: operation key, 735: speaker, 737: hinge, 740: housing, 741: housing, 742: display panel, 743: speaker, 744: microphone, 745: operation key, 746: pointing device, 747: camera lens, 748: external connection terminal, 749: solar cell, 750: external memory slot, 761: main body, 763: eyepiece, 764: operation switch, 765: display portion, 766: battery, 767: display portion, 770: television set, 771: housing, 773: display portion, 775: stand, 780: remote controller, 1000: transistor, 1010: transistor, 1020: capacitor, 1050: memory cell, 1101: CPU, 1102: timing control circuit, 1103: instruction decoder, 1104: register array, 1105: address logic and buffer circuit, 1106: data bus interface, 1107: ALU, 1108: instruction register, 1202: photodiode, 1204: transistor, 1206: transistor, 1212: photodiode reset signal line, 1214: gate signal line, 1216: photosensor output signal line, 1218: photosensor reference signal line, 1222: substrate, 1224: substrate, 1226a: first semiconductor layer, 1226b: second semiconductor layer, 1226c: third semiconductor layer, 1228: adhesive layer, 1230: incident light, 1234: insulating layer, 1236: interlayer insulating layer, 1238: interlayer insulating layer, 1240: gate electrode layer, 1242: electrode layer, 1244: electrode layer, 1246: wiring, and 1248: insulating layer.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/053616

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, G11C11/401, H01L21/336, H01L21/768, H01L21/8242, H01L21/8247, H01L27/10, H01L27/108, H01L27/115, H01L29/788, H01L29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2011
Registered utility model specifications of Japan 1996-2011
Published registered utility model applications of Japan 1994-2011

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 5-166942 A (MITSUBISHI ELECTRIC CORPORATION) 1993.07.02, FULL TEXT (No Family)	1-18
A	JP 2009-141342 A (FUJIFILM CORPORATION) 2009.06.25, FULL TEXT & US 2009/0127551 A1 & EP 2061087 A2 & KR 10-2009-0050971 A	1-18
A	JP 63-169755 A (AGENCY OF INDUSTRIAL SCIENCE AND TECHNOLOGY) 1988.07.13, FULL TEXT (No Family)	1-18

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02.05.2011	17.05.2011

Name and mailing address of the ISA/JP
Japan Patent Office
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer
MIYAZAWA, Takayuki
4M 9278
Telephone No. +81-3-3581-1101 Ext. 3462

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2011/053616

CLASSIFICATION OF SUBJECT MATTER

H01L29/786(2006.01)i, G11C11/401(2006.01)i, H01L21/336(2006.01)i, H01L21/768(2006.01)i, H01L21/8242(2006.01)i, H01L21/8247(2006.01)i, H01L27/10(2006.01)i, H01L27/108(2006.01)i, H01L27/115(2006.01)i, H01L29/788(2006.01)i, H01L29/792(2006.01)i