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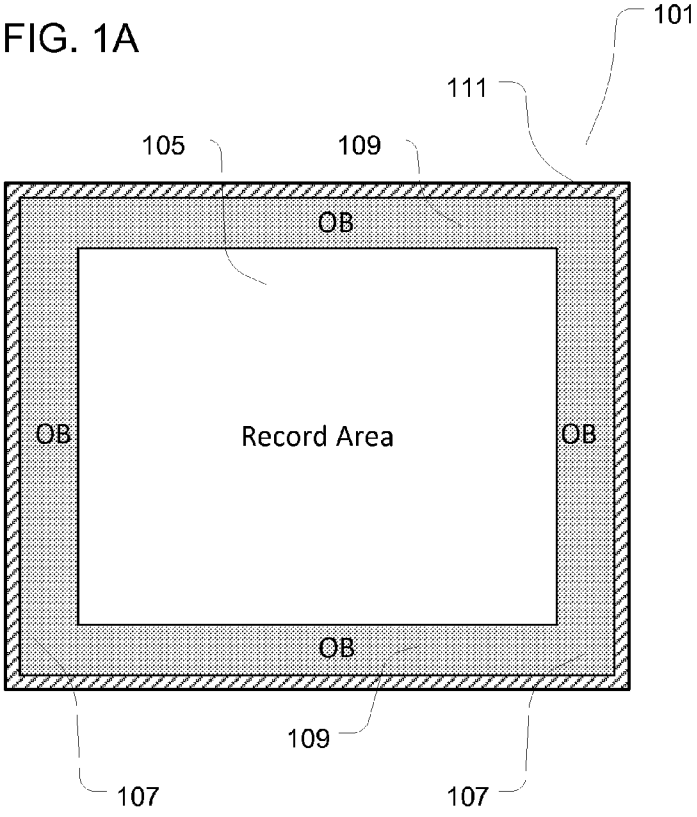
(54) Title: CAMERA SYSTEM WITH MINIMAL AREA MONOLITHIC CMOS IMAGE SENSOR

FIG. 1A



(57) Abstract: The disclosure extends to methods, systems, and computer program products for digitally imaging with area limited image sensors, such as within a lumen of an endoscope.

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CAMERA SYSTEM WITH MINIMAL AREA MONOLITHIC CMOS IMAGE SENSOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Patent Application No. 61/676,289, filed on July 26, 2012, and U.S. Provisional Patent Application No. 61/790,590, filed on March 15, 2013, which are hereby incorporated by reference herein in their entireties, including but not limited to those portions that specifically appear hereinafter, the incorporation by reference being made with the following exception: In the event that any portion of the above-referenced applications is inconsistent with this application, this application supersedes said above-referenced applications.

BACKGROUND

[0001] Advances in technology have provided advances in imaging capabilities for medical use. One area that has enjoyed some of the most beneficial advances may be that of endoscopic surgical procedures because of the advances in the components that make up an endoscope. Conventional endoscopes used in, e.g., arthroscopy and laparoscopy are designed such that the image sensors are placed at the proximal end of the device, within the hand-piece unit. In such a configuration, the endoscope unit should transmit the incident light along its length toward the sensor via a complex set of precisely coupled optical components, with minimal loss and distortion. The cost of the endoscope unit may be dominated by the optics, since the components are expensive and the manufacturing process may be labor intensive. Furthermore, this type of scope may be mechanically delicate and relatively minor impacts can easily damage the components or upset the relative alignments thereof. This necessitates frequent, expensive repair cycles in order to maintain image quality.

[0002] What may be needed are methods and systems for providing reduced area image sensors for endoscopic medical use that may be capable of maintaining high quality video streams in reduced light environments. Reducing the area of the sensor allows it to be located at the distal end of the endoscope, therefore greatly reducing cost. This introduces the possibility of single-use endoscopes, requiring no repair or sterilization cycles. Alternatively they may be disassembled after and have some of their components recycled.

[0003] As may be seen, the disclosure provides methods and systems that can do this in an efficient and elegant manner that will be disclosed herein and will be further enabled by the discussion in the specification and the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Non-limiting and non-exhaustive implementations of the disclosure are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified. Advantages of the disclosure may become better understood with regard to the following description and accompanying drawings where:

[0005] FIG. 1A illustrates an implementation of a pixel array common in the prior art;

[0006] FIG. 1B illustrates an implementation of a pixel array made in accordance with the principles and teachings of the disclosure having optical black pixels formed into optical black columns;

[0007] FIG. 1C illustrates a schematic of system circuitry and complementary system hardware in accordance with the principles and teachings of the disclosure;

[0008] FIG. 2 illustrates an example pixel array showing the relationships between active recording pixel columns and optical black pixel columns in accordance with the principles and teachings of the disclosure;

[0009] FIG. 3 illustrates an example pixel array showing the relationships between active recording pixel columns and reduced number of optical black pixel columns in accordance with the principles and teachings of the disclosure;

[0010] FIG. 4 illustrates a hardware flow chart of an example method according to one implementation in accordance with the principles and teachings of the disclosure;

[0011] FIG. 5 illustrates a hardware flow chart of an example method according to one implementation in accordance with the principles and teachings of the disclosure;

[0012] FIG. 6 illustrates a flow chart of an example method and hardware schematics for use with a partitioned light system according to one implementation in accordance with the principles and teachings of the disclosure;

[0013] FIG. 7 illustrates a flow chart of an example method according to one implementation in accordance with the principles and teachings of the disclosure;

[0014] FIG. 8A illustrates a flow chart of an example method according to one implementation in accordance with the principles and teachings of the disclosure;

[0015] FIG. 8B illustrates a flow chart of an example method according to one implementation in accordance with the principles and teachings of the disclosure;

[0016] FIG. 9 illustrates a flow chart of an example method according to one implementation;

[0017] FIG. 10 illustrates a hardware flow chart of an example method according to one implementation in accordance with the principles and teachings of the disclosure;

[0018] FIGS. 11A and 11B illustrate an implementation having a plurality of pixel arrays for producing a three dimensional image in accordance with the teachings and principles of the disclosure;

[0019] FIGS. 12A and 12B illustrate a perspective view and a side view, respectively, of an implementation of an imaging sensor built on a plurality of substrates, wherein a plurality of pixel columns forming the pixel array are located on the first substrate and a plurality of circuit columns are located on a second substrate and showing an electrical connection and communication between one column of pixels to its associated or corresponding column of circuitry; and

[0020] FIGS. 13A and 13B illustrate a perspective view and a side view, respectively, of an implementation of an imaging sensor having a plurality of pixel arrays for producing a three dimensional image, wherein the plurality of pixel arrays and the image sensor are built on a plurality of substrates.

DETAILED DESCRIPTION

[0021] The disclosure extends to methods, systems, and computer program products for providing advanced endoscopes and uses thereof during medical procedures. In the following discussion of the disclosure, reference may be made to the accompanying drawings, which form a part hereof, and in which may be shown by way of illustration specific implementations in which the disclosure may be practiced. It may be understood that other implementations may be utilized, and structural changes may be made without departing from the scope of the disclosure.

[0022] Conventional endoscopes used in arthroscopy and laparoscopy are designed such that the image sensors are placed at the proximal end of the device, within the hand-piece unit. In such a configuration, the endoscope unit should transmit the incident light along its length toward the sensor via a complex set of precisely coupled optical components, with minimal loss and distortion. The cost of the endoscope unit may be dictated by the costs associated with

the optics, since the components are expensive and the manufacturing process may be labor intensive.

[0023] A solution to the above short comings may be to place the image sensor within the endoscope itself at the distal end within the lumen, thereby potentially providing greater optical simplicity, robustness and economy that may be universally realized within related devices such as for example cell phone cameras. An acceptable solution to this approach may be by no means trivial however as it introduces its own set of engineering challenges, not least of which may be the fact that the sensor should fit within a highly confined area.

[0024] Placing aggressive constraints on sensor area may result in fewer and/or smaller pixels. Accordingly, lowering the pixel count directly affects the spatial resolution. Reducing the pixel area also may reduce the available signal capacity and the sensitivity. Lowering the signal capacity reduces the dynamic range i.e. the ability of the camera to simultaneously capture all of the useful information from scenes with large ranges of luminosity. There are various methods to extend the dynamic range of imaging systems beyond that of the pixel itself. All of them have some kind of penalty however, (e.g. in resolution or frame rate) and they can introduce or emphasize undesirable artifacts which become problematic in extreme cases. Alternatively, reducing the sensitivity has the consequence that greater light power may be required to bring the darker regions of the scene to acceptable signal levels. Lowering the F-number may compensate for a loss in sensitivity too, but at the cost of spatial distortion and reduced depth of focus.

[0025] In imaging sensor technology, CMOS images sensors have largely displaced conventional CCD imagers in modern camera applications such as endoscopy, owing to their greater ease of integration and operation, superior or comparable image quality, greater versatility and lower cost. Yet CMOS sensors bring certain undesirable traits that should be accounted for in order to achieve optimal results.

[0026] Image sensors may include the circuitry necessary to convert the image information into digital data and may have various levels of digital processing incorporated on the sensor chip itself. The digital processes may range from basic algorithms for the purpose of correcting non-idealities of the CMOS sensors which may arise from variations in amplifier behavior, to full image signal processing (ISP) chains, which provide video data in the standard sRGB color space (cameras-on-chip).

[0027] The desired degree of sensor complexity for a given camera system may be driven by several factors, one of which may be the available physical space for the image sensor. The

most extreme functionally minimal CMOS sensor would have only the basic pixel array plus a degree of serializing and buffering circuits to drive the analog data off chip. All of the timing signals required to operate and read out the pixels may be provided externally. The need to supply the control signals externally, may add many pads which consume significant real estate that would be better used for gathering light. Therefore it doesn't necessarily follow that minimal functionality near the pixel array equates to minimal area usage because of the need of electrical communication connections.

[0028] If the support circuits are to be placed remotely and if the second stage may be an appreciable distance from the sensor, it becomes much more desirable to transmit the data in the digital domain, because it may be rendered nearly immune to interference noise and signal degradation. There may be a strong desire to minimize the number of conductors since that reduces the number of pads on the sensor (which consume space), in addition to increasing the complexity and cost of camera manufacture. Although the addition of analog to digital conversion to the sensor may be necessitated, the additional area may be offset to a degree, of not having to compensate for the signal degradation associated with buffering and transmitting an analog signal. In terms of area consumption, given the typical feature size available in CIS technologies, it may be preferable to have all of the internal logic signals be generated on chip via a set of control registers and a simple command interface controlling the registers as seen in FIG. 9.

[0029] High definition imaging with reduced pixel counts in a highly controlled illumination environment may be accomplished by virtue of frame by frame pulsed color switching at the light source in conjunction with high frames capture rates and a specially designed monochromatic sensor. Since the pixels of a reduced area image sensor may be color agnostic, the effective spatial resolution may be appreciably higher than for their color (usually Bayer-pattern filtered) counterparts in conventional single-sensor cameras. They also may have higher quantum efficiency since far fewer incident photons are wasted. Moreover, Bayer based spatial color modulation requires that the MTF of the accompanying optics be lowered compared with the monochrome case, in order to blur out the color artifacts associated with the Bayer pattern. This has a detrimental impact on the actual spatial resolution that can be realized with color sensors.

[0030] This particular disclosure may be also concerned with a system solution for endoscopy applications in which the image sensor may be resident at the distal end of the endoscope. In striving for a minimal area sensor based system, there are other design aspects

that can be developed, as described herein, beyond the obvious reduction in pixel count. In particular, the area of the digital portion of the chip should be minimized, as should the number of connections to the chip (pads). This disclosure describes novel methods that accomplish those goals for the realization of such a system. This involves the design of a full-custom CMOS image sensor with several novel features.

[0031] Implementations of the disclosure may comprise or utilize a special purpose or general-purpose computer including computer hardware, such as, for example, one or more processors and system memory, as discussed in greater detail below. Implementations within the scope of the disclosure may also include physical and other computer-readable media for carrying or storing computer-executable instructions and/or data structures. Such computer-readable media can be any available media that can be accessed by a general purpose or special purpose computer system. Computer-readable media that store computer-executable instructions are computer storage media (devices). Computer-readable media that carry computer-executable instructions are transmission media. Thus, by way of example, and not limitation, implementations of the disclosure can comprise at least two distinctly different kinds of computer-readable media: computer storage media (devices) and transmission media.

[0032] Computer storage media (devices) includes RAM, ROM, EEPROM, CD-ROM, solid state drives ("SSDs") (e.g., based on RAM), Flash memory, phase-change memory ("PCM"), other types of memory, other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to store desired program code means in the form of computer-executable instructions or data structures and which can be accessed by a general purpose or special purpose computer.

[0033] A "network" may be defined as one or more data links that enable the transport of electronic data between computer systems and/or modules and/or other electronic devices. When information may be transferred or provided over a network or another communications connection (either hardwired, wireless, or a combination of hardwired or wireless) to a computer, the computer properly views the connection as a transmission medium. Transmissions media can include a network and/or data links which can be used to carry desired program code means in the form of computer-executable instructions or data structures and which can be accessed by a general purpose or special purpose computer. Combinations of the above should also be included within the scope of computer-readable media.

[0034] Further, upon reaching various computer system components, program code means in the form of computer-executable instructions or data structures that can be transferred

automatically from transmission media to computer storage media (devices) (or vice versa). For example, computer-executable instructions or data structures received over a network or data link can be buffered in RAM within a network interface module (e.g., a "NIC"), and then eventually transferred to computer system RAM and/or to less volatile computer storage media (devices) at a computer system. RAM can also include solid state drives (SSDs or PCIx based real time memory tiered Storage, such as FusionIO). Thus, it should be understood that computer storage media (devices) can be included in computer system components that also (or even primarily) utilize transmission media.

[0035] Computer-executable instructions comprise, for example, instructions and data which, when executed at a processor, cause a general purpose computer, special purpose computer, or special purpose processing device to perform a certain function or group of functions. The computer executable instructions may be, for example, binaries, intermediate format instructions such as assembly language, or even source code. Although the subject matter has been described in language specific to structural features and/or methodological acts, it may be to be understood that the subject matter defined in the appended claims may be not necessarily limited to the described features or acts described above. Rather, the described features and acts are disclosed as example forms of implementing the claims.

[0036] Those skilled in the art may appreciate that the disclosure may be practiced in network computing environments with many types of computer system configurations, including, personal computers, desktop computers, laptop computers, message processors, hand-held devices, hand pieces, camera control units, multi-processor systems, microprocessor-based or programmable consumer electronics, network PCs, minicomputers, mainframe computers, mobile telephones, PDAs, tablets, pagers, routers, switches, various storage devices, and the like. The disclosure may also be practiced in distributed system environments where local and remote computer systems, which are linked (either by hardwired data links, wireless data links, or by a combination of hardwired and wireless data links) through a network, both perform tasks. In a distributed system environment, program modules may be located in both local and remote memory storage devices.

[0037] Further, where appropriate, functions described herein can be performed in one or more of: hardware, software, firmware, digital components, or analog components. For example, one or more application specific integrated circuits (ASICs) and programmable gate arrays (PGA) can be programmed to carry out one or more of the systems and procedures described herein. Certain terms are used throughout the following description and Claims to

refer to particular system components. As one skilled in the art may appreciate, components may be referred to by different names. This document does not intend to distinguish between components that differ in name, but not function.

[0038] Image sensors may incorporate special purpose, optically blind or optical black (OB) rows (at the top and/or bottom of the array) and columns (to the right and/or left of the array), for the purpose of offset calibration. An example layout of an image sensor 101 having pixels 105 in a record area along with top and bottom OB rows 109, and left and right OB columns 107 may be shown in FIG. 1A. The OB rows 109 are usually used to monitor the analog pixel black level, for the OB clamp algorithm. OB rows 109 are also typically used by a digital algorithm for the purpose of cancelling column fixed pattern noise or FPN (CFPN). In an embodiment, a guard ring 111 may surround the circumference of the image sensor 101. OB columns 107 on the other hand, usually have the purpose of assessing the line offset as a means to cancel out any line-noise. Since line-noise may be temporal, the offset should be computed anew for each line in every frame.

[0039] An overall reduction in the size of the pixel array can be achieved by removing the OB rows 109 and using the OB columns 107 instead of OB rows 109 for the OB clamp algorithm (see discussion below). In an implementation, all FPN types, including CFPN, may be cancelled by acquiring frames of dark data, thereby negating the need for a dedicated CFPN correction and its associated OB rows 109. FIG. 1B shows an example of just such an image sensor 101 and a pixel array 105 in which there are no OB rows present, but instead comprise OB columns 107.

[0040] FIG. 1C may be a block diagram illustrating an example computing device 100. Computing device 100 may be used to perform various procedures, such as those discussed herein. Computing device 100 can function as a server, a client, or any other computing entity. Computing device can perform various monitoring functions as discussed herein, and can execute one or more application programs, such as the application programs described herein. Computing device 100 can be any of a wide variety of computing devices, such as a desktop computer, a notebook computer, a server computer, a handheld computer, tablet computer and the like.

[0041] Computing device 100 includes one or more processor(s) 102, one or more memory device(s) 104, one or more interface(s) 106, one or more mass storage device(s) 108, one or more Input/Output (I/O) device(s) 110, and a display device 130 all of which are coupled to a bus 112. Processor(s) 102 include one or more processors or controllers that execute

instructions stored in memory device(s) 104 and/or mass storage device(s) 108. Processor(s) 102 may also include various types of computer-readable media, such as cache memory.

[0042] Memory device(s) 104 include various computer-readable media, such as volatile memory (e.g., random access memory (RAM) 114) and/or nonvolatile memory (e.g., read-only memory (ROM) 116). Memory device(s) 104 may also include rewritable ROM, such as Flash memory.

[0043] Mass storage device(s) 108 include various computer readable media, such as magnetic tapes, magnetic disks, optical disks, solid-state memory (e.g., Flash memory), and so forth. As shown in FIG. 1C, a particular mass storage device may be a hard disk drive 124. Various drives may also be included in mass storage device(s) 108 to enable reading from and/or writing to the various computer readable media. Mass storage device(s) 108 include removable media 126 and/or non-removable media.

[0044] I/O device(s) 110 include various devices that allow data and/or other information to be input to or retrieved from computing device 100. Example I/O device(s) 110 include cursor control devices, keyboards, keypads, microphones, monitors or other display devices, speakers, printers, network interface cards, modems, lenses, CCDs or other image capture devices, and the like.

[0045] Display device 130 includes any type of device capable of displaying information to one or more users of computing device 100. Examples of display device 130 include a monitor, display terminal, video projection device, and the like.

[0046] A pixel array 135 may also be included and may operate remotely relative to other circuits within the system.

[0047] Interface(s) 106 include various interfaces that allow computing device 100 to interact with other systems, devices, or computing environments. Example interface(s) 106 may include any number of different network interfaces 120, such as interfaces to local area networks (LANs), wide area networks (WANs), wireless networks, and the Internet. Other interface(s) include user interface 118 and peripheral device interface 122. The interface(s) 106 may also include one or more user interface elements 118. The interface(s) 106 may also include one or more peripheral interfaces such as interfaces for printers, pointing devices (mice, track pad, etc.), keyboards, and the like.

[0048] Bus 112 allows processor(s) 102, memory device(s) 104, interface(s) 106, mass storage device(s) 108, and I/O device(s) 110 to communicate with one another, as well as other

devices or components coupled to bus 112. Bus 112 represents one or more of several types of bus structures, such as a system bus, PCI bus, IEEE 1394 bus, USB bus, and so forth.

[0049] For purposes of illustration, programs and other executable program components are shown herein as discrete blocks, although it may be understood that such programs and components may reside at various times in different storage components of computing device 100, and are executed by processor(s) 102. Alternatively, the systems and procedures described herein can be implemented in hardware, or a combination of hardware, software, and/or firmware. For example, one or more application specific integrated circuits (ASICs) can be programmed to carry out one or more of the systems and procedures described herein on the fly or before the initialization of the system.

[0050] The number of OB columns might typically be 100 or more, depending on space constraints etc. The more OBs that are available the greater the line-offset precision may be. Greater precision means lower line noise, post-correction. Normally, all of the available physical OBs would be read for each line as shown in FIG. 2. A further degree of array size reduction can be achieved if, instead of having the requisite number of physical OB pixels, (given a certain precision target), a smaller number of physical pixels are implemented are they re-sampled multiple times during the horizontal readout process. This approach is illustrated in FIG. 3.

[0051] Raw CMOS image sensor data present at the output of the digitizer may be far from ideal. It may often be the case that the optimal order with which to read out a horizontal row of pixels does not equate to the actual physical order within the array. Also, raw data usually reveals undesirable artifacts that reflect the nature of the readout architecture too, which become very evident in situations of low light and correspondingly high gain. These readout artifacts may typically include column FPN, arising from the variation in offset from column to column and temporal line-noise which can result from circuit resets associated with the horizontal readout process.

[0052] Another property of CMOS sensors may be that a certain degree of dark signal may be generated by the photodiode within the pixel. The amount of integrated signal arising from this current depends on both the exposure time and the temperature. Since this dark signal may be indistinguishable from photo-signal, changes in it translate to changes in signal pedestal in the analog domain. In order that the available dynamic range of the ADC be fully exploited, it may be important that the dark signal be sampled and adjusted for. FIG. 4 illustrates how this may be usually done in CMOS sensors. Data from the OB pixels may be

averaged in the on-chip logic and compared to a target digital black level. Continuous adjustments are made to an input offset voltage in order to make the black level as close to the target as possible. This may be referred to as the black clamp or OB clamp process.

[0053] The majority of commercially available sensors incorporate the logic on-chip to perform the black-clamp and the digital noise corrections. This logic does not have to be resident on sensor, however and in an effort to develop a camera system with a minimal area sensor, it makes sense to migrate these corrections to the image signal processing chain (ISP). This actually has a net advantage as regards overall system performance, since the corrections are less resource limited if they are resident in an FPGA or ASIC with lots of available logic gates and RAM.

[0054] FIG. 5 shows how the OB clamp logic may be moved off of the sensor (along with the sensor correction algorithms). In this case, information about the analog adjustments from the OB clamp logic may be transmitted to the sensor by means of instructions, via its command interface.

[0055] FIG. 6 shows an example implementation of the front-end of an ISP which has been developed in the context of a system incorporating a minimal area sensor. In this example there are two digitizers on the sensor, converting the even and odd-numbered columns respectively and transmitting serial data on two differential ports.

[0056] Following de-serialization, the first process may be concerned with reconstructing the line for each port into the appropriate order. The next two correction blocks, dealing with the black clamp and the line noise correction, are both data-path specific, i.e. the two chains would be treated separately.

[0057] Black Clamp - The flowchart in FIG. 7 may be an example of how the OB clamp logic might typically operate within a conventional CMOS imaging system on chip. There might typically be multiple samples and analog adjustments made per frame, from multiple OB rows, while the OB-row pixels are present in the digital readout path. As discussed earlier, for a minimal area sensor, the number of OB pixels should be reduced to the minimum necessary and this can be accomplished by eliminating the OB rows and using the OB columns to calibrate the black clamp as well as the line-noise. The flowchart in FIG. 8A and 8B outline a method of accomplishing this. The basic idea may be to accumulate the set of measured, uncorrected line offsets for the whole frame and use the final estimate to make the black clamp adjustment. Meanwhile each individual line offset estimate may be fed to a later process in order to make a digital adjustment to the individual line.

[0058] The adjustment of the black clamp level may be done by means of controlling a DC voltage ($V_{blackclamp}$) using a DAC or charge pump on the sensor. Pixel voltage offsets entering the ADC move around due to dark current in the photodiode e.g., therefore the DAC needs to be regularly adjusted by assessing the black offset in the digital domain.

[0059] Individual OB pixels which do not behave normally may badly degrade the quality of the black offset measurements; therefore it may be very important to deal with them. A good approach may be to take for each OB pixel, the median of a group of 5 including the pixel in question and its four nearest neighbors. The final line offset estimate would then be taken as the mean of all the medians. Some provision should be made not to lose statistics at the beginning and the end, such as buffering the whole sample of OBs and wrapping around the sample of 5. This necessitates pipelining the data, resulting in a delay equal to at least the total number of OBs per ADC channel, per row.

[0060] Line offset estimate for even channel (assuming two ADCs with odd-even interspersion), row# *r*:

$$L_{r,\text{even}} = \frac{2 \cdot \sum_{i=0,2,4\ldots}^{N_{OB}-2} \mu_i}{N_{OB}}$$

[0061] Line offset Where N_{OB} may be the total number of OB pixels per row and μ_i may be the median for OB pixel *i*, computed thus:

$$\mu_0 = \text{median}\left[x_{(N_{OB}-4)}, x_{(N_{OB}-2)}, x_0, x_2, x_4\right]$$
$$\mu_2 = \text{median}\left[x_{(N_{OB}-2)}, x_0, x_2, x_4, x_6\right]$$
$$\mu_4 = \text{median}\left[x_0, x_2, x_4, x_6, x_8\right]$$
$$\ldots$$
$$\mu_{(N_{OB}-2)} = \text{median}\left[x_{(N_{OB}-6)}, x_{(N_{OB}-4)}, x_{(N_{OB}-2)}, x_0, x_2\right]$$

[0062] Likewise, line offset estimate for odd channel (assuming two ADCs with odd-even interspersion), row# *r*:

$$L_{r,\text{odd}} = \frac{2 \cdot \sum_{i=1,3,5\ldots}^{N_{OB}-1} \mu_i}{N_{OB}}$$

where

$$\mu_1 = \text{median}\ \left[x_{(N_{OB}-3)}, x_{(N_{OB}-1)}, x_1, x_3, x_5\right]$$
$$\mu_3 = \text{median}\ \left[x_{(N_{OB}-1)}, x_1, x_3, x_5, x_7\right]$$
$$\mu_5 = \text{median}\ \left[x_1, x_3, x_5, x_7, x_9\right]$$
$$\ldots$$
$$\mu_{(N_{OB}-1)} = \text{median}\ \left[x_{(N_{OB}-5)}, x_{(N_{OB}-3)}, x_{(N_{OB}-1)}, x_1, x_3\right]$$

[0063] To get the overall frame black level, a good practical approach may be afforded by accumulating all of the line offsets to compute the overall black level using simple exponential smoothing (SES). The benefit of using SES may be that the rows towards the end of the frame may have a greater influence on the final black estimate which may be desirable for addressing changes in black offset occurring on sub-frame timescales.

[0064] In SES, a running estimate may be incrementally adjusted each time a sample may be made available. For convenience the sample can be divided by a binary number (2^q) before being added to the previous estimate. The previous estimate may be first multiplied by (2^q-1)/2^q each time, in order to normalize the result. High values of q result in greater statistical precision over time in a stable scenario. Lower values of q may make the correction more reactive to rapid changes. q should be made available as a tunable parameter.

$$k_r = L_r \quad (r = 0)$$
$$k_r = \frac{1}{2^q} L_r + \frac{\left(2^q - 1\right)}{2^q} k_{(r-1)} \quad (r > 0)$$

where k_r may be the black level estimate after row r and L_r may be the line offset estimate for row r. The decision about what to do with the black clamp DACs may be made after the final row in the array has been added.

[0065] The black clamp algorithm would require a target black level which could be provided by an adjustable parameter. The black clamp DAC on the sensor for the channel in question would be pushed up or down, depending on whether the observed black estimate may be above or below the target. The size of the push could be e.g. the smallest unit, i.e. one DAC count, provided the black offset may be close to the target. In the case that the black level may be a long way from the target, a larger proportional push could be made, see FIG. 8A. The algorithm would need to know a rough calibration of the correspondence between black clamp DAC counts and sensor ADC counts and the directionality of DAC adjustments with respect to the output black level.

[0066] Line-Noise Correction - 'Line-Noise' refers to stochastic, temporal variations in the offset of a horizontal row of pixels. There may be multiple sources, but it can be considered as reset-noise arising from analog elements being reset each time a row of pixels may be read out. It may be temporal and a new correction should be computed for each new line per every frame. Since the amplification stage at the ADC input may be the final analog element, there may be good reason to suspect that the line-noise may appear phenomenologically independent per ADC channel. Therefore the optimal approach may be to correct each ADC (channel) separately.

[0067] To eliminate line-noise completely may be impossible, since the sample of OB pixels used for the line offset estimate, may be separate from the sample to which the correction may be being applied (and the sample statistics are finite). Assuming all the noise may be Gaussian, the post-correction line-noise may be approximately equal to the uncertainty in the line offset estimate arising from the pixel temporal noise present in the OB pixels:

$$\sigma_{L,\text{post}} \approx \frac{\sigma_P}{\sqrt{N_{\text{OB}}}}$$

where $\sigma_{L,\text{post}}$ may be the post correction temporal line-noise, $\sigma_{P\ may\ be}$ the OB pixel temporal noise and $N_{\text{OB may be}}$ the number of OB pixels. The line-noise correction also introduces a spatial line-noise component, mostly as a consequence of the pixel FPN present within the OB pixels:

$$\text{FPN}_{L,\text{post}} \approx \frac{\text{FPN}_P}{\sqrt{N_{\text{OB}}}}$$

This artifact would be eliminated by the FPN correction, later in the chain. Simulations have indicated that in order for temporal line-noise to be invisible, the magnitude should be less than approximately 1/10 of the pixel temporal noise. This criterion indicates at least 100 OB pixels would be required per line.

[0068] Line-noise correction application to optically sighted (clear) pixels:

$$x'_i = x_i - L + B$$

Where L may be the line offset estimate for the current line, ported from the 'Black Clamp' module and B may be the black clamp target level.

[0069] Full Line Recombination - This would involve simply combining the two data channels into a full line. They need to be interleaved in such a way that the final clear pixel order reflects the correct order in the array.

[0070] FPN Correction - CMOS image sensors have multiple noise sources, the magnitude and appearance of which depend on a range of physical conditions. Pure Poisson or Gaussian temporal noise with no coherent components (e.g. photon shot noise or source follower 1/f read noise) looks as natural as noise can look. All other perceivable noise types may degrade the image quality to a much greater extent for the same amplitude. Spatial noise (FPN) may be especially egregious and CMOS sensors inherently have at least two sources; pixel FPN and column FPN. The pixel FPN may be mostly due to variations in photodiode leakage current (dark signal) from pixel to pixel (DSNU). This source may be exponentially dependent on junction temperature (T_J) and linearly dependent on exposure time. Column FPN may be a consequence of the readout architecture, in which pixels from within the same column are channeled through common analog readout elements.

[0071] Typically an on-chip digital FPN correction would involve dealing only with the column FPN component, requiring one offset correction register per column. The precision of such a correction might typically be 20 bits or so per column, which translates to around 5kB of RAM for a 1920X1080 array. One of the benefits of migrating the digital sensor corrections to the ISP may be the ready availability of RAM. This opens up the possibility of a comprehensive FPN correction which cancels out any row, column or pixel-wise component. This may be accomplished by means of simple exponential smoothing (SES) in which each fresh dark frame sample may be used to adjust a running offset estimate on a per physical pixel basis.

[0072] Programmable Digital Gain - The final block in FIG. 6 corresponds to a programmable digital amplifier. CMOS iSoCs are usually equipped with digital programmable gain stages with very fine increments. This may be to facilitate auto-exposure processes which typically modulate the gain and the exposure time.

[0073] The digital amplifier can be used to align the range of the sensor ADC to the range of the ISP (e.g. ×2 for 11 bit ADC to 12-bit ISP). A small amount of digital gain may also be used to trim off the imprint of the digital line-noise and FPN corrections which becomes apparent at the full range of the ADC.

[0074] Minimization of configuration register address ROM- Conventional CMOS image sensors incorporate many writeable registers for the purpose of controlling how the sensor operates. They would typically incorporate DAC settings to adjust bias voltages and currents, timing parameters for, e.g., the pixel acquisition and readout cycle, amplifier offsets and gains

etc. The usual convention may be to assign a particular 8-bit or 16-bit address to each register which contains typically 8 or 16 bits of data.

[0075] A more space conservative approach involves combining large amounts of control RAM into single, long registers. In the extreme case, all parameters could be placed into a single register, requiring no address ROM. This solution may be not very practical however since writing control registers takes time and typical video applications involve changing a small number of operational parameters (such as exposure time) on a frame-by-frame basis. The most practical solution may be afforded by concatenating functionally related sets of parameters into a small number of long registers. The difference in space implied by having say, ten registers (requiring 4 address bits) versus one, may be negligible. In particular it makes sense that all of the parameters which are written periodically at a high rate (e.g. every frame) belong together in an exclusive register (the frame register), in order to keep the time required to write it to a minimum. Such parameters include the exposure times, gains, incremental offset adjustments and any others necessary to maintain continuous high quality video. If the digital data-path logic has been migrated off chip as described earlier, the black clamp voltage adjustment data also belongs in such a register since it should be revised every frame too. In an implementation, during this configuration phase can registers be written and therefore the timing of the frame register writes with respect to the overall frame timing should be carefully controlled by the camera.

[0076] Other examples of parametric register groupings could include; analog currents, analog voltages, pixel timing, vertical timing, sensor commands (resets etc.) and so on.
In FIG. 9 the arrangement of registers may be shown for a specific minimal-area sensor design. The "Command" register may be used for top level event-oriented 1-bit commands such as chip resets and the loads for the other registers shown below it. A 2-wire protocol address decoder decides which shift register to direct incoming 2-wire protocol data toward. To load the "Format" register, e.g., the external controller sends a command with the address associated with the Format register. This places the stream of data into the Format-register shift register. Then in order to latch the data, a follow up command may be sent to the Command register with the particular "load Format" bit set. It will be appreciated that a plurality of control registers may be used. The control registers may be digital latches that may be loaded via shift registers. The shift registers may be arbitrary in length. In an embodiment, a majority of the plurality of control registers may be loaded using shift registers that include many tens of bits. In an embodiment, a majority of the plurality of control

registers may be loaded using shift registers that include hundreds of bits. In an embodiment, a majority of the plurality of control registers may be loaded using shift registers that include thousands of bits. In an embodiment, the shift registers may be loaded using a serial, 2-wire protocol. In an embodiment, one of the shift registers may be dedicated to frame-to-frame parameter changes, such as, e.g., integration times and black clamp offset adjustments.

[0077] FIG. 10 shows an overall block diagram for an embodiment of a minimal-area sensor for endoscope applications in which the sensor may be incorporated into the distal end of the endoscope unit.

[0078] FIGS. 11A and 11B illustrate a perspective view and a side view, respectively, of an implementation of a monolithic sensor 2900 having a plurality of pixel arrays for producing a three dimensional image in accordance with the teachings and principles of the disclosure. Such an implementation may be desirable for three dimensional image capture, wherein the two pixel arrays 2902 and 2904 may be offset during use. In another implementation, a first pixel array 2902 and a second pixel array 2904 may be dedicated to receiving a predetermined range of wave lengths of electromagnetic radiation, wherein the first pixel array is dedicated to a different range of wave length electromagnetic radiation than the second pixel array.

[0079] FIGS. 12A and 12B illustrate a perspective view and a side view, respectively, of an implementation of an imaging sensor 3000 built on a plurality of substrates. As illustrated, a plurality of pixel columns 3004 forming the pixel array are located on the first substrate 3002 and a plurality of circuit columns 3008 are located on a second substrate 3006. Also illustrated in the figure are the electrical connection and communication between one column of pixels to its associated or corresponding column of circuitry. In one implementation, an image sensor, which might otherwise be manufactured with its pixel array and supporting circuitry on a single, monolithic substrate/chip, may have the pixel array separated from all or a majority of the supporting circuitry. The disclosure may use at least two substrates/chips, which will be stacked together using three-dimensional stacking technology. The first 3002 of the two substrates/chips may be processed using an image CMOS process. The first substrate/chip 3002 may be comprised either of a pixel array exclusively or a pixel array surrounded by limited circuitry. The second or subsequent substrate/chip 3006 may be processed using any process, and does not have to be from an image CMOS process. The second substrate/chip 3006 may be, but is not limited to, a highly dense digital process in order to integrate a variety and number of functions in a very limited space or area on the substrate/chip, or a mixed-mode or analog process in order to integrate for example precise

analog functions, or a RF process in order to implement wireless capability, or MEMS (Micro-Electro-Mechanical Systems) in order to integrate MEMS devices. The image CMOS substrate/chip 3002 may be stacked with the second or subsequent substrate/chip 3006 using any three-dimensional technique. The second substrate/chip 3006 may support most, or a majority, of the circuitry that would have otherwise been implemented in the first image CMOS chip 3002 (if implemented on a monolithic substrate/chip) as peripheral circuits and therefore have increased the overall system area while keeping the pixel array size constant and optimized to the fullest extent possible. The electrical connection between the two substrates/chips may be done through interconnects 3003 and 3005, which may be wirebonds, bump and/or TSV (Through Silicon Via).

[0080] FIGS. 13A and 13B illustrate a perspective view and a side view, respectively, of an implementation of an imaging sensor 3100 having a plurality of pixel arrays for producing a three dimensional image. The three dimensional image sensor may be built on a plurality of substrates and may comprise the plurality of pixel arrays and other associated circuitry, wherein a plurality of pixel columns 3104a forming the first pixel array and a plurality of pixel columns 3104b forming a second pixel array are located on respective substrates 3102a and 3102b, respectively, and a plurality of circuit columns 3108a and 3108b are located on a separate substrate 3106. Also illustrated are the electrical connections and communications between columns of pixels to associated or corresponding column of circuitry.

[0081] It will be appreciated that the teachings and principles of the disclosure may be used in a reusable device platform, a limited use device platform, a re-posable use device platform, or a single-use/disposable device platform without departing from the scope of the disclosure. It will be appreciated that in a re-usable device platform an end-user is responsible for cleaning and sterilization of the device. In a limited use device platform the device can be used for some specified amount of times before becoming inoperable. Typical new device is delivered sterile with additional uses requiring the end-user to clean and sterilize before additional uses. In a re-posable use device platform a third-party may reprocess the device (e.g., cleans, packages and sterilizes) a single-use device for additional uses at a lower cost than a new unit. In a single-use/disposable device platform a device is provided sterile to the operating room and used only once before being disposed of.

[0082] An embodiment of an endoscope for use in a closed light environment may comprise: an endoscope body providing a hand holding structure, a lumen attached by a lumen base at a first end of the body, a tip portion of the lumen opposite of the lumen base of the, a

lens that may be disposed at the most distal portion of the tip portion, an imaging sensor that may be disposed near the tip portion of the lumen comprising: an array of pixels for sensing electromagnetic radiation; wherein the pixel array may have active pixels and optical black pixels for calibrating output from said pixel array; wherein the optical black pixels may be organized in columns adjacent to active pixels within the pixel array; a transfer port for transmitting data generated by the pixel array; a digitizer to convert analog pixel samples to digital numbers; a black clamp circuit for providing offset control for the data generated by the pixel array; a process that may be stored in memory for controlling the black clamp circuit; electrical connections that may be providing electrical communication between the imaging sensor and image signal processing circuitry that may be disposed remote to the imaging sensor within the endoscope body and a control unit.

[0083] An embodiment of a system for digital imaging in an ambient light deficient environment may comprise: an imaging sensor for sensing electromagnetic radiation; wherein said imaging sensor may further comprise: a pixel array having active pixels and optical black pixels for calibrating output from said pixel array; wherein the optical black pixels may be organized in columns adjacent to active pixels within the pixel array; a transfer port for transmitting data generated by the pixel array; a digitizer to convert analog pixel samples to digital numbers; a black clamp circuit for providing offset control for the data generated by the pixel array; a process that may be stored in memory of the system for controlling the black clamp circuit; an endoscope for accessing the ambient light deficient environment; a hand piece attached to said endoscope and wherein said endoscope may be maneuvered by manipulation of the hand piece; a control unit comprising a processor and wherein said control unit may be in electrical communication with the imaging sensor; and a connection cable electrically connecting the hand piece and the control unit.

[0084] Additionally, the teachings and principles of the disclosure may include any and all wavelengths of electromagnetic energy, including the visible and non-visible spectrums, such as infrared (IR), ultraviolet (UV), and X-ray.

[0085] The foregoing description has been presented for the purposes of illustration and description. It may be not intended to be exhaustive or to limit the disclosure to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. Further, it should be noted that any or all of the aforementioned alternate implementations may be used in any combination desired to form additional hybrid implementations of the disclosure.

[0086] Further, although specific implementations of the disclosure have been described and illustrated, the disclosure may be not to be limited to the specific forms or arrangements of parts so described and illustrated. The scope of the disclosure may be to be defined by the claims appended hereto, any future claims submitted here and in different applications, and their equivalents.

CLAIMS

What is claimed is:

1. An endoscopic device for use in a closed light environment comprising:

an endoscope body comprising:

a hand holding structure;

a lumen attached by a lumen base at a first end of the body;

a tip portion of the lumen opposite of the lumen base of the body;

a lens disposed at the distal most portion of the tip portion;

an imaging sensor disposed near the tip portion of the lumen, wherein the imaging sensor comprises:

an array of pixels for sensing electromagnetic radiation;

a transfer port for transmitting data generated by the pixel array;

a digitizer to convert analog pixel data into digital data;

a black clamp circuit for providing offset control for the data generated by the pixel array;

electrical connections providing electrical communication between the imaging sensor and image signal processing circuitry disposed remotely from the imaging sensor.

2. The endoscopic device of claim 1, further comprising a long registry wherein the long registry comprises control parameter entries for controlling exposure times of the pixel array and gain of the pixel array.

3. The endoscopic device of claim 1, further comprising a long registry comprising control parameter entries for controlling incremental offset adjustment of the pixel array or exposure times of the pixel array.

4. The endoscopic device of claim 1, further comprising a long registry comprising control parameter entries for controlling incremental offset adjustment of the pixel array or gain of the pixel array.

5. The endoscopic device of claim 1, further comprising a long registry consisting of control parameter entries for controlling exposure times of the pixel array or gains of the pixel array and incremental offset adjustments.

6. The endoscopic device of claim 1, further comprising a long registry comprising control parameter entries for controlling incremental offset adjustment of the pixel array and exposure times of the pixel array.

7. The endoscopic device of claim 1, further comprising a long registry comprising a plurality of control parameter entries for controlling the operation of a pixel array by adjusting any of: analog current, analog voltage, pixel timing, vertical timing, sensor reset and sensor initialization.

8. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the active pixels and the optical black pixels calibrate output from said pixel array.

9. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the optical black pixels are organized in columns adjacent to the active pixels within the pixel array.

10. The endoscopic device of claim 1, wherein the imaging sensor comprises a single digitizer.

11. The endoscopic device of claim 1, wherein the imaging sensor comprises a plurality of digitizers.

12. The endoscopic device of claim 1, wherein the imaging sensor comprises a single output port.

13. The endoscopic device of claim 1, wherein the imaging sensor comprises a plurality of output ports.

14. The endoscopic device of claim 9, wherein the columns of optical black pixels are sampled a plurality of times to reduce the number of optical black columns.

15. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the optical black pixels are organized in columns adjacent to the active pixels within the pixel array, wherein the columns of optical black pixels are organized on a right side and a left side of the imaging sensor.

16. The endoscopic device of claim 15, wherein one of the optical black columns on the right side of the imaging sensor is sampled a plurality of times.

17. The endoscopic device of claim 15, wherein one of the optical black columns on the left side of the imaging sensor is sampled a plurality of times.

18. The endoscopic device of claim 15, wherein one of the optical black columns on the right side of the imaging sensor is sampled a plurality of times and one of the optical black columns on the left side of the imaging sensor is sampled a plurality of times.

19. The endoscopic device of claim 15, wherein a plurality of the optical black columns on the right side of the imaging sensor are sampled a plurality of times.

20. The endoscopic device of claim 15, wherein a plurality of the optical black columns on the left side of the imaging sensor are sampled a plurality of times.

21. The endoscopic device of claim 15, wherein a plurality of the optical black columns on the right side of the imaging sensor are sampled a plurality of times and a plurality of the optical black columns on the left side of the imaging sensor are sampled a plurality of times.

22. The endoscopic device of claim 1, wherein the black clamp circuit is located remotely with respect to the imaging sensor.

23. The endoscopic device of claim 22, wherein the device further comprises a command interface to control the black clamp circuit.

24. The endoscopic device of claim 1, wherein the black clamp circuitry senses a voltage generated by a digital to analog converter.

25. The endoscopic device of claim 1, wherein the black clamp circuitry senses a voltage generated by a charge pump.

26. The endoscopic device of claim 1, wherein a portion of the imaging sensor corrections are located remotely with respect to the imaging sensor.

27. The endoscopic device of claim 1, wherein all of the imaging sensor corrections are located remotely with respect to the imaging sensor.

28. The endoscopic device of claim 1, further comprising a plurality of control registers, wherein said control registers are digital latches that are loaded via shift registers.

29. The endoscopic device of claim 28, wherein said shift registers are arbitrary in length.

30. The endoscopic device of claim 28, wherein a majority of the plurality of control registers are loaded using shift registers that include many tens of bits.

31. The endoscopic device of claim 28, wherein a majority of the plurality of control registers are loaded using shift registers that include hundreds of bits.

32. The endoscopic device of claim 28, wherein a majority of the plurality of control registers are loaded using shift registers that include thousands of bits.

33. The endoscopic device of claim 28, wherein said shift registers are loaded using a serial, 2-wire protocol.

34. The endoscopic device of claim 28, wherein one of said shift registers is dedicated to frame-to-frame parameter changes.

35. The endoscopic device of claim 1, wherein the imaging sensor comprises a plurality of pixel arrays, wherein the plurality of pixel arrays are used to create a three-dimensional image.

36. The endoscopic device of claim 1, wherein the imaging sensor further comprises a first substrate comprising the pixel array and a second substrate comprising supporting circuitry for the pixel array, wherein the second substrate comprising the supporting circuitry is located remotely from the first substrate comprising the pixel array.

37. The endoscopic device of claim 36, wherein the first substrate is vertically aligned with respect to the second substrate.

38. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the optical black pixels are organized in columns adjacent to the active pixels within the pixel array, wherein the columns of optical black pixels are sampled a plurality of times to calculate line offsets.

39. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the optical black pixels are organized into a plurality of columns and a plurality of rows adjacent to the active pixels within the pixel array.

40. The endoscopic device of claim 39, wherein a majority of the optical black rows are removed from the pixel array, such that only a minority of the optical black rows are functional.

41. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the optical black pixels are organized into a plurality of columns and does not contain any optical black rows adjacent to the active pixels within the pixel array.

42. The endoscopic device of claim 1, wherein the pixel array comprises active pixels and optical black pixels, wherein the optical black pixels are organized into a plurality of columns adjacent to the active pixels within the pixel array, wherein the plurality of columns are used to calculate a baseline black level for the black clamp circuit and black clamp calculations performed by the image signal processor.

43. The endoscopic device of claim 42, wherein the black clamp calculations are used to control the voltage offset prior to the digitizer and use a plurality of line offsets to determine the overall offset within a whole frame of data using simple exponential smoothing (SES).

44. The endoscopic device of claim 1, wherein the device further comprises two-dimensional frame data stored in memory for compensating for fixed pattern noise generated by the image sensor.

45. The endoscopic device of claim 44, wherein the two-dimensional frame data is derived from dark frame capture.

46. The endoscopic device of claim 45, wherein the dark frame capture is facilitated by not pulsing an emitter.

47. The endoscopic device of claim 45, wherein the pixel offset is computed by simple exponential smoothing for the dark frame capture.

48. A system for digital imaging in an ambient light deficient environment comprising:

an imaging sensor for sensing electromagnetic radiation, wherein said imaging sensor comprises:

an array of pixels for sensing electromagnetic radiation;

a transfer port for transmitting data generated by the pixel array;

a digitizer to convert analog pixel samples to digital numbers;

a black clamp circuit for providing offset control for the data generated by the pixel array;

an endoscope for accessing the ambient light deficient environment;

a hand piece attached to said endoscope wherein said endoscope may be maneuvered by manipulation of the hand piece;

a control unit comprising a processor wherein said control unit may be in electrical communication with the imaging sensor; and

a connection cable electrically connecting the hand piece and the control unit.

49. The system of claim 48, wherein the pixel array comprises active pixels and optical black pixels for calibrating output from said pixel array.

50. The system of claim 49, wherein the optical black pixels are organized in columns adjacent to active pixels within the pixel array.

51. The system of claim 48, further comprising a black clamp control process that may be remotely located from the pixel array.

52. The system of claim 48, further comprising a programmable gate array for processing image data that may be created by the pixel array.

53. The system of claim 48, further comprising optical black pixel columns fewer in number than 50 such that they can be resampled within the operation of the system in order to provide precision.

54. The system of claim 49, further comprising optical black pixel columns disposed equally at opposing sides of the active pixel columns.

55. The system of claim 49, further comprising optical black pixel columns disposed unevenly on opposing sides of the active pixel columns.

56. The system of claim 49, further comprising a black clamp control process that averages the data received by optically black pixels and compares the averages to a predetermined target value stored within memory within the system.

57. The system of claim 48, further comprising memory for accumulating a set of measured uncorrected line offsets for an entire frame.

58. The system of claim 48, further comprising a digital to analog conversion circuit for controlling voltage to compensate for dark current.

59. The system of claim 48, further comprising a charge pump circuit for controlling a voltage to compensate for dark current.

60. The system of claim 48, further comprising a plurality of registers.

61. The system of claim 48, further comprising a command register used for top level event 1-bit commands such as chip resets and the loads for other registers.

62. The system of claim 48, further comprising an image sensor disposed within the endoscope at a distal portion thereof relative to the hand piece.

63. The system of claim 48, further comprising an image sensor disposed within the hand piece.

64. The system of claim 48, further comprising an emitter for emitting pulses of electromagnetic radiation transmitted through fiber optics from the emitter to a tip of the endoscope.

65. The system of claim 48, further comprising a cable comprising fiber optics for transmitting electromagnetic radiation from a light emitter the endoscope, and electrically conductive wires for providing electronic communication from the control unit to the image sensor.

66. The system of claim 48, further comprising a controller disposed within the control unit and in electrical communication with a light emitter and the imaging sensor.

67. The system of claim 48, further comprising an image sensor disposed within the hand piece and in electrical communication with a light emitter and the imaging sensor.

68. The system of claim 48, further comprising an image sensor that is coupled to an emitter.

69. The system of claim 48, further comprising a remotely processed algorithm to correct for line-noise by subtracting line averages measured using a set of optical black pixels in each line.

70. The system of claim 48, further comprising a plurality of transfer ports for transmitting pixel data.

71. The system of claim 48, further comprising a plurality of digitizers.

72. The system of claim 48, further comprising remotely located digitizers relative to the pixel array.

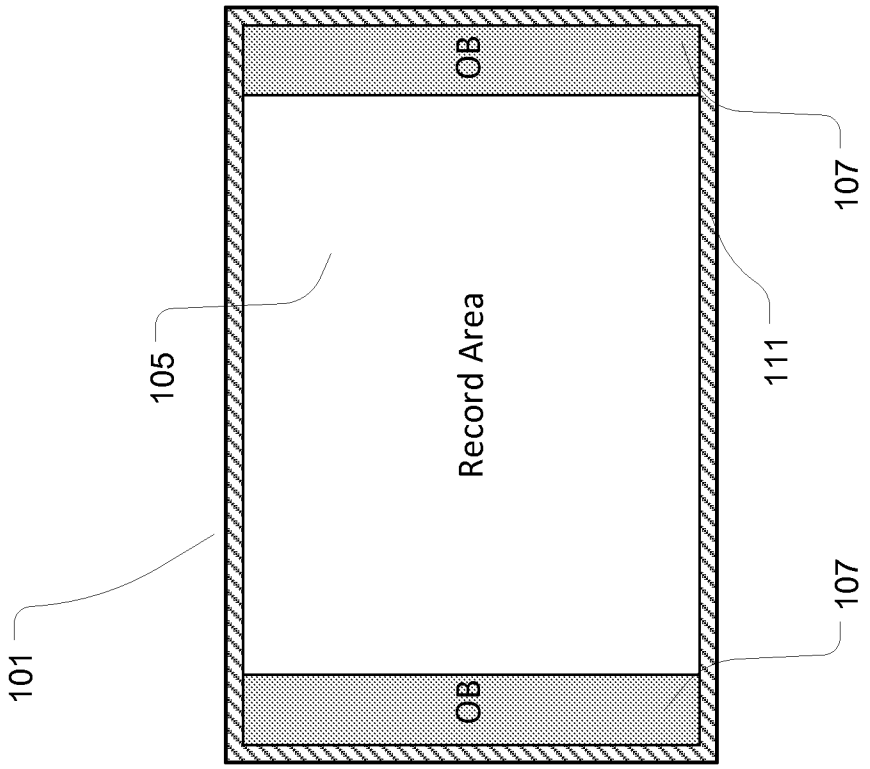
OB
Record Area
OB
101
105
107
111
107

FIG. 1B

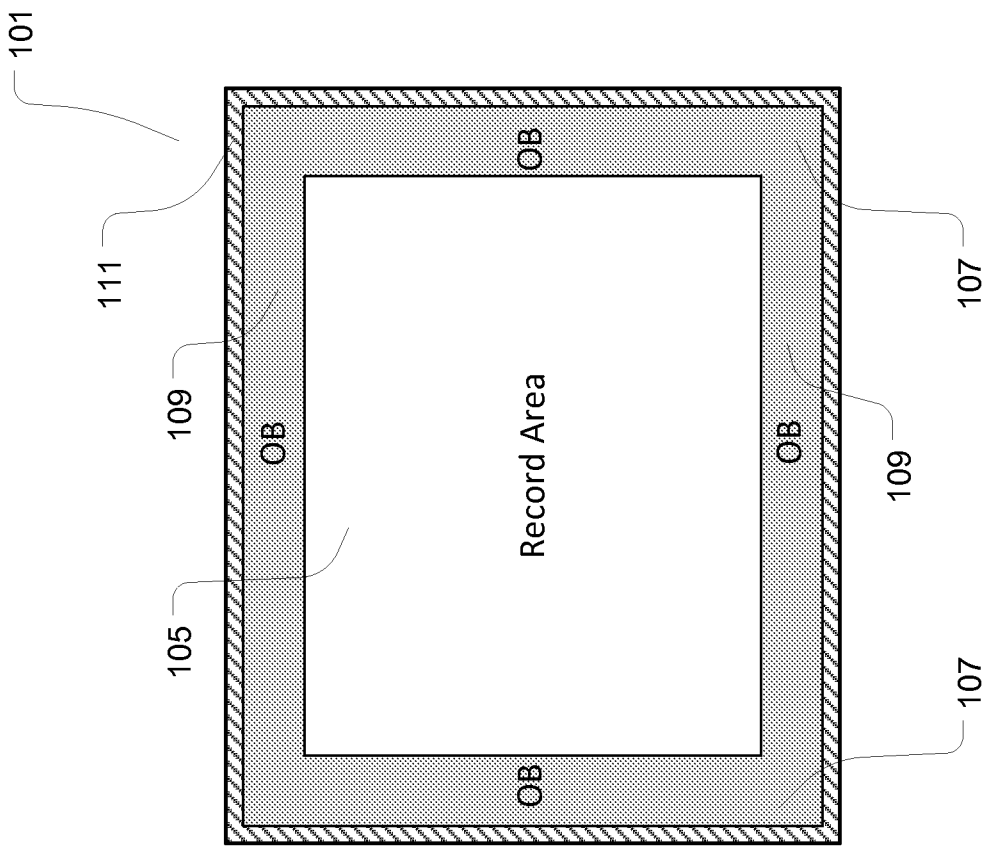
101
111
OB
107
109
OB
Record Area
OB
109
105
107
OB

FIG. 1A

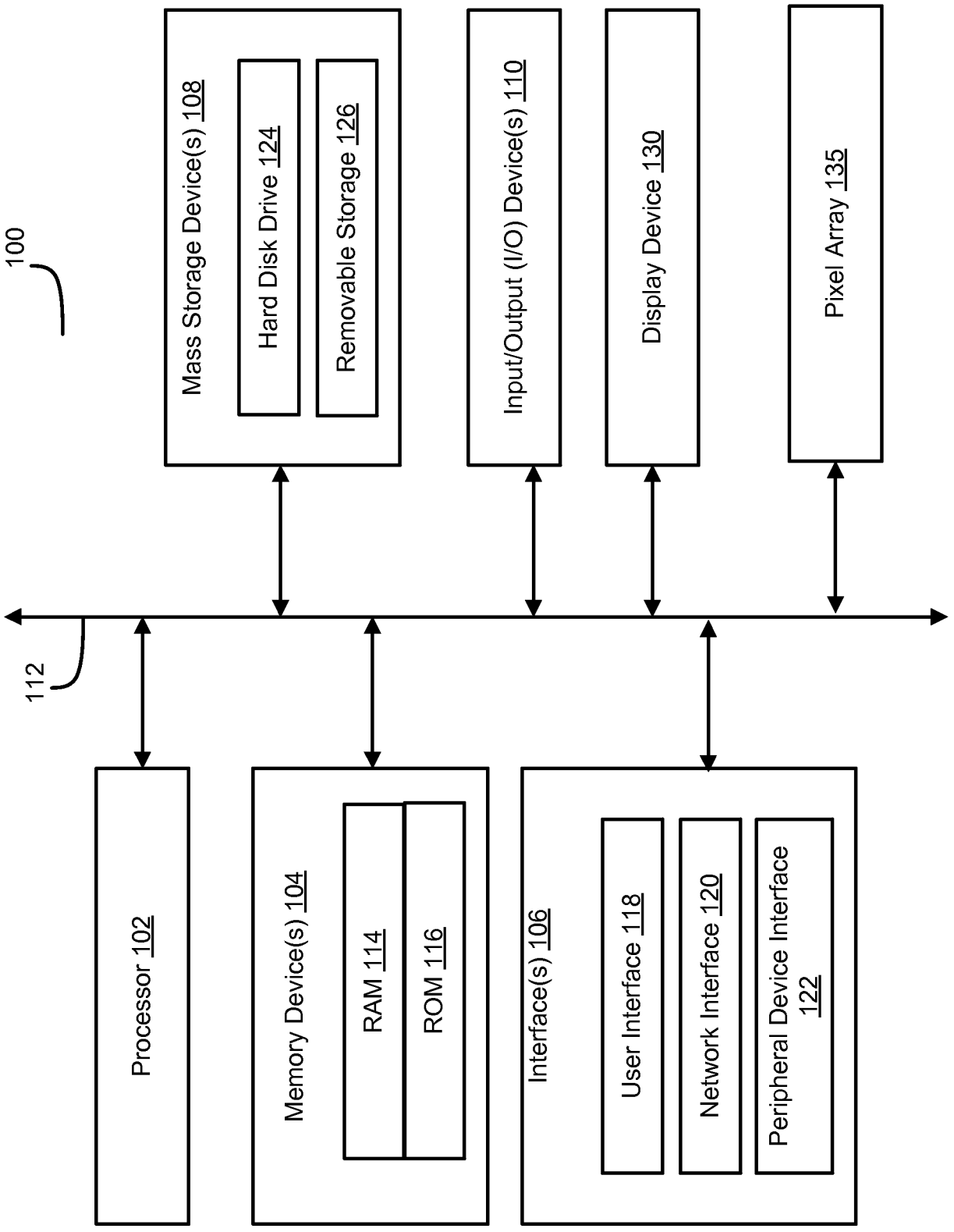
100
Mass Storage Device(s) 108
Hard Disk Drive 124
Removable Storage 126
Input/Output (I/O) Device(s) 110
Display Device 130
Pixel Array 135
112
Processor 102
Memory Device(s) 104
RAM 114
ROM 116
Interface(s) 106
User Interface 118
Network Interface 120
Peripheral Device Interface 122

FIG. 1C

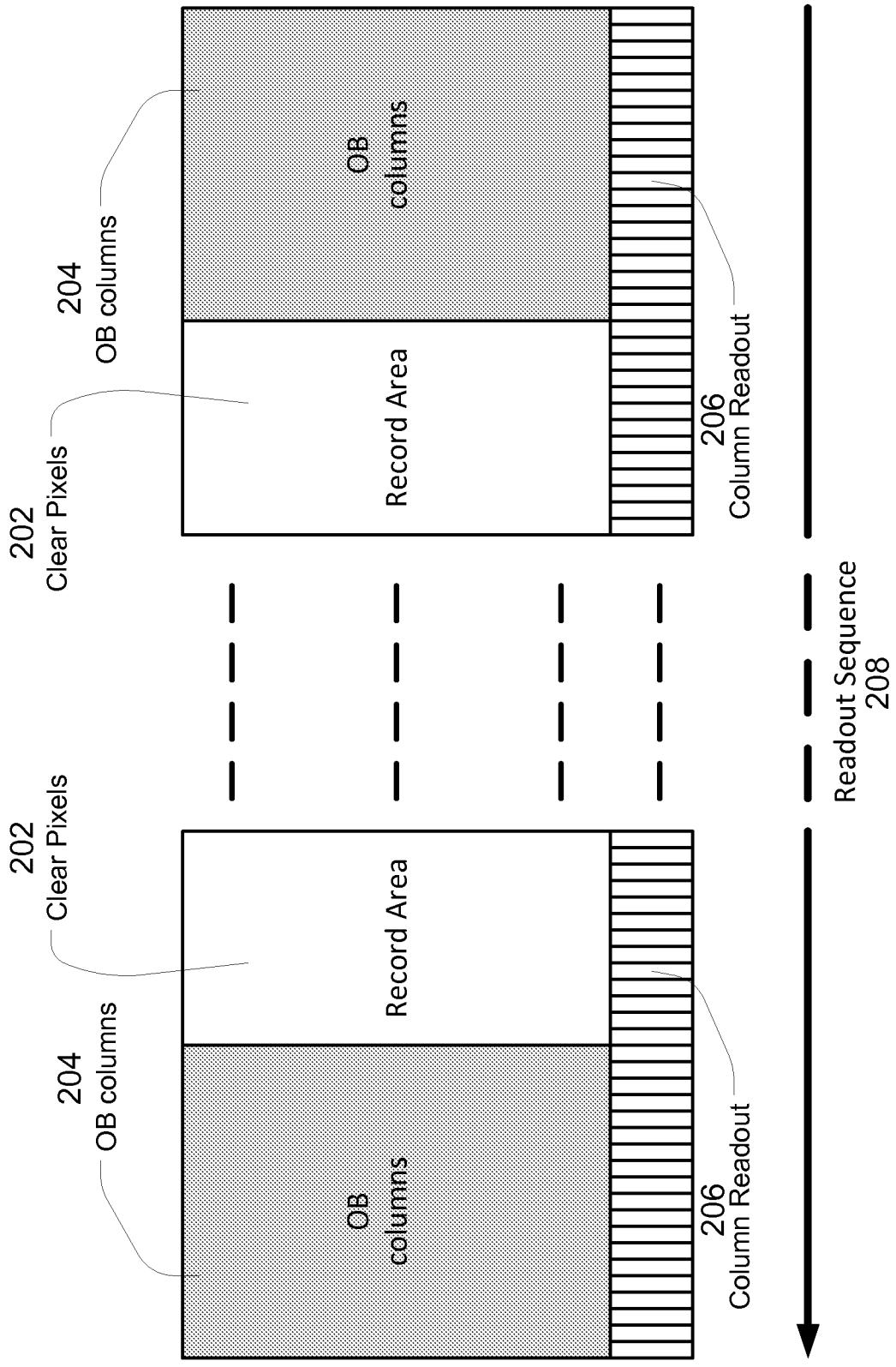
202
Clear Pixels
204
OB columns
Record Area
OB columns
206
Column Readout
Readout Sequence
208

FIG. 2

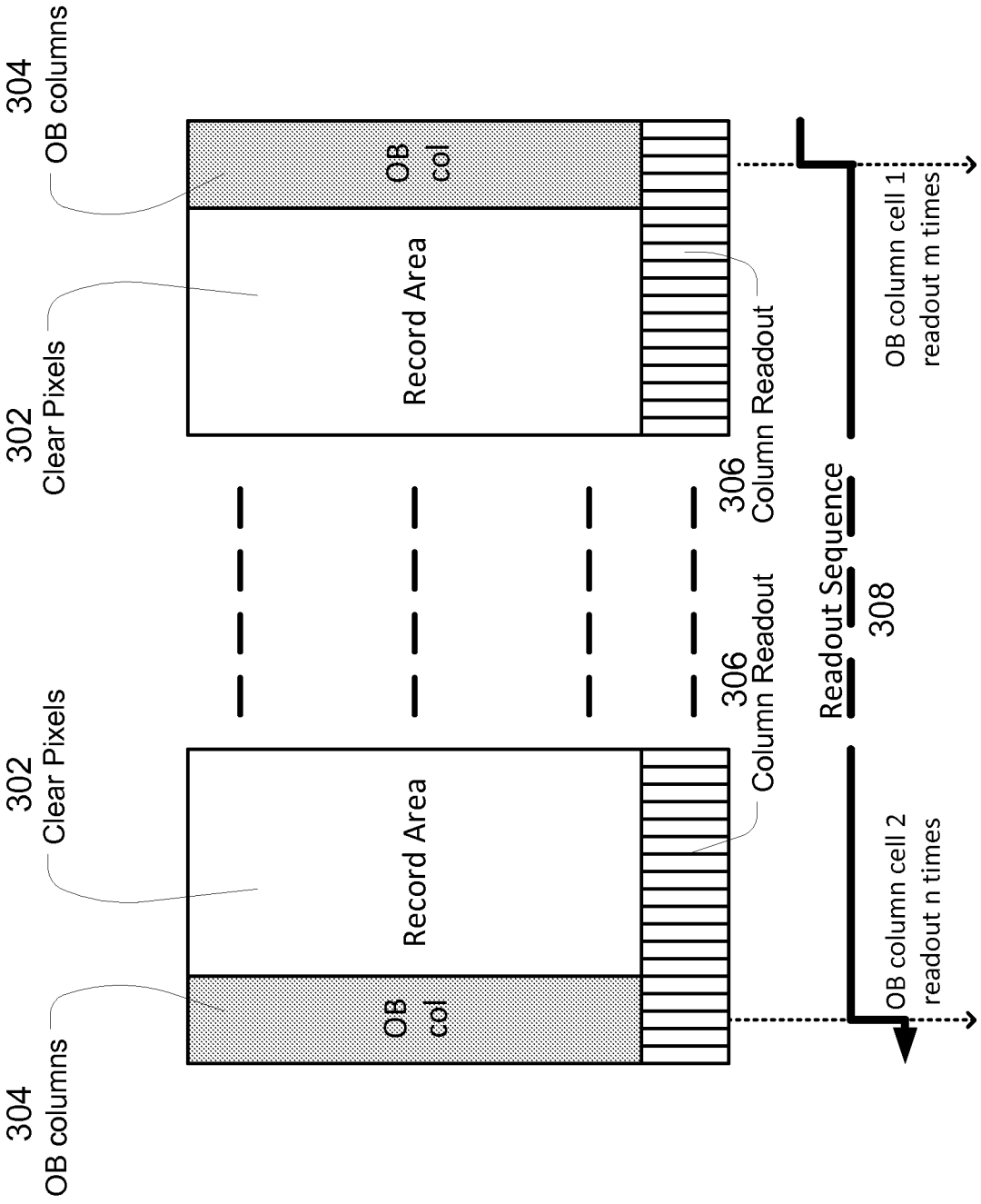
304
OB columns
302
Clear Pixels
OB col
Record Area
306
Column Readout
OB column cell 1
readout m times
Readout Sequence
308
OB column cell 2
readout n times

FIG. 3

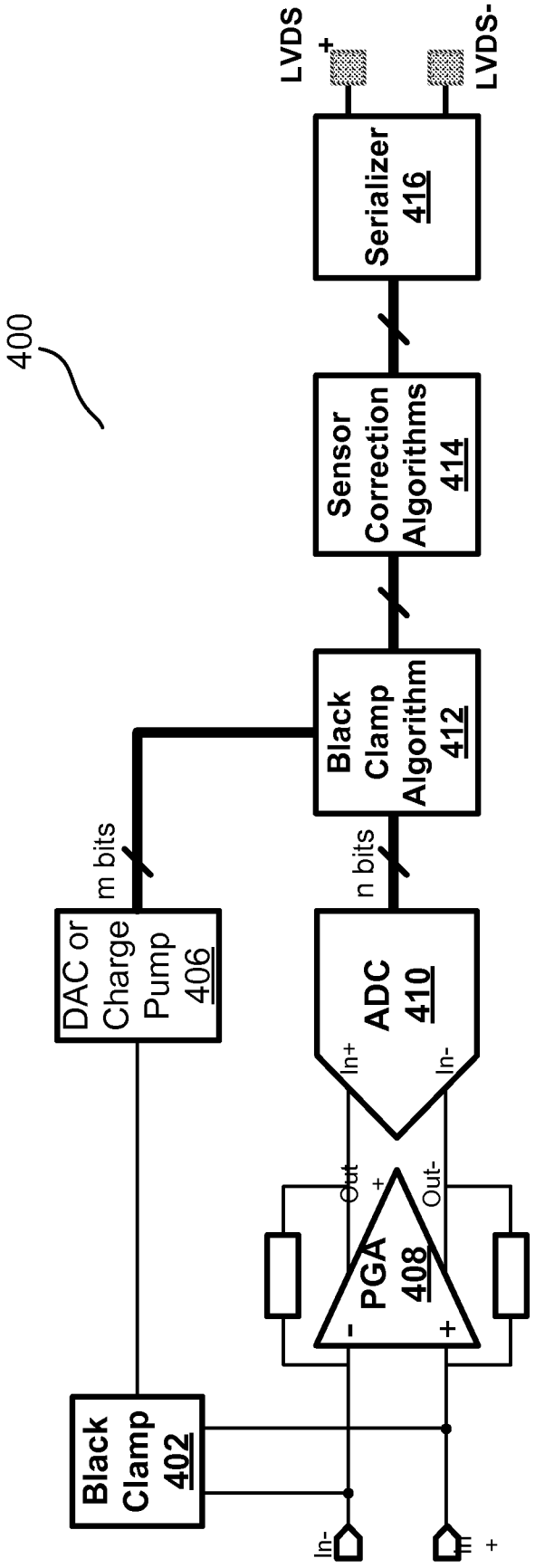
400
LVDS +
LVDS-
Serializer 416
Sensor Correction Algorithms 414
Black Clamp Algorithm 412
m bits
n bits
DAC or Charge Pump 406
ADC 410
In+
In-
Out+
Out-
PGA 408
Black Clamp 402
In-
+

FIG. 4

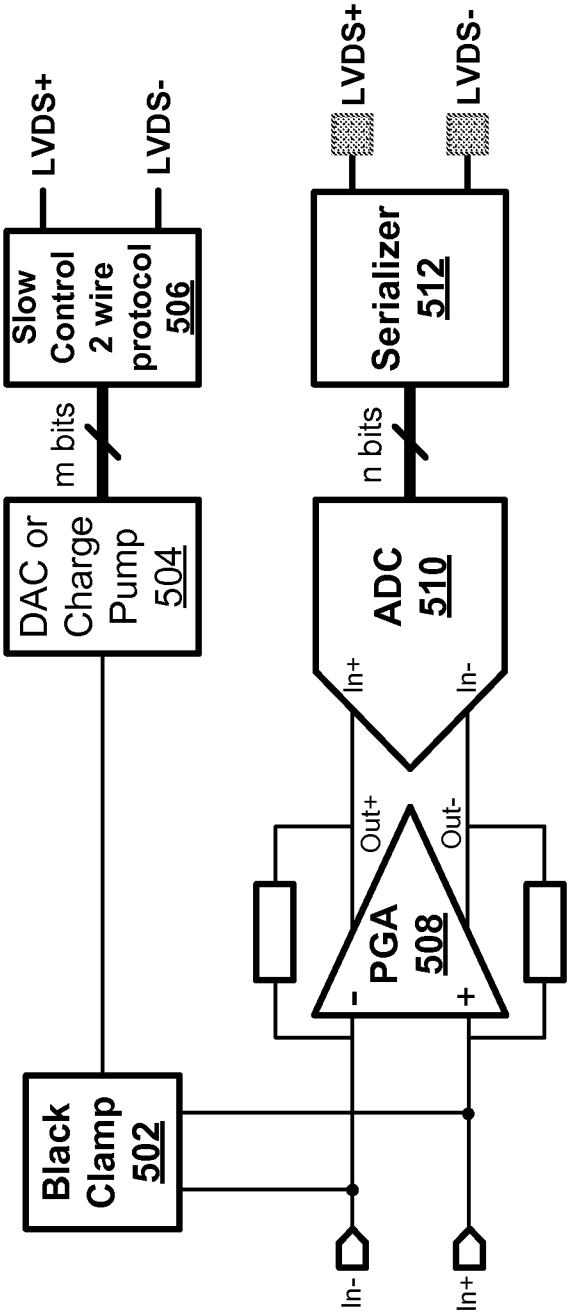
LVDS+
LVDS-
Slow Control 2 wire protocol 506
m bits
DAC or Charge Pump 504
Black Clamp 502
LVDS+
LVDS-
Serializer 512
n bits
ADC 510
In+
In-
Out+
Out-
PGA 508
-
+
In-
In+

FIG. 5

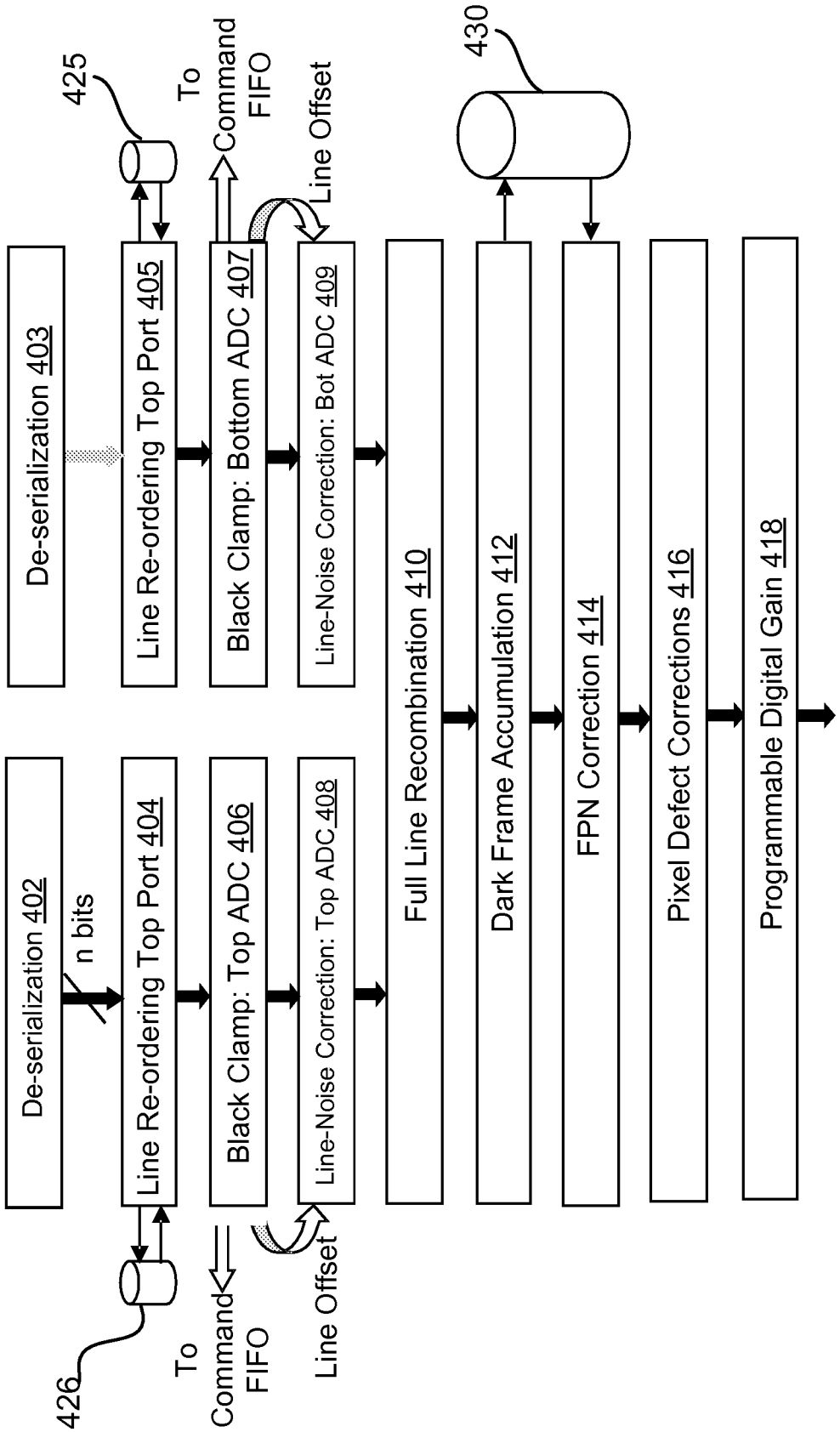
De-serialization 402
n bits
Line Re-ordering Top Port 404
Black Clamp: Top ADC 406
Line-Noise Correction: Top ADC 408
Full Line Recombination 410
Dark Frame Accumulation 412
FPN Correction 414
Pixel Defect Corrections 416
Programmable Digital Gain 418
426
To Command FIFO
Line Offset
De-serialization 403
Line Re-ordering Top Port 405
Black Clamp: Bottom ADC 407
Line-Noise Correction: Bot ADC 409
425
To Command FIFO
Line Offset
430

FIG. 6

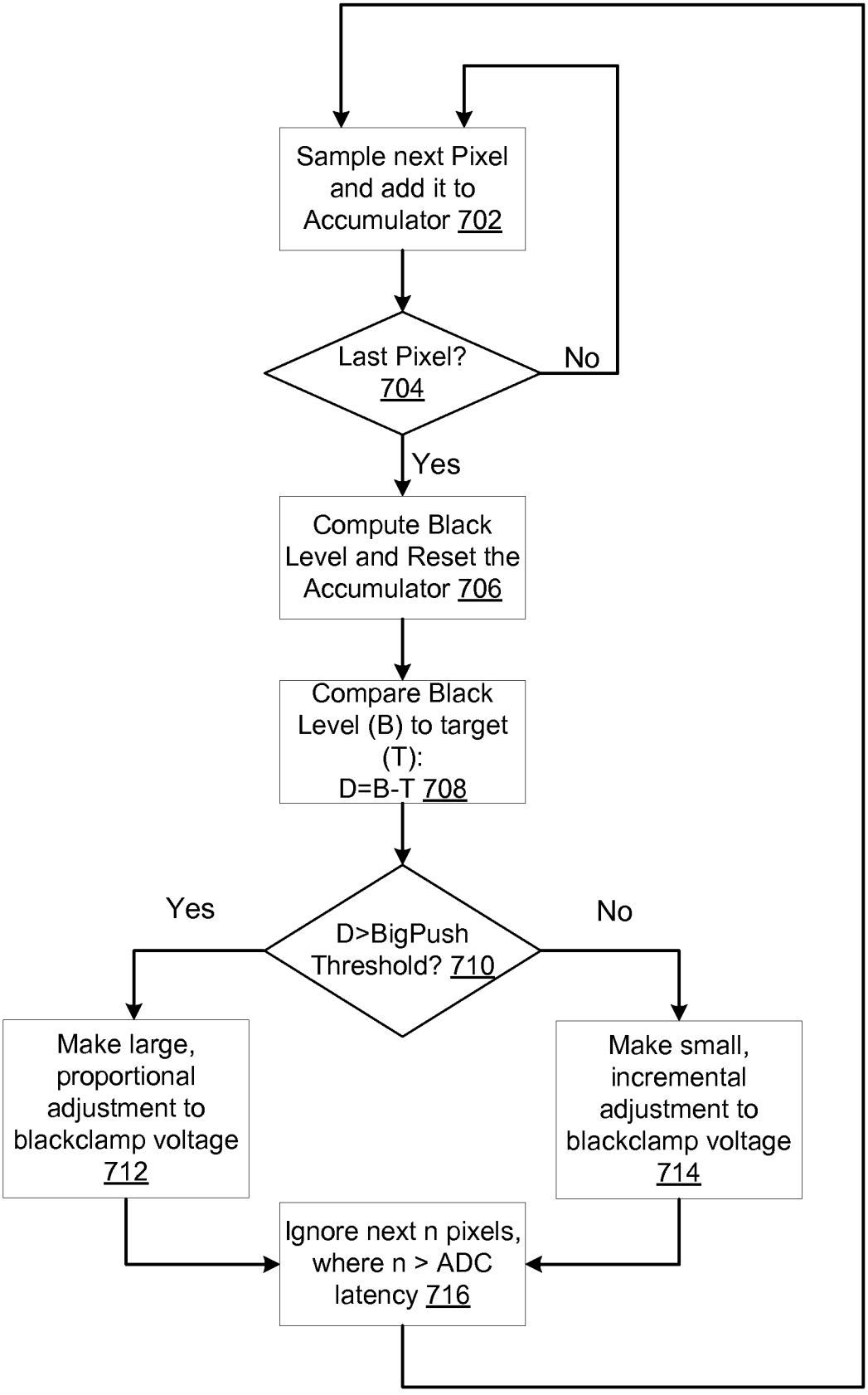
Sample next Pixel and add it to Accumulator 702
Last Pixel? 704
No
Yes
Compute Black Level and Reset the Accumulator 706
Compare Black Level (B) to target (T): D=B-T 708
Yes
D>BigPush Threshold? 710
No
Make large, proportional adjustment to blackclamp voltage 712
Make small, incremental adjustment to blackclamp voltage 714
Ignore next n pixels, where n > ADC latency 716

FIG. 7

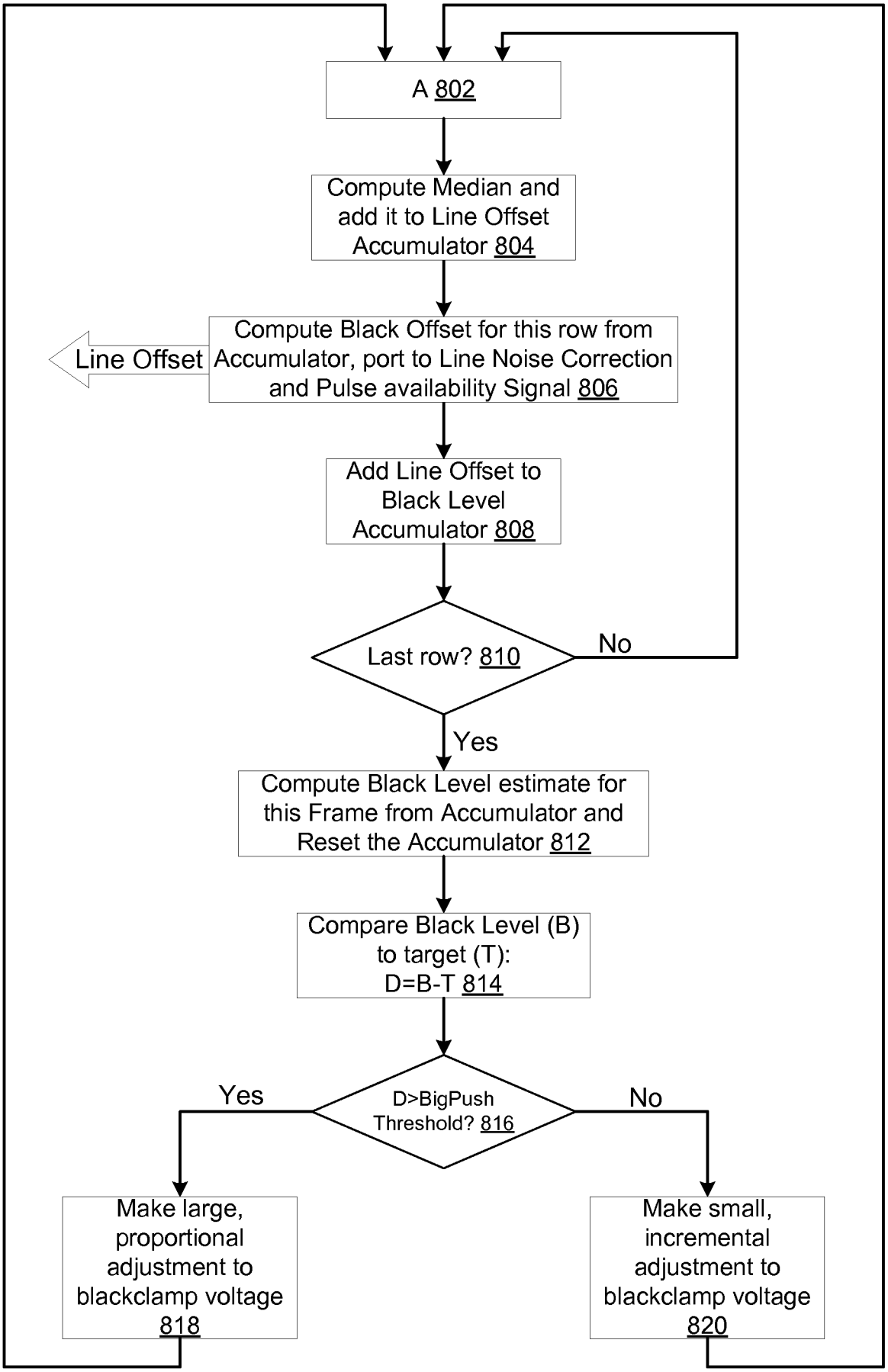
A 802
Compute Median and add it to Line Offset Accumulator 804
Compute Black Offset for this row from Accumulator, port to Line Noise Correction and Pulse availability Signal 806
Line Offset
Add Line Offset to Black Level Accumulator 808
Last row? 810
No
Yes
Compute Black Level estimate for this Frame from Accumulator and Reset the Accumulator 812
Compare Black Level (B) to target (T): D=B-T 814
D>BigPush Threshold? 816
Yes
No
Make large, proportional adjustment to blackclamp voltage 818
Make small, incremental adjustment to blackclamp voltage 820

FIG. 8A

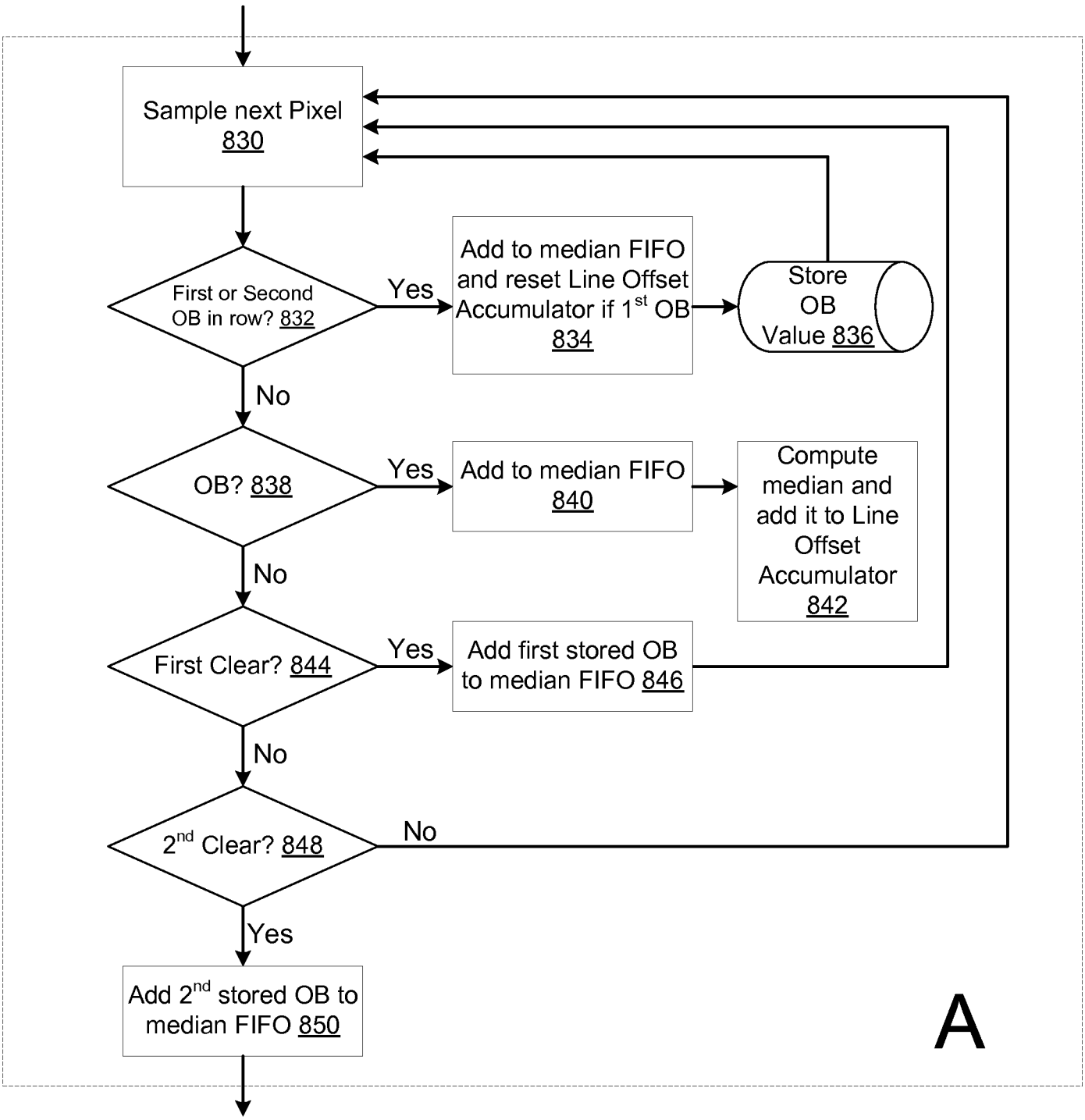
Sample next Pixel 830
First or Second OB in row? 832
Yes
Add to median FIFO and reset Line Offset Accumulator if 1st OB 834
Store OB Value 836
No
OB? 838
Yes
Add to median FIFO 840
Compute median and add it to Line Offset Accumulator 842
No
First Clear? 844
Yes
Add first stored OB to median FIFO 846
No
2nd Clear? 848
No
Yes
Add 2nd stored OB to median FIFO 850
A

FIG. 8B

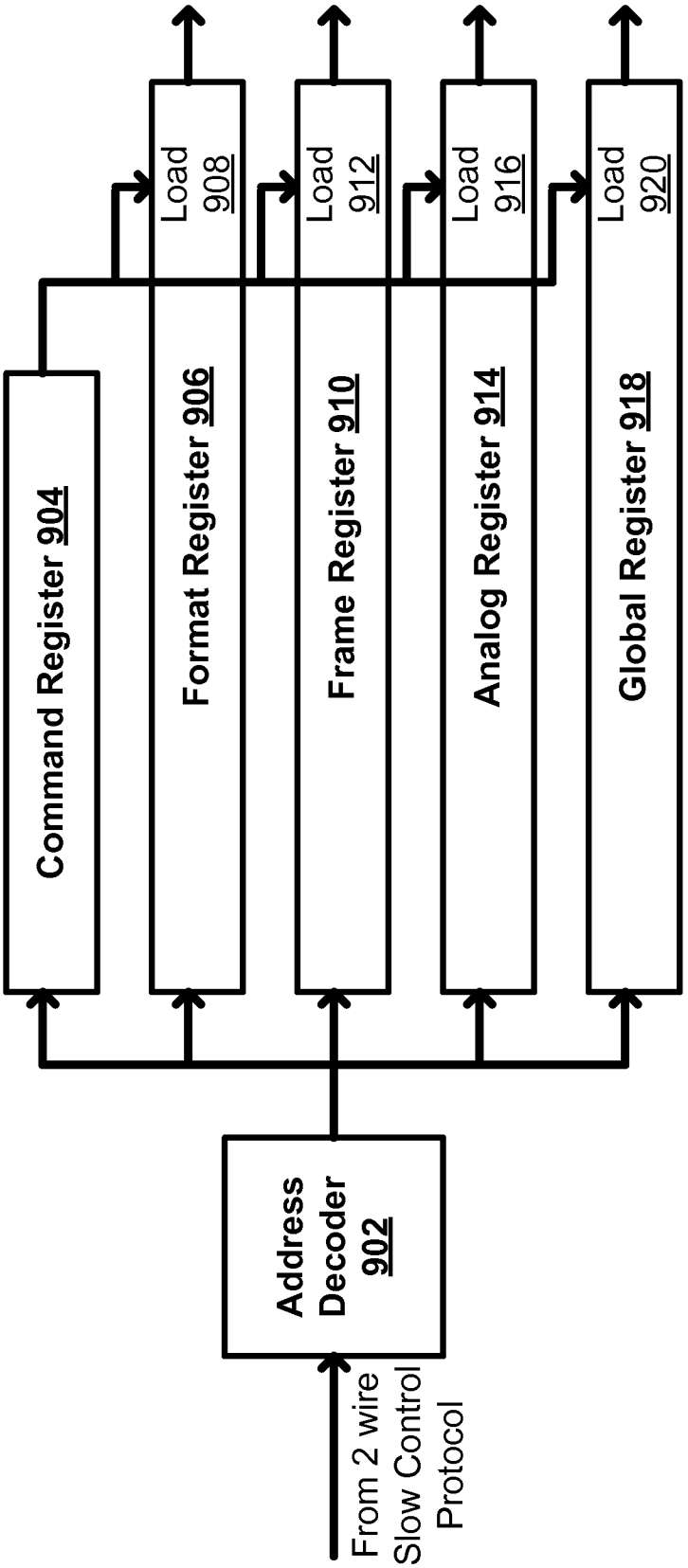
From 2 wire Slow Control Protocol
Address Decoder 902
Command Register 904
Format Register 906
Frame Register 910
Analog Register 914
Global Register 918
Load 908
Load 912
Load 916
Load 920

FIG. 9

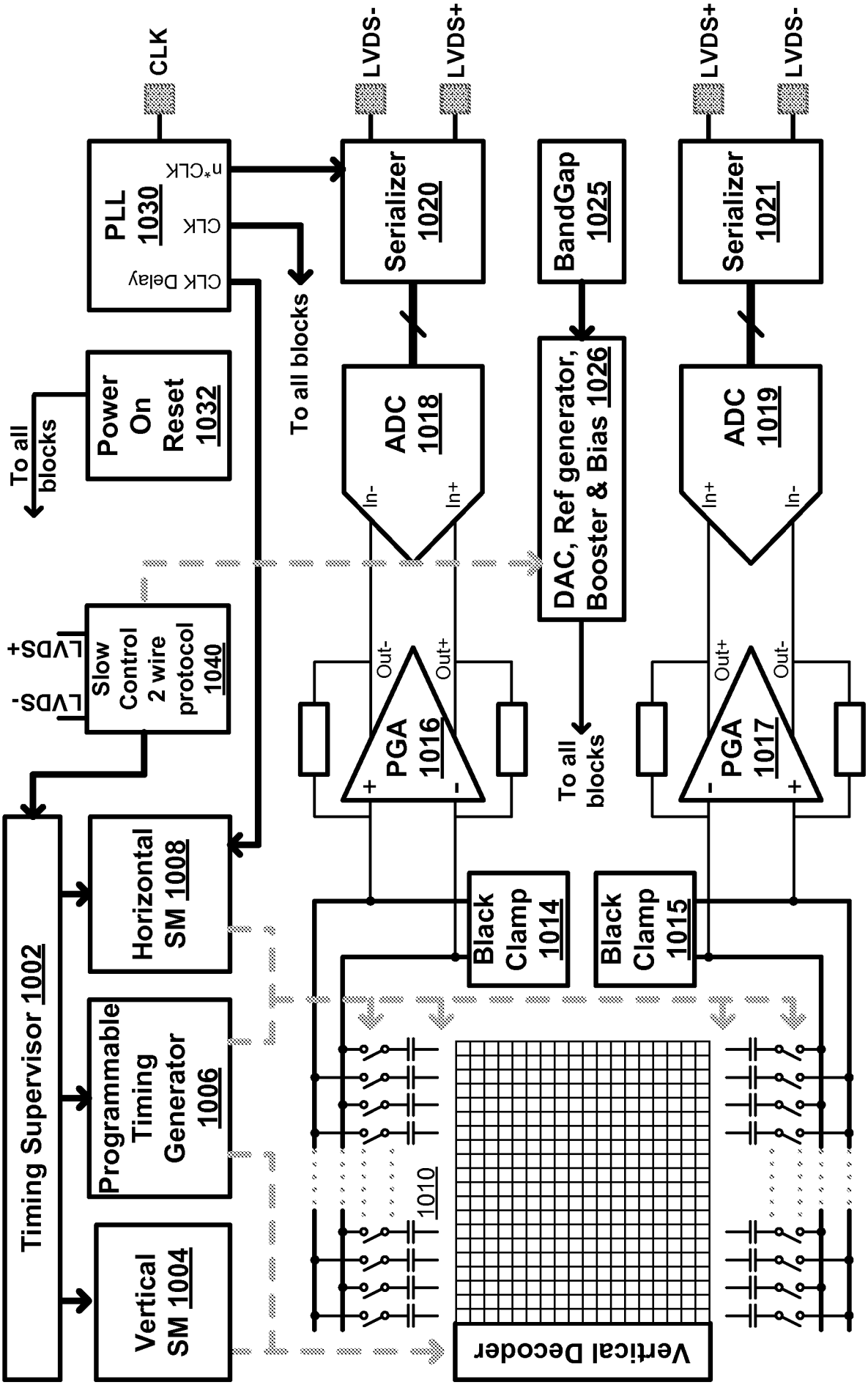
CLK
LVDS-
LVDS+
LVDS+
LVDS-
PLL 1030
n*CLK
CLK
CLK Delay
Serializer 1020
Serializer 1021
BandGap 1025
Power On Reset 1032
To all blocks
To all blocks
ADC 1018
ADC 1019
In-
In+
In+
In-
DAC, Ref generator, Booster & Bias 1026
Slow Control 2 wire protocol 1040
LVDS+
LVDS-
Out-
Out+
Out+
Out-
PGA 1016
PGA 1017
To all blocks
Timing Supervisor 1002
Horizontal SM 1008
Programmable Timing Generator 1006
Vertical SM 1004
Black Clamp 1014
Black Clamp 1015
1010
Vertical Decoder

FIG. 10

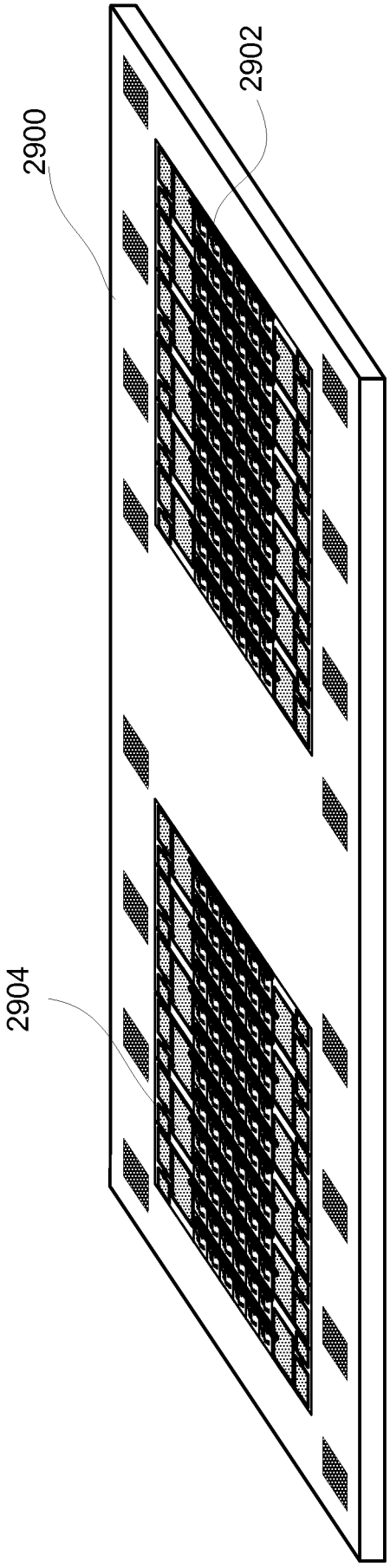

FIG. 11A

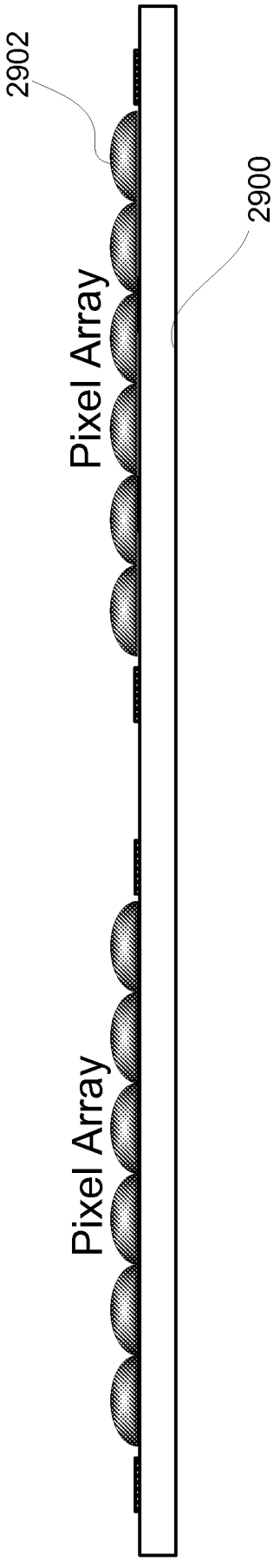

FIG. 11B

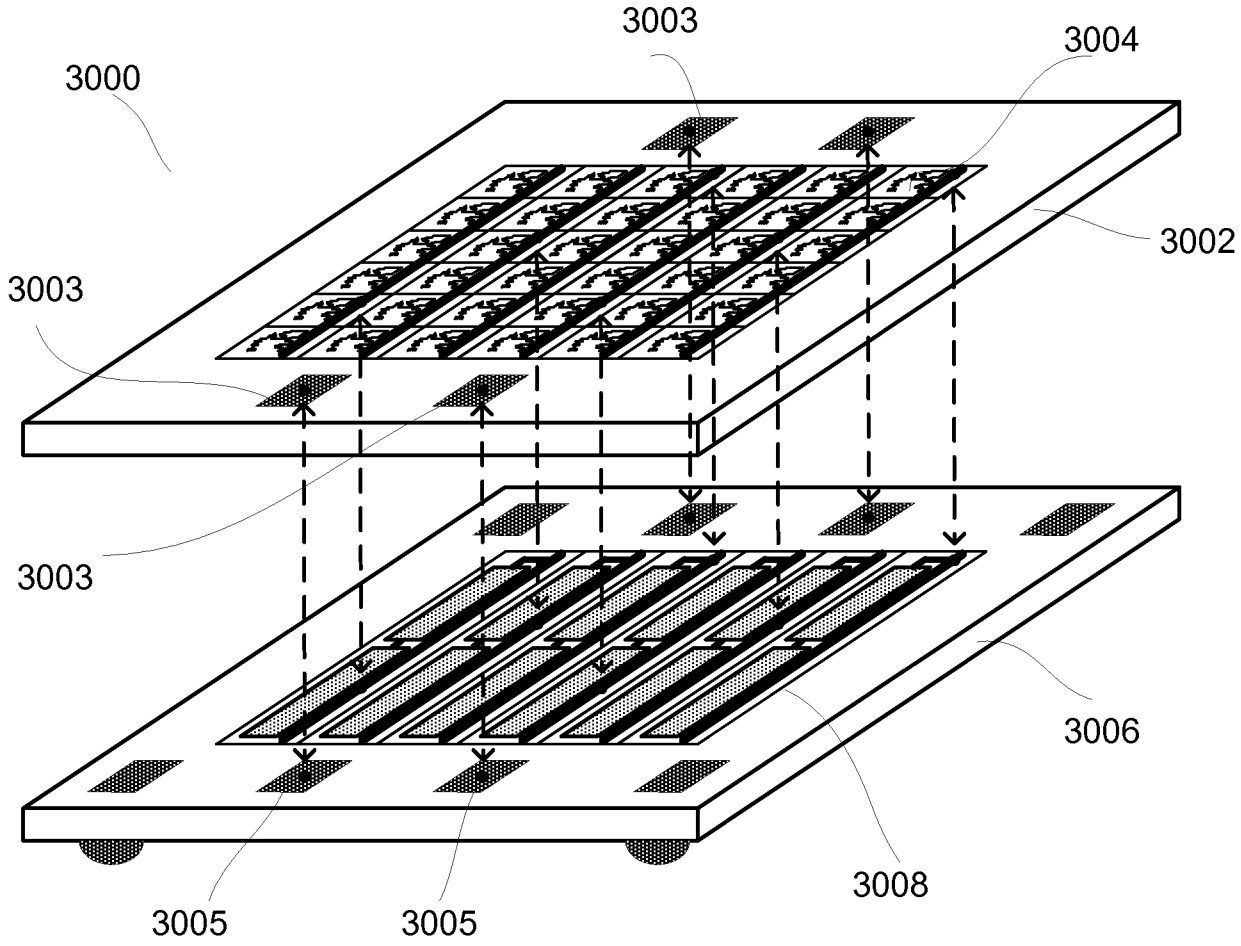

FIG. 12A

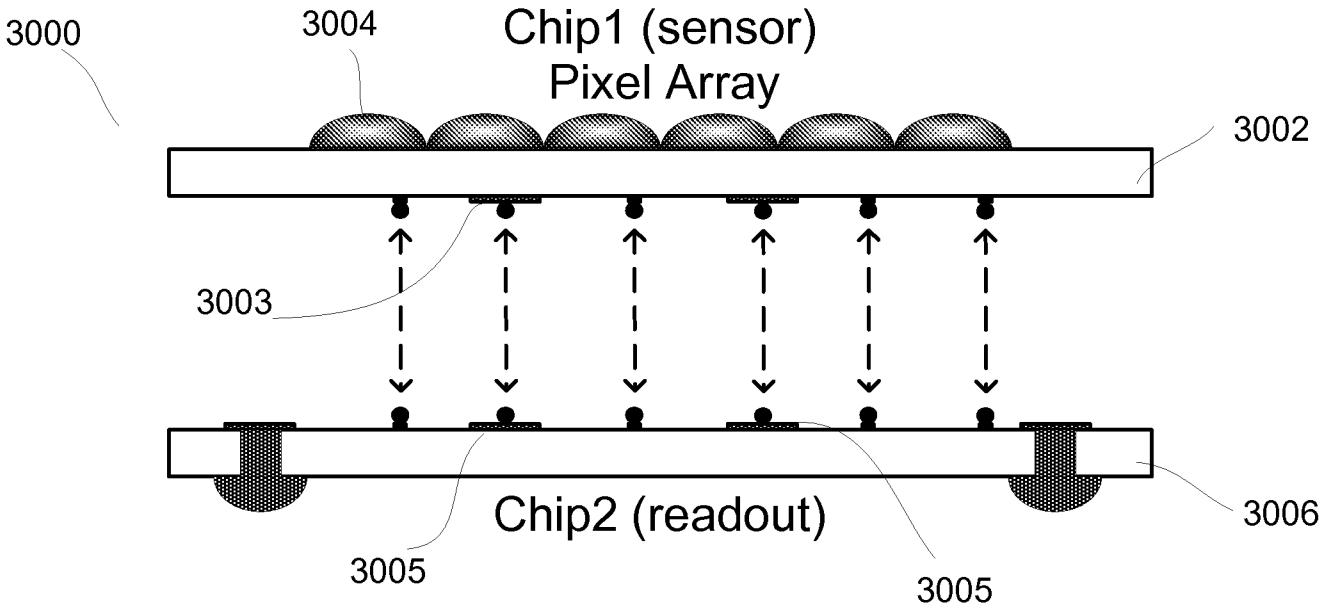

FIG. 12B

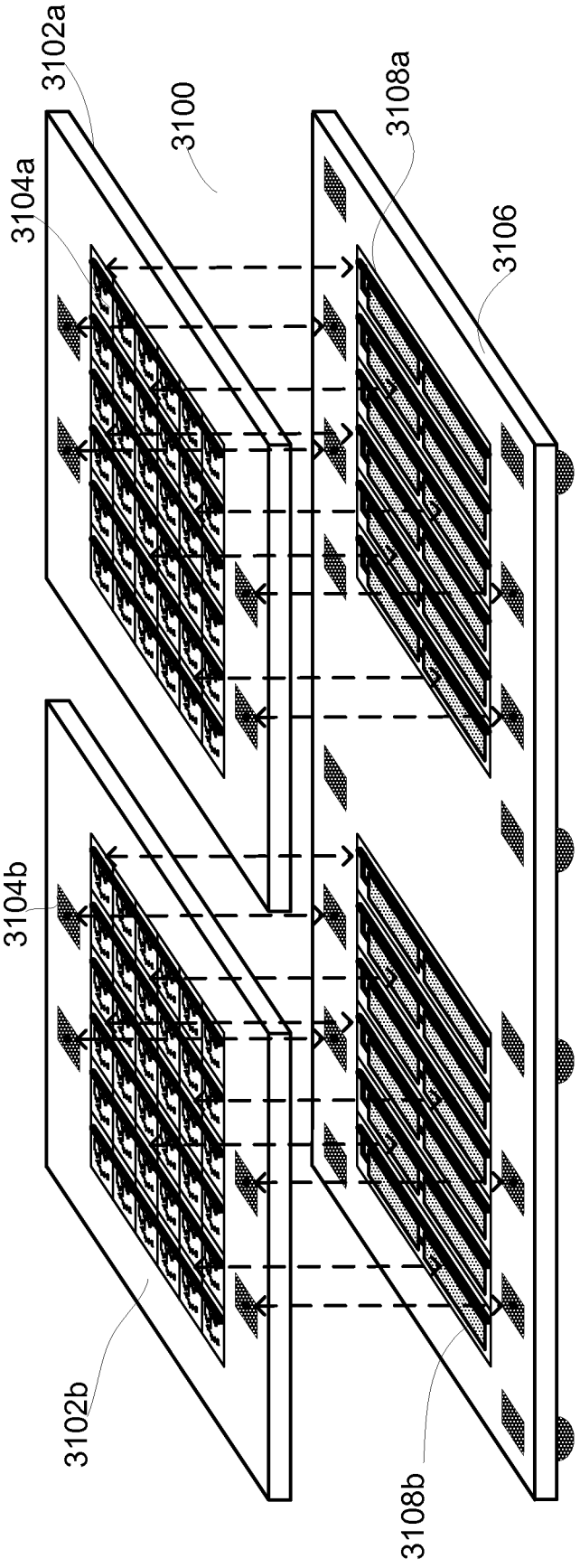

FIG. 13A

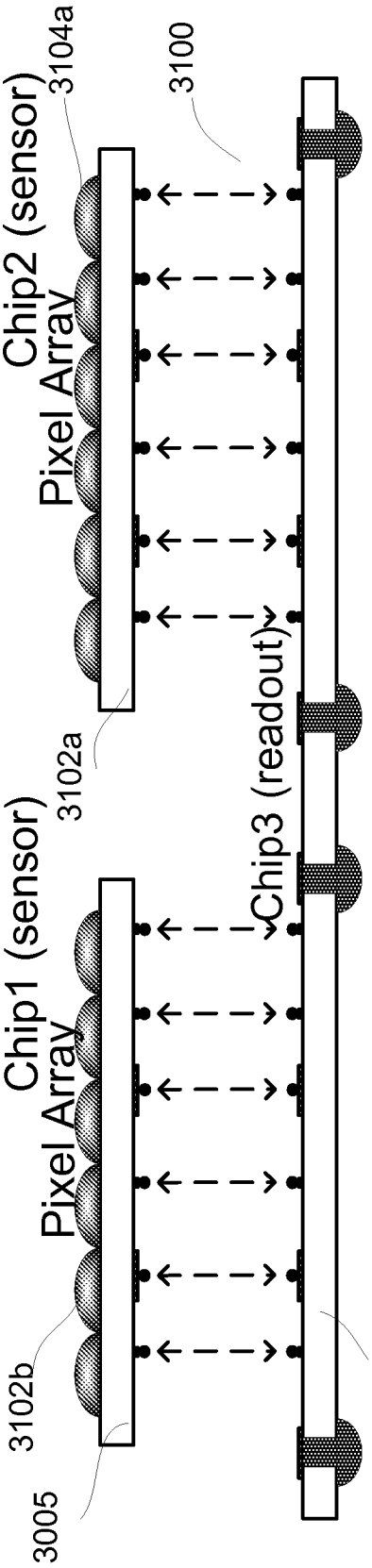

FIG. 13B

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(74) Agent: **EDWARDS, Terrence, J.**; Techlaw Ventures, PLLC, 3290 West Mayflower Way, Lehi, UT 84043 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

[Continued on next page]

(54) Title: CAMERA SYSTEM WITH MINIMAL AREA MONOLITHIC CMOS IMAGE SENSOR

(57) Abstract: The disclosure extends to methods, systems, and computer program products for digitally imaging with area limited image sensors, such as within a lumen of an endoscope.

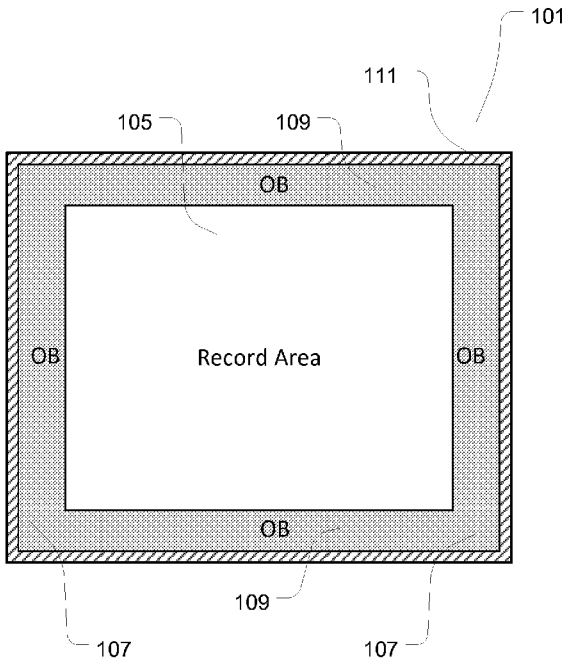

FIG. 1A

WO 2014/018948 A3

TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 13/52423

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - A61B 1/04 (2014.01)
USPC - 348/68
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 348/68

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 348/65, 68, 272, 274 (keyword limited--see terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Patbase; Google Patents; Google Scholar; Google web
Search Terms Used: Endoscope, imaging, black, clamp, long, register, registry, exposure, timing, lens, handhold, hand, hold, handle, lens, pixel, tip, electromagnet, digitizer, ADC, analog, digital, light, illumination, lumen

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/0021271 A1 (PASERO et al.) 24 January 2008 (24.01.2008), para [0044], [0048], [0050], [0054], [0068], Fig. 1	1-7, 48
Y	US 2006/0250513 A1 (YAMAMOTO et al.) 09 November 2006 (09.11.2006), Abstract, para [0021]-[0022], [0058]	1-7, 48
Y	US 5,339,275 A (HYATT) 16 August 1994 (16.08.1994), col 10, ln 52-58, col 55, ln 60- col 56, ln 22, col 85, ln 28-57	2
Y	US 6,469,739 B1 (BECHTEL et al.) 22 October 2002 (22.10.2002), col 8, ln 37-55, col 18, ln 25-col 19, ln 20, col 23, ln 15-22	3-7

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 May 2014 (13.05.2014)	03 JUN 2014
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 13/52423

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

---see extra sheet---

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-7, 48

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 13/52423

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: Claims 1, 48, 2-7 drawn to a long registry
Group II: Claims 1, 48, 8-9, 14-25, 35-43, 49-51, 53-56, 59, 69 drawn to a pixel array comprises active pixels and optical black pixels, further including a black clamp circuit and a charge pump.
Group III: Claims 1, 48, 10-11, 71-72 drawn to digitizers.
Group IV: Claims 1, 48, 12-13, 70 drawn to transfer ports.
Group V: Claims 1, 48, 26-27 drawn to imaging sensor corrections.
Group VI: Claims 1, 48, 28-34, 60-61 drawn to control registers, latches, and shift registers.
Group VII: Claims 1, 48, 44-47 drawn to two dimensional frame data.
Group VIII: Claims 1, 48, 52 drawn to programmable gate array.
Group IX: Claims 1, 48, 57 drawn to a memory for accumulating a set of measured uncorrected line offsets.
Group X: Claims 1, 48, 58 drawn to digital to analog conversion.
Group XI: Claims 1, 48, 62-68 drawn to a hand piece having optical fiber and a light emitter.

NOTE
Claims 1 and 48 are considered generic.

The inventions listed as Groups I though XI do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special technical features
The invention of Group I includes the special technical feature of a long registry wherein the long registry comprises control parameter entries, not required by Groups II-XI.
The invention of Group II includes the special technical feature of a pixel array comprises active pixels and optical black pixels, further including a black clamp circuit and a charge pump, not required by Groups I and III-XI.
The invention of Group III includes the special technical feature of digitizers, not required by Groups I-II and IV-XI.
The invention of Group IV includes the special technical feature of transfer ports, not required by Groups I-III and V-XI.
The invention of Group V includes the special technical feature of imaging sensor corrections, not required by Groups I-IV and VI-XI.
The invention of Group VI includes the special technical feature of control registers, latches, and shift registers, not required by Groups I-V and VII-XI.
The invention of Group VII includes the special technical feature of two dimensional frame data, not required by Groups I-VI and VIII-XI.
The invention of Group VIII includes the special technical feature of programmable gate array, not required by Groups I-VII and IX-XI.
The invention of Group IX includes the special technical feature of a memory for accumulating a set of measured uncorrected line offsets, not required by Groups I-VIII and X-XI.
The invention of Group X includes the special technical feature of digital to analog conversion, not required by Groups I-IX and XI.
The invention of Group XI includes the special technical feature of a hand piece having optical fiber and a light emitter, not required by Groups I-X.

Common technical features:
The only features shared by Groups I through XI that would otherwise unify the groups are the features of claims 1 and 48. However, claims 1 and 48 are considered generic, and are made obvious over US 2008/0021271 A1 to Pasero et al. (hereinafter, 'Pasero') in view of US 2006/0250513 A1 to Yamamoto et al. (hereinafter, 'Yamamoto').

As per claim 1, Pasero discloses an endoscopic device (Fig.1) for use in a closed light environment comprising: an endoscope body (para [0044]- disclosing endoscope 1) comprising: a hand holding structure (para [0044]- hand part 4); a lumen attached by a lumen base at a first end of the body (para [0044], [0068]); a tip portion of the lumen opposite of the lumen base of the body (para [0044], [0068]); a lens disposed at the distal most portion of the tip portion (para [0044]- disclosing lens 5 fixed to the head part 3); an imaging sensor disposed near the tip portion of the lumen (para [0044]- imaging sensor 6), wherein the imaging sensor comprises: an array of pixels for sensing electromagnetic radiation (para [0044], [0048]); a transfer port for transmitting data generated by the pixel array (para [0044]- disclosing a USB transfer port); a digitizer to convert analog pixel data into digital data (para [0048]); electrical connections providing electrical communication between the imaging sensor and image signal processing circuitry disposed remotely from the imaging sensor (para [0044], [0048], [0050], [0054]). However, Pasero does not disclose a black clamp circuit for providing offset control for the data generated by the pixel array. However, Yamamoto does disclose a black clamp circuit for providing offset control for the data generated by the pixel array (Abstract, para [0021]-[0022], [0058]- disclosing black clamp circuit for controlling offset values). It would have been obvious to one of ordinary skill in the art to combine the device taught by Pasero with the black clamp circuit taught by Yamamoto, since such would allow for correcting or adjusting the black levels of an image.

As per claim 48, Pasero discloses a system for digital imaging in an ambient light deficient environment comprising: an imaging sensor for sensing electromagnetic radiation (para [0044]- imaging sensor 6); wherein said imaging sensor comprises: an array of pixels for sensing electromagnetic radiation (para [0044], [0048]); a transfer port for transmitting data generated by the pixel array (para [0044]- disclosing a USB transfer port); a digitizer to convert analog pixel samples to digital numbers (para [0048]); an endoscope for accessing the ambient light deficient environment (para [0044]); a hand piece attached to said endoscope wherein said endoscope may be maneuvered by manipulation of the hand piece (para [0044]- hand part 4); a control unit comprising a processor wherein said control unit may be in electrical communication with the imaging sensor para [0055]-[0059]; and a connection cable electrically connecting the hand piece and the control unit (para [0054]). However, Pasero does not disclose a black clamp circuit for providing offset control for the data generated by the pixel array. However, Yamamoto does disclose a black clamp circuit for providing offset control for the data generated by the pixel array (Abstract, para [0021]-[0022], [0058]- disclosing black clamp circuit for controlling offset values). It would have been obvious to one of ordinary skill in the art to combine the system taught by Pasero with the black clamp circuit taught by Yamamoto, since such would allow for correcting or adjusting the black levels of an image.

Therefore, Groups I though XI lack unity under PCT Rule 13.

(19)中华人民共和国国家知识产权局

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A61B 1/04(2006.01)

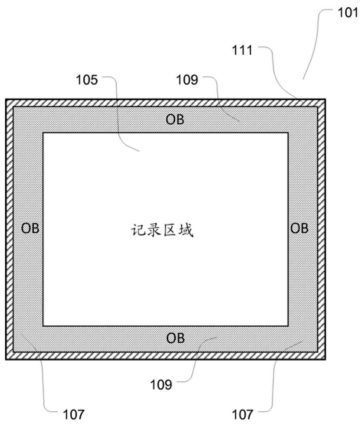
权利要求书5页 说明书11页 附图15页

(54)发明名称

具有最小面积单片式CMOS图像传感器的相机系统

(57)摘要

本公开涉及在例如内窥镜的内腔内利用面积有限成像传感器来数字成像的方法、系统和计算机程序产品。



CN 104486987 A

1. 一种在封闭光环境中使用的内窥镜设备，包括：

内窥镜主体，其包括：

手持结构；

内腔，其由所述主体第一末端的处的内腔基座附接；

所述内腔的尖端部，其与所述主体的所述内腔基座相对；

透镜，其设置在所述尖端部的最远端部；

成像传感器，其靠近所述内腔的所述尖端部设置，其中所述成像传感器包括：

像素阵列，其用于感测电磁辐射；

传递端口，其用于传递由所述像素阵列生成的数据；

数字转换器，其将模拟像素数据转换成为数字数据；

黑钳位电路，其提供对由所述像素阵列生成的数据的偏移控制；

电连接，其提供在所述成像传感器和远离所述成像传感器图像设置的信号处理电路之间的电通信。

2. 根据权利要求 1 所述的内窥镜设备，进一步包括长寄存器，其中所述长寄存器包括用于控制所述像素阵列的曝光时间和所述像素阵列的增益的控制参数项目。

3. 根据权利要求 1 所述的内窥镜设备，进一步包括长寄存器，其包括用于控制所述像素阵列的增量偏移调整或者所述像素阵列的曝光时间的控制参数项目。

4. 根据权利要求 1 所述的内窥镜设备，进一步包括长寄存器，其包括用于控制所述像素阵列的增量偏移调整或者所述像素阵列的增益的控制参数项目。

5. 根据权利要求 1 所述的内窥镜设备，进一步包括长寄存器，其包括用于控制增量偏移调整和所述像素阵列的曝光时间或者所述像素阵列的增益的控制参数项目。

6. 根据权利要求 1 所述的内窥镜设备，进一步包括长寄存器，其包括用于控制所述像素阵列的增量偏移调整和所述像素阵列的曝光时间的控制参数项目。

7. 根据权利要求 1 所述的内窥镜设备，进一步包括长寄存器，其包括用于通过调整模拟电流、模拟电压、像素定时、垂直定时、传感器复位和传感器初始化中的任意一个来控制像素阵列的所述操作的多个控制参数项目。

8. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述有源像素和所述光学黑色像素校准来自所述像素阵列的输出。

9. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述光学黑色像素组织在与所述像素阵列内的所述有源像素邻近的列中。

10. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器包括单个数字转换器。

11. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器包括多个数字转换器。

12. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器包括单个输出端口。

13. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器包括多个输出端口。

14. 根据权利要求 9 所述的内窥镜设备，其中，对所述光学黑色像素的列多次抽样以降低光学黑色列的数目。

15. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述光学黑色像素组织在与所述像素阵列内的所述有源像素邻近的列中，其中所述光学黑色像素的列组织在所述成像传感器的右侧和左侧。

16. 根据权利要求 15 所述的内窥镜设备，其中，所述成像传感器右侧的光学黑色列中的一个被多次抽样。

17. 根据权利要求 15 所述的内窥镜设备，其中，所述成像传感器左侧的光学黑色列中的一个被多次抽样。

18. 根据权利要求 15 所述的内窥镜设备，其中，所述成像传感器右侧的光学黑色列中的一个被多次抽样，并且所述成像传感器左侧的光学黑色列中的一个被多次抽样。

19. 根据权利要求 15 所述的内窥镜设备，其中，所述成像传感器右侧的光学黑色列中的多个被多次抽样。

20. 根据权利要求 15 所述的内窥镜设备，其中，所述成像传感器左侧的光学黑色列中的多个被多次抽样。

21. 根据权利要求 15 所述的内窥镜设备，其中，所述成像传感器右侧的光学黑色列中的多个被多次抽样，并且所述成像传感器左侧的光学黑色列中的多个被多次抽样。

22. 根据权利要求 1 所述的内窥镜设备，其中，所述黑钳位电路关于所述成像传感器远程地设置。

23. 根据权利要求 22 所述的内窥镜设备，其中，所述设备还包括命令接口以控制所述黑钳位电路。

24. 根据权利要求 1 所述的内窥镜设备，其中，所述黑钳位电路感测由数模转换器生成的电压。

25. 根据权利要求 1 所述的内窥镜设备，其中，所述黑钳位电路感测由电荷泵生成的电压。

26. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器纠错的一部分关于所述成像传感器远程地设置。

27. 根据权利要求 1 所述的内窥镜设备，其中，所有的成像传感器纠错关于所述成像传感器远程设置。

28. 根据权利要求 1 所述的内窥镜设备，进一步包括多个控制寄存器，其中所述控制寄存器是经由移位寄存器加载的数字锁存器。

29. 根据权利要求 28 所述的内窥镜设备，其中，所述移位寄存器是任意长度的。

30. 根据权利要求 28 所述的内窥镜设备，其中，所述多个控制寄存器中的大多数是使用包括数十比特的移位寄存器被加载的。

31. 根据权利要求 28 所述的内窥镜设备，其中，所述多个控制寄存器中的大多数是使用包括数百比特的移位寄存器被加载的。

32. 根据权利要求 28 所述的内窥镜设备，其中，所述多个控制寄存器中的大多数是使用包括数千比特的移位寄存器被加载的。

33. 根据权利要求 28 所述的内窥镜设备，其中，所述移位寄存器是使用串行的 2 线协议被加载的。

34. 根据权利要求 28 所述的内窥镜设备，其中，所述移位寄存器中的一个专用于帧到帧参数改变。

35. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器包括多个像素阵列，其中多个像素阵列用于创建三维图像。

36. 根据权利要求 1 所述的内窥镜设备，其中，所述成像传感器还包括：包括所述像素阵列的第一基板和包括用于所述像素阵列的支持电路的第二基板，其中包括所述支持电路的所述第二基板远离包括所述像素阵列的第一基板设置。

37. 根据权利要求 36 所述的内窥镜设备，其中，所述第一基板关于所述第二基板垂直对齐。

38. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述光学黑色像素组织在与所述像素阵列内的所述有源像素邻近的列中，其中所述光学黑色像素的列被多次抽样以计算列偏移。

39. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述光学黑色像素组织在与所述像素阵列内的所述有源像素相邻的多个列和多个行中。

40. 根据权利要求 39 所述的内窥镜设备，其中，所述光学黑色行的大部分从所述像素阵列移除，使得仅有所述少数光学黑色行是具有功能的。

41. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述光学黑色像素组在多个列中并且不包括与所述像素阵列内的所述有源像素邻近的任何光学黑色行。

42. 根据权利要求 1 所述的内窥镜设备，其中，所述像素阵列包括有源像素和光学黑色像素，其中所述光学黑色像素组织在与所述像素阵列内的所述有源像素邻近的多个列中，其中多个列用于计算所述黑钳位电路的基线黑电平和由所述图像信号处理器执行的黑钳位计算。

43. 根据权利要求 42 所述的内窥镜设备，其中，所述黑钳位用于在数字转换器之前计算控制电压偏移，并且使用多个列偏移利用简单指数平滑法 (SES) 确定数据整个帧内的总偏移。

44. 根据权利要求 1 所述的内窥镜设备，其中，所述设备还包括存储在存储器中的二维帧数据以用于抵消由图像传感器生成的固定模式噪声。

45. 根据权利要求 44 所述的内窥镜设备，其中，所述二维帧数据是从暗帧捕获中得到的。

46. 根据权利要求 45 所述的内窥镜设备，其中，通过不对发射器施加脉冲来助于所述暗帧捕获。

47. 根据权利要求 45 所述的内窥镜设备，其中，通过所述暗帧捕获的简单指数平滑法来计算所述像素偏移。

48. 一种用于在环境光线不足环境中数字成像的系统，包括：

用于感测电磁辐射的成像传感器，其中所述成像传感器包括：

像素阵列，其用于感测电磁辐射；

传递端口，其用于发射由所述像素阵列生成的数据；

数字转换器，其转换模拟像素抽样成数字数值；

黑钳位电路，其提供对由所述像素阵列生成的数据的偏移控制；

内窥镜，其用于接近环境光线不足的环境；

手持件，其附接至所述内窥镜，其中，能够通过所述手持件的操作来操作所述内窥镜；

包括处理器的控制单元，其中，所述控制单元能够与成像传感器电通信；以及

连接线缆，其电连接所述手持件和所述控制单元。

49. 根据权利要求 48 所述的系统，其中，所述像素阵列包括用于校准来自所述像素阵列的输出的光学黑色像素和有源像素。

50. 根据权利要求 49 所述的系统，其中，所述光学黑色像素组织在与所述像素阵列内的有源像素邻近的列中。

51. 根据权利要求 48 所述的系统，进一步包括能够远离所述像素阵列设置的黑钳位控制过程。

52. 根据权利要求 48 所述的系统，进一步包括用于处理可能由所述像素阵列创建的图像数据的可编程门阵列。

53. 根据权利要求 48 所述的系统，进一步包括少于 50 个的光学黑色像素列，使得其能够在所述系统的操作内被再抽样以提供精确性。

54. 根据权利要求 49 所述的系统，进一步包括光学黑色像素列，其均匀设置在所述有源像素列的相对侧。

55. 根据权利要求 49 所述的系统，进一步包括光学黑色像素列，其不均匀地设置在所述有源像素列的相对侧。

56. 根据权利要求 49 所述的系统，进一步包括黑钳位控制过程，其对由光学黑色像素接收的数据取平均值，并且将所述平均值和存储在所述系统内的存储器内的预定目标值比较。

57. 根据权利要求 48 所述的系统，进一步包括用于累加整个帧的所测量未纠错列偏移的集合的存储器。

58. 根据权利要求 48 所述的系统，进一步包括用于控制补偿暗电流的电压的数模转换电路。

59. 根据权利要求 48 所述的系统，进一步包括用于控制电压的电荷泵电流以抵消暗电流。

60. 根据权利要求 48 所述的系统，进一步包括多个寄存器。

61. 根据权利要求 48 所述的系统，进一步包括命令寄存器，其用于高级别事件的 1 比特命令如芯片复位和其它寄存器的负载。

62. 根据权利要求 48 所述的系统，进一步包括设置在内窥镜内位于其关于所述手持件的远端部的成像传感器。

63. 根据权利要求 48 所述的系统，进一步包括设置在所述手持件内的成像传感器。

64. 根据权利要求 48 所述的系统，进一步包括发射器，其发射通过光纤从所述发射器传输至所述内窥镜的尖端的电磁辐射的脉冲。

65. 根据权利要求 48 所述的系统，进一步包括这样一种缆线，该缆线包括：用于将来自光发射器的电磁辐射传输至内窥镜的光纤，以及提供从所述控制单元到所述成像传感器的电子通信的导电线。

66. 根据权利要求 48 所述的系统，进一步包括设置在所述控制单元内并且与光发射器和所述成像传感器电通信的控制器。

67. 根据权利要求 48 所述的系统，进一步包括设置在手持件内并且与光发射器和所述

成像传感器电通信的成像传感器。

68. 根据权利要求 48 所述的系统，进一步包括与发射器耦接的成像传感器。

69. 根据权利要求 48 所述的系统，进一步包括远程处理算法，以通过使用每个列中的光学黑色像素集合减去所测量列平均值来纠错列噪声。

70. 根据权利要求 48 所述的系统，进一步包括用于传输像素数据的多个传递端口。

71. 根据权利要求 48 所述的系统，进一步包括多个数字转换器。

72. 根据权利要求 48 所述的系统，进一步包括关于所述像素阵列远程设置的数字转换器。

具有最小面积单片式 CMOS 图像传感器的相机系统

[0001] 相关申请交叉引用

[0002] 本申请要求 2012 年 7 月 26 日递交的美国临时专利申请号 No.61/676,289 以及 2013 年 3 月 15 日递交的美国临时专利申请号 No.61/790,590 的优先权，通过引用的方式将其整体并入本文，包括但是不限制至下文特别明显的这些部分，参考的并入具有以下例外：如果以上参考申请的任何部分与本申请不一致，则本申请取代以上参考的申请。

背景技术

[0003] 技术的进步已经为医疗用途的成像能力提供了进展。因为组成内窥镜的组件中的进展，因此已享有一些最有利的进展的一个领域可以是内窥镜外科手术。在例如关节镜检查和腹腔镜检查中使用的传统内窥镜设计为使得成像传感器放置在设备的近端，手持件单元内。在这样的配置中，内窥镜单元应当经由一组复杂的精确耦合的光学组件朝向传感器沿着其长度传以最小的损耗和失真输入射光。由于组件是昂贵的并且制造过程可以是劳动密集的，因此内窥镜单元的成本可以由光学器件占主要部分。此外，这种类型的范围可以是机械方面精致的并且相对较小的影响可以很容易损坏组件或者打乱其相对排列。

[0004] 可能需要提供用于能够保持减少光环境中高质量视频流的内窥镜医疗用途的减小面积成像传感器的方法和系统。传感器的减小面积允许其被设置在内窥镜的远端，进而极大降低成本。这引起了无需维修或者消毒循环的单次使用的内窥镜的可能性。可替换地，它们可以以后被拆卸并且使得它们的一些组件回收利用。

[0005] 如可以看到的，本公开提供了可以以文中将要公开的并且将由说明书中所讨论的和附图而进一步使能的有效和简练的方式做到这一点的方法和系统。

附图说明

[0006] 参照以下附图描述本公开的非限制和非详尽实现，其中贯彻各个图相同的附图标记指代相同的部件，除非另作说明。参考下面的描述和附图本公开的优点可以变得更好理解，其中：

[0007] 图 1A 示出了现有技术中通常的像素阵列的实现；

[0008] 图 1B 示出了根据本公开的原理和教导的具有形成为光学黑色列的像素阵列的实现；

[0009] 图 1C 示出了根据本公开的原理和教导的系统电路和互补系统硬件的示意；

[0010] 图 2 示出了根据本公开的原理和教导的示例性像素阵列，其示出有源记录像素列和光学黑色像素列之间的关系；

[0011] 图 3 示出了根据本公开的原理和教导的示例性像素阵列，其示出有源记录像素列和光学黑色像素列的降低数目之间的关系；

[0012] 图 4 示出了根据本公开的原理和教导的根据一个实现的实例方法的硬件流程图；

[0013] 图 5 示出了根据本公开的原理和教导的根据一个实现的实例方法的硬件流程图；

[0014] 图 6 示出了根据本公开的原理和教导的根据一个实现的使用分区光系统的实例

方法和硬件示意的流程图；

[0015] 图 7 示出了根据本公开的原理和教导的根据一个实现的实例方法的流程图。

[0016] 图 8A 示出了根据本公开的原理和教导的根据一个实现的实例方法的流程图；

[0017] 图 8B 示出了根据本公开的原理和教导的根据一个实现的实例方法的流程图；

[0018] 图 9 示出了根据一个实现的实例方法的流程图；

[0019] 图 10 示出了根据本公开的原理和教导的根据一个实现的实例方法的硬件流程图；

[0020] 图 11A 和图 11B 示出了根据本公开的原理和教导的具有用于生成三维图像的多个像素阵列的实现；

[0021] 图 12A 和图 12B 分别示出建立在多个基板上的成像传感器的实现的立体图和侧视图，其中形成像素阵列的多个像素列位于第一基板上并且多个电路列位于第二基板上，还示出一列像素至其关联或者对应的电路列的电连接和电通信；以及

[0022] 图 13A 和 13B 分别示出了具有用于生成三维图像的多个像素阵列的传感器的实现的立体图和侧视图，其中多个像素阵列和成像传感器被构建在多个基板上。

[0023] 具体实现方式

[0024] 本公开涉及用于提供先进的内窥镜的方法、系统和计算机程序产品以及它们在医疗过程期间的使用。在本公开的以下讨论中，参考形成本公开的一部分的附图，并且附图中可以通过示出本公开可以实践的具体实现的方式示出。可以理解的是可以利用的其它实现并且可以改变结构而不偏离本公开的范围。

[0025] 关节镜检查和腹腔镜检查中使用的传统内窥镜设计为使得成像传感器放置在设备的近端，手持件单元内。在这样的配置中，内窥镜单元应当沿着其长度以最小的损耗和失真，经由一组复杂的精确耦合的光学组件，朝向传感器传输入射光。由于组件是昂贵的并且制造过程可以是劳动密集的，因此内窥镜单元的成本可以由光学器件关联的成本决定。

[0026] 以上缺点的解决方案可以是将内窥镜自身内的成像传感器放置在内腔的远端，进而潜在地提供更大的光学简单性、坚固性和经济性，其可以在相关设备例如手机相机内得到普遍实现。然而这个方法的一个可接受的解决方案绝不是普通的，因为其引入了它自己的一套工程挑战，尤其可能是传感器应该适应在高度受限区域内的事实。

[0027] 对传感器面积设置过分的约束可以导致更少和 / 或者更小的像素。因此，降低像素数直接影响空间分辨率。减小像素面积也可能减少可用信号容量和敏感性。降低信号容量降低了动态范围，即相机利用大范围亮度同时获取来自传感器的所有有用信息的能力。存在各种方法以延伸成像系统的动态范围超过像素自身。然而它们均具有某种不利（例如在分辨率或者帧速率中），并且它们可以引入或者加重在极端的情况下成为问题的不希望的伪影。可替换地，降低灵敏度导致是需要更大的光功率以给场景的较暗区域带来可接受的信号级。降低 F 数也可以补偿灵敏度的损失，但是以空间失真和焦点深度减小为代价。

[0028] 在成像传感器技术中，由于 CMOS 成像传感器更易于集成和操作、优越的或者可比较的图像质量、更大的灵活性和较低的成本，CMOS 成像传感器已在很大程度上取代在现代相机应用例如内窥镜检查中的常规 CCD 成像器。然而为了达到最佳的效果，CMOS 传感器带来应该考虑的一定不利特性。

[0029] 成像传感器可以包括转换图像信息成为数字数据所必须的电路，并且可以具有包

括在传感器芯片自身上的各种层次的数字处理。数字处理的范围可以从用于纠错从放大器特性中变化生成的非理想 CMOS 传感器目的的基本算法至提供标准 RGB 彩色空间（芯片上相机）的视频数据的完整的图像信号处理（ISP）链条。

[0030] 给定相机系统的传感器复杂性的希望程度可以由几个因素驱动，其中一个因素可以是成像传感器的可用物理空间。功能极小 CMOS 传感器将仅具有基本像素阵列加上一定程度上序列化和缓冲的电路以驱动芯片的模拟数据。操作和读出像素所需要的所有定时信号可以从外部提供。从外部供给控制信号的需求可以增加许多焊盘，其消耗大量可以更好地用于集聚光的基面板。因为需要电通信连接，因此其无需使得靠近像素阵列的最小功能等同于最小使用面积。

[0031] 如果支持电路被远程放置并且如果第二级可以是距离传感器的明显距离，则变得更加希望在数字域中传输数据，因为可以使得其几乎不受噪声干扰和信号衰减影响。由于减少除了增加相机制造的复杂性和成本（之外还消耗空间）的传感器上焊盘的数量，因此可能存在强烈希望以减少导体的数量。尽管增加模数转换至传感器可以是必要的，但是增加的面可以被抵消至无需对与缓冲和传输模拟信号关联的信号恶化进行补偿的程度。在面积消耗的方面，考虑到 CIS 技术中可用的典型特征尺寸，优选的可以是经由图 9 中可见的一组控制寄存器和控制该寄存器的简单命令接口从而使得在芯片上生成的所有内部逻辑信号。

[0032] 在高度受控照明环境中的具有减小象素计数的高清晰度图像可以通过光源处逐帧脉冲彩色切换结合高帧获取率和专门设计的单色传感器来实现。由于减小面积成像传感器的像素可以是色彩无关的，因此有效的空间分辨率可以比传统单传感器相机中它们的色彩（通常为贝尔模板过滤）相应物明显更高。由于少得多的入射光子被浪费，因此它们还可以具有更高的量子效率。此外，为了弄模糊与贝尔模板关联的彩色伪影，基于拜耳的空间色彩调制要求与单色情况相比所附的光学器件的 MTF 被降低。这对于可以利用彩色传感器实现的实际空间分辨率的具有不利影响。

[0033] 这个特定公开还可以涉及用于内窥镜应用中的系统解决方案，其中成像传感器可以是在内窥镜的远端。为得到基于最小面积传感器的系统，存在如文中所描述的可以开发的超出明显减少像素计数的其它设计方面。特别是，芯片数字部分的面积应该随着至芯片（焊盘）的连接的数量而减少。该公开描述完成实现这样系统的目标的新颖方法。这涉及具有多个新颖特征的全定制 CMOS 成像传感器的设计。

[0034] 本公开的实现可以包括或者利用专用或者通用计算机，其包括计算机硬件，诸如，例如，如以下更详细地讨论的一个或者多个处理器和系统存储器。本公开范围内的实现还可以包括用于携带或者存储计算机可执行指令和 / 或者数据结构的物理和其它计算机可读介质。这种计算机可读介质可以是可由通用或者专用计算机系统访问的任何可用介质。存储计算机可执行指令的计算机可读介质是计算机储存器介质（设备）。携带计算机可执行指令的计算机可读介质是传输介质。因此，通过举例而不是限制的方式，本公开的实现可以包括至少两种完全不同类型的计算机可读介质 :计算机储存器介质（设备）和传输介质。

[0035] 计算机存储介质（设备）包括 RAM、ROM、EEPROM、CD-ROM、固态驱动器（"SSDs"）（例如，基于 RAM）、闪速存储器，相变存储器（“PCM”），其它类型的存储器，其它光盘储存器，磁盘储存器或者其它磁储存器设备，或者可以用于存储计算机可执行指令或者数据结构形式

的所希望程序代码装置并且可以由通用或者专用计算机访问的任何其它介质。

[0036] “网络”可以被定义为允许在计算机系统和/或模块和/或其他电子设备之间传输电子数据的一个或多个数据链路。当信息经由网络或者其它通信连接（电路、无线或者电路或者无线的组合）可以被传递或者提供至计算机时，计算机适当地将连接视为传输介质。传输介质可以包括网络和/或数据链路，其可以用以携带计算机可执行指令或者数据结构形式的所希望程序代码装置并且并且可以由通用或者专用计算机访问。以上的组合还应该包括在计算机可读介质的范围之内。

[0037] 另外，计算机可执行指令或者数据结构形式的程序代码装置在到达各种计算机系统组件后可以从传输介质至计算机储存器介质（设备）自动传递（或反之亦然）。例如，经由网络或者数据链路接收的计算机可执行指令或数据结构可以在网络接口模块（例如，“NIC”）内在 RAM 中被缓冲并且然后最终被传递至计算机系统 RAM 和/或计算机系统处的较不易失性计算机储存器介质（设备）。RAM 还可以包括固体驱动器（基于 SSD 或者 PCI_X 的实时内存分层储存器，如 FusionIO）。因此，应当理解的是计算机储存器介质（设备）可以包括在也（或者甚至主要）利用传输介质的计算机系统组件中。

[0038] 计算机可执行指令包括例如指令和数据，其当在处理器处被执行时导致通用计算机、专用计算机或者专用处理设备执行一定功能或一组功能。计算机可执行指令可以是例如二进制、中间格式指令，例如汇编语言，或者甚至源代码。尽管主题已经以针对结构特征和/或方法动作的语言进行了描述，但是可以理解的是在附上的权利要求书中限定的主题不必限制至所描述的特征或者以上所描述的动作。相反，所描述的特征和动作被公开为实现权利要求的示例形式。

[0039] 本领域的技术人员可以理解的是本公开可以利用许多类型计算机系统配置在网络计算环境中实践，算机系统配置包括个人计算机、台式计算机、膝上型计算机、消息处理器、手持式设备、手机、相机控制单元、多处理器系统、基于微处理器或者可编程消费电子产品、网络 PC、小型计算机、大型计算机，移动电话，掌上电脑，平板电脑，寻呼机，路由器，交换机，各种存储设备等等。本公开还可以在分布式系统环境中实践，其中通过网络链接（由电路数据链路、无线数据链路或者电路和无线数据链路的组合）的本地和远程计算机系统两者均执行任务。在分布式系统环境中，程序模块可以位于本地和远程记忆存储设备中。

[0040] 另外，在适当情况下，文中所描述的功能可以在一个或者多个硬件，软件、固件、数字组件或者类似组件中执行。例如，一个或多个专用集成电路 (ASIC) 和可编程门阵列 (PGA) 可以被编程以执行本文所描述的一个或多个系统和程序。某些术语贯彻下面的描述和权利要求书使用以指代特定的系统组件。如本领域技术人员可以理解的，组件可以由不同的名称指代。本文并不旨在以名称不同而不是功能对组件之间区别。

[0041] 为了偏移校准的目的，成像传感器可以包括特殊用途，光学盲或光学黑 (OB) 的行（在阵列的顶部和/或底部）和列（向阵列的右侧和/或左侧）。在图 1A 中可以示出成像传感器 101 的示例布局，其具有记录区域中的像素 105 连同顶部和底部 OB 行 109 和左侧和右侧 OB 列 107。对于 OB 钳位算法，OB 行 109 通常用于监视模拟像素黑电平。OB 行 109 还通常被数字算法用于取消列固定模式噪声或者 FPN(CFPN)。在实施例中，保护环 111 可以围绕成像传感器 101 的周围。在另一方面，OB 列 107 通常用于估计列偏移以作为一种抵消任何列噪声的装置。由于列噪声可能是时间的，因此偏移应当对于每一帧中的每一列重新计

算。

[0042] 可以通过对于 OB 钳位算法去除 OB 行 109 和使用 OB 列 107 代替 OB 行 109 而实现像素阵列尺寸的总体减少（见以下讨论）。在实现中，通过获取暗数据帧可以取消包括 CFPN 的所有 FPN 类型，进而消除了对专用 CFPN 纠错和其相关联的 OB 行 109 的需求。图 1B 示出了正是这样的成像传感器 101 和像素阵列 105 的实例，其中不存在 OB 行展示但是相反包括 OB 列 107。

[0043] 图 1C 可以是示出了示例计算设备 100 的框图。计算设备 100 可用于执行各种程序，如本文所讨论的那些。计算设备 100 可以用作服务器、客户端或者任何其它计算实体。计算设备 100 可以执行如文中所讨论的各种监视功能并且可以执行一个或者多个应用程序，例如文中所描述的应用程序。计算设备 100 可以是多种计算设备中的任何一个，例如台式计算机、笔记本电脑、服务器计算机、手持式计算机、平板计算机等。

[0044] 计算设备 100 包括一个或者多个处理器 102、一个或者多个存储器设备 104、一个或者多个接口 106、一个或者多个大容量储存器设备 108、一个或者多个输入 / 输出 (I/O) 设备 110 以及显示设备 130，所有这些都耦接至总线 112。处理器 102 包括执行存储在存储器设备 104 和 / 或大容量储存器设备 108 中指令的一个或者多个处理器或控制器。处理器 102 还可以包括各种类型的计算机可读介质例如高速缓冲存储器。

[0045] 存储器设备 104 包括各种计算机可读介质例如易失性存储器（例如，随机存取存储器 (RAM)114) 和 / 或非易失性存储器（例如，只读存储器 (ROM)116)。存储器设备 104 也可以包括可重写的 ROM 例如闪速存储器。

[0046] 大容量储存器设备 108 包括各种计算机可读介质例如，磁带，磁盘，光盘，固态存储器（例如，闪速存储器）等等。如图 1C 中所示，特定大容量储存器设备可以是硬盘驱动器 124。各种驱动器也可包括在大容量储存器设备 108 中从而允许对各种计算机可读介质读取和 / 或写入。大容量储存器设备 108 包括可去除介质 126 和 / 或不可去除的介质。

[0047] I/O 设备 110 包括各种设备，其允许数据和 / 或其它信息被输入到或从计算设备 100 中获取到。实例 I/O 设备 110 包括光标控制设备、键盘、辅助键盘、麦克风、监视器或者其它显示设备、扬声器、打印机、网络接口卡、调制解调器、透镜、CCD 或者其它图像获取设备，等等。

[0048] 显示设备 130 包括能够为计算设备 100 的一个或多个用户显示信息的任何类型的设备。显示设备 130 的实例包括监视器、显示终端、视频投影设备等等。

[0049] 像素阵列 135 还可以被包括以及相对于系统内的其它电路可以远程操作。

[0050] 接口 106 包括各种接口，其允许计算设备 100 与其它系统、设备或者计算环境进行交互作用。实例接口 106 可以包括任何数量的不同网络接口 120，例如，局域网 (LAN)、广域网 (WAN)、无线网络以及互联网的接口。其它接口包括用户接口 118 和外围设备接口 122。接口 106 也还可以包括一个或多个用户接口元件 118。接口 106 还可以包括一个或者多个外围接口例如对于打印机的接口、定点设备（鼠标、轨迹板等）、键盘等等。

[0051] 总线 112 允许处理器 102、存储器设备 104、接口 106、大容量储存器设备 108 以及 I/O 设备 110 彼此通信以及耦接至总线 112 的其它设备或者组件。总线 112 代表一个或者多个多种类型的总线结构，例如系统总线、PCI 总线、IEEE 1394 总线、USB 总线等等。

[0052] 为了说明的目的，程序和其它可执行程序组件在文中示出为离散的块，尽管可以

理解的是这样的程序和组件可以在不同的时间位于计算设备 100 的不同储存器组件中并且由处理器 102 可执行。可替换地，文中所描述的系统和程序可以在硬件或者硬件、软件和 / 或固件的组合中实现。例如，一个或者多个专用集成电路 (ASIC) 联机或者在系统的初始化之前可以被编程以执行一个或者多个文中所描述的系统和程序。

[0053] OB 列的数目通常可以是 100 或更多，取决于空间限制等。可用的 OB 列越多，列偏移精确度越大。更大的精确度意味着更低的列噪声、后期纠错。通常，对于如图 2 中所示的每个列所有的可用物理 OB 将被读出。如果实现较小数量的物理像素，而不是具有所需数量的物理 OB 像素，(考虑到一定精确度目标)，被实现的较小数量的物理像素在水平读出过程期间多次重新抽样，则可以达到阵列尺寸减小的进一步程度。这个方法在图 3 中示出。

[0054] 存在于数字转换器的输出处的原始 CMOS 成像传感器数据可能是很不理想的。它通常情况可能是读出的像素的水平行的最佳顺序并不等同于阵列内的实际物理顺序。另外，原始数据通常显示还反映读出结构的性质的不希望的伪影，其在弱光和相应的高增益的情况中变得非常明显。这些读出伪影通常可以包括列 FPN，其从逐列偏移中的变化中生成 ；以及时间列噪声，其由与水平读出过程相关联的电路复位造成。

[0055] CMOS 传感器的另一个兴致属性可以是 ：一定程度的暗信号可以由像素内的光电二极管生成。从该电流所生成的积分信号的量取决于曝光时间和温度。由于暗信号可能无法与光信号区分，因此其中的改变转换为模拟域中信号基准中的改变。为了可使 ADC 的可用动态范围得到充分的利用，可能重要的是 ：对暗信号进行抽样和调整。图 4 示出了在 CMOS 传感器中这个通常是如何完成的。来自 OB 像素的数据可能是片上逻辑的平均并且与目标数字黑电平比较。为了使得黑电平尽可能靠近目标，对输入偏移电压进行连续调整。这可以被称为黑钳位或者 OB 钳位过程。

[0056] 大多数的市售传感器包括片上逻辑以执黑钳位和数字噪声纠错。这个逻辑不必位于传感器上，然而并且为了开发具有最小面积传感器的相机系统，将这些纠错移至图像信号处理链 (ISP) 是有意义的。如果它们位于具有很多可用的逻辑门和 RAM 的 FPGA 或者 ASIC 中，由于纠错是更少资源限制的，因此这实际上对于整个系统的性能有净利益。

[0057] 图 5 示出了如何将 OB 钳位逻辑移动离开传感器 (连同传感器纠错算法)。在这种情况下，来自 OB 钳位逻辑的关于模拟调整的信息可以经由其命令接口通过指令被传递至传感器。

[0058] 图 6 示出了实现已经在包括最小面积传感器的系统的背景下开发的 ISP 前端的实例。在此实例中传感器上存在两个数字转换器，其分别转换偶数和奇数列并且传递两个查分端口上的串行数据。

[0059] 在解串行化之后，第一过程可以涉及重建每个端口的列成为适当顺序。接下来两个纠错块即处理黑钳位和列噪声纠错是数据路径专用的，也就是两条链将被分别处理。

[0060] 黑钳位—图 7 中的流程图可以是如何在片上传统 CMOS 成像系统内通常操作 OB 钳位逻辑的实例。可能通常存在多个抽样并且对来自多个 OB 行的每帧做模拟调整，同时 OB 行像素存在于数字读出路径中。如前面所讨论的，对于最小面积传感器，OB 像素的数目可以降低至必要的最低值，并且这可以通过消除 OB 行和使用列以纠错黑钳位以及列噪声来实现。图 8A 和 8B 中的流程图概述了实现这的一种方法。基本理念可以是累积对于整个帧所测得的、未纠错的列偏移的集合并且使用最终估计以进行黑钳位调整。同时，为了使得对单独列

做出数字调整，每个单独列偏移估计可以供给给后续过程。

[0061] 黑钳位电平的调整可以使用传感器上的 DAC 或电荷泵通过控制 DC 电压（$V_{黑钳位}$）而完成。由于例如光电二极管中的暗电流，进入 ADC 的像素电压偏移四处移动，进而 DAC 需要通过估计数字域中的黑偏移而定期调整。

[0062] 行为不正常的各个 OB 像素可以严重降低黑偏移测量的质量；进而处理它们是十分重要的。一个好方法可能是对每个 OB 像素取包括问题像素和其最邻近 4 个像素的一组 5 个像素的中值。最后列偏移估计将然后被认为是所有中值的平均值。应当做出一些准备以在开始和结束时不失去的统计资料，例如缓冲 OB 的整个抽样和裹住 5 个抽样。这需要流水线处理数据，导致延迟至少等于每行每个 ADC 通道的 OB 总数。

[0063] 偶数通道的列偏移估计（假设两个 ADC 具有奇偶布置），行号 r：

[0064] $$L_{r,\text{even}} = \frac{2 \cdot \sum_{i=0,2,4\ldots}^{N_{OB}-2} \mu_i}{N_{OB}}$$

[0065] 列偏移，其中 N_{OB} 可以是每行 OB 像素的总数并且 u_i 可以是 OB 像素 i 的中值 (median)，因此计算为：

[0066]
$$\mu_0 = \text{median}\ [x_{(N_{OB}-4)}, x_{(N_{OB}-2)}, x_0, x_2, x_4]$$
$$\mu_2 = \text{median}\ [x_{(N_{OB}-2)}, x_0, x_2, x_4, x_6]$$
$$\mu_4 = \text{median}\ [x_0, x_2, x_4, x_6, x_8]$$
$$\ldots$$
$$\mu_{(N_{OB}-2)} = \text{median}\ [x_{(N_{OB}-6)}, x_{(N_{OB}-4)}, x_{(N_{OB}-2)}, x_0, x_2]$$

[0067] 同样地，列偏移估计计数通道（确保两个 ADC 具有奇偶布置），行号 r“

[0068] $$L_{r,\text{odd}} = \frac{2 \cdot \sum_{i=1,3,5\ldots}^{N_{OB}-1} \mu_i}{N_{OB}}$$

[0069] 其中：

[0070]
$$\mu_1 = \text{median}\ [x_{(N_{OB}-3)}, x_{(N_{OB}-1)}, x_1, x_3, x_5]$$
$$\mu_3 = \text{median}\ [x_{(N_{OB}-1)}, x_1, x_3, x_5, x_7]$$
$$\mu_5 = \text{median}\ [x_1, x_3, x_5, x_7, x_9]$$
$$\ldots$$
$$\mu_{(N_{OB}-1)} = \text{median}\ [x_{(N_{OB}-5)}, x_{(N_{OB}-3)}, x_{(N_{OB}-1)}, x_1, x_3]$$

[0071] 要获得总帧黑电平，一个好的实用方法可以通过累计所有列偏移以使用简单指数平滑法 (SES) 计算总黑电平而提供。使用 SES 的好处可以是：朝向帧的端部的行可以对最终黑估计具有较大影响，这对于发生在子帧时间尺度上黑偏移中的寻址变化可能是希望的。

[0072] 在 SES 中，每当抽样可用时，可以递增地调整节运行估计。为方便起见，在被添加至先前估计之前，抽样可以由二进制数 (2^q) 分割。为了将结果标准化，先前估计可以可以

每次首先与 $(2^q-1)/2^q$相乘。q 的高值导致稳定情况中一段时间较大的统计精确度。Q 的较低值可以使得纠错对快速变化反应更大，q 应当作为可调参数。

[0073] $k_r = L_r (r = 0)$

[0074] $$k_r = \frac{1}{2^q} L_r + \frac{(2^q - 1)}{2^q} k_{(r-1)} \quad (r > 0)$$

[0075] 其中，k_r可以是行 r 之后的黑电平估计，并且 L_r可以是对于每行 r 的列偏移估计。在阵列中的最后行已经增加之后，可以决定对黑钳位 DAC 做什么。

[0076] 黑钳位算法将要求可以由可调整参数提供的目标黑电平。根据所观察到的黑色估计是否高于或者低于目标，所讨论的通道的传感器上的黑钳位 DAC 将被向上或者向下推送。只要黑电平可能靠近目标，推送的大小可以是例如的最小单位，即一个 DAC 计数。在黑钳位可能距离目标很远的情况下，可以作出较大比例的推送，参见图 8A。该算法需要知道黑钳位 DAC 计数和传感器 ADC 计数之间对应关系的粗略校准和相对于输出黑电平的 DAC 调整的定向性。

[0077] 列噪声纠错中“列噪声”是指像素的水平行的偏移中随机的时间变化。可能存在多个源，但是其可以被看作是每当可以读出像素行时复位模拟元件导致的复位噪声。它可能是时间的并且应该对于每帧的每个新列计算新的纠错。由于在 ADC 输入处的放大级可能是最终的模拟元件，因此可以有很好的理由怀疑：列噪声可以现象学地显得每个 ADC 通道不独立。因此，最佳的做法可能是独立地纠正每个 ADC（通道）。

[0078] 由于用于列偏移估计的 OB 像素的抽样可以与被施加纠错的（并且抽样统计是有限的）抽样是分开的，因此完全消除列噪声也许是不可能的。假设所有的噪声可以是高斯的，纠错后的列噪声可以近似等于存在于 OB 像素中的像素时间噪声引起的列偏移估算中的不确定性。

[0079] $$\sigma_{L,\mathrm{post}} \approx \frac{\sigma_P}{\sqrt{N_{\mathrm{OB}}}}$$

[0080] 其中，$\sigma_{L,post}$可以是纠错后时间列噪声，σ_P可以是 OB 像素时间噪声并且 N_{OB}可以是 OB 像素的数量。列噪声纠错还引入空间列噪声分量，主要由于存在于 OB 像素内的像素 FPN：

[0081] $$\mathrm{FPN}_{L,\mathrm{post}} \approx \frac{\mathrm{FPN}_P}{\sqrt{N_{\mathrm{OB}}}}$$ 。

[0082] 伪影可以后续在链中由 FPN 纠错消除。模拟已经指示：为了使时间列噪声不可见，幅度应该小于像素时间噪声的约 1/10。该纠错指示每行需要 1000B 像素。

[0083] 列噪声纠错应用至光学观测（清楚的）像素：

[0084] $x'_i = x_i - L + B$

[0085] 其中 L 可以是对于当前列的列偏移估计，从“黑钳位”模块传输并且 B 可以是黑钳位目标电平。

[0086] 完整列重组。这将涉及简单组合两个数据通道成为完整列。它们需要被交错为使得最终清楚像素顺序反映阵列中的正确顺序。

[0087] FPN 纠错，CMOS 图像传感器具有多个噪声源，噪声源的幅度和外观取决于物理条

件的范围。没有相干分量的纯泊松或高斯时间噪声（例如光子散粒噪声或者源极跟随器 1/f 读噪声）看起来像噪声可以看起来一样自然。所有的其它可感知的噪声类型可以对于相同的幅度降低图像质量至更大的程度。空间噪声 (FPN) 可能是特别令人震惊并且 CMOS 传感器固有地具有至少两个源 ;像素 FPN 和列 FPN。像素 FPN 可能主要是由于来自逐个像素 (DSNU) 的光电二极管漏电流（暗信号）中的变化。这个源可以是以指数方式依赖于结温 (7) 和并且线性地依赖于曝光时间。列 FPN 可以是读出结构的结果，读出结构中相同列内的像素通过公共模拟读出元件被引导。

[0088] 通常，片上数字 FPN 纠错将涉及仅处理列 FPN 分量，需求每列一个偏移纠错寄存器。这样纠错的精确度可能通常是每列 20 比特左右，其转换成用于 1920 X 1080 阵列约为 5kB 的 RAM。迁移数字传感器纠错至 ISP 的一个好处可以是 RAM 的随时可用。这开创了取消任何行、列或者逐像素组件的全面 FPN 纠错的可能性。这可以通过简单指数平滑法 (SES) 而实现，指数平滑法中每个新的黑帧抽样可以用于调节每个物理像素基础上的运行偏移估计。

[0089] 可编程数字增益。图 6 中的最后一块对应于可编程数字放大器。CMOS iSoC 通常装配具有非常精细的增量的数字可编程增益级。这可能是有助于自动曝光过程，其通常调节增益和曝光时间。

[0090] 数字放大器可以用于将传感器 ADC 的范围与 ISP（例如，对于 11 比特 ADC×2 至 12 比特 ISP) 的范围对齐。少量的数字增益也可以被用于修剪数字列噪声的印记和 FPN 纠错，其在 ADC 的全部范围变得明显。

[0091] 配置寄存器地址 ROM 的最小化。传统 CMOS 图像传感器包括用于控制传感器如何操作的许多可写寄存器。它们将通常包括 DAC 设置以调节偏置电压和电流、定时参数，以例如用于像素获取和读出周期，放大器偏移和增益等。通常的惯例可以分配一个特定的 8 比特或 16 比特的地址给通常包括 8 或者 16 比特数据的每个寄存器。

[0092] 一个更节省空间的方法涉及组合大量的控制 RAM 成为单个、长寄存器。在极端情况下，所有参数可以被放置进单个寄存器，不需要地址 ROM。然而由于写控制寄存器需要时间并且典型的视频应用涉及基于逐帧改变少量操作参数（例如曝光时间），因此这种解决方案可能不是很实际的。最实际的解决方案可以通过功能地连接相关的参数集合成为少量长寄存器来提供。具有比如 10 个寄存器（需要 4 个地址比特）相对一个寄存器而言的空间上的差异可以忽略不计。具体而言，以高速率（例如每帧）周期性地写入的所有参数一切属于唯一的寄存器（帧寄存器）是有意义的。这些参数包括曝光时间、收益、增量偏移调整和维持连续高品质视频所需的任何其它。如果如前面所描述地数字数据通路逻辑已经被迁移出芯片，则黑钳位电压调节数据也属于该寄存器，因此它也应该每帧都被修正。在实现中，在该配置阶段期间，寄存器可以被写入并且进而相对于总帧定时的帧寄存器写入的定时应当由相机仔细控制。

[0093] 参数寄存器分组的其它实例可以包括模拟电流、模拟电压、像素定时、垂直定时、传感器命令（复位等）等。在图 9 中，寄存器的布置可以示出为具体最小面积传感器设计。“命令”寄存器可用于最高级别面向事件的 1 比特命令，例如芯片复位和其它寄存器下方示出的对于其它寄存器的负载。2 线协议地址译码器决定哪些移位寄存器直接输入 2 线协议数据。为了下载“格式”寄存器，例如外部控制器发送具有与格式寄存器关联的地址的命令。

这放置数据流进入格式寄存器移位寄存器。然后为了锁存数据，跟踪命令被发送至设置有特定“负载格式”比特的命令寄存器。可以理解的是，可以使用多个控制寄存器。控制寄存器可以是数字锁存器，其经由移位寄存器被加载。移位寄存器可以是任意长度的。在一个实施例中，多个控制寄存器中的大部分可以使用包括数十比特的移位寄存器被加载。在一个实施例中，移位寄存器可以使用串行的、2线协议而被加载。在一个实施例中，移位寄存器中的一个可以专用于帧到帧参数变化诸如，例如，积分时间和黑钳位偏移调整。

[0094] 图10示出了用于内窥镜应用的最小面积传感器的实施例的整体框图，其中传感器可以包括入内窥镜单元的远端。

[0095] 图11A和图11B分别示出了根据本公开的教导和原理具有用于生成三维图像的多个像素阵列的单片式传感器2900的实现的立体图和侧视图。这样的实现对于三维图像获取是希望的，其中两个像素阵列2902和2904可以在使用过程中被抵消。在另一个实现中，第一像素阵列2902和第二像素阵列2904可以是专用于接收电磁辐射的波长的预定范围，其中第一像素阵列专用于与第二像素阵列不同的电磁辐射的波长范围。

[0096] 图12A和图12B分别示出建立在多个基板上的成像传感器3000的实现的立体图和侧视图。如图所示，形成像素阵列的多个像素列3004位于第一基板3002上并且多个电路列3008位于第二基板3006上。还在图中示出的是一列像素至其关联或者对应的列的电路的电连接和电通信。在一个实现中，或者可以是利用其像素阵列制造的并且支撑单个、单片式基板/芯片上电路的成像传感器可以具有与所有或者大部分支撑电路分开的像素阵列。本公开可使用利用三维堆叠技术被堆叠在一起的至少两个基板/芯片。两个基板/芯片的第一基板/芯片3002可以使用图像CMOS方法进行处理。第一基板/芯片3002可以包括专有的像素阵列或者由有限的电路包围的像素阵列。第二或者随后的基板/芯片3006可以使用任何方法进行处理，并且不必是来自图像CMOS方法。为了在或者基板/芯片上十分有限的空间或者面积中集成多种和多个功能，或者混合模式或者模拟方法，为了集成例如精确的模拟功能或者RF方法，为了实现无线功能或者MEMS(微机电系统)，为了集成MEMS设备，第二基板/芯片3006可以是但是不限于高密度的数字处理。可以使用任何三维技术，将图像CMOS基板/芯片3002与第二或者后续基板/芯片3006堆叠。第二基板/芯片3006可以支持大多或者大部分电路，其否则将在第一图像CMOS芯片3002(如果在单片基板/芯片上实现)中实现为外围电路并且进而增加了整个系统的面积同时保持像素阵列的尺寸不变，并且因此在最大可能程度说被优化。两个基板/芯片之间的电连接可以通过3003和3005的互连实现，其可以是线接合，碰撞和/或TSV(硅穿孔)。

[0097] 图13A和13B分别示出了用于生成三维图像的多个像素阵列的传感器3100的实现的立体图和侧视图。三维成像传感器可以被构建在多个基板上并且可以包括多个像素阵列和其它关联电路，其中形成第一像素阵列的多个像素列3104a和形成第二像素阵列的多个像素列3104b分别位于相应的3102a和3102b，并且多个电路列3108a和3108b都位于分开基板3106上。还示出的是像素列至关联或者电路对应列之间的电连接和通信。

[0098] 可以理解的是，本公开的教导和原理可以在可重复使用设备平台、有限使用设备平台、重新仿真(re-posable)使用设备平台或者单次使用/一次性设备平台中使用，而不偏离本公开的范围。可以理解的是，在可重复使用设备平台中，最终用户负责设备的清洁和灭菌。在有限使用设备平台中，在变得不可操作前设备可以被使用一些特定的次数。典型

的新设备利用需要最终用户在附加用途之前清洁和灭菌的附加用途无菌交付。在重新仿真(re-posable)使用设备平台中,第三方可以重新处理设备(例如,清洁、打包和灭菌),用于附加用途的单次使用设备以比新单元更低的成本使用。在单次使用/一次性设备平台中,设备提供对操作室的灭菌并且在被布置前仅能使用一次。

[0099] 在封闭光环境中使用的内窥镜的实施例可以包括:内窥镜主体,其提供手持结构;内腔,其由主体第一端处的内腔基座附接;内腔的尖端部,其与内腔基座相对;透镜,其可以设置在尖端部的最远端部;成像传感器,其可以靠近内腔的尖端部设置,包括用于感测电磁辐射的像素阵列,其中,像素阵列可以具有有源像素和光学黑色像素以用于纠错来自所述像素阵列的输出;其中光学黑色像素可被组织在与像素阵列内有源像素邻近的列中;传递端口,其用于传递由像素阵列生成的数据;数字转换器,其转换模拟像素抽样成数字数值;黑钳位电路,其提供对由像素阵列生成的数据的偏移控制;可以存储在用于控制黑钳位电路的存储器内的过程;电连接,其可以提供成像传感器和图像信号处理电路之间的电通信,图像信号处理电路可以远离内窥镜主体和控制单元内的成像传感器设置。

[0100] 环境光线不足的环境中用于数字成像的系统实施例可以包括:成像传感器,其用于感测电磁辐射,其中所述成像传感器可进一步包括:像素阵列,其具有有源像素及光学黑色像素以纠错来自所述像素阵列的输出;其中光学黑色像素可被组织在与像素阵列内有源像素邻近的列中;传递端口,其用于传递由像素阵列生成的数据;数字转换器,其转换模拟像素抽样成数字数值;黑钳位电路,其提供对由像素阵列生成的数据的偏移控制;可以存储在用于控制黑钳位电路的系统的存储器内的过程;内窥镜,其用于接近环境光线不足的环境;手持件,其附接至所述内窥镜并且其中所述内窥镜可以由操作手持件而操作;控制单元,其包括处理器并且其中所述控制单元可以与成像传感器电通信;以及电连接手持件和控制单元的连接线缆。

[0101] 此外,本公开的教导和原理可以包括电磁能的任何和所有的波长,其包括可见光和非可见光光谱,例如红外(IR)、紫外线(UV)和X射线。

[0102] 前面的描述是为了说明和描述的目的而展示。其并不旨在详尽地或限制本公开至精确形式的公开。许多修改和变化根据上述教导是可能的。此外,应该指出的是,前述替换实施的任何或者全部可以用于所希望的任何组合以形成本公开的其它混合实施。

[0103] 此外,尽管本公开的具体实施已经描述和示出,但是本公开并不限制至所描述和示出的部件的具体形式或者布置。本公开的范围可以由此处所附上的权利要求、此处和不同申请中递交的任何其它权利要求及其等同物而限定。

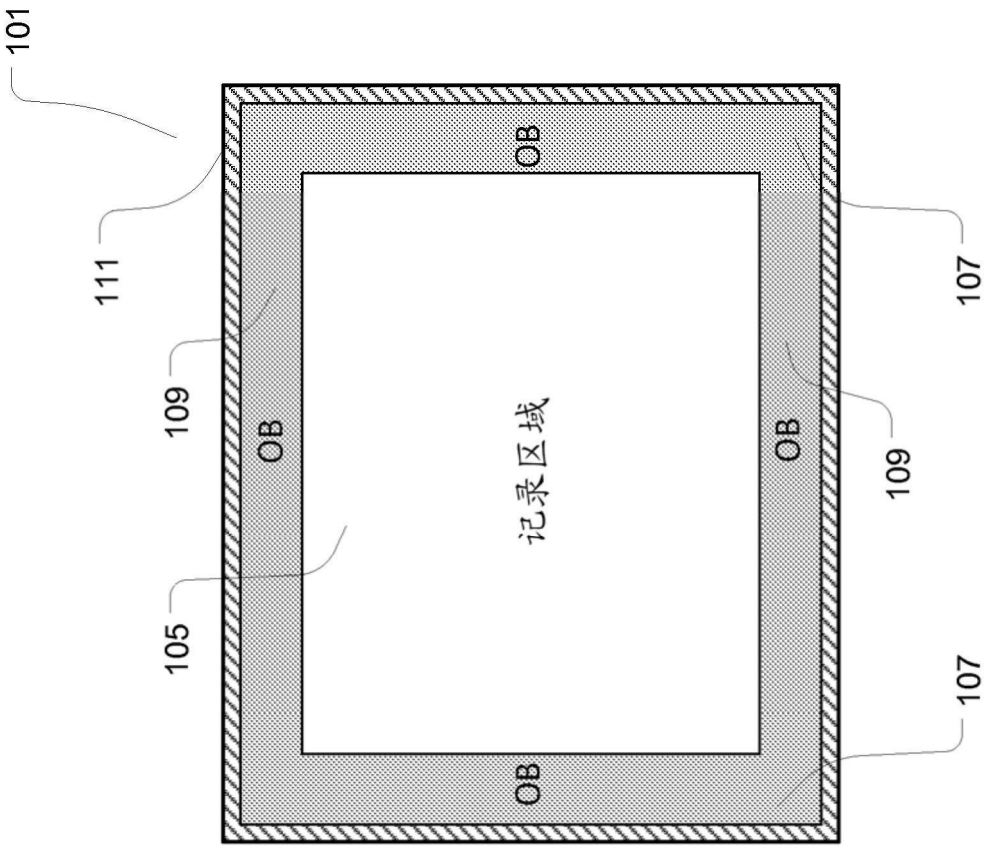


图 1A

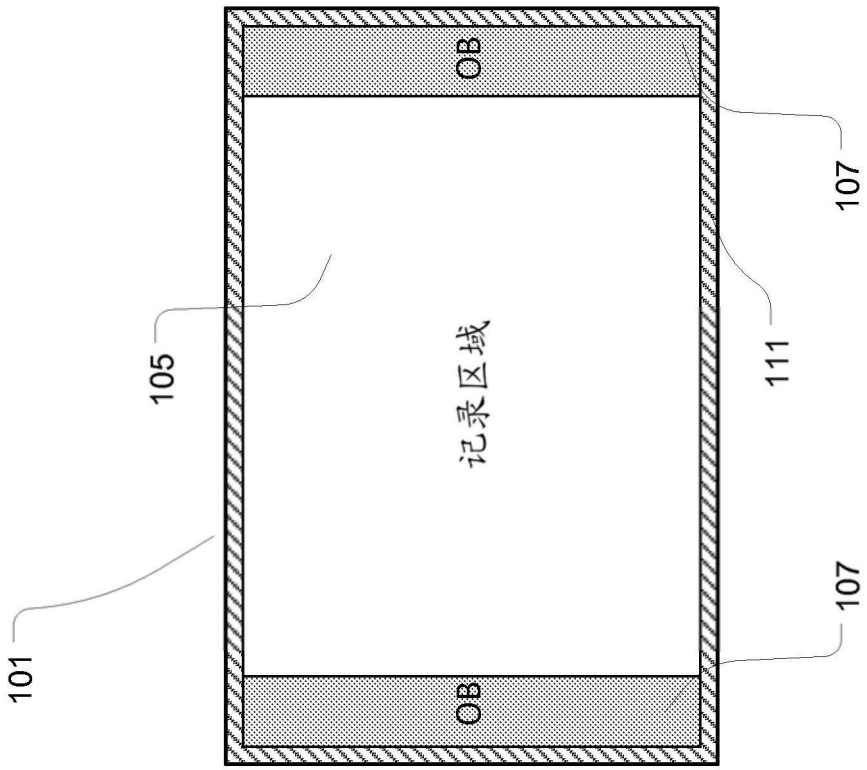


图 1B

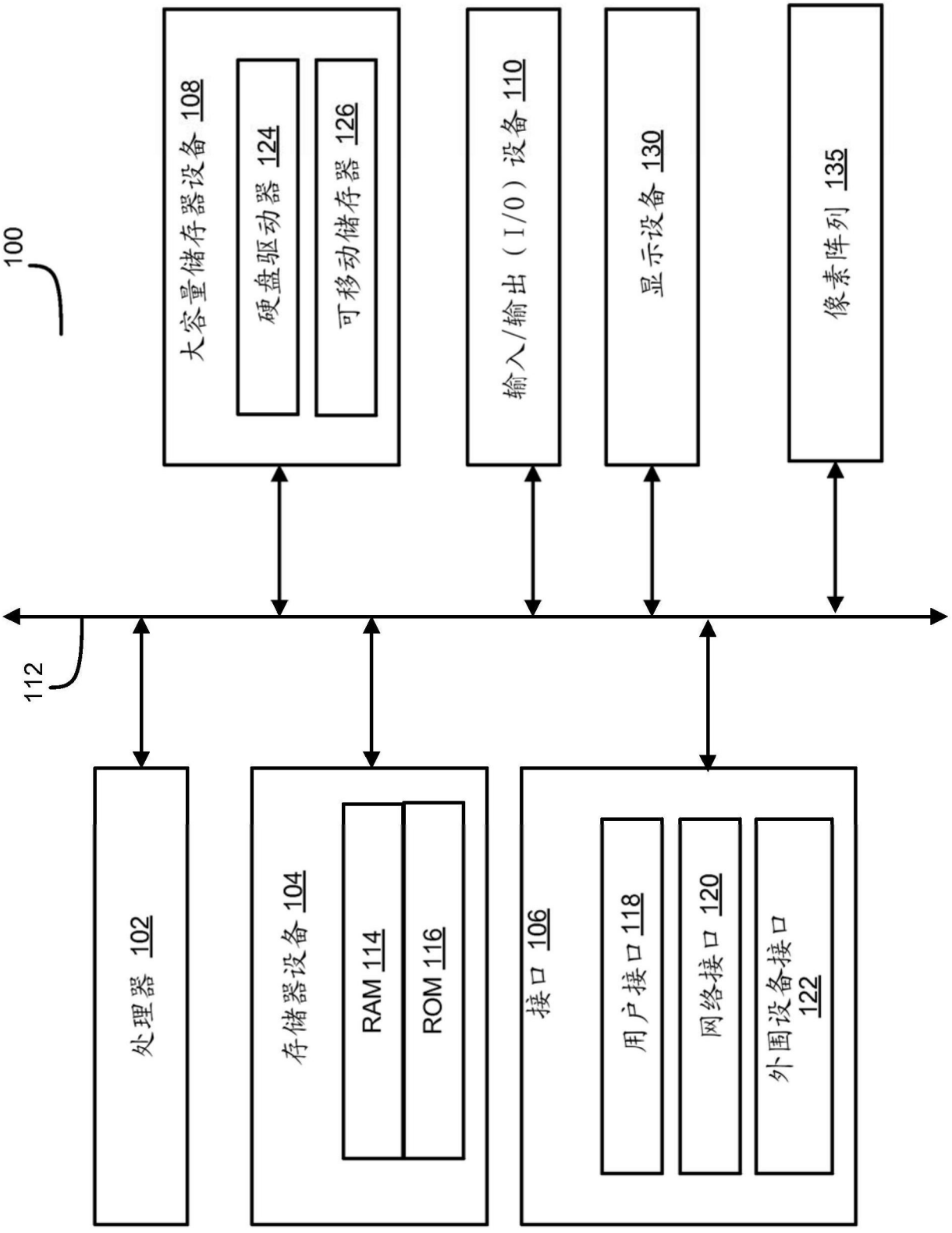

100
大容量储存器设备 108
硬盘驱动器 124
可移动储存器 126
输入/输出（I/O）设备 110
显示设备 130
像素阵列 135
112
处理器 102
存储器设备 104
RAM 114
ROM 116
接口 106
用户接口 118
网络接口 120
外围设备接口 122

图 1C

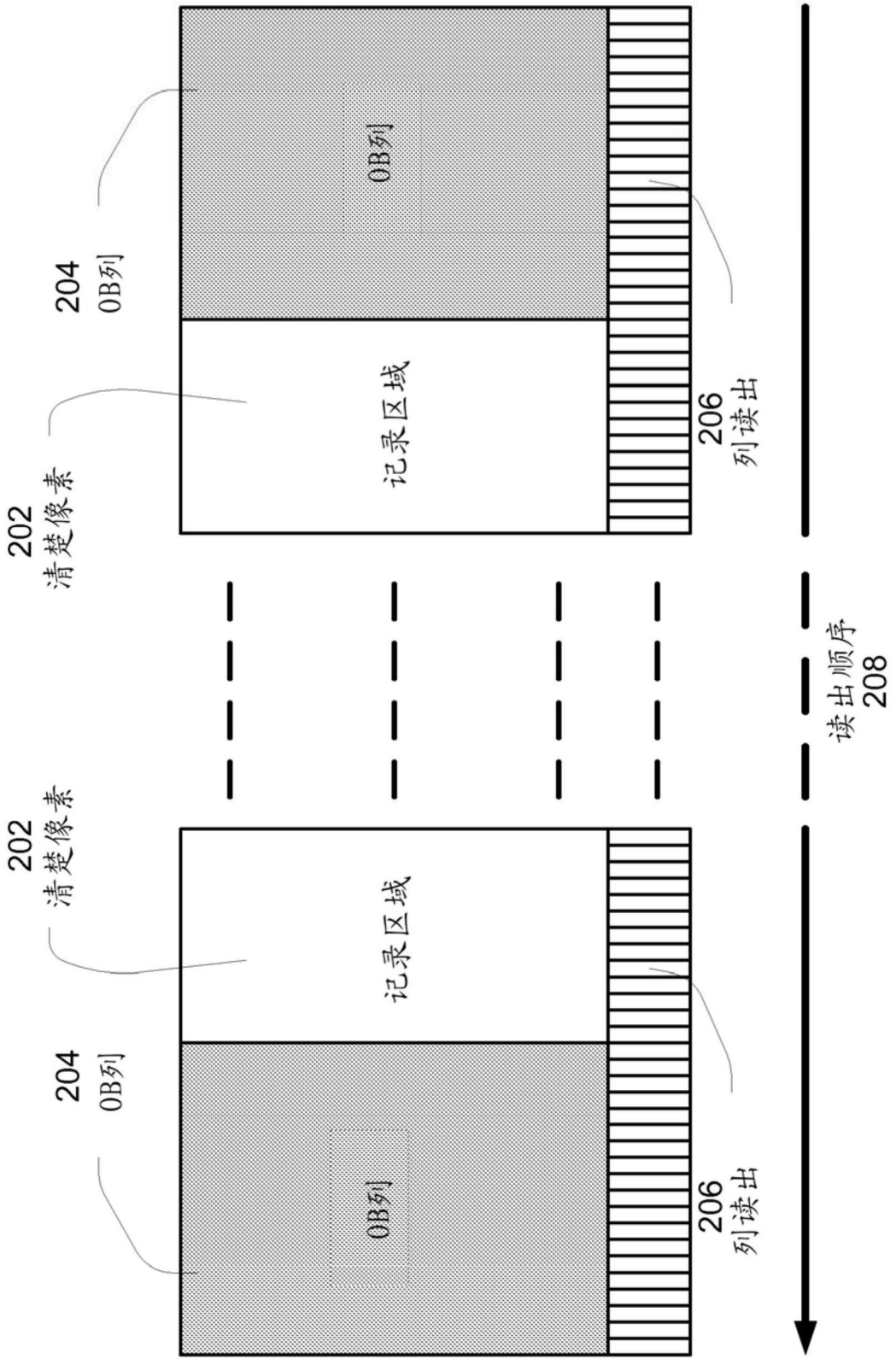


图 2

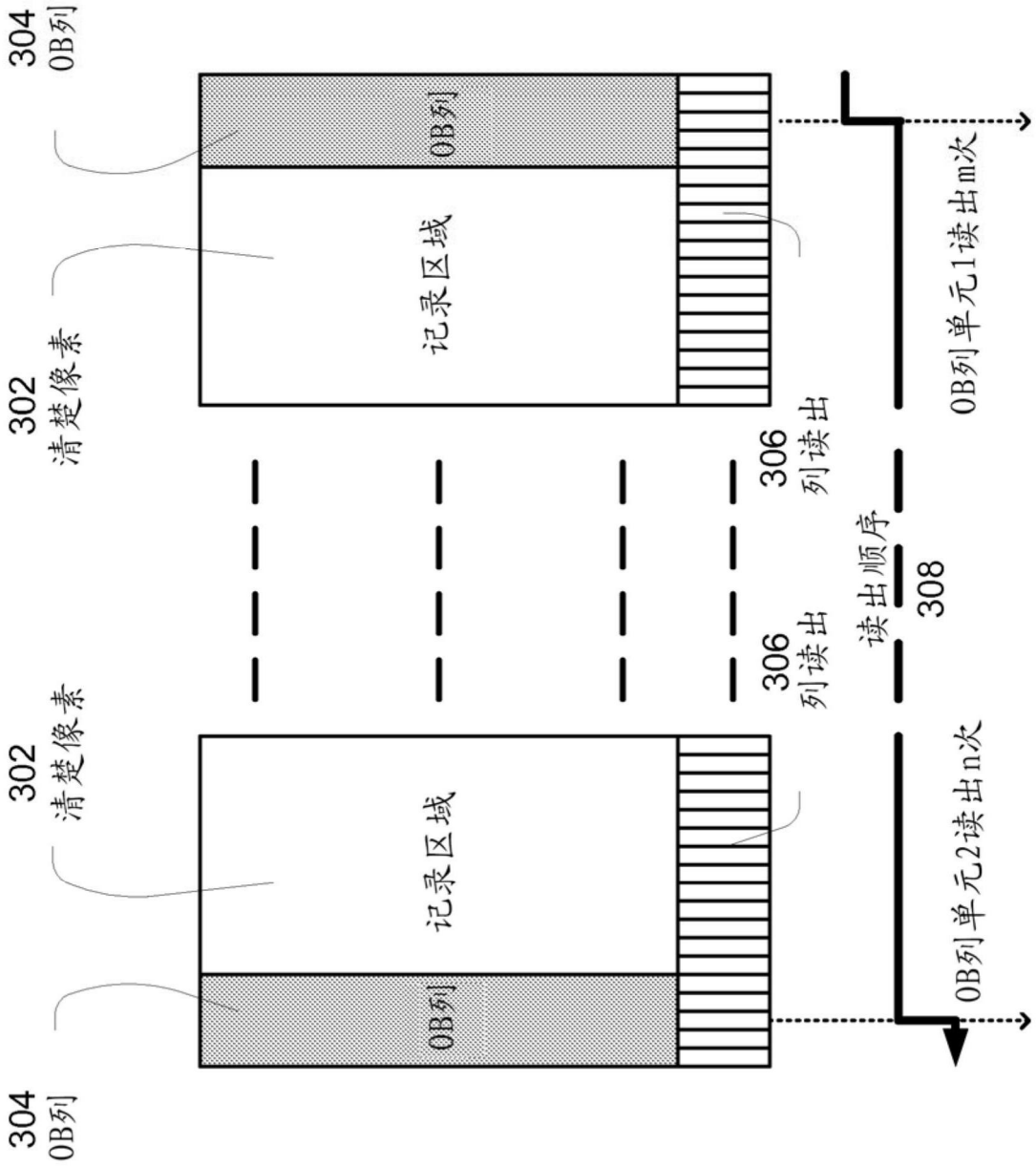

304
OB列
302
清楚像素
记录区域
OB列
306
列读出
读出顺序
308
OB列单元1读出m次
OB列单元2读出n次

图 3

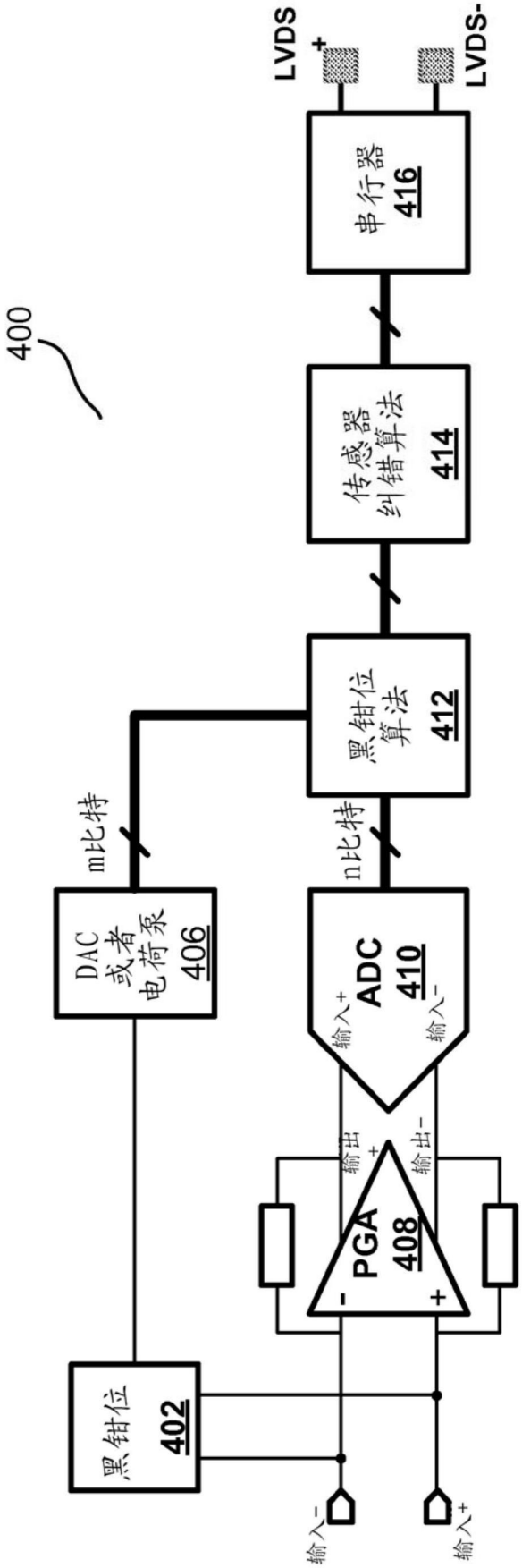

400
LVDS+
LVDS-
串行器
416
传感器
纠错算法
414
黑钳位
算法
412
m比特
n比特
DAC
或者
电荷泵
406
ADC
410
输入+
输入-
输出+
输出-
PGA
408
黑钳位
402
输入-
输入+

图 4

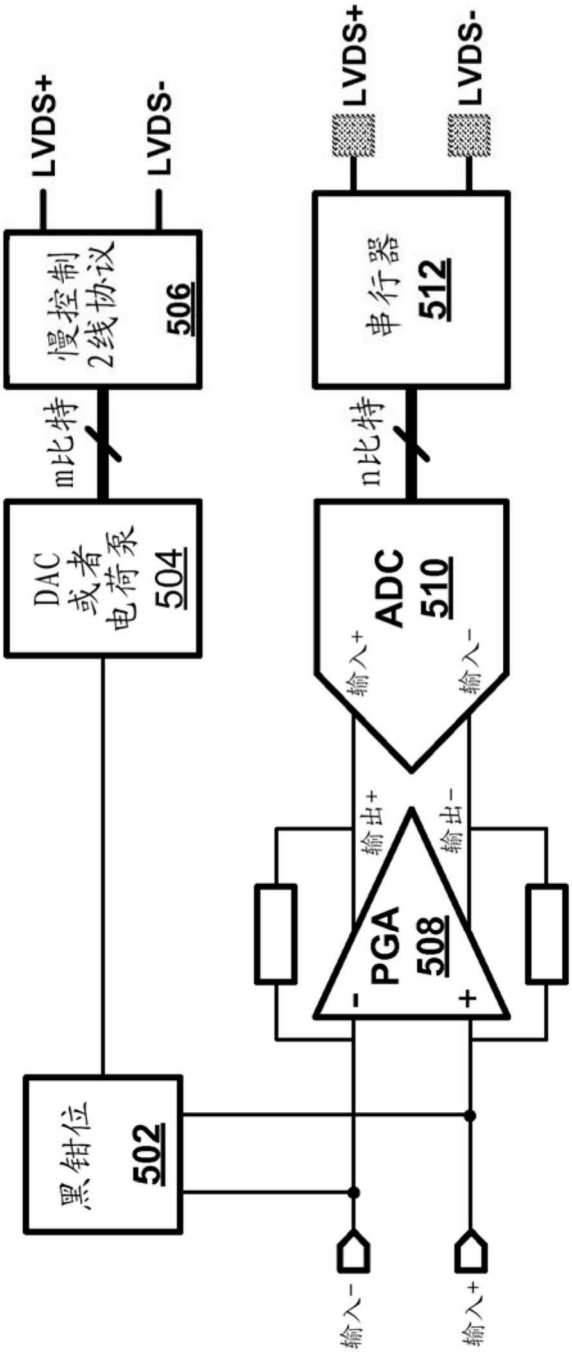

LVDS+
LVDS-
慢控制
2线协议
506
m比特
DAC
或者
电荷泵
504
黑钳位
502
LVDS+
LVDS-
串行器
512
n比特
ADC
510
输入+
输入-
输出+
输出-
PGA
508
输入-
输入+

图 5

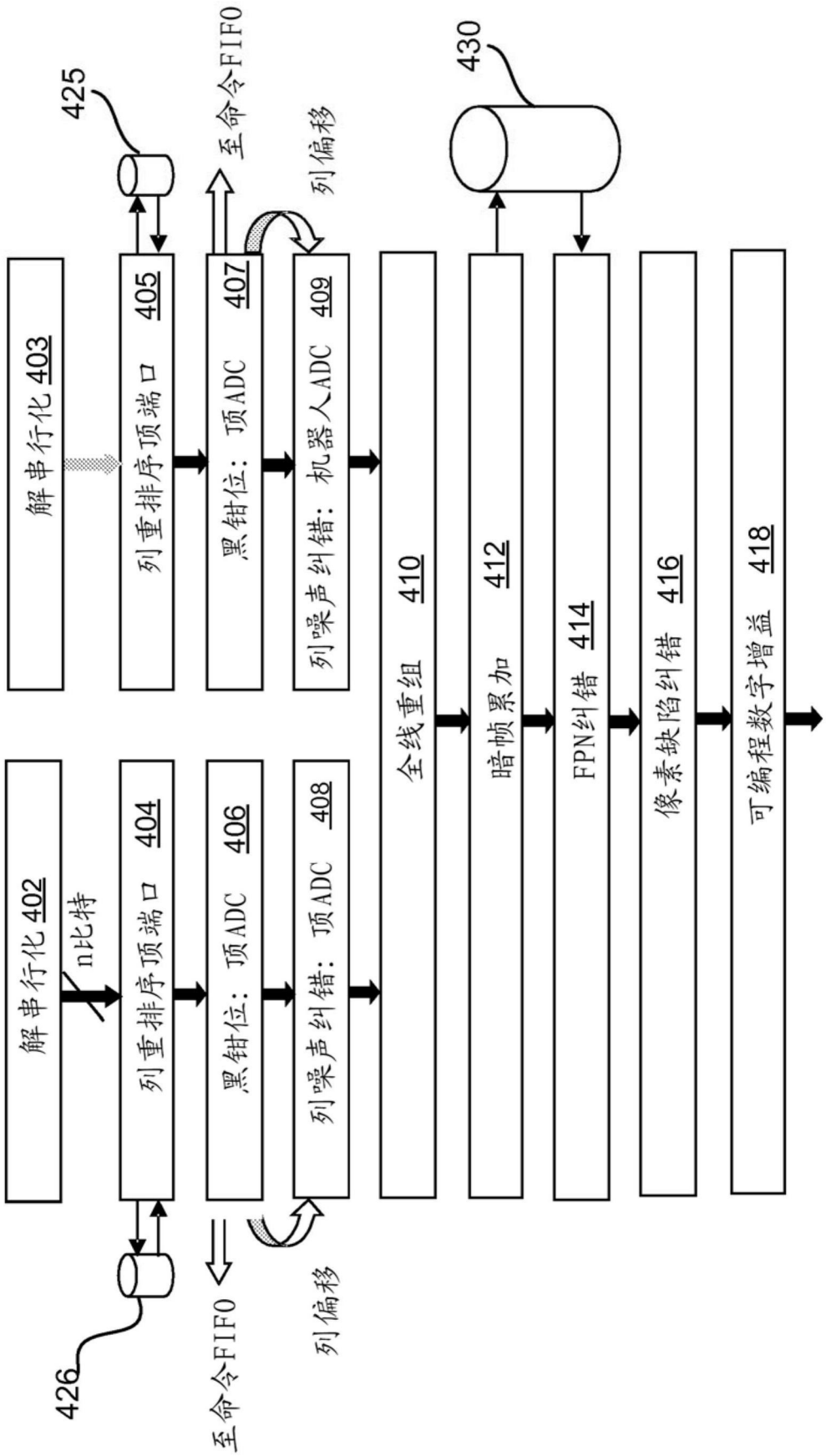

解串行化 402
n比特
列重排序顶端口 404
黑钳位：顶ADC 406
列噪声纠错：顶ADC 408
全线重组 410
暗帧累加 412
FPN纠错 414
像素缺陷纠错 416
可编程数字增益 418
426
至命令FIFO
列偏移
解串行化 403
列重排序顶端口 405
黑钳位：顶ADC 407
列噪声纠错：机器人ADC 409
425
至命令FIFO
列偏移
430

图 6

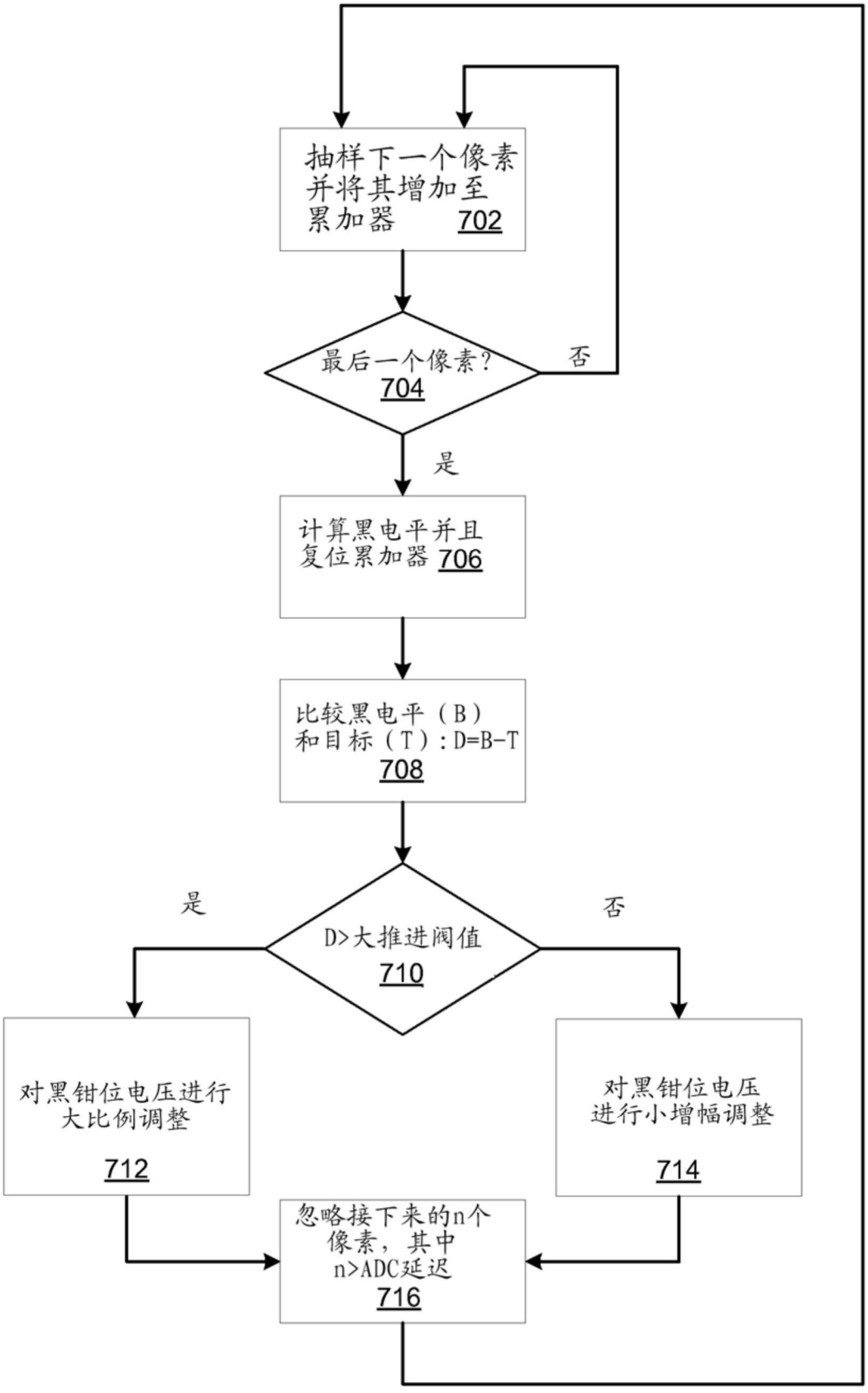

抽样下一个像素并将其增加至累加器 702
最后一个像素? 704
否
是
计算黑电平并且复位累加器 706
比较黑电平（B）和目标（T）：D=B-T 708
是
D>大推进阀值 710
否
对黑钳位电压进行大比例调整 712
对黑钳位电压进行小增幅调整 714
忽略接下来的n个像素，其中n>ADC延迟 716

图 7

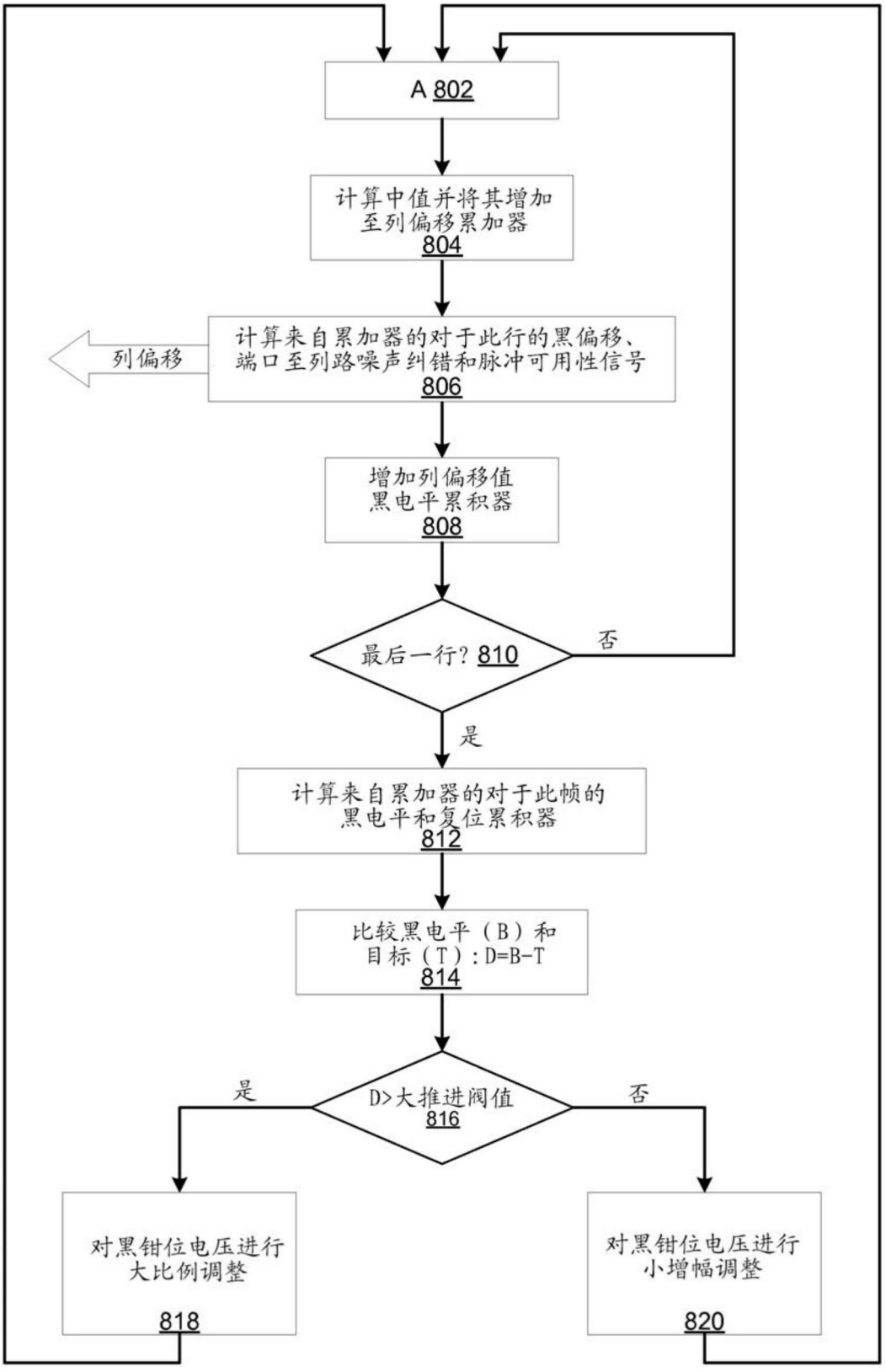

A 802
计算中值并将其增加至列偏移累加器 804
计算来自累加器的对于此行的黑偏移、端口至列路噪声纠错和脉冲可用性信号 806
列偏移
增加列偏移值黑电平累积器 808
最后一行? 810
否
是
计算来自累加器的对于此帧的黑电平和复位累积器 812
比较黑电平（B）和目标（T）：D=B-T 814
D>大推进阀值 816
是
否
对黑钳位电压进行大比例调整 818
对黑钳位电压进行小增幅调整 820

图 8A

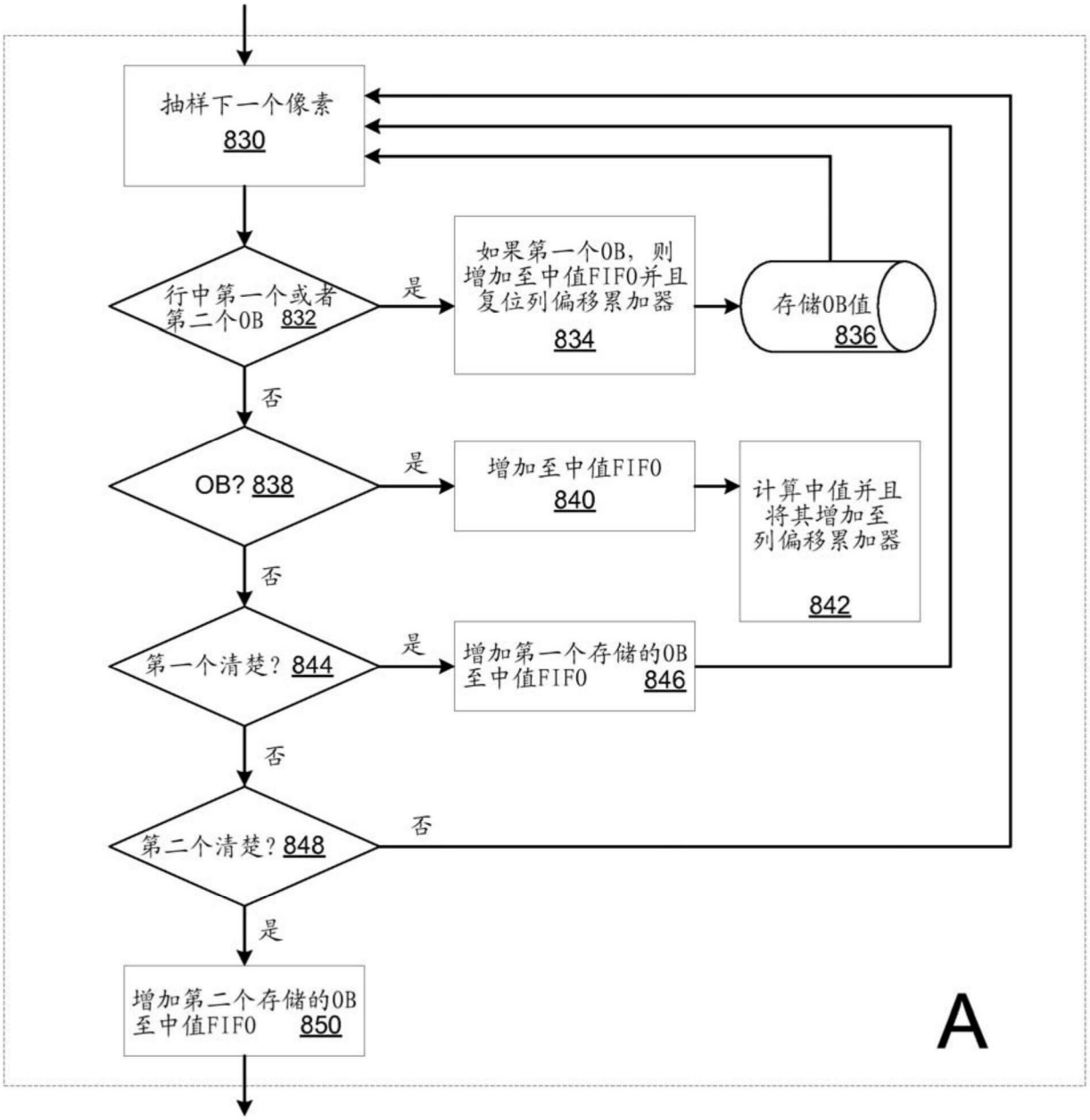

抽样下一个像素
830
行中第一个或者第二个OB 832
是
如果第一个OB，则增加至中值FIFO并且复位列偏移累加器
834
存储OB值
836
否
OB? 838
是
增加至中值FIFO
840
计算中值并且将其增加至列偏移累加器
842
否
第一个清楚？844
是
增加第一个存储的OB至中值FIFO 846
否
第二个清楚？848
否
是
增加第二个存储的OB至中值FIFO 850
A

图 8B

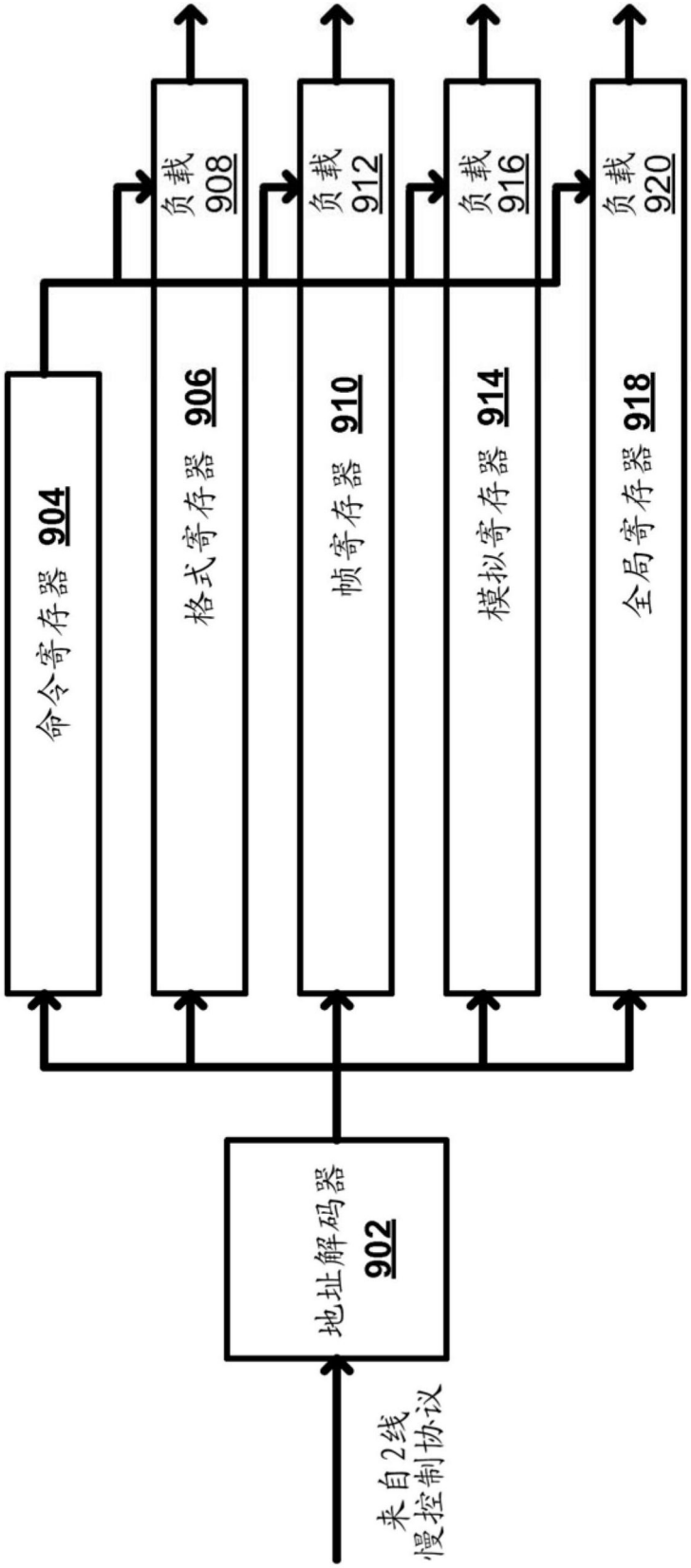

来自2线
慢控制协议
地址解码器
902
命令寄存器 904
格式寄存器 906
帧寄存器 910
模拟寄存器 914
全局寄存器 918
负载
908
负载
912
负载
916
负载
920

图 9

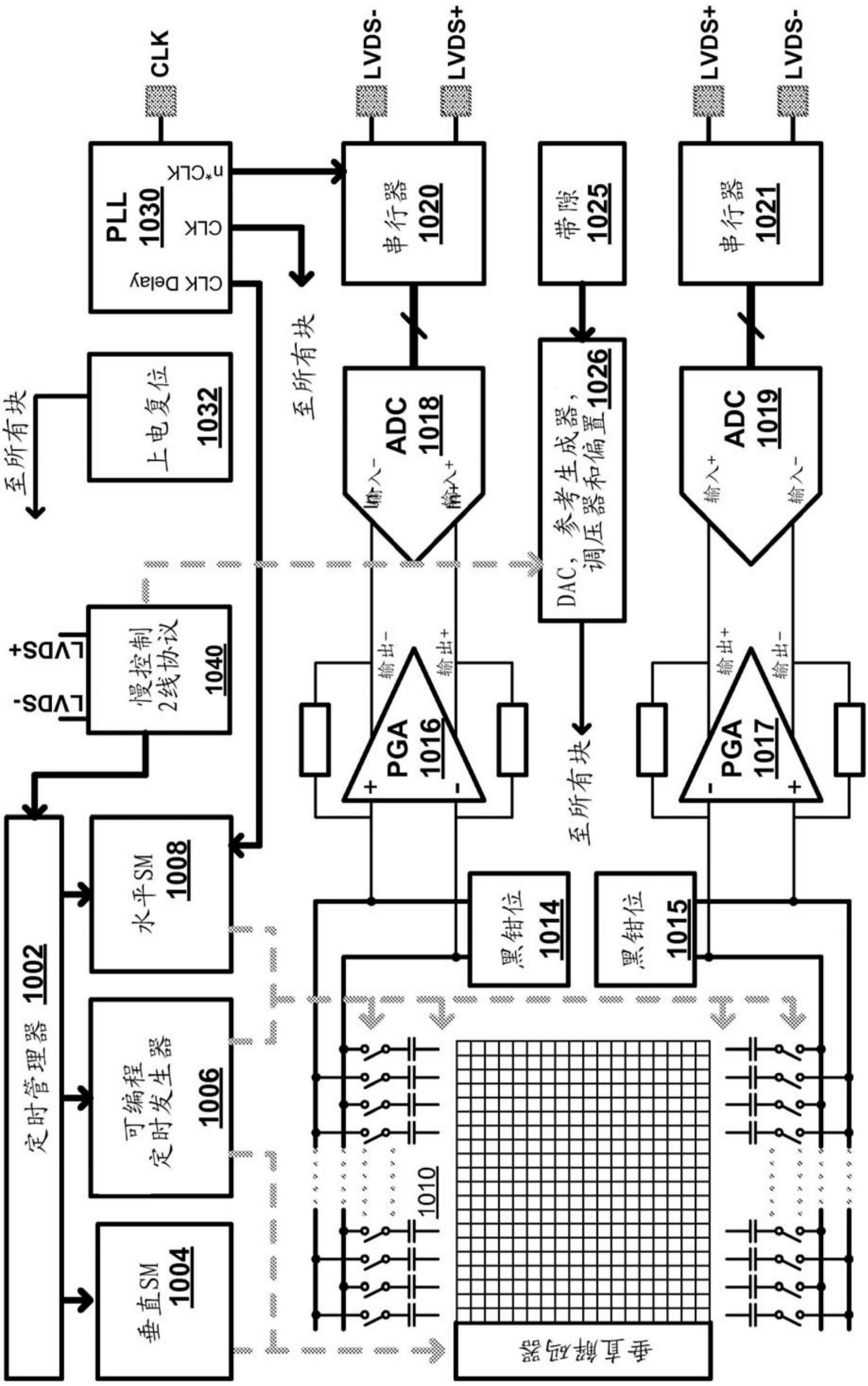

CLK
LVDS-
LVDS+
LVDS+
LVDS-
PLL 1030
n*CLK
CLK
CLK Delay
串行器 1020
带隙 1025
串行器 1021
至所有块
至所有块
上电复位 1032
至所有块
ADC 1018
输入-
输入+
DAC，参考生成器，调压器和偏置 1026
ADC 1019
输入+
输入-
慢控制 2线协议 1040
LVDS+
LVDS-
输出-
输出+
PGA 1016
+
-
输出+
输出-
PGA 1017
-
+
至所有块
定时管理器 1002
水平SM 1008
黑钳位 1014
黑钳位 1015
可编程 定时发生器 1006
1010
垂直SM 1004
垂直解码器

图 10

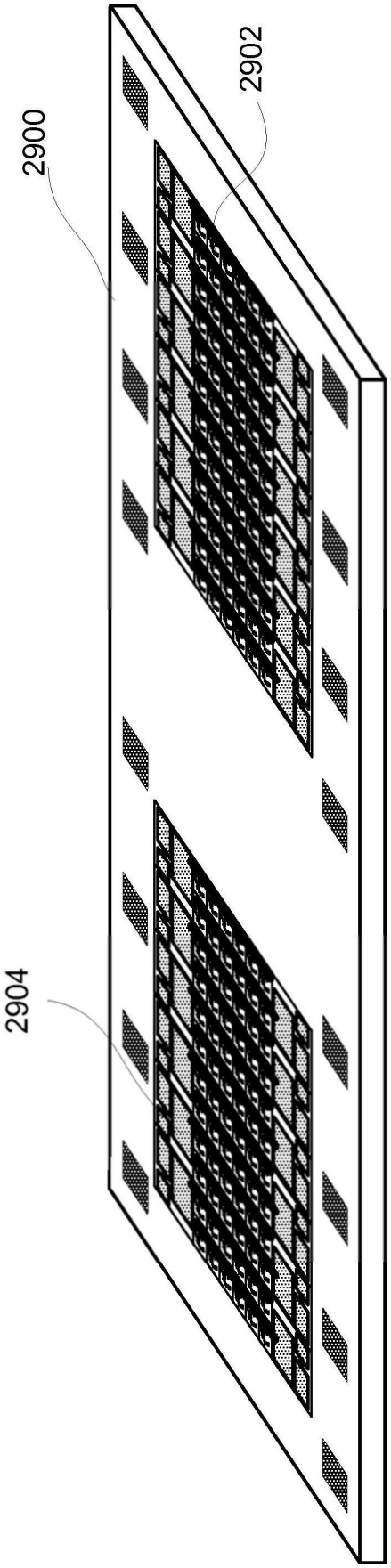


图 11A

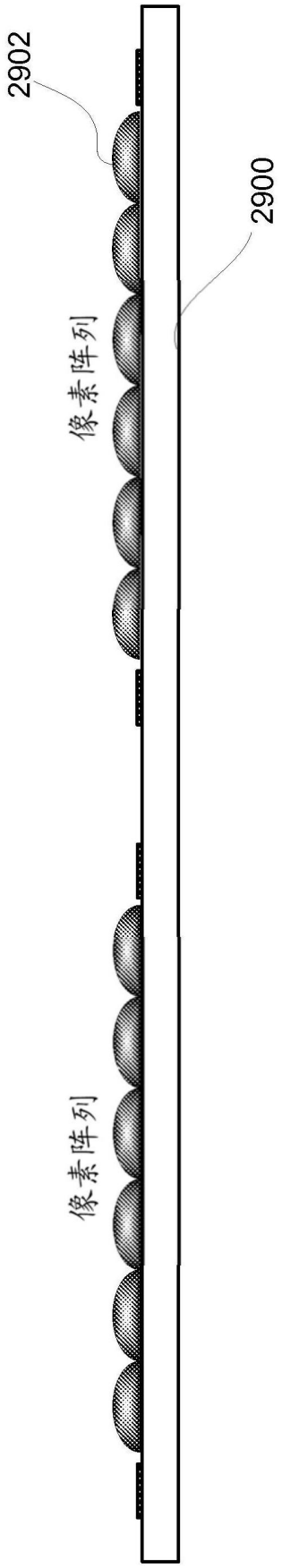


图 11B

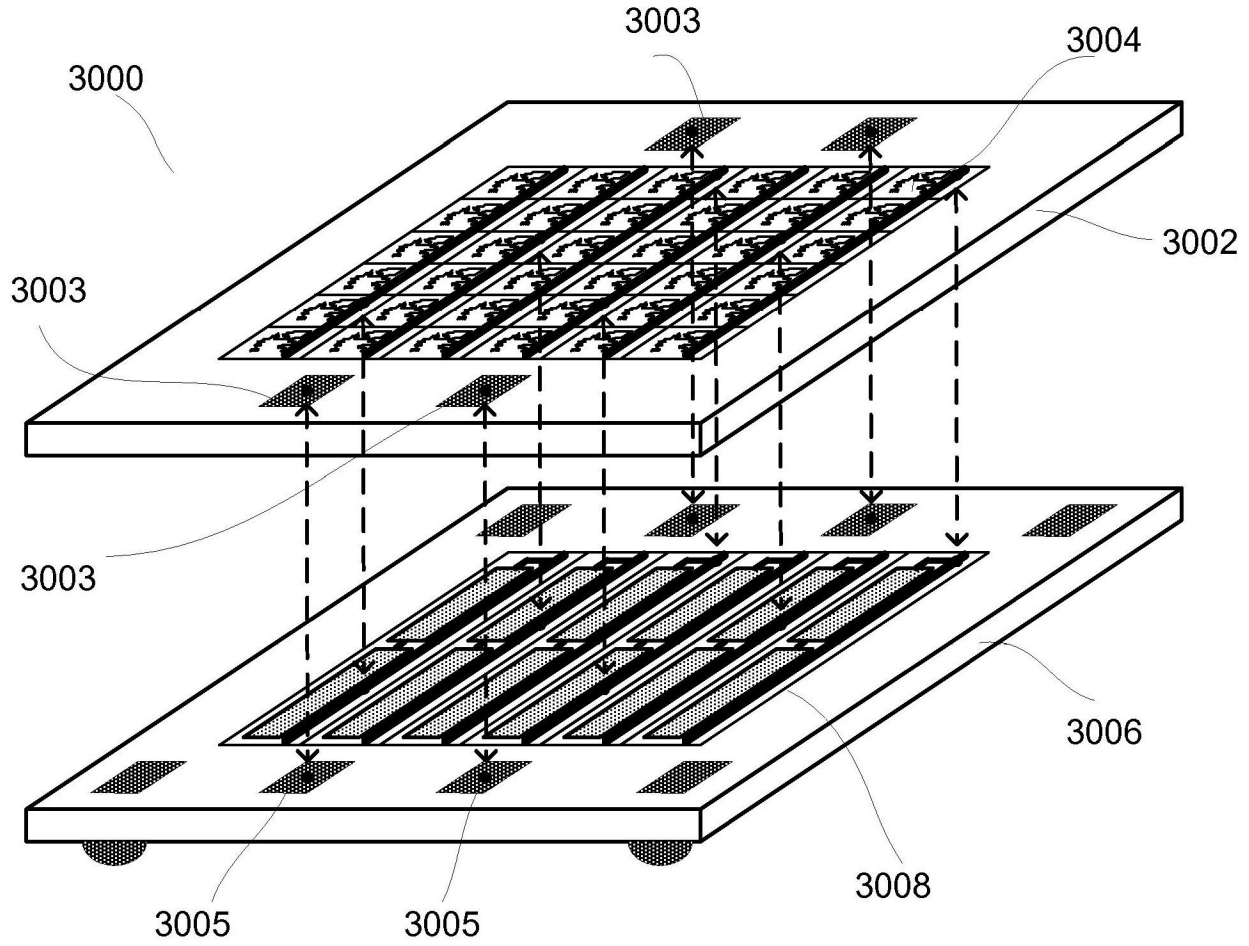

3003
3004
3000
3002
3003
3003
3006
3008
3005
3005

图 12A

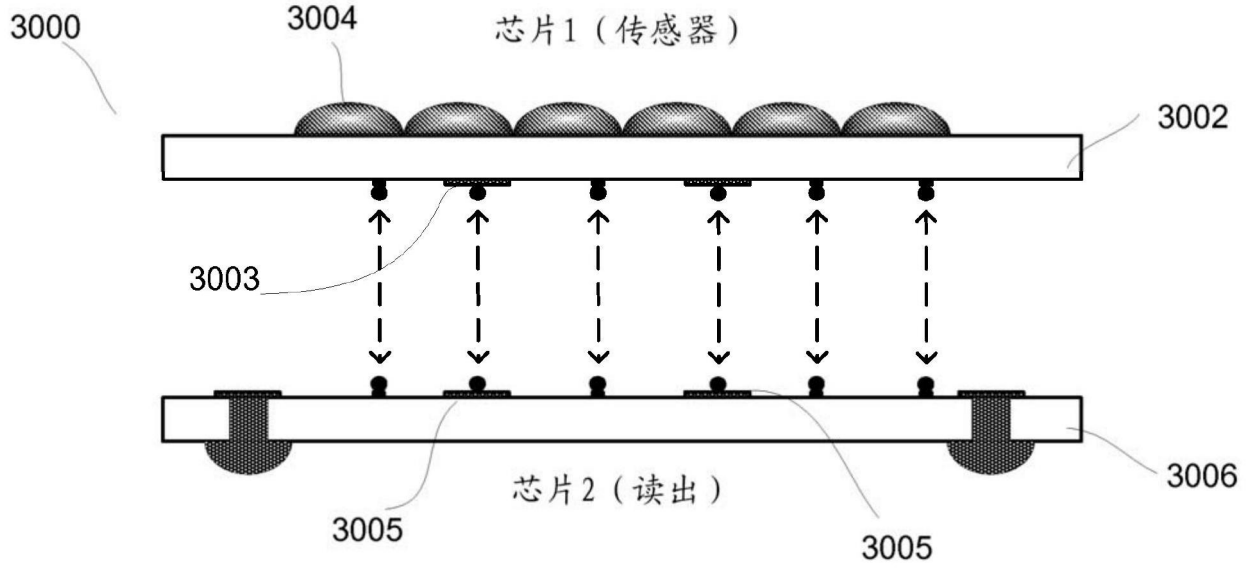

3000
3004
芯片1（传感器）
3002
3003
3006
芯片2（读出）
3005
3005

图 12B

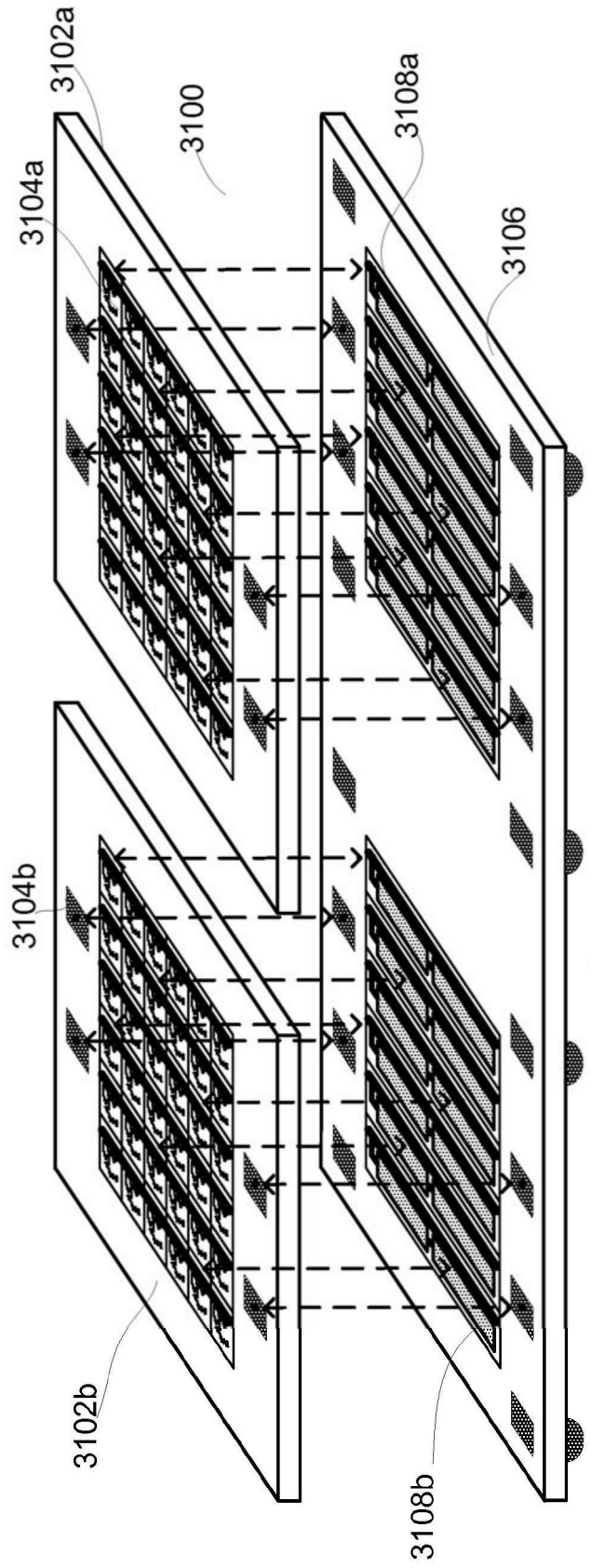

3102a
3100
3108a
3104a
3106
3104b
3102b
3108b

图 13A

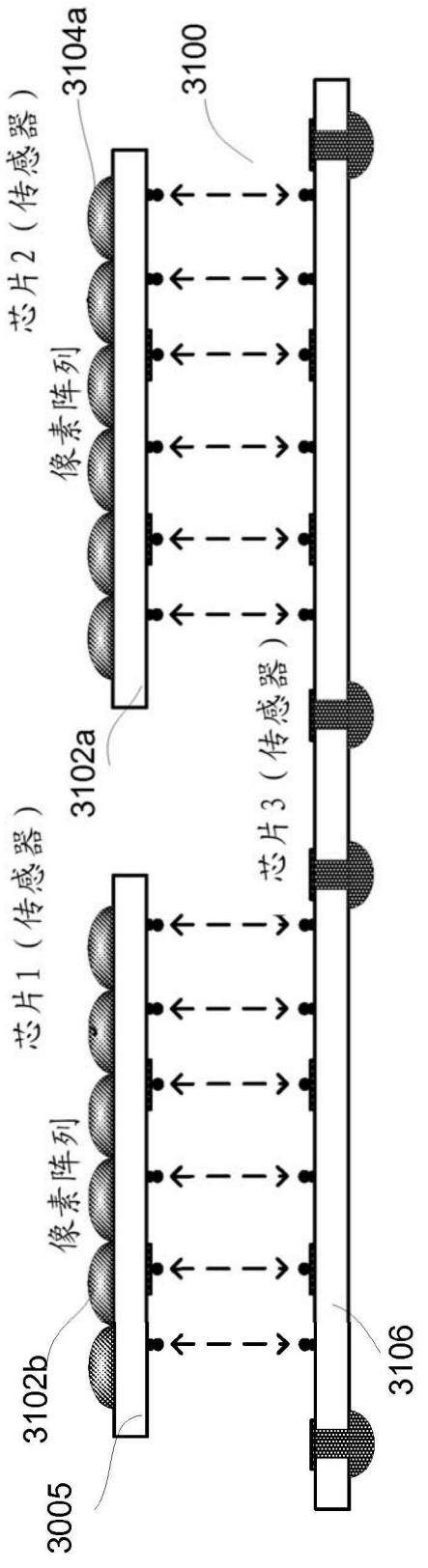

3104a
3100
芯片 2（传感器）
像素阵列
3102a
芯片 3（传感器）
芯片 1（传感器）
像素阵列
3102b
3005
3106

图 13B

Abstract

The disclosure extends to methods, systems, and computer program products for digitally imaging with area limited image sensors, such as within a lumen of an endoscope.