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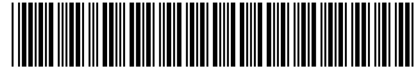

(11) **EP 1 956 612 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
31.12.2014 Bulletin 2015/01

(51) Int Cl.:
H01C 7/10 *(2006.01)*

(21) Application number: **07102045.7**

(22) Date of filing: **09.02.2007**

(54) **Ceramic material used for protection against electrical overstress and low-capacitance multilayer chip varistor using the same**

Keramikmaterial zur Verwendung als Schutz gegen elektrische Überspannung und Mehrschicht-Chip-Varistor mit niedriger Kapazität umfassend dieses Keramikmaterial

Matériau céramique utilisé pour la protection contre les surcharges électriques et varistance à puce multicouche à faible capacité l'utilisant

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR

(43) Date of publication of application:
13.08.2008 Bulletin 2008/33

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Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The invention relates to a porous ceramic material for protection against electrical overstress and being applied among positive and negative electrodes for suppressing transient surge voltage and electrostatic shock. Further, the invention relates to a low-capacitance multilayer chip varistor.

2. Description of the Related Art

[0002] The trend in electronic industry is towards higher working frequencies and smaller sizes. Therefore, the need of using varistors for protecting IC from damage due to electrical overstress is getting greater for high frequency application.

[0003] Conventional varistor is mainly composed of ZnO or $SrTiO_3$, and completed by sintering after oxides are added. Take ZnO varistor as an example, it is composed of ZnO and oxides of Bi, Sb, Si, Co, Mn, Cr and so on. At the high temperature more than 1000°C, Bi_2O_3 and oxides of Co, Mn, Cr and so on form a grain boundary among ZnO particles which has a microstructure like a grain boundary barrier capacitor. Thus, varistor composed of such materials has higher capacitance ranging from tens of pF to thousands of pF. Even the above materials are used in multilayer chip varistor, the varistor capacitance ranges from about 3pF to hundreds of pF at 1MHz. In circuits for high frequencies, when capacitance of the component for providing protection exceeds 3pF, signals will distort. Therefore, the above component for providing protection is not suitable for high frequencies circuits.

[0004] Similarly, varistor component composed of $SrTiO_3$ has capacitance more than thousands of pF and is not suitable for circuits for high frequencies. In addition, when the transmission frequency is higher, the capacitance should be lower to prevent the signals from distortion.

[0005] U.S. Pat. No. 5,976,420 disclosed a chip type multilayer varistor having a low capacitance and high non-linearity coefficient, mainly composed of SiC containing at least two oxides selected from among SiO_2, Bi_2O_3, PbO, B_2O_3 and ZnO in an amount of from 0.1 to 20 mol %, and then combined with toluene and a binder agent and mixed by using a ball mill to obtain slurries, and thereafter become ceramic green sheets by using a doctor blade process. A paste was printed on the surface of the green sheets to form an inner electrode thereon. A predetermined number of ceramic green sheets were stacked to form a layered body. The resultant layered body was bonded by pressing at a constant pressure. The resultant green compact was cut into small-sized chips. The green chip was baked at a temperature in the range from 700 to 1100°C to complete a ceramic multilayer chip type varistor resisting electrostatic shock and having surge voltage suppressing capability and a high non-linear coefficient from 10 to 20. The chip has a capacitance in the range from 10 to 40pF, though not quite high, being much greater than 3pF, and thus not suitable for using in high frequency circuits.

[0006] U.S. Pat. No. 6,251,513 disclosed a component for providing protection. Materials of the component comprise conductive and semi-conductive particles having a particle size of less than 10μm and they are mixed with a polymer insulating binder to become a paste-like material. Left and right conductive electrodes are printed on a same surface of an insulating substrate and the paste-like material is filled in the gap between two conductive electrodes and then baked. Although the capacitance thereof is low and smaller than 0.25pF at 1MHz, the component is suitable for providing protection for high frequencies circuits. The insulating material is composed of polymer material, it is meant that heat generated by electrostatic shock or surge electrical overstress will carbonize the polymer material, make the component to be conductive and lose protection effect for electronic circuits or components. Thus, this component will not have good electrostatic shock withstanding capability and the lifetime thereof is short. Failure will occur only after 500 times of electrostatic shock when static electricity of direct contact 8KV is applied.

[0007] U.S. Pat. No. 3,725,836 disclosed a varistor material consisting essentially of 30 to 95 wt-% of finely divided doped zinc oxide dispersed in 5 to 70 wt-% of glass frit.

SUMMARY OF THE INVENTION

[0008] The objective of the present invention is to improve electrostatic shock withstanding capability and lifetime of a low-capacitance multilayer chip varistor.

[0009] This is achieved by means of a porous ceramic material according to claim 1 and a low-capacitance multilayer chip varistor according to claim 5. Advantageous embodiments are laid down in further claims.

[0010] The new material allows to provide a varistor having capacitance smaller than 0.5pF at 1MHz. The varistor has surge withstanding capability and a protection effect against static electricity, and more particularly, has a characteristic

of resisting more than thousands of times of 8KV electrostatic shock, and maintains original function after thousands times of electrostatic shock. The Varistor also has alow-breakdown-voltage. The trigger voltage of the varistor can be controlled by thickness of ceramic green sheets, sintering temperature of ceramic compact, glass layer thickness of grain boundary, size of conductive or semi-conductive particles and the quantity added of conductive or semi-conductive particles of nanometer sizes for secondary dispersion.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

FIG. 1 is a schematic figure of the low-capacitance multilayer chip varistor in one preferred embodiment of the present invention.
FIG. 2 is a schematic microstructure of the ceramic body of the low-capacitance multilayer chip varistor in the A area of the FIG 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0012] As shown in FIG. 1, a low-capacitance multilayer chip varistor 10 in one preferred embodiment of the present invention is made by multilayer technology process. The varistor 10 is made by multilayer ceramic processes comprising high-temperature sintering and so on, and comprises a ceramic main body 11, outer electrodes 13 disposed at two ends of the ceramic main body 11 and inner electrodes 12 disposed therein.

[0013] The ceramic main body 11 is made by a protective material against electrical overstress with tiny holes 17, e.g. pores, and the microstructure thereof is shown in FIG. 2, which has high proportion of holes 17. The material of this specimen comprises inorganic glass of 3~50wt% and semi-conductive or conductive particles 14 of 50~97wt% with a particle size of more than 0.1μm. A layer of inorganic glass film 15 that resists high temperature covers the surface of semi-conductive or conductive particles 14.

[0014] The inorganic glass film 15 further comprises of the submicron or nanometer of semi-conductive or conductive particles 16, which is smaller than 1 micron for secondary dispersion. The quantity contained of semi-conductive or conductive particles is less than 20wt% of that of inorganic glass.

[0015] According to the low-capacitance multilayer chip varistor 10 in the preferred embodiment of the present invention, the microstructure of the ceramic body 11 has high proportion of holes 17 and low capacitance, which is less than 0.5pF at 1MHz.

[0016] In addition, according to the low-capacitance multilayer chip varistor 10 in the preferred embodiment of the present invention, the inorganic glass film 15 that resists high temperature exists among the semi-conductive or conductive particles 14 of the ceramic main body 11 for resisting heat generated when suppressing electrostatic shock or surge electrical overstress. Most of all, the inorganic glass film 15 comprises semi-conductive or conductive particles 16 of 0.1 micron or nanometer for secondary dispersion, and the gap among the particles 16 is quite small, so that when abnormal electrical overstress occurs the tunnel effect will occur. Consequently, the low-capacitance multilayer chip varistor 10 disclosed in the present invention suppresses electrical overstress, resists electrostatic shock and has a long lifetime.

[0017] The process of making the low-capacitance multilayer chip varistor 10 according to one preferred embodiment of the invention comprises steps of:

(1) Using a solution composed of glass component and made by sol-gel process,
wherein the glass component comprises silicate glass, aluminosilicate glass, borate glass, phosphate glass, plumbate glass and so on, to disperse the nano-metal particles or semi-conductive particles uniformly into the solution composed of the glass component. The nano-particles have particle sizes smaller than 1000 nanometer, and comprise metal conductive particles comprising Pt, Pd, Au, Ag, Ni, Cu and so on, or semi-conductive particles comprising SiC, ZnO, TiO_2, SnO_2, $SrTiO_3$, $BaTiO_3$ and so on.
(2) Mixing semi-conductive or conductive particles uniformly into the above-mentioned solution with metal or semi-conductive nanoparticles dispersed therein, and milling them into composite material after drying and calcining at proper temperature (lower than 1000°C). Semi-conductive or conductive particle sizes are of submicron or micron that is larger than 0.1μm. The conductive particles comprise Pt, Pd, Au, Ag, Ni, Cu and so on; while the semi-conductive particles comprise SiC, ZnO, TiO_2, SnO_2, $SrTiO_3$, $BaTiO_3$ and so on, or particles of above-mentioned semi-conductive particles.
(3) Using conventional multilayer technique to obtain slurries by adding a binder agent into the above-mentioned composite material, a doctor blade process used for becoming ceramic green sheets of thickness of 10~50μm. Then, use multilayer chip process to print two or more than two layers of staggered inner electrodes. The inner electrodes comprise metals comprising Pt, Pd, Au, Ag, Ni and so on. After laminating with the upper and lower cover

layer and cutting, sintering is done at 700~1200°C. Two ends of the component are attached with silver plaste to be sintered to become external electrodes. Then, low-capacitance multilayer chip varistor suppressing static electricity and surge is completed. Besides, materials of the external electrode comprise Ag, Cu, Ag-Pd alloy and so on.

[0018] The low-capacitance multilayer chip varistor in the preferred embodiment of the invention made by above processes has advantages of low capacitance, low breakdown voltage and so on, and suppresses thousands of times of 8KV electrostatic shock, while the capacitance thereof is smaller than 0.5pF and thus can be used to protect electronic circuits for high frequencies.

Preferred Embodiments

[0019] The following paragraphs will describe some preferred embodiments of the low-capacitance multilayer chip varistor according to the present invention, wherein the varistor has characteristics of 0.5pF capacitance at 1MHz, suppressing thousands of times of 8KV electrostatic shock, suppressing electrical overstress, suppressing electrostatic shock and protecting electronic circuits for high frequencies.

[0020] In addition, following preferred embodiments will take multilayer chip varistor as an example. However, the process in the present invention can also be used to produce disc type varistor, or the material according to the present invention can be uses to be placed in between any two electrodes for suppressing transient surge voltage or electrostatic shock.

Example 1

[0021] SiC powder of particle size ranging from 0.1~20μm and nano-metal Pt of particle size ranging from 0.01~2μm are added into the gel-like solution composed of nano-silicate glass, which made by sol-gel process, and well stirred the previous mixed solution. Thus, the SiC powder uniformly surrounded a layer of organic film containing glass component. Eight samples with different solutions are obtained according to the weight proportion of the SiC powder, nano-Pt and glass as shown in following Table 1.

Table 1

Sample	SiC wt %	Pt particle wt %	Glass wt %
1	100	0	10
2	100	1	10
3	100	0	15
4	100	1	15
5	100	0	20
6	100	1	20
7	100	0	40
8	100	1	40

[0022] The mixed solutions as shown in Table 1 are dried to become powders and disposed in a calcining oven for being calcined at 700°C to become SiC powders coated with glass film.

[0023] The calcined powder is milled roughly and then finely, and a solution (such as toluene or butanol), a binder agent (such as polyvinyl butyral) and a dispersing agent are put together into a ball mill to be milled to obtain slurries. Then, it becomes ceramic green sheets of 30μm thickness by using a doctor blade process.

[0024] As shown in Table 1, eight sheets of these kinds are stacked and pressed to become lower covers with about 200μm thickness. After printing inner electrode on the lower covers and drying, a thin sheet with 30μm thickness is disposed and then inner electrode is printed again. This inner electrode and the inner electrode on the lower layer are connected to the right and left ends of the component in a stagger manner. Materials of the inner electrode comprise Pt, Ag, Pd or alloy of any two of these metals.

[0025] Eight sheets of these kinds are stacked and pressed to become upper covers with about 200μm thickness. Upper covers and above-mentioned lower covers with inner electrodes are stacked together and pressed, and then be cut into ceramic sheet chips of size of 1.2 mm * 0.6 mm * 0.6 mm. The ceramic sheet chips are disposed in a sintering oven for sintering, and the sintering temperature is about 800~1000°C. After sintering, the size of the chips is 1.0 mm *

0.5 mm * 0.5 mm. Two ends of the chips are soaked in outer electrodes which are heated to be attached thereon at 600~900°C, and then a low- low-capacitance, low-voltage and surge or static electricity suppressing multilayer chip varistor is completed.

[0026] The breakdown voltages of multilayer chip varistor and the breakdown voltages after 8KV electrostatic tests are shown in Table 2.

Table 2

Sample	Breakdown Voltage (V1mA)	Capacitance (pF at 1MHz)	Trigger Voltage (V)	Breakdown Voltage Variation After 1000 Times of Electrostatic Shock (%)
1	67	0.25	120	-23.0
2	54	0.28	110	-15.1
3	110	0.14	205	-9.0
4	75	0.12	154	-7.2
5	234	0.09	422	-7.5
6	137	0.08	257	-6.0
7	415	0.08	1032	-11.4
8	343	0.07	730	-8.6

[0027] As shown in Table 2, the more glass is contained, the high breakdown voltage and the less capacitance. This phenomenon is related to the high resistance of the glass. When the glass contained is more, the grain boundary insulating layer is thicker, and thus the multilayer chip varistor has higher breakdown voltage and smaller capacitance.

[0028] In addition, when the weight proportion of SiC to glass is from 100:15 to 100:20, the multilayer chip varistor has preferred electro-static discharge (ESD) suppressing capability. When the glass contained is less, the insulating resistance will be not enough, and the variation of breakdown voltage at 1mA will be larger than 10% for the multilayer chip varistor after ESD. Thus, the electrical characteristics are better when the glass contained is more than 15wt%. However, when the glass contained is more than 20wt%, because the grain boundary is thicker, the breakdown voltage and trigger voltage will be too high (the trigger voltage is more than 800V) and not suitable as protective component. Therefore, the quantity of glass addition is preferred to be controlled between 15wt% to 20wt%.

[0029] As shown in Table 2, no matter what proportion of SiC to glass added is, the nano-metal particles added have effects of lowering trigger voltages and improving variation of breakdown voltage after electrostatic shock; however, the capacitance is relatively higher.

[0030] As shown in Table 2, when the glass contained is from 10wt% to 40wt%, the capacitance of each multilayer chip varistor is small and less than 0.5pF.

Example 2

[0031] Oxides such as ZnO powder, Bi_2O_3, CoO and so on of particle size ranging from 0.1~20μm and nano-metal Pd of particle size ranging from 0.01~2μm are added into the gel-like solution composed of nano-silicate glass, which made by sol-gel process, well stirred the previous mixed solution. Thus, the SiC powder uniformly surrounded a layer of organic film containing glass component. The weight proportion of the ZnO, Bi_2O_3, CoO, nano-metal Pd particles and nano-glass is shown in Table 3.

Table 3

	ZnO	Bi_2O_3	CoO	Pd	Glass
wt %	100	5	2	1	20

[0032] Then, in the same manner as the Example 1, the above-mentioned powder is processed to become multilayer chip varistor. The breakdown voltages of component, the breakdown voltage variation after 8KV electrostatic shocks and the capacitance are shown in Table 4.

Table 4

Sheet Thickness (μm)	Breakdown Voltage (V1mA)	Capacitance (pF at 1MHz)	Trigger Voltage (V)	Breakdown Voltage Variation After 1000 Times of Electrostatic Shock (%)
30	206	0.27	420	10

[0033] Table 4 shows that when oxides such as ZnO and so on are taken as semi-conductive particles and the process of the present invention is used, the low-capacitance and static electricity suppressing multilayer chip varistor can be made.

[0034] Table 4 also shows that the multilayer chip varistor using ZnO as material has higher trigger voltage. For lowering the trigger voltage, the thickness of sheets among electrodes is changed from 30μm to 15μm, and then the result is shown in Table 5.

Table 5

Sheet Thickness (μm)	Breakdown Voltage (V1mA)	Capacitance (pF at 1MHz)	Trigger Voltage (V)	Breakdown Voltage Variation After 1000 Times of Electrostatic Shock (%)
15	143	0.43	257	15

[0035] Comparing the results in Table 4 and Table 5, when the thinner sheets are used, the trigger voltage is lower and the capacitance is higher. This result is similar to general multilayer ZnO varistors. Thus, in a predetermined range, the thickness of sheets can be adjusted to control the trigger voltage.

Example 3

[0036] SiC powder of particle size ranging from 2~7μm and nano-metal Pt of particle size ranging from 0.03~0.5μm are added into the gel-like solution composed of nano-silicate glass, which made by sol-gel process, well stirred the previous mixed solution. Thus, the SiC powder uniformly surrounded a layer of organic film containing glass component. Then, in the same manner of the first preferred embodiment, a multilayer chip varistor is completed. The electrical characteristics of the multilayer chip varistor are measured and shown in Table 6.

Table 6

	Particle Size for Secondary Dispersion (μm)	Breakdown Voltage (V1mA)	Capacitance (pF at 1MHz)	Trigger Voltage (V)
SiC (30μm sheet)	0.5	58	0.26	124
	0.03	45	0.29	68

[0037] As shown in Table 6, when the particle size for secondary dispersion is smaller, the multilayer chip varistor has lower breakdown voltage; however, the capacitance is relatively higher.

Example 4

[0038] The multilayer chip varistor sheets made in the Example 1 are sintered at 850~1000°C, and the effects of different sintering conditions are shown in Table 7. It shows that when the sintering temperature is higher, the breakdown voltage is lower; however the capacitance is increased and the leakage current is decreased. Similarly, when the sintering time is increased, the breakdown voltage is lower.

Table 7

Sintering Temperature (°C)	Sintering Time (hr)	Breakdown Voltage (V1mA)	Capacitance (pF at 1MHz)	Leakage Current (μA at 24V)
850	2	265	0.10	0.67
850	5	228	0.11	0.53
950	2	185	0.13	0.50

Example 5

[0039] When changing the overlapping area of inner electrodes of the multilayer chip varistor sheets made according to the same manner in the first preferred embodiment, a varistor of 0.02pF is completed as shown in Table 8. Accordingly, the size of the overlapping area of inner electrodes can be used to adjust the capacitance substantially.

Table 8

Overlapping Area of Inner Electrodes (mm^2)	0.12	0.06	0.03
Capacitance (pF at 1MHz)	0.12	0.07	0.03

[0040] As shown in the above-mentioned embodiments, after adjusting various parameters, the multilayer chip varistor according to the present invention has quite low capacitance, and is particularly suitable to be applied in the protection for high frequency circuits against electrical overstress such as static electricity or transient surge.

Claims

1. A porous ceramic material for protection against electrical overstress and being applied among positive and negative electrodes for suppressing transient surge voltage and electrostatic shock, comprising:

   3~50wt% inorganic glass; and
   50~97wt% semi-conductive or conductive particles (14) with a particle size larger than 0.1 μm;
   wherein said inorganic glass covers surfaces of said semi-conductive or conductive particles (14) as a layer of inorganic glass film (15), and
   wherein the inorganic glass film (15) contains semi-conductive or conductive particles (16) which are smaller than 1 μm, and the quantity of the semi-conductive or conductive particles (16) contained in said inorganic glass film (15) is less than 20wt% of that of inorganic glass.

2. The porous ceramic material as described in claim 1, wherein the inorganic glass comprises one or more of silicate glass, aluminosilicate glass, borate glass, phosphate glass, plumbate glass and other inorganic acid-ate glass.

3. The porous ceramic material as described in claim 1 or 2, wherein the semi-conductive particles (14, 16) are selected from one of ZnO, TiO_2, SnO_2, Si, Ge, SiC, Si-Ge alloy, InSb, GaAs, InP, GaP, ZnS, ZnSe, ZnTe, $SrTiO_3$ and $BaTiO_3$.

4. The porous ceramic material as described in one of claims 1 to 3, wherein the conductive particles (14, 16) are selected from one or more of Pt, Pd, W, Au, Al, Ag, Ni, Cu and alloy thereof.

5. A low-capacitance multilayer chip varistor (10), comprising:

   a porous ceramic main body (11),
   outer electrodes (13) disposed at two ends of the ceramic main body (11) and inner electrodes (12) being disposed therein,
   wherein the porous ceramic main body (11) comprises 3~50wt% inorganic glass and 50~97wt% semi-conductive or conductive particles (14) with a particle size of more than 0.1 μm,
   wherein said inorganic glass covers surfaces of said semi-conductive or conductive particles (14) as a layer of inorganic glass film (15), and
   wherein the inorganic glass film (15) contains semi-conductive or conductive particles (16) which are smaller than 1 μm, and the quantity of the semi-conductive or conductive particles (16) contained in said inorganic glass film (15) is less than 20wt% of that of inorganic glass.

6. The low-capacitance multilayer chip varistor as described in claim 5, wherein the inorganic glass comprises one or more of silicate glass, aluminosilicate glass, borate glass, phosphate glass, plumbate glass and other inorganic acid-ate glass.

7. The low-capacitance multilayer chip varistor as described in claim 5 or 6, wherein the semi-conductive particles (14, 16) are selected from one of ZnO, TiO_2, SnO_2, Si, Ge, SiC, Si-Ge alloy, InSb, GaAs, InP, GaP, ZnS, ZnSe, ZnTe,

$SrTiO_3$ and $BaTiO_3$.

8. The low-capacitance multilayer chip varistor as described in one of claims 5 to 7, wherein the conductive particles (14, 16) are selected from one or more of Pt, Pd, W, Au, Al, Ag, Ni, Cu and alloy thereof.

Patentansprüche

1. Poröses Keramikmaterial zum Schutz vor elektrischer Überspannung, das zwischen positiven und negativen Elektroden zur Unterdrückung von transienter Überspannung und elektrostatischen Entladungsstößen aufgebracht wird, umfassend: 3-50 Gew.-% anorganisches Glas; und 50~97 Gew.-% halbleitende oder leitende Partikel (14) mit einer Partikelgröße von über 0,1 μm;
wobei das anorganische Glas Flächen der halbleitenden oder leitenden Partikel (14) als eine Schicht aus einem anorganischen Glasfilm (15) abdeckt, und
wobei der anorganische Glasfilm (15) halbleitende oder leitende Partikel (16) enthält, die kleiner als 1 μm sind, und die Quantität der in dem anorganischen Glasfilm (15) enthaltenen halbleitenden oder leitenden Partikel (16) weniger als 20 Gew.-% von der des anorganischen Glases beträgt.

2. Poröses Keramikmaterial nach Anspruch 1, wobei das anorganische Glas ein oder mehrere aus Silikatglas, Aluminosilikatglas, Boratglas, Phosphatglas, Plumbatglas und anderem anorganischem Glas auf Basis eines Salzes einer Sauerstoffelementsäure oder Sauerstoffpersäure umfasst.

3. Poröses Keramikmaterial nach Anspruch 1 oder 2, wobei die halbleitenden Partikel (14, 16) aus einem aus ZnO, TiO_2, SnO_2, Si, Ge, SiC, Si-Ge-Legierung, InSb, GaAs, InP, GaP, ZnS, ZnSe, ZnTe, $SrTiO_3$ und $BaTiO_3$ ausgewählt sind.

4. Poröses Keramikmaterial nach einem der Ansprüche 1 bis 3, wobei die leitenden Partikel (14, 16) aus einem oder mehreren aus Pt, Pd, W, Au, Al, Ag, Ni, Cu und Legierungen daraus gewählt sind.

5. Mehrschicht-Chip-Varistor (10) mit niedriger Kapazität, umfassend:

einen porösen Keramikhauptkörper (11),
äußere Elektroden (13), die an zwei Enden des Keramikhauptkörpers (11) angeordnet sind, und innere Elektroden (12), die darin angeordnet sind,
wobei der poröse Keramikhauptkörper (11) 3~50 Gew.-% an anorganischem Glas und 50~97 Gew.-% an halbleitenden oder leitenden Partikeln (14) mit einer Partikelgröße von mehr als 0,1 μm umfasst,
wobei das anorganische Glas Flächen der halbleitenden oder leitenden Partikel (14) als eine Schicht aus einem anorganischen Glasfilm (15) abdeckt, und
wobei der anorganische Glasfilm (15) halbleitende oder leitende Partikel (16) enthält, die kleiner als 1 μm sind, und die Quantität der in dem anorganischen Glasfilm (15) enthaltenen halbleitenden oder leitenden Partikel (16) weniger als 20 Gew.-% von der des anorganischen Glases beträgt.

6. Mehrschicht-Chip-Varistor mit niedriger Kapazität nach Anspruch 5, wobei das anorganische Glas ein oder mehrere aus Silikatglas, Aluminosilikatglas, Boratglas, Phosphatglas, Plumbatglas und anderem anorganischem Glas auf Basis eines Salzes einer Sauerstoffelementsäure oder Sauerstoffpersäure umfasst.

7. Mehrschicht-Chip-Varistor mit niedriger Kapazität nach Anspruch 5 oder 6, wobei die halbleitenden Partikel (14, 16) aus einem aus ZnO, TiO_2, SnO_2, Si, Ge, SiC, Si-Ge-Legierung, InSb, GaAs, InP, GaP, ZnS, ZnSe, ZnTe, $SrTiO_3$ und $BaTiO_3$ ausgewählt sind.

8. Mehrschicht-Chip-Varistor mit niedriger Kapazität nach einem der Ansprüche 5 bis 7, wobei die leitenden Partikel (14, 16) aus einem oder mehreren aus Pt, Pd, W, Au, Al, Ag, Ni, Cu und Legierungen daraus gewählt sind.

Revendications

1. Matériau céramique poreux pour la protection contre les surcharges et appliqué parmi des électrodes positives et négatives pour supprimer la surtension transitoire et les chocs électrostatiques comprenant :

3 à 50% en poids de verre inorganique et
50 à 97% en poids de particules semi-conductrices ou conductrices (14) avec une taille de particules supérieure à 0,1 μm,
ledit verre inorganique couvrant des surfaces desdites particules semi-conductrices ou conductrices (14) en tant que couche de film de verre inorganique (15) et
ledit film de verre inorganique (15) contenant des particules semi-conductrices ou conductrices (14) qui sont plus petites qu'l μm et la quantité de particules semi-conductrices ou conductrices (16) contenues dans ledit film de verre inorganique (15) étant inférieure à 20% en poids de celui de verre inorganique.

2. Matériau céramique poreux selon la revendication 1, le verre inorganique comprenant l'une ou plusieurs des substances verre de silicate, verre d'aluminosilicate, verre de borate, verre de phosphate, verre de plombate ou un autre verre inorganique à base d'un sel d'un acide contenant l'élément oxygène ou de peracide d'oxygène.

3. Matériau céramique poreux selon la revendication 1 ou 2, les particules semi-conductrices (14, 16) étant sélectionnées parmi l'une des matières ZnO, TiO_2, SnO_2, Si, Ge, SiC, alliage de Si-Ge, InSb, GaAs, InP, GaP, ZnS, ZnSe, ZnTe, $SrTiO_3$ et $BaTiO_3$.

4. Matériau céramique poreux selon l'une des revendications 1 à 3, les particules conductrices (14, 16) étant sélectionnées parmi l'une ou plusieurs des matières Pt, Pd, W, Au, Al, Ag, Ni, Cu et les alliages de celles-ci.

5. Varistance à puce multicouche à faible capacité (10) comprenant :

un corps principal en céramique poreuse (11),
des électrodes extérieures (13) disposées à deux extrémités du corps principal en céramique (11) et des électrodes intérieures (12) qui sont déposées à l'intérieur,
le corps principal en céramique poreuse (11) comprenant 3 à 50% en poids de verre inorganique et 50 à 97% en poids de particules semi-conductrices ou conductrices (14) avec une taille de particules supérieure à 0,1 μm,
ledit verre inorganique couvrant des surfaces desdites particules semi-conductrices ou
conductrices (14) en tant que couche de film de verre inorganique (15) et
ledit film de verre inorganique (15) contenant des particules semi-conductrices ou
conductrices (14) qui sont plus petites qu'l μm et la quantité de particules semi-conductrices ou conductrices (16) contenues dans ledit film de verre inorganique (15) étant inférieure à 20% en poids de celui de verre inorganique.

6. Varistance à puce multicouche à faible capacité selon la revendication 5, le verre inorganique comprenant l'une ou plusieurs des substances verre de silicate, verre d'aluminosilicate, verre de borate, verre de phosphate, verre de plombate ou un autre verre inorganique à base d'un sel d'un acide contenant l'élément oxygène ou de peracide d'oxygène.

7. Varistance à puce multicouche à faible capacité selon la revendication 5 ou 6, les particules semi-conductrices (14, 16) étant sélectionnées parmi l'une des matières ZnO, TiO_2, SnO_2, Si, Ge, SiC, alliage de Si-Ge, InSb, GaAs, InP, GaP, ZnS, ZnSe, ZnTe, $SrTiO_3$ et $BaTiO_3$.

8. Varistance à puce multicouche à faible capacité selon l'une des revendications 5 à 7, les particules conductrices (14, 16) étant sélectionnées parmi l'une ou plusieurs des matières Pt, Pd, W, Au, Al, Ag, Ni, Cu et les alliages de celles-ci.

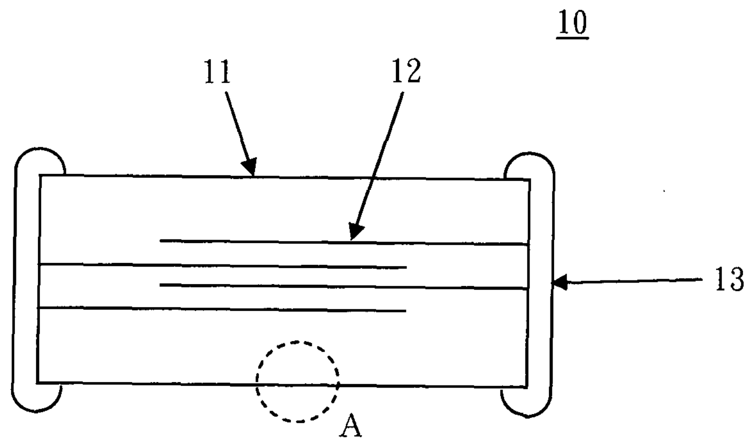

FIG. 1

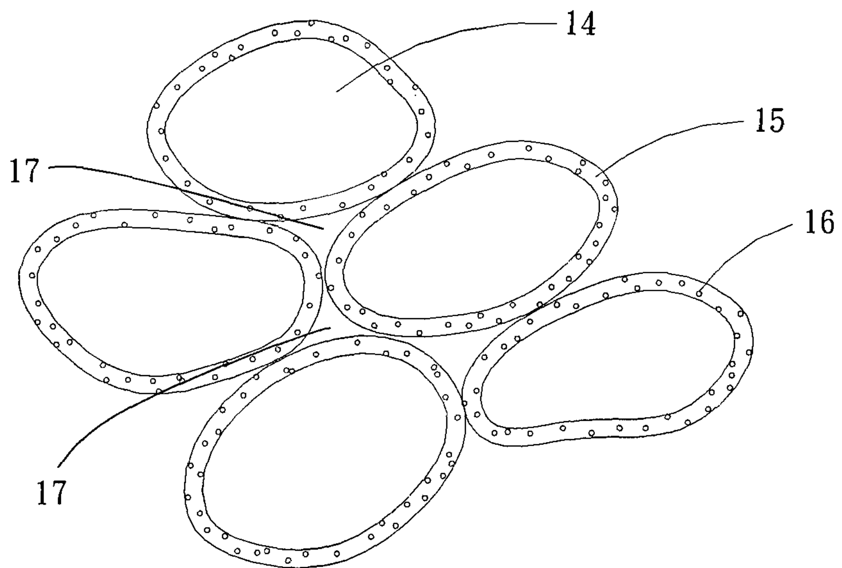

FIG. 2

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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