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(54) **METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING OXIDE FILMS WITH DIFFERENT THICKNESS**

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(30) **Foreign Application Priority Data**

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H01L 21/8238 (2006.01)

(52) **U.S. Cl.** **257/410**; 257/411; 438/216

(57) **ABSTRACT**

After a first gate oxide film is formed on a substrate, a nitride layer is formed by a first oxynitriding process. The first gate oxide film is selectively removed from a thinner film part area of the substrate. A second gate oxide film forming process forms a second gate oxide film in the thinner film part area and a third gate oxide film in a thicker film part area. By executing second oxynitriding process, nitride layers are formed at the thinner and the thicker part areas.

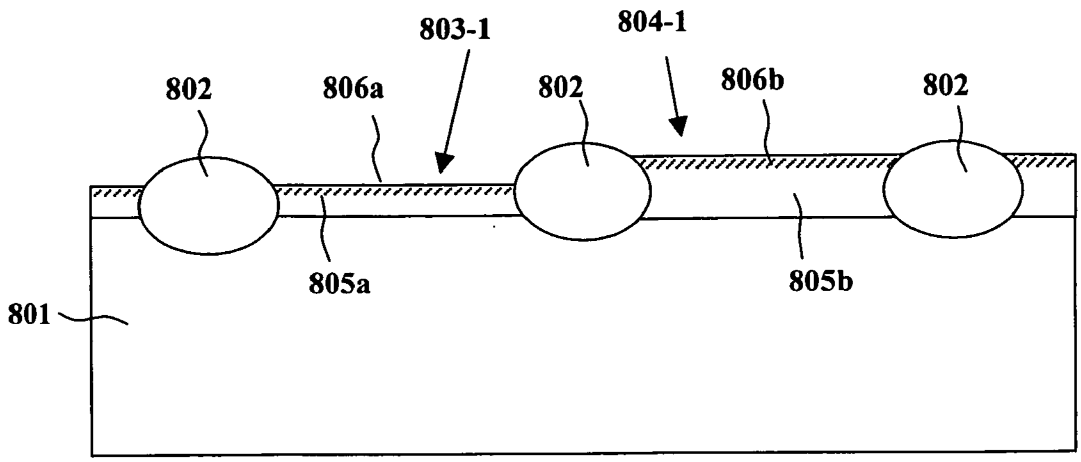


FIG. 1A
PRIOR ART

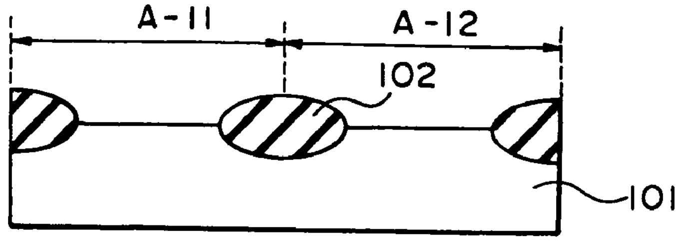


FIG. 1B
PRIOR ART

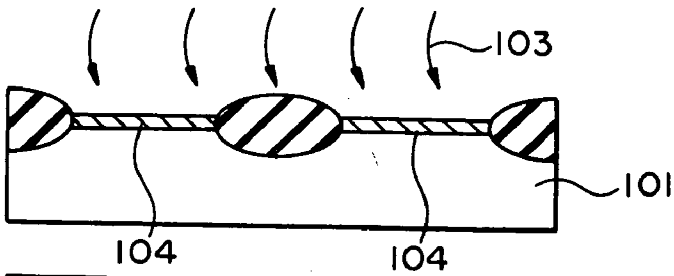


FIG. 1C
PRIOR ART

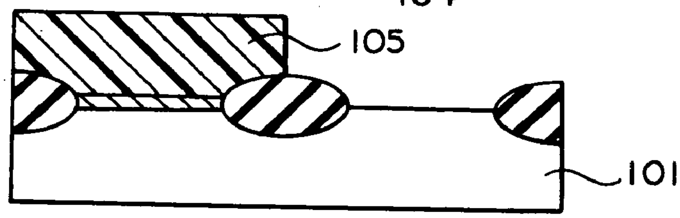


FIG. 1D
PRIOR ART

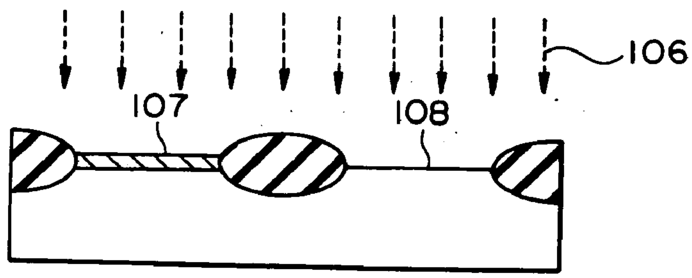


FIG. 1E
PRIOR ART

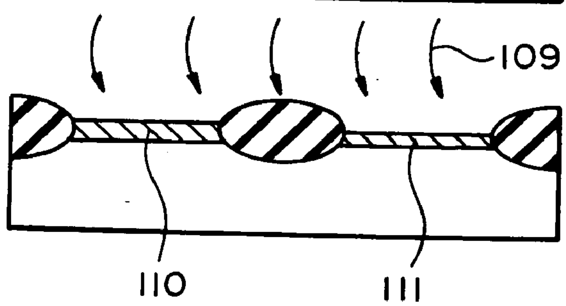
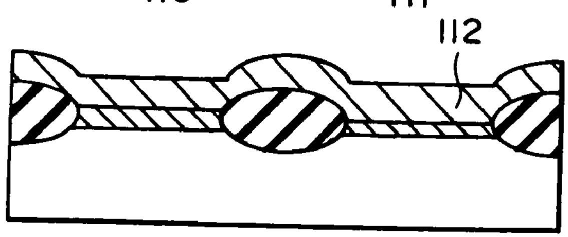
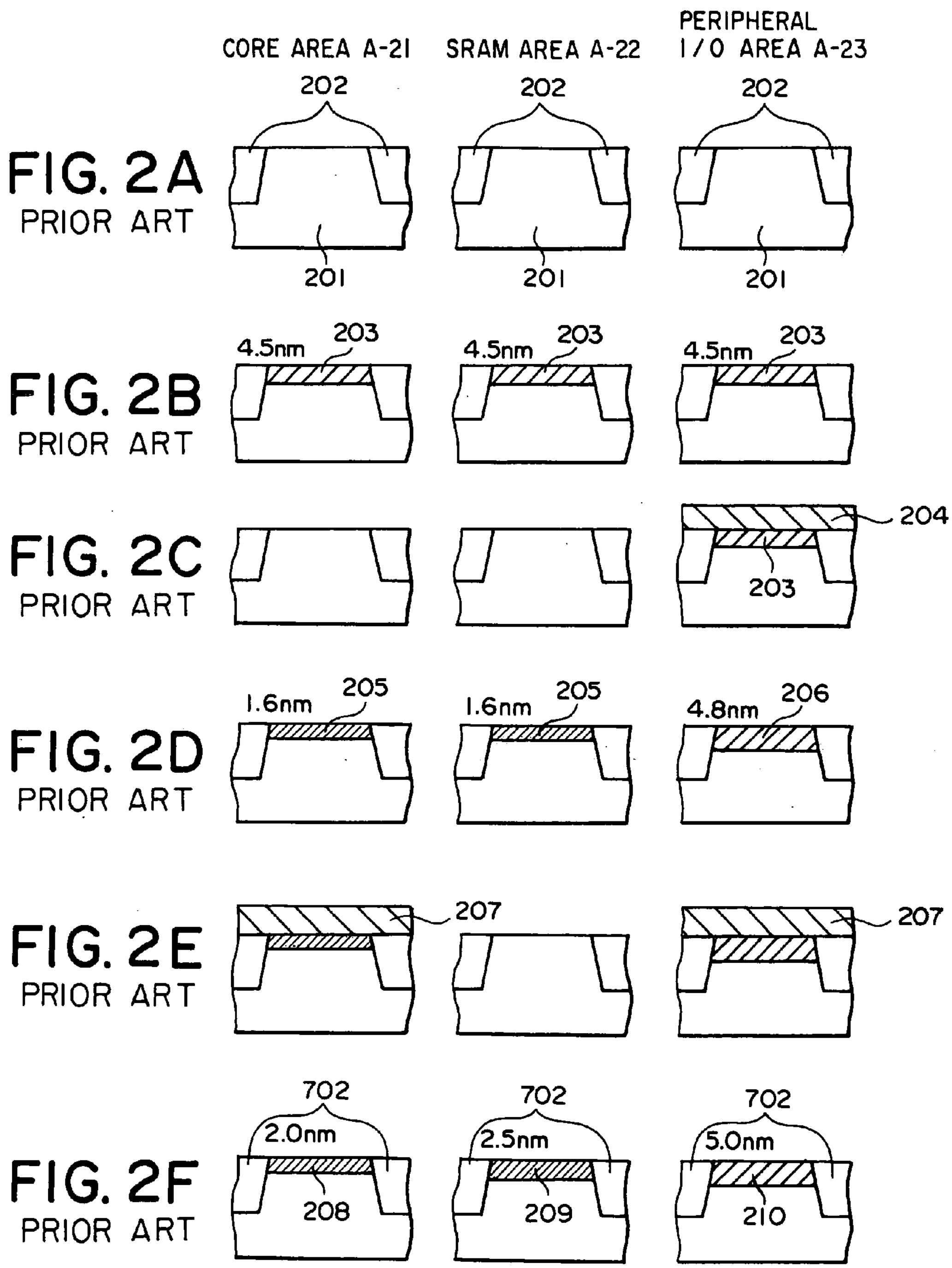


FIG. 1F
PRIOR ART




CORE AREA A-21
SRAM AREA A-22
PERIPHERAL I/O AREA A-23
202
201
FIG. 2A PRIOR ART
4.5nm
203
FIG. 2B PRIOR ART
204
203
FIG. 2C PRIOR ART
1.6nm
205
4.8nm
206
FIG. 2D PRIOR ART
207
FIG. 2E PRIOR ART
702
2.0nm
2.5nm
5.0nm
208
209
210
FIG. 2F PRIOR ART

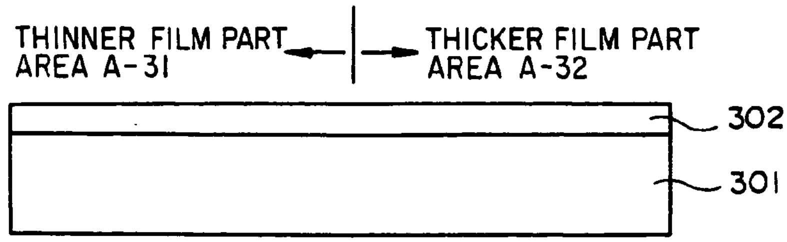


FIG. 3A

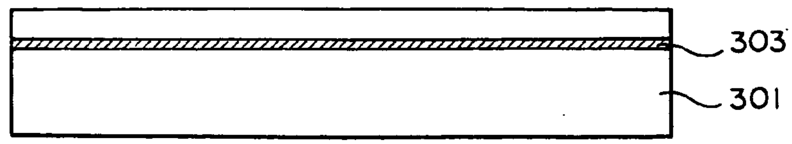


FIG. 3B

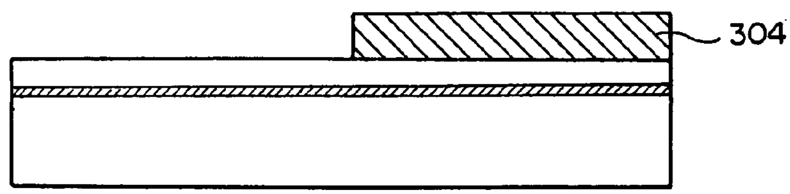


FIG. 3C

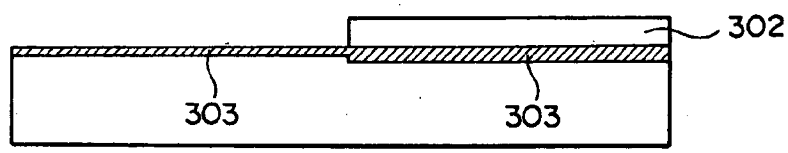


FIG. 3D

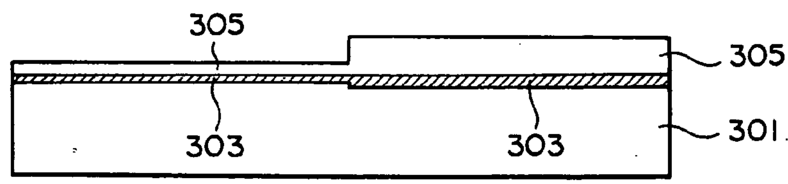


FIG. 3E

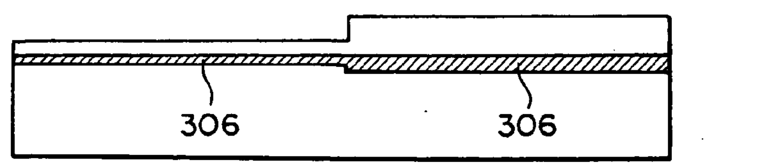


FIG. 3F

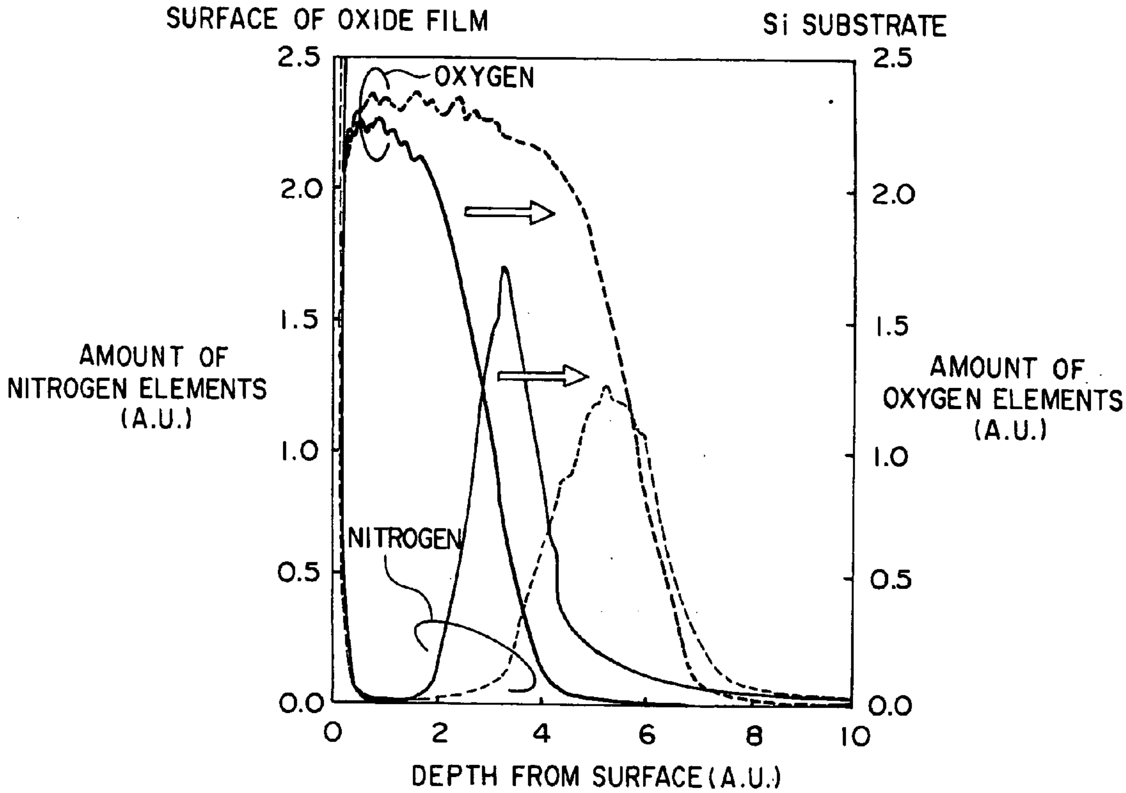
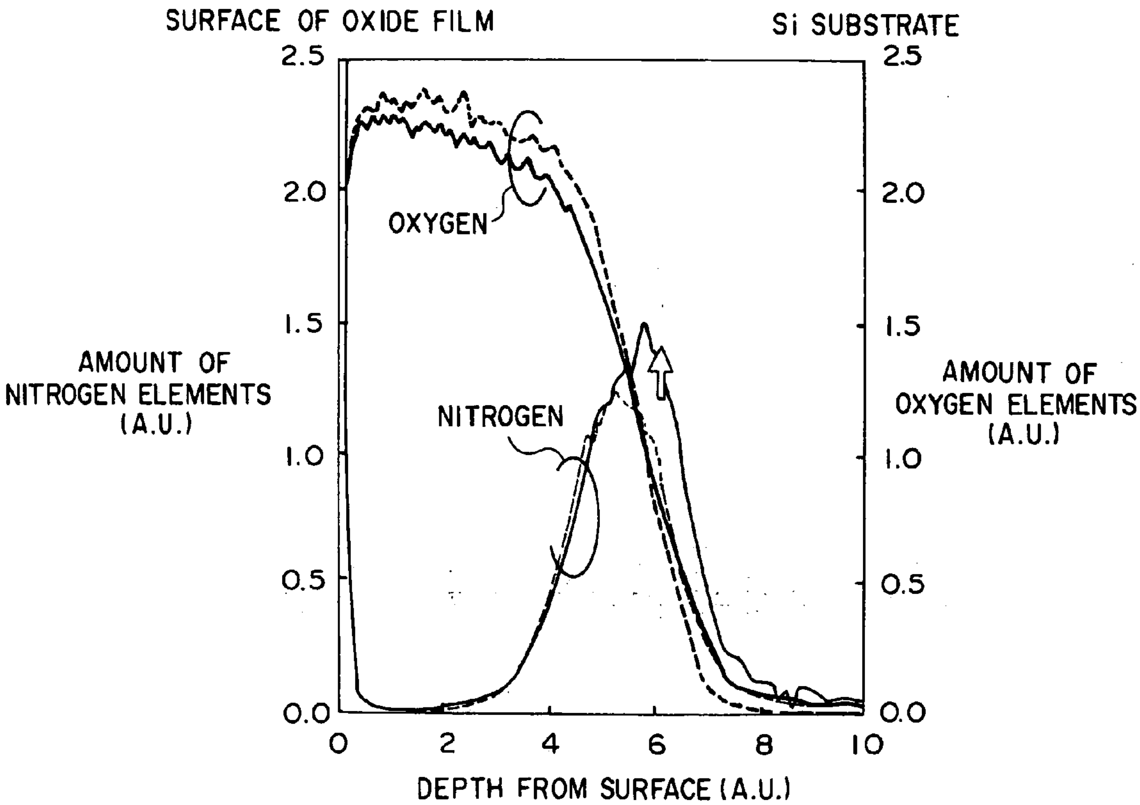

SURFACE OF OXIDE FILM
Si SUBSTRATE
OXYGEN
NITROGEN
AMOUNT OF NITROGEN ELEMENTS (A.U.)
AMOUNT OF OXYGEN ELEMENTS (A.U.)
2.5
2.0
1.5
1.0
0.5
0.0
0
2
4
6
8
10
DEPTH FROM SURFACE (A.U.)

FIG. 4



SURFACE OF OXIDE FILM
Si SUBSTRATE
2.5
2.0
1.5
1.0
0.5
0.0
OXYGEN
NITROGEN
AMOUNT OF NITROGEN ELEMENTS (A.U.)
AMOUNT OF OXYGEN ELEMENTS (A.U.)
0
2
4
6
8
10
DEPTH FROM SURFACE (A.U.)

FIG. 5

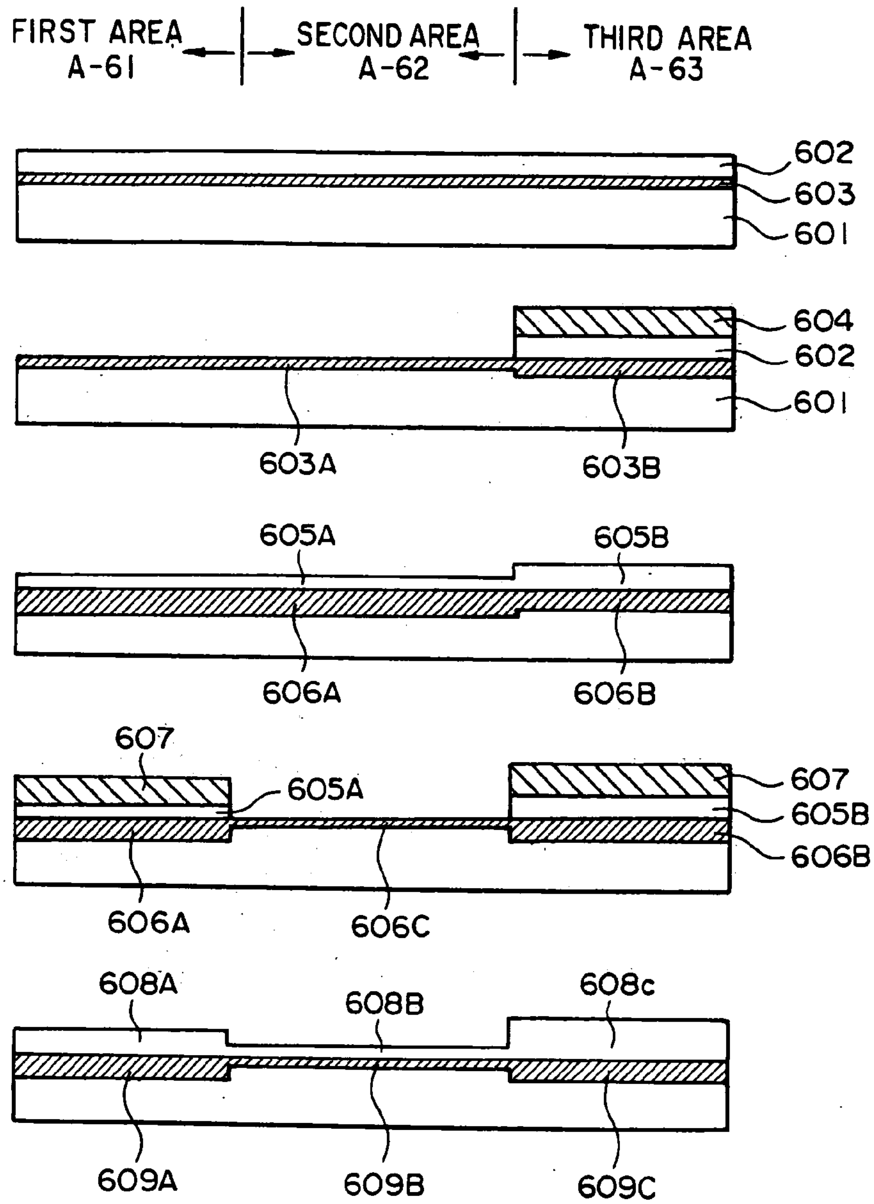


FIG. 6A

FIG. 6B

FIG. 6C

FIG. 6D

FIG. 6E

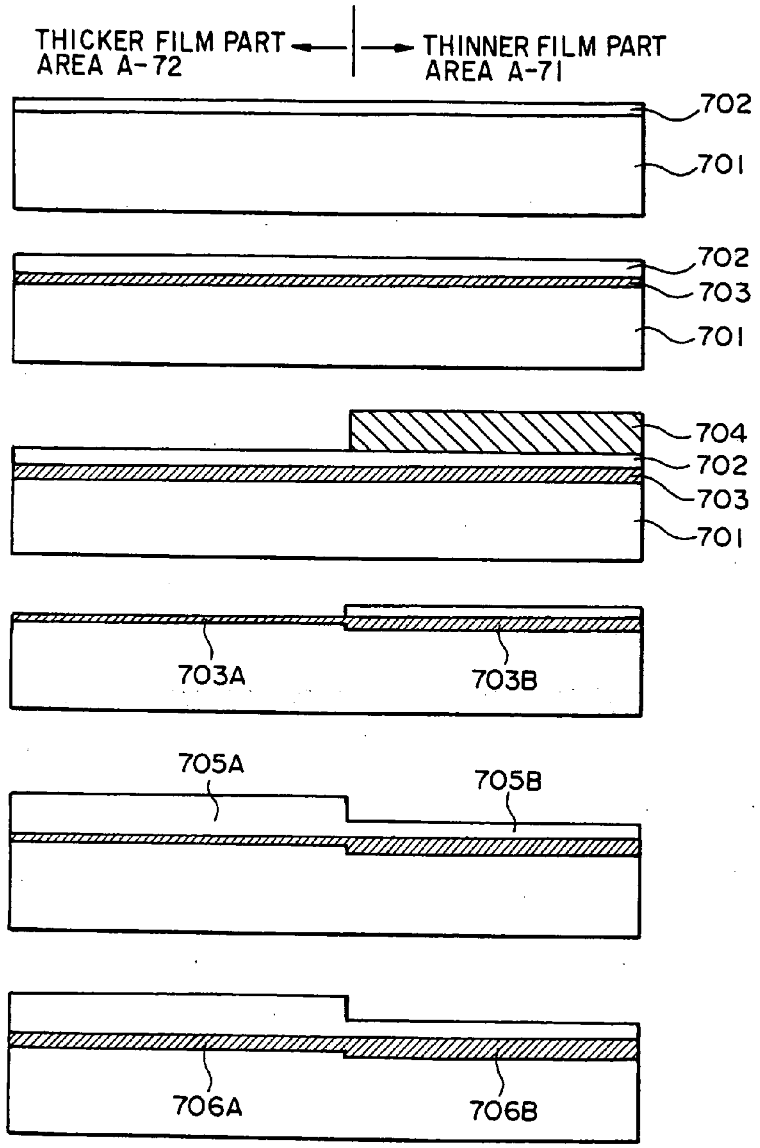


FIG. 7A

FIG. 7B

FIG. 7C

FIG. 7D

FIG. 7E

FIG. 7F

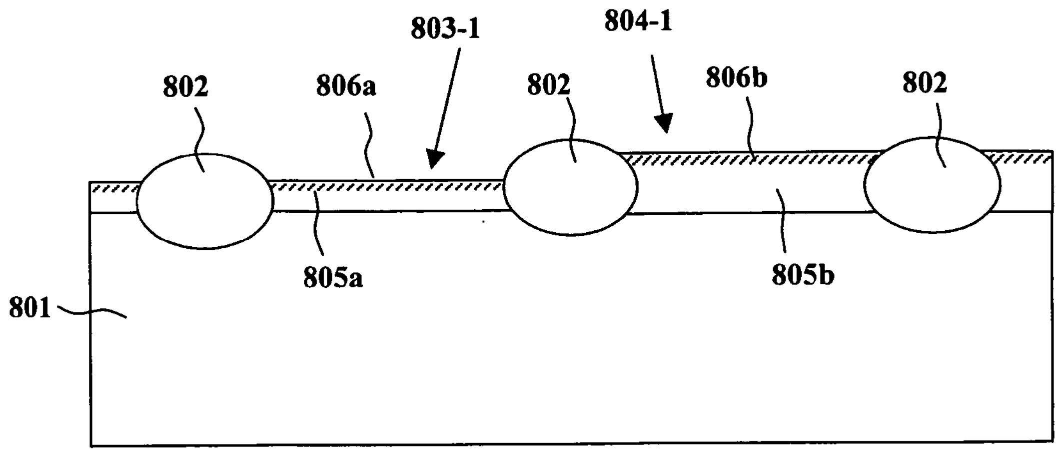


FIG. 8

FIG. 9A

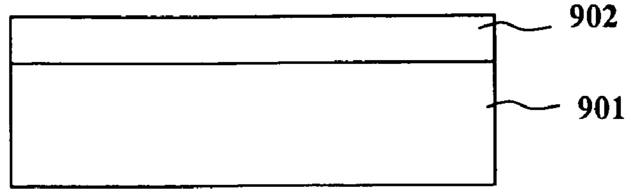


FIG. 9B

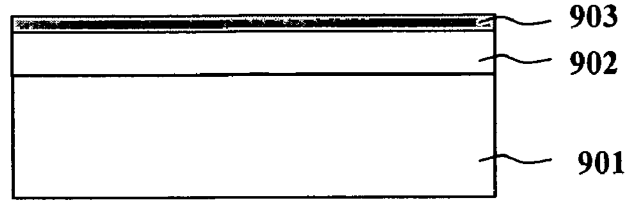


FIG. 9C

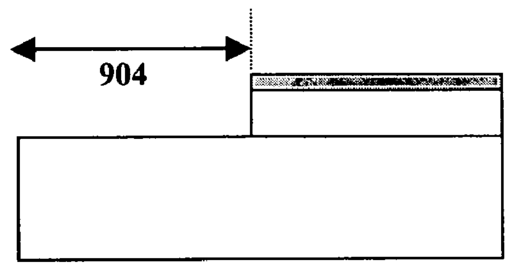


FIG. 9D

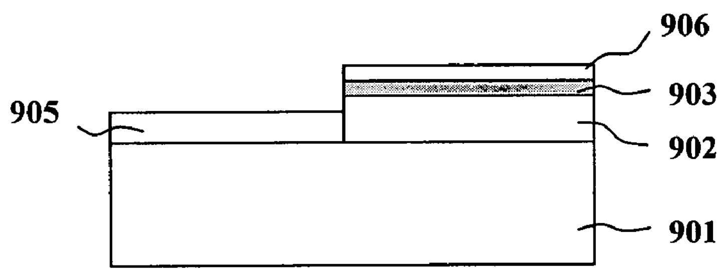
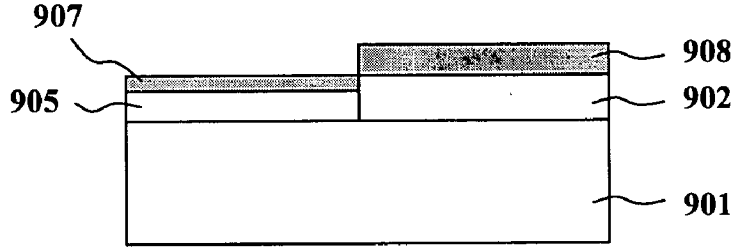


FIG. 9E



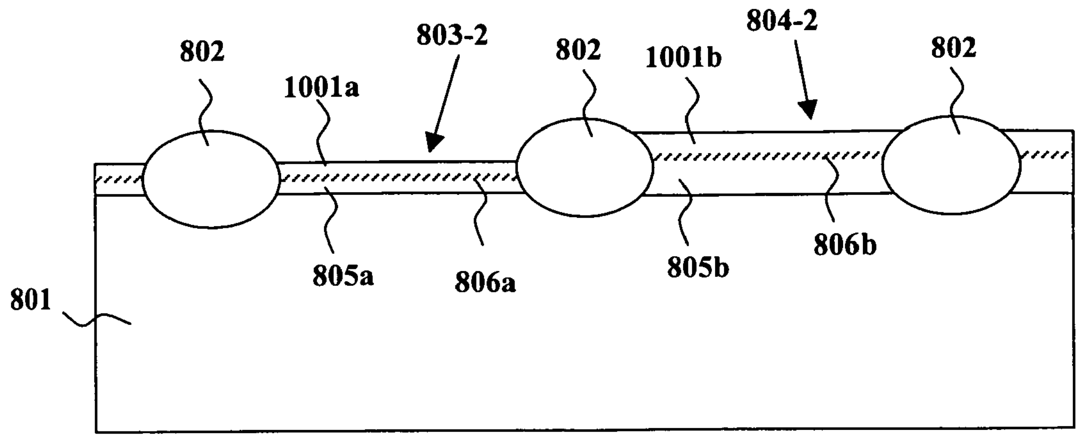


FIG. 10

FIG. 11A

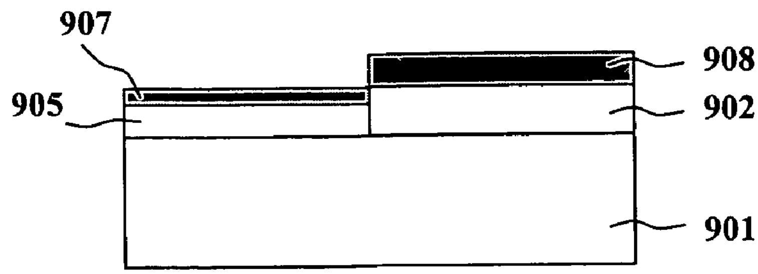
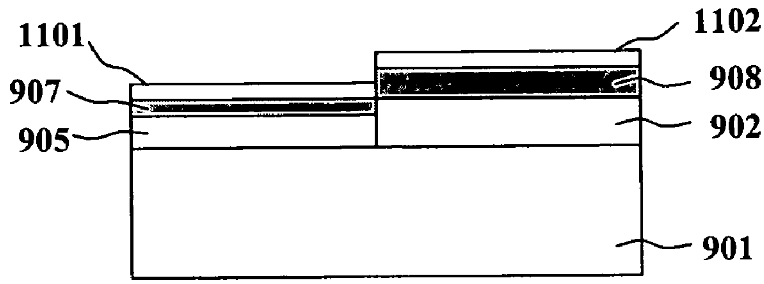


FIG. 11B



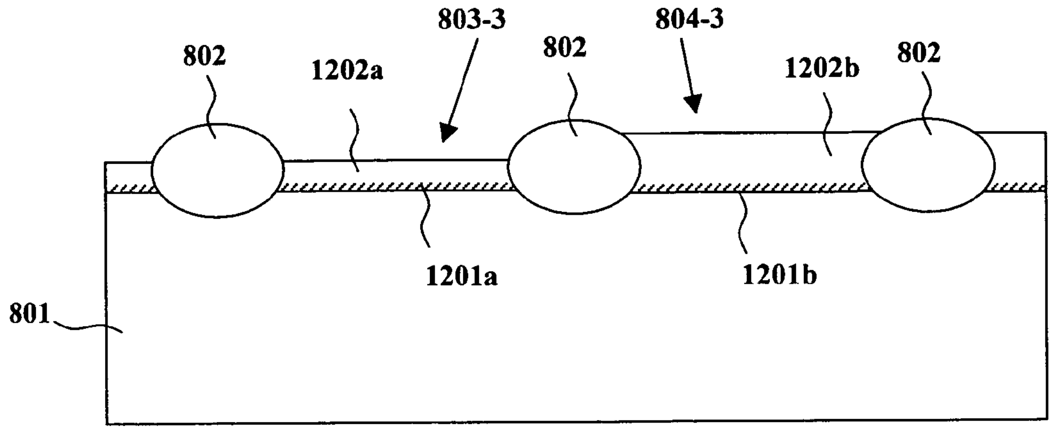


FIG. 12

FIG. 13A

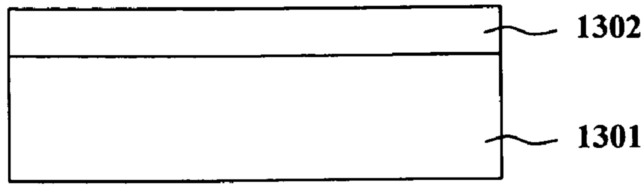


FIG. 13B

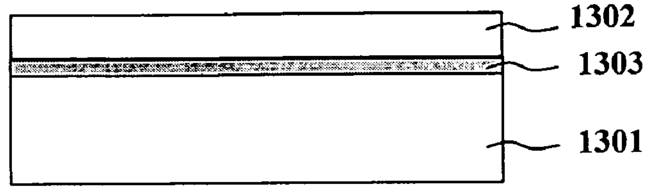


FIG. 13C

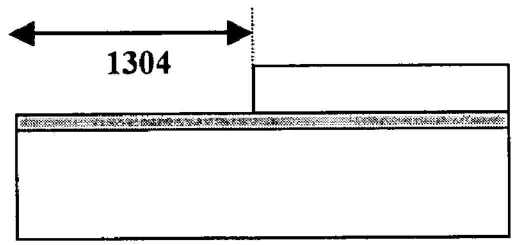
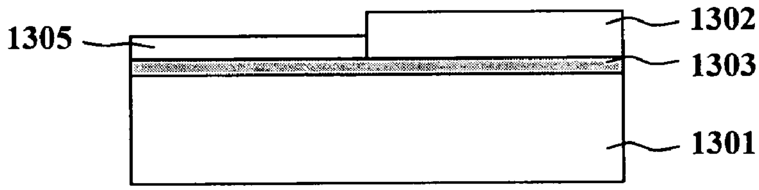


FIG. 13D



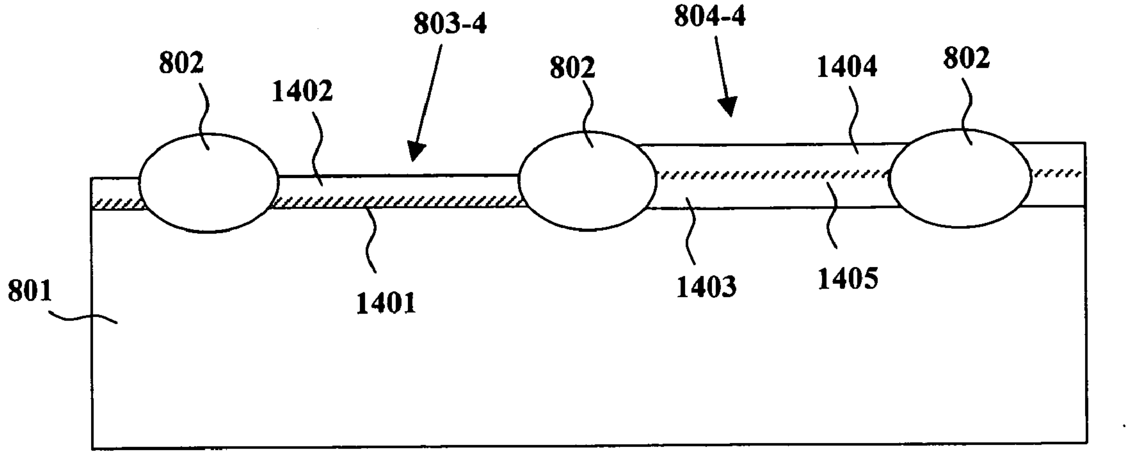


FIG. 14

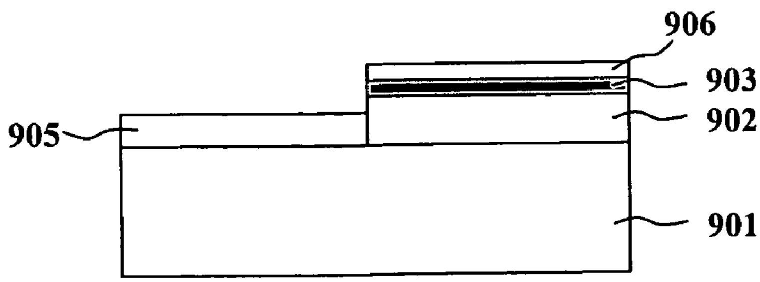


FIG. 15A

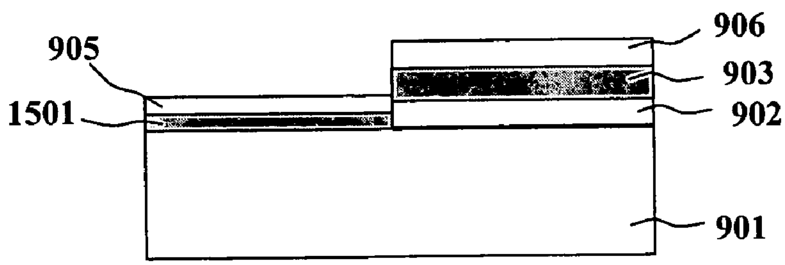


FIG. 15B

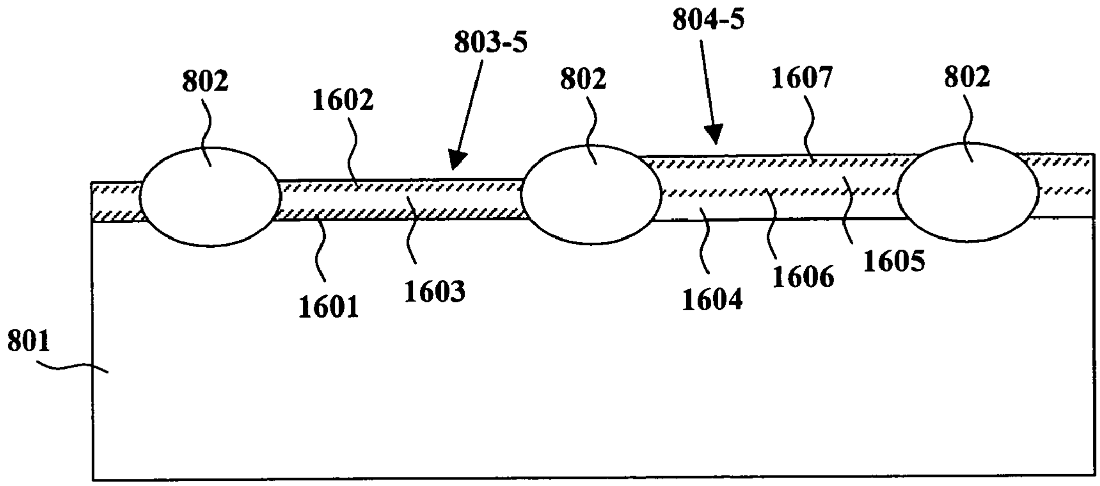


FIG. 16

FIG. 17A

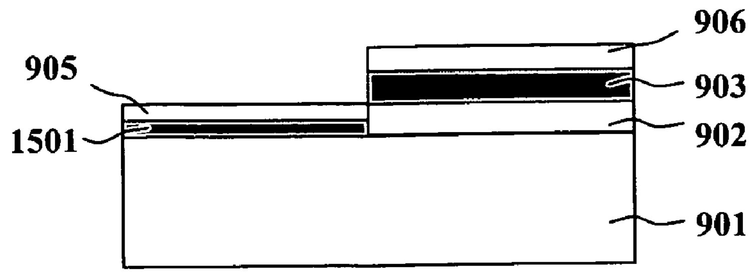
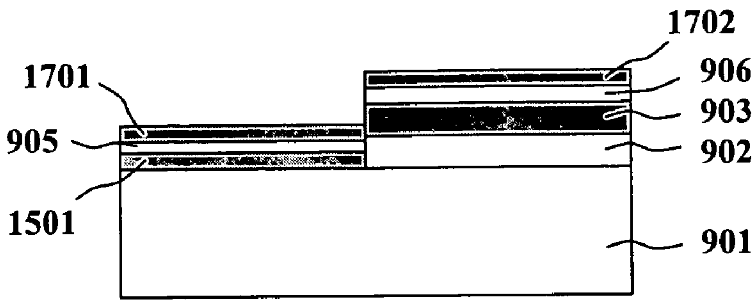


FIG. 17B



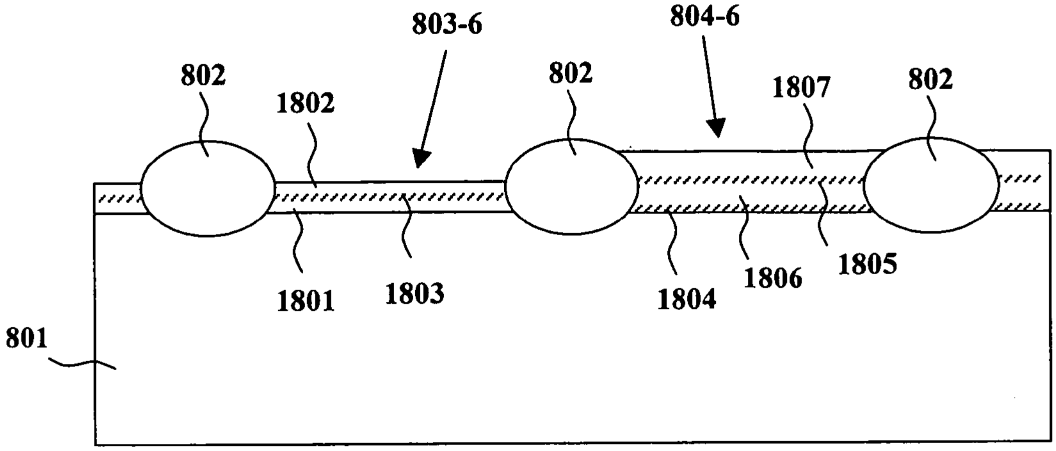


FIG. 18

FIG. 19A

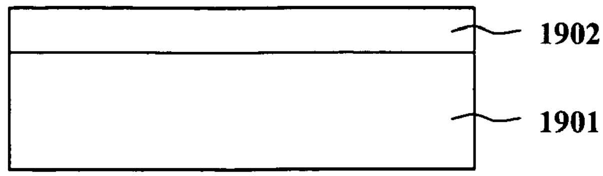


FIG. 19B

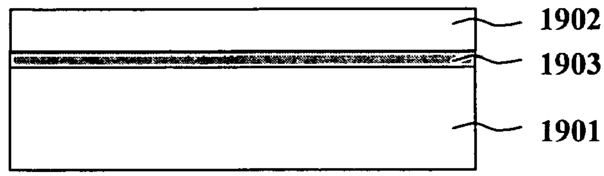


FIG. 19C

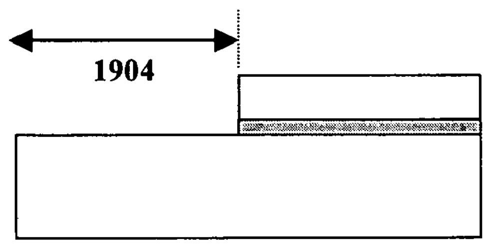


FIG. 19D

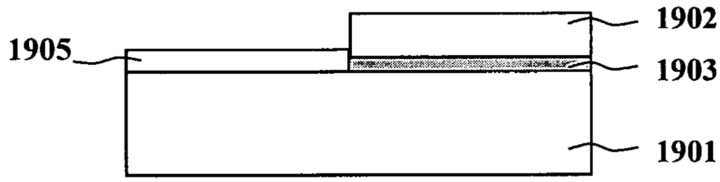


FIG. 19E

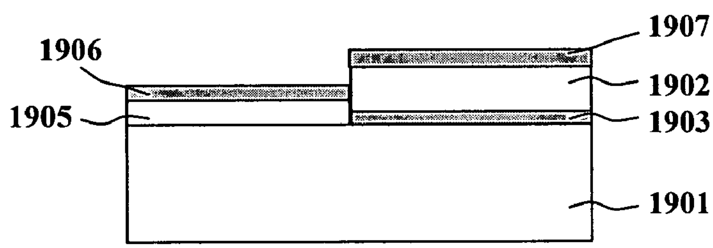
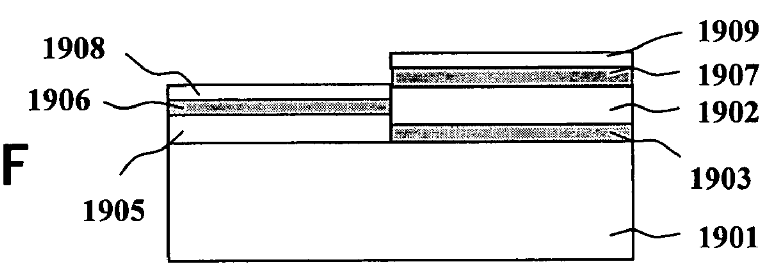


FIG. 19F



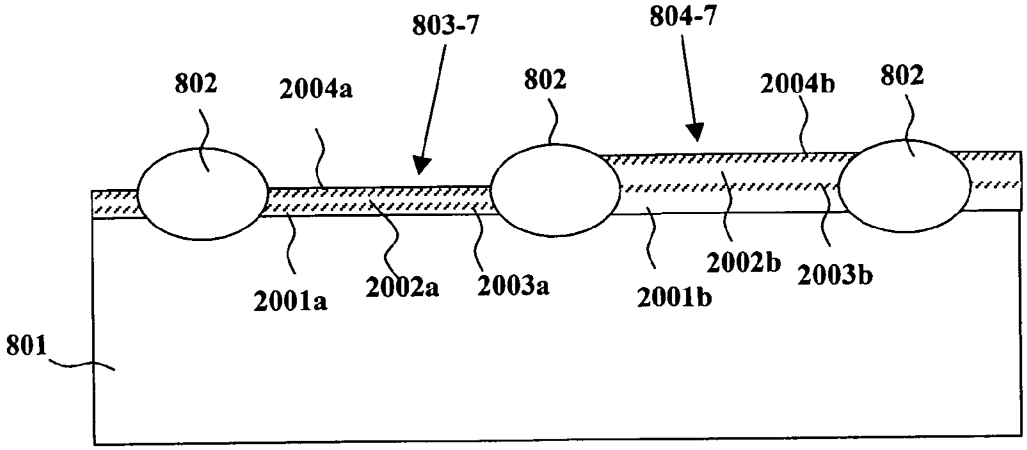

803-7
804-7
802
2004a
802
2004b
802
2001a
2002a
2003a
2001b
2002b
2003b
801

FIG. 20

FIG. 21A

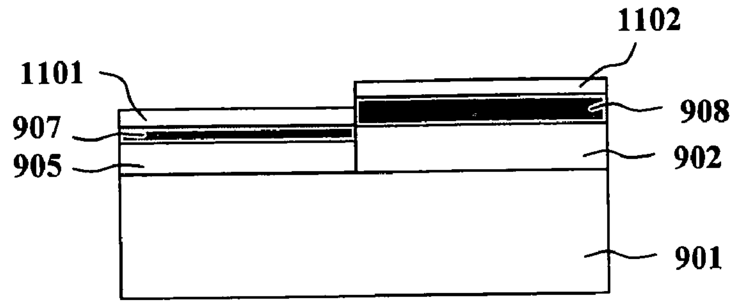
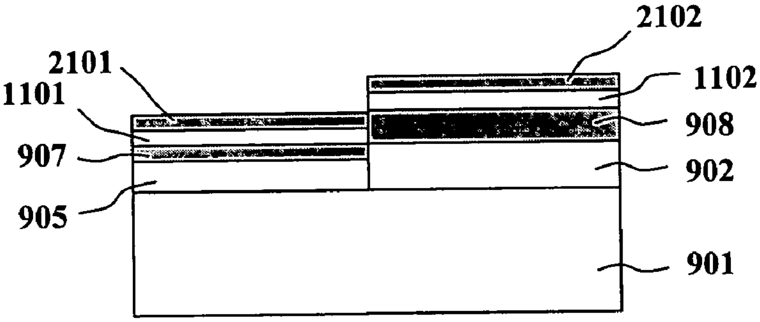
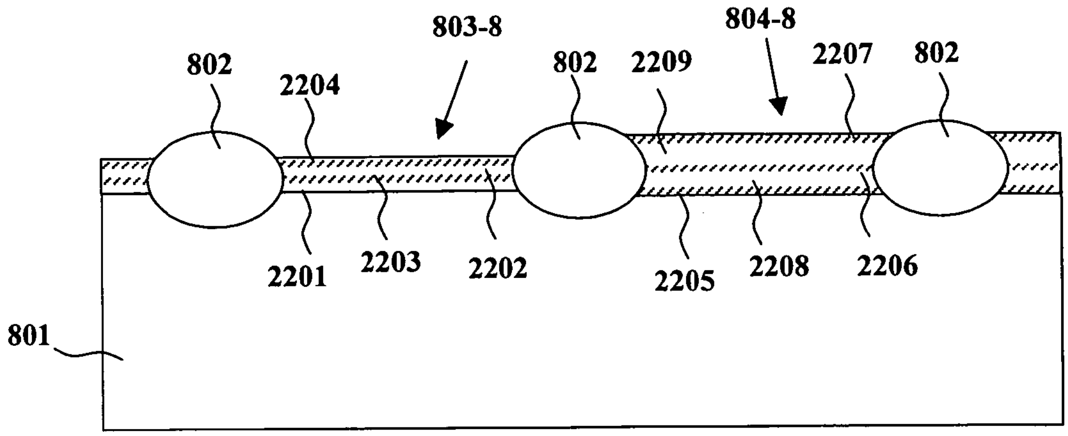


FIG. 21B




803-8
804-8
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801

FIG. 22

FIG. 23A

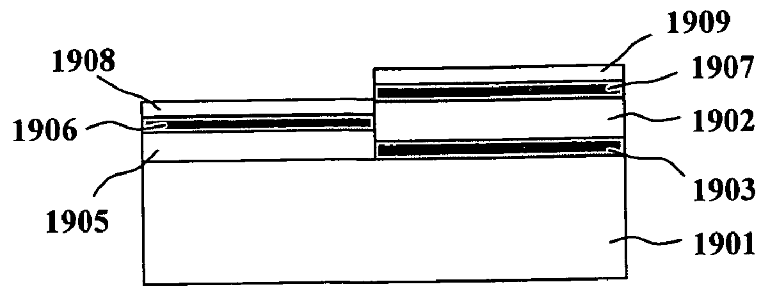
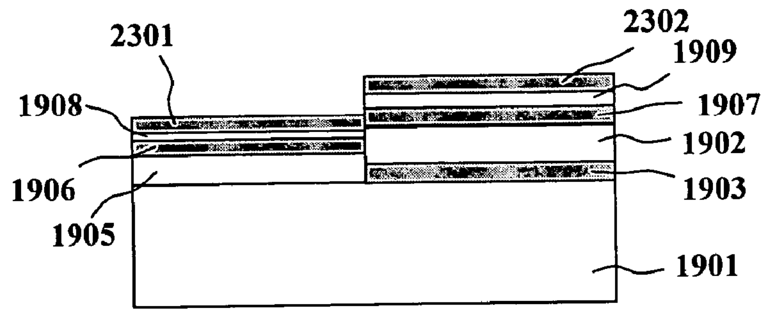


FIG. 23B



METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING OXIDE FILMS WITH DIFFERENT THICKNESS

[0001] This application is a Continuation in Part of U.S. patent application Ser. No. 10/843,694, filed on May 12, 2004. This application claims priority to prior Japanese Application JP 2003-134265, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] This invention relates to a method of manufacturing a semiconductor device, in particular, to a manufacturing method of a semiconductor device including transistors having gate insulating films with different thickness.

[0003] There is a known semiconductor device, in which plural kinds of transistors having gate insulating films with different thickness are formed on a common substrate as a combination of a semiconductor memory and peripheral circuits thereof.

[0004] A conventional method of manufacturing the semiconductor device of the above type uses an oxynitriding process for a thinner gate insulating film for one of the transistors. That is, nitrogen elements are mainly introduced into the thinner gate insulating film. No or few nitrogen elements are introduced into a thicker gate insulating film for another one of the transistors.

[0005] Generally, when thickness of a gate oxide film is 7 nm or more as before, the oxynitriding process is unnecessary. This is because the thicker gate oxide film equal to or more than 7 nm has no problem such as leakage current and boron leakage. Moreover, the oxynitriding process is undesirable when the thickness of the gate oxide film is 5 nm or more because it deteriorates reliability of the gate oxide film.

[0006] However, the gate oxide film of the transistor tends to become thin according to demands of miniaturizing, implementing thin design, and saving power consumption of the semiconductor device recently. Thus, importance of the oxynitriding process becomes high to suppress leakage current and to improve operating characteristics of the transistor. Therefore, in a case of manufacturing the semiconductor device including plural kinds of transistors having gate insulating films with different thickness, it becomes important to introduce nitrogen elements into not only the thinner gate insulating film but also the thicker gate insulating film.

SUMMARY OF THE INVENTION

[0007] In view of the foregoing and other exemplary problems, drawbacks, and disadvantages of the conventional methods and structures, an exemplary feature of the present invention is to provide a method of manufacturing a semiconductor device capable of introducing nitrogen elements into not only a thinner gate insulating film formed on a substrate but also a thicker gate insulating film formed on the substrate.

[0008] Other exemplary features of this invention will become clear as the description proceeds.

[0009] According to an exemplary aspect of this invention, a method of manufacturing semiconductor device includes multi-oxidation process for forming oxide films with different thickness on a substrate. The method includes executing an oxide film forming process for forming each of said oxide films on said substrate, and inevitably executing an oxynitriding process for forming nitride layer in each of said oxide films after the oxide film forming process.

[0010] According to another exemplary aspect of this invention, a semiconductor device has a substrate with a plurality of regions. The semiconductor device comprises oxide films which are formed in the regions and which have different thickness. Nitride layers are formed at vicinities of interfaces between the oxide films and the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIGS. 1A-1F** are schematic sectional views for describing a method of manufacturing a related semiconductor device including transistors having gate insulating films with different thickness;

[0012] **FIGS. 2A-2F** are schematic sectional views for describing another method of manufacturing another related semiconductor device including transistors having gate insulating films with different thickness;

[0013] **FIGS. 3A-3F** are schematic sectional views for describing a method of manufacturing a semiconductor device according to a first embodiment of this invention;

[0014] **FIG. 4** shows oxygen and nitrogen profiles before and after a second oxide film forming process using ISSG or plasma oxidation;

[0015] **FIG. 5** shows oxygen and nitrogen profiles before and after a second oxynitriding process;

[0016] **FIGS. 6A-6E** are schematic sectional views for describing a method of manufacturing a semiconductor device according to a second embodiment of this invention;

[0017] **FIGS. 7A-7F** are schematic sectional views for describing a method of manufacturing a semiconductor device according to a third embodiment of this invention;

[0018] **FIG. 8** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0019] **FIGS. 9A-9E** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0020] **FIG. 10** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0021] **FIGS. 11A-11B** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0022] **FIG. 12** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0023] **FIGS. 13A-13D** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0024] **FIG. 14** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0025] **FIGS. 15A-15B** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0026] **FIG. 16** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0027] **FIGS. 17A-17B** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0028] **FIG. 18** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0029] **FIGS. 19A-19F** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0030] **FIG. 20** depicts a semiconductor device according to an exemplary embodiment of this invention;

[0031] **FIGS. 21A-21B** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention;

[0032] **FIG. 22** depicts a semiconductor device according to an exemplary embodiment of this invention; and

[0033] **FIGS. 23A-23B** are schematic sectional views for describing a method of manufacturing a semiconductor device according to an exemplary embodiment of this invention.

DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

[0034] Referring to **FIGS. 1A** to 1F, description will be at first directed to a method of manufacturing a related semiconductor device including transistors having gate insulating films with different thickness. Such a process is disclosed in Unexamined Japanese Patent Publication No. 2000-216257.

[0035] At first, as illustrated in **FIG. 1A**, a silicon substrate **101** is provided and LOCOS (Local Oxidation of Silicon) oxide films **102** are formed in the silicon substrate **101**. The LOCOS oxide films **102** define device forming areas including higher and lower voltage system transistor forming areas A-**11** and A-**12** and isolate them from each other.

[0036] Next, as shown in **FIG. 1B**, a first heat-treating process is executed to the silicon substrate **101** in atmosphere of oxidation seeds **103**. The first heat-treating process oxidizes exposed surfaces of the silicon substrate **101** and thereby silicon oxide films **104** are formed on/in the silicon substrate **101**.

[0037] Next, as shown in **FIG. 1C**, after a resist film **105** is formed at the higher voltage system transistor forming area A-**11**, the silicon oxide film **104** of the lower voltage system transistor forming area A-**12** is removed by a wet etching process to expose the silicon substrate **101**. Then the resist **105** is completely removed from the higher voltage system transistor forming area A-**11**.

[0038] Subsequently, as shown in **FIG. 1D**, nitrogen ions **106** are implanted in the areas A-**11** and A-**12** by an ion implanter (not shown). As a result, an azotized silicon oxide film **107** is formed at the higher voltage system transistor forming area A-**11** while a silicon nitride film **108** is formed at the lower voltage system transistor forming area A-**12**.

[0039] Next, as shown in **FIG. 1E**, a second heat-treating process is made to the silicon substrate **101** in atmosphere of oxidation seeds **109** and thereby a thicker gate oxide film **110** and a thinner gate oxide film **111** are formed at the areas A-**11** and A-**12**, respectively.

[0040] Lastly, as shown in **FIG. 1F**, a polysilicon film **112** is deposited on the upper exposed surface of the silicon substrate **101** with the thicker gate oxide film **110** and the thinner gate oxide film **111**.

[0041] After that, the polysilicon film **112** is patterned in a predetermined pattern. Then, gate electrodes and source-drain regions are formed on/in the semiconductor substrate **101** to form the semiconductor device. Thus, the semiconductor device including two (or more) kinds of transistors with different thickness of gate insulating film is completed.

[0042] Another method of manufacturing another related semiconductor device of the type is described in reference to **FIGS. 2A-2F**. Such a method is disclosed in Unexamined Japanese Patent Publication No. 2001-53242.

[0043] At first, as shown in **FIG. 2A**, a silicon substrate **201** is provided and device isolation layers **202** are formed in the substrate **201** by a trench isolation method. The device isolation layers **202** define device areas A-**21**, A-**22** and A-**23**. The device areas A-**21**, A-**22** and A-**23** are used for a core area, a SRAM area and a peripheral I/O area, respectively. Furthermore, necessary preprocessing such as ion implantation is performed to the silicon substrate **201** with the device isolation layers **202**.

[0044] Next, as shown in **FIG. 2B**, oxide films **203** are formed at the device areas A-**21**, A-**22** and A-**23** by a thermal oxidation method using oxygen gas supplied on the silicon substrate **201**. Each of the oxide films **203** has thickness, for example, of 4.5 nm.

[0045] As shown in **FIG. 2C**, after only the peripheral I/O area A-**23** and vicinity is covered by a resist film **204**, the oxide films **203** of the core area A-**21** and the SRAM area A-**22** are removed by etching. Then the resist **204** is completely removed from the peripheral I/O are A-**23** and the vicinity.

[0046] Next, a first oxynitriding process is performed to form oxynitride films **205** at the device areas A-**21** and A-**22**. In this event a two-layer film **206** consist of the oxide film and an oxynitride film is formed at the device area A-**23**. Each of the oxynitride films **205** has a thickness, for example, of 1.6 nm while the two-layer film **206** has a thickness, for example, of 4.8 nm.

[0047] Next, as shown in **FIG. 2E**, after the device areas A-**21** and A-**23** are covered by resist films **207**, the oxynitride film **205** of the device area A-**22** is removed by etching. Then the resist films **207** are completely removed from the device areas A-**21** and A-**23**.

[0048] After that, a second oxynitriding process is performed to the silicon substrate **201** with the oxynitride film

205 at the device area A-**21** and the two-layer film **206** at the device area A-**23**. The second oxynitriding process uses source gas whose density of nitrogen is lower than that of the source gas used in the first oxynitriding process. Accordingly, as shown in **FIG. 2F**, an oxynitride film **208**, an oxynitride film **209** having nitrogen density lower than that of the oxynitride film **208**, and a two layer film **210** are formed at the core area A-**21**, the SRAM area A-**22**, and the peripheral I/O area A-**23**, respectively. For example, the films **208**, **209** and **210** have thickness of 2.0 nm, 2.5 nm and 5.0 nm, respectively. The films **208**, **209** and **210** are used for gate insulating films of transistors.

[**0049**] In the former of the related methods mentioned above, the oxynitride process (e.g. nitrogen ion implantation) is performed only after the first gate oxide film (**104**) is formed. Moreover, in the latter of the related methods, the oxynitride processes are used for forming the second and third gate insulating films (**208** and **209**). At any rate, the oxynitride process(es) is(are) used to introduce nitrogen into the thinner (oxide) film part area(s). Accordingly, the related methods can insufficiently introduce nitrogen into the thicker (oxide) film part area. In addition, each of the related methods cannot form a nitride layer in the vicinity of interface between the substrate and the gate insulating film. This makes it difficult to obtain desirable characteristics of the semiconductor device manufactured by the method.

[**0050**] Referring to **FIGS. 3A-3F**, the description will proceed to a method of manufacturing a semiconductor device according to a first exemplary embodiment of this invention.

[**0051**] In each of **FIGS. 3A-3F**, the left hand side shows a thinner film part area A-**31** (or a low voltage transistor forming area) while the right hand side shows a thicker film part area A-**32** (or a high voltage transistor forming area). Though the thinner film part area A-**31** must be isolated from the thicker film part area A-**32** by a device isolating region, the device isolating region has no relation with this invention and illustrating thereof is omitted in the present specification and drawings. Other parts, such as gate, source and drain regions, having no relation to this invention are also omitted in the present specification and drawings.

[**0052**] Hereafter, the description will be mainly directed to forming gate oxide films and oxynitriding the gate oxide films. Known processes can be used for other necessary processes in the method of manufacturing the semiconductor device.

[**0053**] As illustrated in **FIG. 3A**, at first, a semiconductor substrate (e.g. Si substrate) **301** is provided and a first gate oxide film **302** is formed by a first oxide film forming process on the surface of the semiconductor substrate **301**. For the first gate oxide film forming process, various processes may be used. For instance, there are a wet, dry or halogen oxidation using a vertical diffusion equipment, an RTO (Rapid Thermal Oxidation), ISSG (In-Situ Steam Generation) or WVG (Water Vapor Generation) using a sheet fed equipment, and a plasma oxidation with a plasma treatment equipment.

[**0054**] Next, a first oxynitriding process is applied to the semiconductor substrate **301** on which the first gate oxide film **302** is formed. As a result, a first nitride layer **303** is formed in the first gate oxide film **302** as illustrated in **FIG. 3B**. To execute the oxynitriding process, an NO (nitric oxide), N_2O (nitrous oxide) or NH_3 (ammonia) treatment using the vertical diffusion equipment or a sheet fed equipment, or a plasma nitriding using the plasma treatment equipment can be used, for example.

[**0055**] Here, the NO or N_2O treatment tends to form the first nitride layer **303** at vicinity of an interface between the first gate oxide film **302** and the semiconductor substrate **301**. Moreover, the NH_3 treatment tends to form the first nitride layer **303** both at the vicinity of an upper surface of the first gate oxide film **302** and at the vicinity of the interface between the first gate oxide film **302** and the semiconductor substrate **301**. Furthermore, the plasma nitriding tends to form the first nitride layer **303** at the vicinity of the upper surface of the first gate oxide film **302**.

[**0056**] Next, a resist film for an etching mask is deposited on the upper surface of the first gate oxide film **302**. Then the resist film is selectively removed from the thinner film part area A-**31** by etching to leave the part thereof at the thicker film part area A-**32** as illustrated in **FIG. 3C**. That is, the remaining part of the resist film forms the etching mask **304** at the thicker film part area A-**32**.

[**0057**] Next, the first gate oxide film **302** of the thinner film part area A-**31** is removed by a wet etching method using diluted or buffered hydrofluoric acid or a dry etching method. In this event, the first nitride layer **303** of the thinner film part area A-**31** is partly removed together with the first gate oxide film **302**. As a result, the first nitride layer **303** is divided into a second nitride layer **303**A of the thinner film part area A-**31** and a third nitride layer **303**B of the thicker film part area A-**32**. Then, the etching mask **304** is completely removed to expose the first oxide film **302** of the thicker film part area A-**32** as illustrated in **FIG. 3D**.

[**0058**] Subsequently, a second oxide film forming process which may be similar to or different from the first oxide film forming process is executed to the semiconductor substrate **301** of **FIG. 3D**. As a result, as shown in **FIG. 3E**, a second gate oxide film **305**A is formed on the second nitride layer **303**A of the thinner film part area A-**31**. At the same time, a third gate oxide film **305**B (including the first oxide film **302**) is formed at the thicker film part area A-**32**.

[**0059**] Here, the third nitride layer **303**B (which is maldistributed at the vicinity of interface between the substrate **301** and the third gate oxide film **305**B) migrates to the inner part of the third gate oxide film **305**B accordingly as the third gate oxide film **305**B increases the thickness thereof when the above mentioned oxide film forming methods are used for the second oxide film forming process except the ISSG and the plasma oxidation.

[**0060**] To the contrary, when the ISSG or the plasma oxidation is used for the second oxide film forming process, the third nitride layer **303**B remains at the vicinity of interface between the substrate **301** and the third gate oxide film **305**B as shown in **FIG. 4** regardless of increase of the thickness of the third gate oxide film **305**B (and/or **302**). This is because the ISSG and the plasma oxidation are strong oxidizing methods and cause the oxidative reaction even in the nitride film. By each of the ISSG and the plasma oxidation, the oxidative reaction is advanced at a surface side of the nitride layer previous to at an interface side between the oxide film and the substrate. Thus, the ISSG and the plasma oxidation can execute additional oxidative reaction without losing shape of a nitride profile of a sample having a nitride layer at vicinity of interface between an oxide film and a substrate. In other words, the ISSG and the plasma oxidation can substantially keep the nitride profile formed by previous process(es). Therefore, the ISSG and the plasma oxidation are very useful for a manufacturing process of a semiconductor device whose electronic characteristics of the vicinity of the interface between the oxide film and the substrate are important.

[0061] Next, a second oxynitriding process, which may be similar to or different from the first oxynitriding process, is performed to the semiconductor substrate **301** with the second and the third gate oxide film **305**A and **305**B. Hereby, as shown in **FIG. 3F**, fourth and fifth nitride layers **306**A and **306**B are formed at the thinner and thicker film part areas A-**31** and A-**32**, respectively. An amount of nitrogen elements and distribution profile in each nitride layer (**306**A, **306**B) depends on the etching process for partially (selectively) etching the first gate oxide film **302**, thickness of the gate oxide film (**305**A, **305**B), treatment condition of the second oxynitriding process and so on.

[0062] **FIG. 5** shows an example of changing oxide and nitride profiles in the NO treatment as the second oxynitriding process. As understood from **FIG. 5**, the amount of nitrogen in the nitride layer can be increased with hardly changing the position of the nitride layer. This means that it is possible to replenish new nitrogen elements by the second oxynitriding process when the nitrogen elements doped by the first oxynitriding process are missed by the second oxide film forming process.

[0063] According to this exemplary embodiment, the oxide films (**305**A and **305**B) having different thickness can be formed in the thinner and the thicker film part area A-**31** and A-**32** respectively, while the nitride films (**306**A and **306**B) having enough nitrogen elements can be formed in the thinner and the thicker film part areas A-**31** and A-**32**, respectively.

[0064] For instance, nitrogen density of 3-5% can be introduced into the vicinity of the interface between the oxide film and the semiconductor substrate in both of the thinner and the thicker film part areas A-**31** and A-**32**, if the first NO (nitric oxide) treatment using NO (2L) of 100% is executed for about 30 seconds at 1050° C. with the sheet-fed equipment after the oxide film of thickness 5.0 nm is formed as the first gate oxide film, and the second NO treatment using NO (**2**L) of 100% is executed for about 30 seconds at 1050° C. with the sheet-fed equipment after the oxide film of thickness 3.0 nm is formed as the second gate oxide film.

[0065] Generally, if the thickness of the oxide film is equal to or less than 5 nm, it is not a considerable problem that the reliability of the oxidation film is decreased by the introduction of nitrogen. Moreover, because the oxide film forming methods described above can form the oxide film with high reliability, it is hard that introduction of the nitrogen decreases the reliability of the oxide film formed by those methods.

[0066] According to the exemplary embodiment, the amount of nitrogen element introduced into the thinner film part area A-**31** and the thicker film part area A-**32** can be independently controlled. For instance, to introduce nitrogen into the thicker film part area A-**32** chiefly, the amount of the introduction of nitrogen by the second oxynitriding process only has to be decreased. Oppositely, to introduce nitrogen into the thinner film part area A-**31** chiefly, the amount of the introduction of nitrogen by the first oxynitriding process only has to be decreased. Additionally, the amount of the introduction of nitrogen is controlled by changing treatment time of the oxynitoriding process, gas pressure, and/or treatment temperature.

[0067] As mentioned above, because the amounts of the nitrogen elements in the nitride layers formed in the thinner and the thicker film part areas can be adjusted in the method of this exemplary embodiment, prevention of missing B (boron) and reduction of current leakage in the thinner film part area A-31 and improvement of characteristic regarding interface between the oxide film and the substrate in the thicker film part area A-**32** can be both achieved.

[0068] Referring to **FIGS. 6A** to **6**E, the description will be made about a second exemplary embodiment of this invention. In each of **FIGS. 6A** to **6**E, first, second and third device areas A-**61**, A-**62** and A-**63** are arranged from the left side to the right side.

[0069] At first, like the first exemplary embodiment, the first oxide film forming process and the first oxynitriding process are executed to a semiconductor substrate **601**. As a result, as shown in **FIG. 6A**, a first gate oxide film **602** is formed on the semiconductor substrate **601** while a first nitride layer **603** is formed in the first gate oxide film **602**.

[0070] Next, a first resist mask **604** is formed by means of the known method on the third device area A-**63**. By the use of the first resist mask **604**, the first gate oxide film **602** of the first and the second device areas A-**61** and A-**62** is etched as shown in **FIG. 6B**. At this time, the first nitride layer **603** is divided into a second nitride layer **603**A at the first and the second device areas A-**61** and A-**62** and a third nitride layer **603**B at the third device area A-**63**.

[0071] After the first resist mask **604** is removed from the third device area A-**63**, the second oxide film forming process and the second oxynitriding process are executed to form a second gate oxide film **605**A and a fourth nitride layer **606**A at the first and the second device areas A-**61** and A-**62** and a third gate oxide film **605**B and a fifth nitride layer **606**B at the third device area A-**63** as shown in **FIG. 6C**.

[0072] Next, a second resist mask(s) **607** is formed at the first and the third device area A-**63**. The second oxide film **605**A of the second device area A-**62** is etched by the use of the resist mask **607**. Then, the fourth nitride layer **606**A of the second device area A-**62** is changed into a sixth nitride film **606**C as shown in **FIG. 6D**.

[0073] After the resist mask **707** is removed from the first and the third device areas A-**61** and A-**63**, the third oxide film forming process and the third oxynitriding process are executed. Consequently, as shown in **FIG. 6E**, first, second and third gate oxide films **608**A, **608**B and **608**C are formed in the first, the second and the third device areas A-**61**, A-**62** and A-**63** respectively. Furthermore, first, second and third final nitride layers **609**A, **609**B and **609**C are formed in the first, the second and the third device areas A-**61**, A-**62** and A-**63** respectively.

[0074] As mentioned above, according to this exemplary embodiment, three gate oxide films different from one another in thickness can be formed. Furthermore, the final nitride layers different from one another in amount of doped nitrogen elements can be formed in the interfaces between the gate oxide films and the substrate. In other words, according to the exemplary embodiment, it is possible to make three elemental devices, such as transistors, having different (gate) oxide films in thickness and different amounts of nitrogen elements in the nitride layers at the first, the second and the third device areas of the common substrate.

[0075] Additionally, the methods used in the first embodiment can be used for the oxide film forming process, the oxynitriding process and the etching process of the second embodiment.

[0076] This invention is used for manufacturing four or more elements having different gate oxide films in thickness on a common substrate.

[0077] Though the explanation is made for manufacturing the three elemental devices different from one another in thickness of the oxide film on the substrate, this invention can be used for manufacturing four or more elemental devices different from one another in thickness of the gate oxide film on a substrate.

[0078] Referring to **FIGS. 7A** to **7**F, the description will be made about a method of manufacturing a semiconductor device according to a third exemplary embodiment. **FIGS. 7A** to **7**F are different from **FIGS. 3A** to **3**F in arrangement of device area. In each of **FIGS. 7A** to **7**F, a right hand side shows a thinner film part area A-**71** while a left hand side shows a thicker film part area A-**72**.

[0079] At first, as shown in **FIG. 7A**, a semiconductor substrate **701** is provided and dealt with a first oxide film forming process to form a first gate oxide film **702**.

[0080] Next, a first oxynitriding process is executed to the semiconductor substrate **701** with the first gate oxide film **702** to form a first nitride layer **703** in the vicinity of an interface between the semiconductor **701** and the first gate oxide film **702** as shown in **FIG. 7B**. The first nitride layer **703** is formed so that a lot of nitrogen elements are doped compared with the case of the first exemplary embodiment.

[0081] After an etching resist mask **704** is formed in the thinner film part area A-**71** as illustrated in **FIG. 7C**, the first oxide film **702** of the thicker film part area A-**72** is selectively removed as shown in **FIG. 7D**. In this event, the first nitride layer **703** is divided into second and third nitride layers **703**A and **703**B. Then, the resist mask **704** is completely removed from the thinner film part area A-**71**.

[0082] Next a second oxide film forming process is executed to form a second gate oxide film **705**A as shown in **FIG. 7E**. In this event, the first oxide film **702** of the thinner film part area A-**71** is changed into a third oxide film **705**B. The third oxide film **705**B is slightly thicker than the first oxide film **702** and thinner than the second gate oxide film **705**A. This is because introduction of a large amount of the nitrogen elements reduces an oxidation rate of the semiconductor substrate **701**.

[0083] After that, execution of a second oxynitiriding process forms fourth and fifth nitride layers **706**A and **706**B in the thicker and the thinner film part areas A-**72** and A-**71**, respectively, as shown in **FIG. 7F**.

[0084] As mentioned above, according to the exemplary embodiment, the oxide films with different thickness can be formed at the thinner and the thicker part areas of the semiconductor substrate. Furthermore, the nitride layers with sufficient nitrogen elements can be formed by the exemplary embodiment. In addition, a single layer film formed by the second gate oxide film forming process and the subsequent oxynitriding process can be assigned to the thicker film part area which needs high reliability in its oxide film while a double layer film formed by two oxide film forming processes can be assigned to the thinner film part area which needs prevention of boron leakage and reduction of current leakage rather than the high reliability in its oxide film.

[0085] The method according to this exemplary embodiment can be used for manufacturing three or more elements with different gate oxide films in thickness on a common substrate.

[0086] Referring to **FIG. 8**, a semiconductor device has a silicon substrate **801**. The silicon substrate **801** has thin and thick film regions, which are isolated by oxide films **802**. The thin and the thick film regions are shown on the left and the right sides of **FIG. 8**, respectively. Gate insulating films **803-1** and **804-1** having different thicknesses are formed on the silicon substrate **801**. Each of the gate insulating films **803-1** and **804-1** has a two layer structure including an oxide layer **805*a*** (or **805*b***) including no nitrogen atoms and a nitride layer **806*a*** (or **806*b***) disposed on the oxide layer **805*a*** (or **805*b***). The gate insulating films **803-1** and **804-1** may be different from each other in number of nitrogen atoms per unit area. The nitride layer **806*a*** (or **806*b***) may be smaller than the oxide layer **805*a*** (or **805*b***) in thickness.

[0087] The semiconductor device according to the exemplary embodiment depicted in **FIG. 8** may be manufactured by the process depicted in **FIGS. 9A-9E**. First, a silicon substrate **901** is prepared and a first oxidizing process is executed to form a gate oxide layer **902** on a silicon substrate **901** (**FIG. 9A**). Next, a first nitriding process, such as plasma nitriding, is executed to form a nitride layer **903** at a surface of the gate oxide layer **902** (**FIG. 9B**). Then, an etching process using a photo resist is executed to partially remove the nitride layer **903** and the gate oxide layer **902** from a thin film region **904** of the silicon substrate **901** (**FIG. 9C**).

[0088] Next, a second oxidizing process, such as ISSG or plasma oxidizing, is executed to form a gate oxide layer **905** on an exposed surface of the silicon substrate **901** and a surface oxide layer **906** at a surface of the nitride layer **903** (**FIG. 9D**). Finally, a second nitriding process, such as plasma nitriding, is executed to form a nitride layer **907** at a surface of the gate oxide layer **905**. The second nitriding process simultaneously nitrides the surface oxide film **906** to form a unified nitride layer **908** integrated with the nitride layer **903** (**FIG. 9E**).

[0089] In **FIGS. 9A-9E**, the elements designated by the reference numerals of **901**, **902**, **905**, **907** and **908** correspond to those designated by the reference numerals of **801**, **805*b***, **805*a***, **806*a*** and **806*b*** of **FIG. 8**, respectively.

[0090] The gate insulating films **803-1** and **804-1** have the two-layer structure including the oxide layer and the nitride layer in common. Therefore, they have equal reliability and allow matching characteristics of transistors formed in the thin and the thick film regions.

[0091] The nitride layers **806***a* and **806***b* suppress the diffusion of dopants doped in gate electrodes into the silicon substrate **801**. In addition, good controllability of dopant profile in the silicon semiconductor **801** is obtained as a relatively small heat treatment is executed to form the two-layer structure.

[0092] Referring to **FIG. 10**, a semiconductor device is similar to that of **FIG. 8** except for upper oxide layers **1001***a* and **1001***b* on the nitride layers **806***a* and **806***b*. Hereinafter the oxide layers **805***a* and **805***b* are referred as lower oxide layers to be distinguished from the upper oxide layers **1001***a* and **1001***b*. The upper oxide layer **1001***a* forms a gate insulating film **803-2** together with the lower oxide layer **805***a* and the nitride layer **806***a*. Similarly, the upper oxide layer **1001***b* forms a gate insulating film **804-2** together with the lower oxide layer **805***b* and the nitride layer **806***b*. The gate insulating films **803-2** and **804-2** are different from each other in thickness.

[0093] Each of the oxide layers **805***a*, **805***b*, **1001***a* and **1001***b* may include nitrogen atoms whose density is lower than that of the nitride layer **806***a* or **806***b* adjacent thereto. The gate insulating films **803-2** and **804-2** may be different from each other in number of nitrogen atoms per unit area. The lower oxide layer **805***a* (or **805***b*) may be different from the upper oxide layer **1001***a* (or **1001***b*) in thickness. Furthermore, when the lower oxide layer **805***a* is thinner/thicker than the upper oxide layer **1001***a*, the lower oxide layer **805***b* may be thicker/thinner than the upper oxide layer **1001***b*.

[0094] The semiconductor device according to the exemplary embodiment depicted in **FIG. 10** may be manufactured by the process depicted in **FIGS. 1A-11B**. The steps mentioned above with referring to **FIGS. 9A-9E** are executed to obtain a product depicted in **FIG. 11A** (or **FIG. 9E**). Next, a third oxidizing process, such as ISSG or plasma oxidizing, is executed to form oxide layers **1101** and **1102** at the surfaces of the nitride layers **907** and **908** (**FIG. 11B**).

[0095] In **FIG. 11B**, the elements designated by the reference numerals of **901**, **902**, **905**, **907**, **908**, **1101** and **1102** correspond to those designated by the reference numerals of **801**, **805***b*, **805***a*, **806***a*, **806***b*, **1001***a* and **101***b* of **FIG. 10**, respectively.

[0096] The gate insulating films **803-2** and **804-2** have the three layer structure including the lower and the upper oxide layers and the nitride layer between the upper and the lower oxide layers in common. Therefore, they have equal reliability and allow matching characteristics of transistors formed in the thin and the thick film regions.

[0097] The oxide layers **805***a* and **805***b* are in contact with the silicon substrate **801**. The upper oxide layers **1001***a* and **1001***b* are formed in contact with the gate electrodes (not shown in **FIG. 10**). The nitride layers **806***a* and **806***b* are between the oxide layers. Therefore, the gate insulating films **803-2** and **804-2** show high reliability in comparison with a case that the silicon substrate **801** and/or the gate electrode are/is in contact with nitride layer(s) of a gate insulating film.

[0098] The nitride layers **806***a* and **806***b* suppress diffusion of dopants doped in the gate electrode into the silicon substrate **801**. The oxide layers **805***a* and **1001***a* (or **805***b* and **1001***b*) disposed at both sides of the nitride layer **806***a* (or **806***b*) reduces internal stress caused by the nitride layer **806***a* (or **806***b*) and thereby a leakage current is suppressed. The nitride layer **806***a* (or **806***b*) causes large internal stress in the gate insulating film **803-2** and **804-2**.

[0099] Referring to **FIG. 12**, gate insulating films **803-3** and **804-3** are different from each other in thicknesses. Each of the gate insulating films **803-3** and **804-3** has a two-layer structure including a nitride layer **1201***a* (or **1201***b*) and an oxide layer **1202***a* (or **1202***b*) disposed on the nitride layer **1201***a* (or **1201***b*). Each of the oxide layers **1202***a* and **1202***b* may include nitrogen atoms whose density is smaller than that of the adjacent nitride layer **1201***a* or **1201***b*. The gate insulating films **803-3** and **804-3** may be different from each other in number of nitrogen atoms per unit area. The nitride layer **1201***a* (or **1201***b*) may be smaller than the oxide layer **1202***a* (or **1202***b*) in thickness.

[0100] The semiconductor device according to the embodiment depicted in **FIG. 12** may be manufactured by the process depicted in **FIGS. 13A-13D**. First, a silicon substrate **1301** is prepared and a first oxidizing process is executed to form a gate oxide layer **1302** on a silicon substrate **1301** (**FIG. 13A**). Next, an oxynitriding process, such as NO or N_2O treatment, is executed to form a nitride layer **1303** between the silicon substrate **1301** and the gate oxide layer **1302** (**FIG. 13B**).

[0101] Then, an etching process using a photo resist is executed to partially remove the oxide layer **1302** from a thin film region **1304** of the silicon substrate **1301** (**FIG. 13C**). Next, a second oxidizing process, such as ISSG or plasma oxidizing, is executed to form a gate oxide layer **1305** on an exposed surface of the nitride layer **1303** (**FIG. 13D**). The second oxidizing process keeps a position of the nitride layer **1303** on the interface of the silicon substrate **1301**.

[0102] In **FIG. 13D**, the elements designated by the reference numerals of **1301**, **1302**, **1303** and **1305** correspond to those designated by the reference numerals of **801**, **1202***b*, **1201***b* and **1202***a* of **FIG. 12**, respectively.

[0103] The gate insulating films **803-3** and **804-3** have the two-layer structure including the oxide layer and the nitride layer in common. Therefore, they have equal reliability and allow matching characteristics of transistors formed in the thin and the thick film regions.

[0104] The structure that the nitride layer include in the gate insulating film is in contact with the silicon substrate enlarges a range of feasible threshold voltage of transistors having the gate insulating film. Therefore, the nitride layer **1201***a* (or **1201***b*) allows manufacturing transistors having a high threshold voltage easily.

[0105] Referring to **FIG. 14**, gate insulating films **803-4** and **804-4** are different from each other in thicknesses and in structure. The gate insulating film **803-4** has a two-layer structure including a nitride layer **1401** and an oxide layer **1402** disposed on the nitride layer **1401**. On the other hand, the gate insulating film **804-4** has a three-layer structure including a pair of oxide layers **1403** and **1404** and a nitride layer **1405** disposed between the oxide layers **1403** and **1404**.

[0106] The oxide layer **1402** may include nitrogen atoms whose density is lower than that of the nitride layer **1401**. At least one of the oxide layers **1403** and **1404** may include nitrogen atoms whose density is lower than that of the nitride layer **1405**. The gate insulating films **803-4** and **804-4** may be different from each other in number of nitrogen atoms per unit area. In the gate insulating film **803-4**, the oxide layer **1402** may be disposed on the nitride layer **1401** that is disposed on the substrate **801**.

[0107] The semiconductor device according to the exemplary embodiment depicted in **FIG. 14** may be manufactured by the process depicted in **FIGS. 15A-15B**. The steps mentioned above with referring to **FIGS. 9A-9D** are executed to obtain a partly finished product depicted in **FIG. 15A** (or **FIG. 9D**).

[0108] Next, an oxynitriding process, such as NO or N_2O treatment, is executed to form a nitride layer **1501** at interface between the silicon substrate **901** and the oxide layer **905** (**FIG. 15B**). In the thick layer region, the nitride layer **903** obstructs the nitrogen atoms which are added by the oxynitriding process and moves toward the silicon substrate **901**. Consequently, the nitride layer **903** increases the thickness thereof.

[0109] In **FIG. 15B**, the elements designated by the reference numerals of **901**, **902**, **903**, **905**, **906** and **1501** correspond to those designated by the reference numerals of **801**, **1403**, **1405**, **1402**, **1404** and **1401** of **FIG. 14**, respectively.

[0110] The structure that the nitride layer include in the gate insulating film is in contact with the silicon substrate enlarges a range of feasible threshold voltage of a transistor having the gate insulating film. Therefore, the nitride layer **1501** allows manufacturing transistors having a high threshold voltage easily even if the gate insulating film is thin.

[0111] Referring to **FIG. 16**, gate insulating films **803-5** and **804-5** are different from each other in thicknesses and in structure. The gate insulating film **803-5** has a three-layer structure including a pair of nitride layers **1601** and **1602** and an oxide layer **1603** between the nitride layers **1601** and **1602**. On the other hand, the gate insulating film **804-5** has a four layer structure including two oxide films **1604** and **1605** and two nitride films **1606** and **1607** which are alternately disposed. In other words, the gate insulating film **804-5** has the three-layer structure on the oxide film **1604**.

[0112] The oxide layer **1603** may include nitrogen atoms whose density is lower than that of each of the nitride layers **1601** and **1602**. Each of the oxide layers **1604** and **1605** may include nitrogen atoms whose density is lower than that of each of the nitride layers **1606** and **1607**. The gate insulating films **803-5** and **804-5** may be different from each other in number of nitrogen atoms per unit area.

[0113] The semiconductor device according to the exemplary embodiment depicted in **FIG. 16** may be manufactured by the process depicted in **FIGS. 17A-17B**. The steps mentioned above with referring to **FIGS. 9A-9D** and **15**B are executed to obtain a partly finished product depicted in **FIG. 17A** (or **FIG. 15B**). Next, an additional nitriding process, such as plasma nitriding, is executed to form nitride layers **1701** and **1702** at surfaces of the oxide layers **905** and **906**, respectively (**FIG. 17B**).

[0114] In **FIG. 17B**, the elements designated by the reference numerals of **901**, **902**, **903**, **905**, **906**, **1501**, **1701** and **1702** correspond to those designated by the reference numerals of **801**, **1604**, **1606**, **1603**, **1601**, **1602** and **1607** of **FIG. 16**, respectively.

[0115] Because the gate insulating film **803-5** (or **804-5**) includes two nitride layers **1601** and **1602** (or **1606** and **1607**), each nitride layer can be thin in comparison with a case that a gate insulating film includes one nitride layer. Therefore, the gate insulating film **803-5** (or **804-5**) can be reduced its internal stress caused by the nitride layers **1601** and **1602** (or **1606** and **1607**) and thereby a leak current can be reduced.

[0116] The structure that the nitride layer included in the gate insulating film is in contact with the silicon substrate enlarges a range of feasible threshold voltage of transistors having the gate insulating film. Therefore, the nitride layer **1601** allows manufacturing a transistor having a high threshold voltage easily even if the gate insulating film is thin.

[0117] Referring to **FIG. 18**, gate insulating films **803-6** and **804-6** are different from each other in thicknesses and in structure. The gate insulating film **803-6** has a three-layer structure like the gate insulating film **803-2** of **FIG. 10**. The gate insulating film **803-6** includes oxide layers **1801** and **1802** and a nitride layer **1803** disposed between the oxide layers **1801** and **1802**. The gate insulating film **804-6** has a four-layer structure including nitride layers **1804** and **1805** and oxide layers **1806** and **1807** which are alternately disposed. Each of the oxide layers **1801** and **1802** may include nitrogen atoms whose density is smaller than that of the nitride layer **1803**. Each of the oxide layers **1806** and **1807** may also include nitrogen atoms whose density is smaller than that of each of the nitride layers **1804** an **1805**. The gate insulating films **803-6** and **804-6** may be different from each other in number of nitrogen atoms per unit area.

[0118] The semiconductor device according to the exemplary embodiment depicted in **FIG. 18** may be manufactured by the process depicted in **FIGS. 19A-19F**. First, a silicon substrate **1901** is prepared and a first oxidizing process is executed to form a gate oxide layer **1902** on a silicon substrate **1901** (**FIG. 19A**).

[0119] Next, an oxynitriding process, such as a NO or N_2O treatment, is executed to form a nitride layer **1903** between the silicon substrate **1901** and the gate oxide layer **1902** (**FIG. 19B**). Then, an etching process using a photo resist is executed to partially remove the oxide layer **1902** and the nitride layer **1903** from a thin film region **1904** of the silicon substrate **1901** (**FIG. 19C**).

[0120] Next, a second oxidizing process, such as ISSG or plasma oxidizing, is executed to form a gate oxide layer **1905** in the thin layer region **1904** (**FIG. 19D**). The second oxidizing process keeps a position of the nitride layer **1903** of a thick film region (at a right hand side of **FIG. 19D**) on the interface of the silicon substrate **1901**. A nitriding process, such as a plasma nitriding, is then executed to form nitride films **1906** and **1907** on the oxide layers **1905** and **1902**, respectively (**FIG. 19E**). Finally, a third oxidizing process, such as ISSG or plasma oxidizing, is executed to form oxide layers **1908** and **1909** on the nitride films **1906** and **1907**, respectively (**FIG. 19F**).

[0121] In **FIG. 19F**, the elements designated by the reference numerals of **1901**, **1902**, **1903**, **1905**, **1906**, **1907**,

1908 and **1909** correspond to those designated by the reference numerals of **801**, **1806**, **1804**, **1801**, **1803**, **1805**, **1802**, and **1807** of **FIG. 18**, respectively.

[**0122**] Because the gate insulating film **804-6** includes two nitride layers **1804** and **1805**, each nitride layer can be thin in comparison with a single nitride layer structure case that a gate insulating film includes one nitride layer. Therefore, the gate insulating film **804-6** can reduce internal stress caused by the nitride layers **1804** and **1805** and thereby a leakage current can be reduced.

[**0123**] Referring to **FIG. 20**, gate insulating films **803-7** and **804-7** are different from each other in thicknesses. Each of the gate insulating films **803-7** and **804-7** has a four layer structure including oxide layers **2001***a* and **2002***a* (or **2001***b* and **2002***b*) and nitride layers **2003***a* and **2004***a* (or **2003***b* and **2004***b*) which are alternately disposed.

[**0124**] Each of the oxide layers **2001***a* and **2002***a* may include nitrogen atoms whose density is lower than that of each of the nitride layers **2003***a* and **2004***a*. Similarly, each of the oxide layers **2001***b* and **2002***b* may include nitrogen atoms whose density is lower than that of each of the nitride layers **2003***b* and **2004***b*. The gate insulating films **803-7** and **804-7** may be different from each other in number of nitrogen atoms per unit area.

[**0125**] The semiconductor device according to the exemplary embodiment depicted in **FIG. 20** may be manufactured by the process depicted in **FIGS. 21A-21B**. The steps mentioned above with referring to **FIGS. 9A-9E** and **11**B are executed to obtain a partly finished product depicted in **FIG. 21A** (or **FIG. 11B**). Next, a third nitriding process, such as plasma nitriding, is executed to form nitride layers **2101** and **2102** at surfaces of the oxide layers **1101** and **1102**, respectively (**FIG. 21B**).

[**0126**] In **FIG. 21B**, the elements designated by the reference numerals of **901**, **902**, **905**, **907**, **908**, **1101**, **1102**, **2101** and **2102** correspond to those designated by the reference numerals of **801**, **2001***b*, **2001***a*, **2003***a*, **2003***b*, **2002***a*, **2002***b*, **2004***a* and **2004***b* of **FIG. 20**, respectively.

[**0127**] Because the gate insulating film **803-7** (or **804-7**) includes two nitride layers **2003***a* and **2003***b*, each nitride layer can be thin in comparison with the case that a gate insulating film includes one nitride layer. Therefore, the gate insulating film **803-7** (or **804-7**) can reduce internal stress caused by the nitride layers **2003***a* and **2004***a* (or **2003***b* and **2004***b*) and thereby a leak current can be reduced.

[**0128**] Referring to **FIG. 22**, gate insulating films **803-8** and **804-8** are different from each other in thicknesses and in structure. The gate insulating film **803-8** has a four-layer structure like the gate insulating film **803-7** of **FIG. 20**. The gate insulating film **803-8** includes oxide layers **2201** and **2202** and nitride layers **2203** and **2204** which are alternately disposed. The gate insulating film **804-8** has a five-layer structure including nitride layers **2205**, **2206** and **2207** and oxide layers **2208** and **2209** which are alternately disposed. Each of the oxide layers **2201** and **2202** may include nitrogen atoms whose density is smaller than that of each of the nitride layers **2202** and **2204**. Each of the oxide layers **2208** and **2209** may include nitrogen atoms whose density is smaller than that of each of the nitride layers **2205**, **2206** and **2207**. The gate insulating films **803-8** and **804-8** may be different from each other in number of nitrogen atoms per unit area. Furthermore, the gate insulating films **803-8** and **804-8** may be different from each other in number of nitrogen layers.

[**0129**] The semiconductor device according to the exemplary embodiment depicted in **FIG. 22** may be manufactured by the process depicted in **FIGS. 23A-23B**. The steps mentioned above with referring to **FIGS. 19A-19F** are executed to obtain a partly finished product depicted in **FIG. 23A** (or **FIG. 19F**). Next, an additional nitriding process, such as a plasma nitriding, is executed to form nitride films **2301** and **2302** on the oxide layers **1908** and **1909**, respectively (**FIG. 23B**).

[**0130**] In **FIG. 23B**, the elements designated by the reference numerals of **1901**, **1902**, **1903**, **1905**, **1906**, **1907**, **1908**, **1909**, **2301** and **2302** correspond to those designated by the reference numerals of **801**, **2208**, **2205**, **2201**, **2203**, **2206**, **2202**, **2209**, **2204** and **2207** of **FIG. 22**, respectively.

[**0131**] Because the gate insulating film **804-8** includes three nitride layers **2205**, **2206** and **2207**, each nitride layer can be thin in comparison with the case that the gate insulating film includes two nitride layers. Therefore, the gate insulating film **804-8** can further reduce internal stress caused by the nitride layers **2205**, **2207** and **2208** and thereby a leak current can be reduced.

[**0132**] In addition, an increase of the number of nitride layers in the gate insulating film improves the ability of the suppressing diffusion of the dopants from the gate electrode into the silicon substrate **801**.

[**0133**] Though each of the exemplary embodiments mentioned above includes two regions having different thicknesses, this invention may be applied to a device which includes three or more regions having different thickness.

[**0134**] The gate insulating films may be used for MOSFETs.

[**0135**] While this invention has thus far been described in conjunction with the exemplary embodiments thereof, it will readily be possible for those skilled in the art to put this invention into practice in various other manners.

[**0136**] While the invention has been described in terms of several exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

[**0137**] Further, it is noted that, Applicants' intent is to encompass equivalents of all claim elements, even if amended later during prosecution.

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein each of said gate insulating films includes a two-layer structure comprising an oxide layer and a nitride layer disposed on said oxide layer.

2. A semiconductor device as claimed in claim 1, wherein said gate insulating films are different from each other in number of nitrogen atoms per unit area.

3. A semiconductor device as claimed in claim 1, wherein said nitride layer is thinner than said oxide layer in one of said gate insulating films.

4. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein each of said gate insulating films includes a three layer structure including lower and upper oxide layers and a nitride layer disposed between said lower and said upper oxide layers.

5. A semiconductor device as claimed in claim 4, wherein one of said lower and said upper oxide layers includes nitrogen atoms whose density is lower than that of said nitride layer.

6. A semiconductor device as claimed in claim 4, wherein said gate insulating films are different from each other in number of nitrogen atoms per unit area.

7. A semiconductor device as claimed in claim 4, wherein said lower and said upper oxide layers have different thicknesses in one of said gate insulating films.

8. A semiconductor device as claimed in claim 4, wherein said lower oxide layer is thinner than said upper oxide layer in one of said gate insulating films, and said lower oxide layer is thicker than said upper oxide layer in the other of said gate insulating films.

9. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein each of said gate insulating films includes a two-layer structure comprising a nitride layer and an oxide layer disposed on said nitride layer.

10. A semiconductor device as claimed in claim 9, wherein said oxide layer includes nitrogen atoms whose density is lower than that of said nitride layer.

11. A semiconductor device as claimed in claim 9, wherein one of said gate insulating films is different from the other in number of nitrogen atoms per unit area.

12. A semiconductor device as claimed in claim 9, wherein said nitride layer is thinner than said oxide layer in one of said gate insulating films.

13. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein one of said gate insulating films includes a two layer structure comprising a first nitride layer and a first oxide layer, and

wherein the other of said gate insulating films includes a three layer structure comprising second and third oxide layers and a second nitride layer disposed between said second and said third oxide layers.

14. A semiconductor device as claimed in claim 13, wherein each of said first, said second and said third oxide layers includes nitrogen atoms whose density is lower than that of an adjacent one of said first and said second nitride layers.

15. A semiconductor device as claimed in claim 13, wherein one of said gate insulating films is different from the other in number of nitrogen atoms per unit area.

16. A semiconductor device as claimed in claim 13, wherein said first oxide layer is disposed on said first nitride layer.

17. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein one of said gate insulating films includes a three layer structure comprising first and second nitride layers and an oxide layer disposed between said first and said second nitride layers.

18. A semiconductor device as claimed in claim 17, wherein said oxide layer includes nitrogen atoms whose density is lower than that of each of said first and said second nitride layers.

19. A semiconductor device as claimed in claim 17, wherein the other of said gate insulating films includes at least one nitride layer, and

wherein said gate insulating films are different from each other in number of nitrogen atoms per unit area.

20. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein one of said gate insulating films includes a four layer structure comprises a lower nitride layer, a lower oxide layer disposed on said lower nitride layer, an upper nitride layer disposed on said lower oxide layer and an upper oxide layer disposed on said upper nitride layer.

21. A semiconductor device as claimed in claim 20, wherein each of said lower and said upper oxide layers includes nitrogen atoms whose density is lower than that of each of said lower and said upper nitride layers.

22. A semiconductor device as claimed in claim 20, wherein the other of said gate insulating films includes a nitride layer, and

wherein said gate insulating films are different from each other in number of nitrogen atoms per unit area.

23. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein one of said gate insulating films includes a four layer structure comprising a lower oxide layer, a lower nitride layer disposed on said lower oxide layer, an upper oxide layer disposed on said lower nitride layer and an upper nitride layer disposed on said upper oxide layer.

24. A semiconductor device as claimed in claim 23, wherein each of said lower and said upper oxide layers includes nitrogen atoms whose density is lower than that of each of said lower and said upper nitride layers.

25. A semiconductor device as claimed in claim 23, wherein the other of said gate insulating films includes a nitride layer, and

wherein said gate insulating films are different from each other in number of nitrogen atoms per unit area.

26. A semiconductor device, comprising:

a semiconductor substrate; and

two gate insulating films having different thicknesses on said semiconductor substrate,

wherein one of said gate insulating films includes a five-layer structure comprising three nitride layers and two oxide layers which are alternately disposed.

27. A semiconductor device as claimed in claim 26, wherein each of said oxide layers includes nitrogen atoms whose density is lower than that of each of said nitride layers.

28. A semiconductor device as claimed in claim 26, wherein the other of said gate insulating films includes a nitride layer, and

wherein said gate insulating films are different from each other in number of nitrogen atoms per unit area.

29. A semiconductor device as claimed in claim 26, wherein the other of said gate insulating films includes a nitride layer, and

wherein said gate insulating films are different from each other in number of nitrogen layers.

30. A semiconductor device having two gate insulating film different from each other in thickness, produced by a process comprising:

executing a first oxide process for forming a first oxide layer;

executing a nitriding process for forming a nitride layer;

executing an etching process for partially etching the first oxide layer; and

executing a second oxide process for forming a second oxide layer.

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