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(54) Title: TEMPERATURE VARIATION COMPENSATION OF A MEMORY

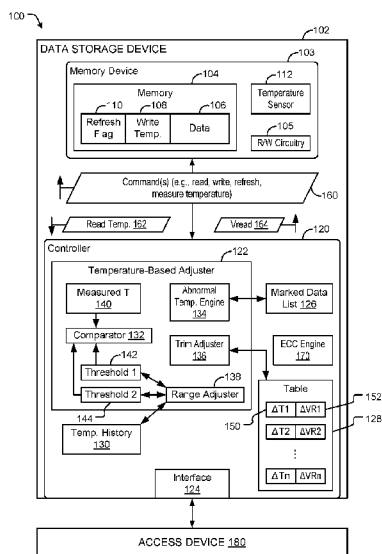


FIG. 1

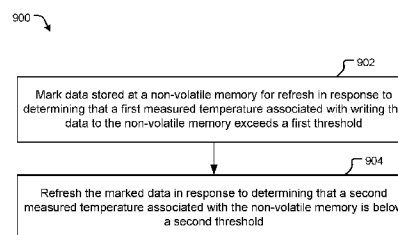


FIG. 9

(57) Abstract: A data storage device is configured to mark data for refresh in response to determining that a first measured temperature associated with writing the data to the memory exceeds a first threshold. The data storage device is further configured to refresh the marked data in response to determining that a second measured temperature associated with the memory is below a second threshold.



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TEMPERATURE VARIATION COMPENSATION OF A MEMORY**CROSS-REFERENCE TO RELATED APPLICATIONS**

The present application claims priority from U.S. Application No. 15/167,316 filed May 27, 2016, which claims the benefit of U.S. Provisional Application No. 62/303,891,
5 filed March 4, 2016, the contents of each of which are incorporated by reference herein in their entirety.

FIELD OF THE DISCLOSURE

This disclosure is generally related to data storage devices and more particularly to temperature variation compensation techniques.

BACKGROUND

Non-volatile data storage devices, such as flash solid state drive (SSD) memory devices or removable storage cards, have allowed for increased portability of data and software applications. Flash memory devices can enhance data storage density by storing multiple bits in each flash memory cell. For example, Multi-Level Cell (MLC) flash
15 memory devices provide increased storage density by storing 2 bits per cell, 3 bits per cell, 4 bits per cell, or more. Although increasing the number of bits per cell and reducing device feature dimensions may increase a storage density of a memory device, a bit error rate (BER) of data stored at the memory device may also increase.

In addition, increased BER due to temperature changes between programming
20 temperature (e.g., a temperature of a memory when data is written to the memory) and later reading temperature (e.g., a temperature of the memory when the data is read from the memory) is becoming an increasingly significant issue in recent memory generations. Because each storage element of a non-volatile data storage device may have a distinct cross temperature coefficient, each storage element may exhibit a
25 different threshold voltage (V_t) shift due to a temperature change relative to the temperature at which the storage element was programmed and verified. The V_t shift per storage element is a function of the temperature difference. As a result, reading a page at a different temperature than the programming temperature of the page results in shifting and widening of the cell voltage distributions (CVDs) of the different states of

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the storage devices and in an increased BER. Shifting and widening of the CVDs and increased BER arises in both temperature change directions, such as when data is read from storage elements at a higher temperature than the data was written to the storage elements, and also when the data is read from storage elements at a lower temperature
5 than the data was written to the storage elements.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an illustrative example of a system including a data storage device configured to adjust memory access parameters based on temperature;

FIG. 2 is a diagram illustrating a particular examples of temperature ranges associated
10 with the data storage device of FIG. 1;

FIG. 3 is a diagram illustrating a particular example of tables that may be used by the data storage device of FIG. 1;

FIG. 4 is a diagram illustrating a particular example of a first configuration of multiple memory dies of the data storage device of FIG. 1;

15 FIG. 5 is a diagram illustrating a particular example of a second configuration of multiple memory dies of the data storage device of FIG. 1;

FIG. 6 is a block diagram of an illustrative example of the data storage device of FIG. 1;

FIG. 7 is a block diagram of another illustrative example of the data storage device of FIG. 1;

20 FIG. 8 is a diagram illustrating a particular example of a configuration of a memory device of the data storage device of FIG. 1;

FIG. 9 is a flow diagram of a particular example of a method of refreshing data that may be performed by the data storage device of FIG. 1;

FIG. 10 is a flow diagram of a particular example of a method of temperature-based
25 control that may be performed by the data storage device of FIG. 1;

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FIG. 11 is a flow diagram of another particular example of a method of temperature-based control that may be performed by the data storage device of FIG. 1;

FIG. 12 is a flow diagram of another particular example of a method of determining a read voltage value that may be performed by the data storage device of FIG. 1;

- 5 FIG. 13 is a flow diagram of another particular example of a method of temperature-based control that may be performed by the data storage device of FIG. 1; and

FIG. 14 is a flow diagram of another particular example of a method of determining a temperature range that may be performed by the data storage device of FIG. 1.

DETAILED DESCRIPTION

- 10 Devices and methods provide compensation for shifting and widening of V_t levels due to differences of programming temperatures as compared to reading temperature variations. For example, a “write temperature” may be measured and stored during programming of data. To illustrate, a write temperature may be stored once for each programmed block (e.g., an erase block of an NAND flash memory) or once for each
15 programmed word line (WL), as non-limiting examples. In some implementations, if the programming temperature is in an “abnormal” range, a compensation scheme may be performed.

- In some implementations, during reading data, a “read temperature” for each read block or WL may be measured. One or more memory access parameters, such as read
20 threshold voltages, may be adjusted based on tracking the CVD, based on BER, based on tables that are based on the difference between the write temperature and the read temperature, or any combination thereof, as illustrative, non-limiting examples.

- In some implementations, when an “abnormal” programming temperature is detected, one of more compensation schemes may be performed. For example, the “abnormal”
25 programmed data may be marked for “urgent” refresh. To illustrate, marking the data for “urgent” refresh may cause a data storage device to refresh the marked data as a high priority task in response to detecting that the memory temperature has returned to the “normal” temperature range. As another example, the “abnormal” programmed data may be stored using a slower and more reliable trim (e.g., a set of write parameters that

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cause data to be written with increased accuracy). As other examples, the "abnormal" programmed data may be stored using a SLC mode instead of using an MLC mode, may be stored as multiple redundant copies, may be protected using a greater number of parity bits, or any combination thereof.

- 5 In some implementations, non-volatile memory (NVM) cell V_t shifting may be compensated by adjusting read thresholds. Adjusting read thresholds may be performed based on the difference between the temperature measured during reading compared to the temperature logged during programming (which may be measured and stored per block or per word line (WL)). The read thresholds adjustment value may also be a
- 10 function of the logged programming temperature (and not only of the temperature difference), in case the shifting is different when programming at low temperature vs. high temperature. The read thresholds adjustment may be performed using a predefined table as a function of the temperature difference and optionally as a function of the programming temperature. Alternatively, read thresholds adjustment may be performed
- 15 by running a read thresholds calibrations algorithm, such as CVD tracking or BER Estimation Scan (BES), on representative page(s) from the block(s) that were programmed at the same temperature.

- If "extreme" temperature differences are rare events, then foreground CVD tracking or BES method may provide accurate results with relatively low complexity because
- 20 logging and managing the programming temperature per WL or per block may be omitted. If such extreme temperature differences are expected to occur more frequently, accurate results with enhanced performance may be provided by measuring and storing write temperatures and adjusting for temperature differences as compared to performing foreground CVD tracking or BES operations. Alternatively, groups of blocks or WLs
- 25 that were programmed roughly at the same time and temperature may be associated with a certain time & temperature tag for which an appropriate set of read or memory access parameters may be maintained. The read or memory access parameters of the group associated with a given time & temperature tag may be adjusted from time to time by running a read thresholds calibrations algorithm, such as CVD tracking or BES, on
- 30 representative page(s) from the group. This may be performed as a background maintenance process, or triggered when suboptimal read or memory access parameters are encountered (e.g. high BER encountered during a host read).

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The above operations (e.g., CVD tracking, BES operations, storing write temperatures and adjusting read voltages based on temperature change) may be used to compensate for the V_t shifting due to programming vs. reading temperature differences. However, use of such operations may still result in increased BER due to V_t distribution widening.

5 V_t distribution widening may be compensated as in the following example.

In an example implementation of V_t distribution widening compensation, the maximal temperature difference that the memory allows is 80 degrees Celsius (80°C). Because the maximum allowed temperature difference is 80°C, successful reading of any data experiencing a write/read temperature difference above 80°C is not guaranteed, even
10 after read thresholds adjustment/shifting. In this case, a "normal" operating temperature range may be defined as the temperature range spanning from 5°C to 65°C. Anything programmed outside of this normal temperature range receives "special treatment," such as one or more of the operations described above (e.g., marked for urgent refresh, stored using a slower and more reliable trim, stored using a SLC mode instead of using an
15 MLC mode, stored as multiple redundant copies, protected using a greater number of parity bits). Because programming data outside the "normal" temperature range may be expected to be a rare event, the "special treatment" may be implemented for a small fraction of the traffic and therefore has minor overall impact on device performance.

If data is programmed at a temperature that is outside of the "normal" temperature
20 range, the data is protected more carefully by one of the options above (or refreshed urgently once temperature gets back in the normal range). On the other hand, if the data is programmed at a temperature that is inside of the "normal" temperature range, even if the data is read at an extreme temperature outside the normal range (e.g., at -25°C or at 85°C), the maximal temperature difference between writing the data and reading the
25 data does not exceed the allowed 80°C difference.

Additional temperature ranges may be implemented. For example, there may be a "normal" temperature range and several "abnormal" temperature ranges, from a slightly out of range temperature to an extreme out of range temperature. The countermeasures ("special treatment") taken when programming outside of the "normal" temperature
30 range may be adjusted based on the specific temperature range (i.e. based on how different it is from the "normal" temperature range). For example, a nominal

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programming trim ("trim0") may be used for programming when in the "normal" temperature range. A slower and finer trim ("trim1") may be used for programming when in a slightly "abnormal" temperature range. An even slower and finer trim ("trim2") may be used for programming when in an extreme "abnormal" temperature range.

The temperature ranges (both "normal" and "abnormal") may be predefined. Alternatively, they may be adjusted dynamically, either per region of the memory or adaptively by a controller of the memory. For example, the controller may track the temperature range at which most of the traffic is being programmed and define this range as the "normal" temperature range.

Optionally, a hybrid partition may be used to store one or more additional copies of data stored at an "extreme" temperature instead of moving the data if the amount of data written at the "extreme" temperature is relatively small. A decoder that includes an error correction coding (ECC) engine may be used to decode the two or more copies and retrieve the data. The LLR inputs for the decoder may be based on the two copies, such as be summing the LLRs of the two copies. This is equivalent to assigning high reliability to bits for which the two copies agree and low reliability (or zero reliability, if both copies have same reliability) whenever the two copies disagree.

In some implementations, in order to prevent wide programming temperature variations within a block, partially written open blocks may be closed in response to a change in programming temperature changes above some value. Closing the blocks avoids a mixture of data programmed in various temperatures that may be problematic, and especially in an abnormal temperature region, such as described in further detail with reference to FIGs. 4-5. Boundary word lines /string lines may be "padded" by writing dummy data isolating the boundary WLs and thus protecting the boundary WLs from temperature cross effect, as described with reference to FIG. 4. Optionally, affected boundary string lines/WLs may be evacuated immediately or within a short time after a decision is made to prematurely close a block with high priority.

In some implementations, rather than storing memory access parameters (e.g., read voltages) corresponding to specific temperatures or temperature ranges, offset values may instead be used. For example, when programming data at a given temperature,

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there is a set of read parameters that is “optimum” for reading the data at the given temperature. This temperature can be recorded at the system level, and the “optimum” read condition can also be calculated or determined (e.g., by means of CVD tracking or BES). When the data is read, the read temperature can be measured. If the
5 temperature difference between the write temperature and the read temperature is larger than a threshold, then a read offset may be applied to the original read condition (e.g., as an adjustment from the “optimum” read parameter) so that the resulting read parameters enable a more accurate read of the data based on the temperature difference. If the temperature difference is relatively small, then the data may be
10 accessed with the original reading condition without any offset compensation.

After generating adjusted read parameters based on the temperature difference and reading the data, a BER for the data may be determined. If the BER is above a threshold (e.g., exceeds an error correction capacity of the ECC scheme that encodes the data), then the original read condition may be inadequate, or the offset may be
15 inadequate. In this case, read parameters may be calibrated via CVD tracking or BES and data may be read again with the calibrated parameters with a reduced number of errors.

In some implementations, temperature compensation may not be applied other than during “heroics” when a BER of data read from the memory renders the data
20 undecodable. In such cases, application of offset values to read parameters based on the temperature difference may enable the data to be read with reduced BER. In some implementations, temperature compensation may be applied in response to detecting a pattern of relatively-high BER during a sequence of read operations. For example, in response to a sequence of reads from the memory resulting in high (but still
25 correctable) BER, a memory controller may read a write temperature associated with the data and may apply a read voltage offset based on the temperature difference for remaining read operations of the sequence, as described in further detail with reference to FIG. 7.

Particular examples in accordance with the disclosure are described below with
30 reference to the drawings. In the description, common features are designated by common reference numbers. As used herein, “exemplary” may indicate an example, an

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implementation, and/or an aspect, and should not be construed as limiting or as indicating a preference or a preferred implementation. Further, it is to be appreciated that certain ordinal terms (e.g., “first” or “second”) may be provided for identification and ease of reference and do not necessarily imply physical characteristics or ordering.

5 Therefore, as used herein, an ordinal term (e.g., “first,” “second,” “third,” etc.) used to modify an element, such as a structure, a component, an operation, etc., does not necessarily indicate priority or order of the element with respect to another element, but rather distinguishes the element from another element having a same name (but for use of the ordinal term). In addition, as used herein, indefinite articles (“a” and “an”) may
10 indicate “one or more” rather than “one.” As used herein, a structure or operation that “comprises” or “includes” an element may include one or more other elements not explicitly recited. Further, an operation performed “based on” a condition or event may also be performed based on one or more other conditions or events not explicitly recited.

FIG. 1 depicts an illustrative example of a system 100 that includes a data storage
15 device 102 and an access device 180 (e.g., a host device or another device). The data storage device 102 includes a temperature-based adjuster 122 that is configured to perform compensation based on temperature differences between writing data to a memory 104 and reading the data from the memory 104. The temperature-based
20 adjuster 122 is also configured to perform compensation based on a programming temperature (e.g., a temperature of the memory 104 that is measured just before, during, or after data is written into the memory 104) being outside of a “normal” temperature range.

The data storage device 102 and the access device 180 may be coupled via a connection (e.g., a communication path), such as a bus or a wireless connection. The data storage
25 device 102 may include a first interface 124 (e.g., an access device or host interface) that enables communication via the communication path between the data storage device 102 and the access device 180.

The data storage device 102 may include or correspond to a solid state drive (SSD) which may be included in, or distinct from (and accessible to), the access device 180.
30 For example, the data storage device 102 may include or correspond to an SSD, which may be used as an embedded storage drive (e.g., a mobile embedded storage drive), an

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enterprise storage drive (ESD), a client storage device, or a cloud storage drive, as illustrative, non-limiting examples. In some implementations, the data storage device 102 is coupled to the access device 180 indirectly, e.g., via a network. For example, the network may include a data center storage system network, an enterprise storage system network, a storage area network, a cloud storage network, a local area network (LAN), a wide area network (WAN), the Internet, and/or another network. In some implementations, the data storage device 102 may be a network-attached storage (NAS) device or a component (e.g., a solid-state drive (SSD) device) of a data center storage system, an enterprise storage system, or a storage area network.

10 In some implementations, the data storage device 102 may be embedded within the access device 180, such as in accordance with a Joint Electron Devices Engineering Council (JEDEC) Solid State Technology Association Universal Flash Storage (UFS) configuration. For example, the data storage device 102 may be configured to be coupled to the access device 180 as embedded memory, such as eMMC® (trademark of
15 JEDEC Solid State Technology Association, Arlington, Virginia) and eSD, as illustrative examples. To illustrate, the data storage device 102 may correspond to an eMMC (embedded MultiMedia Card) device. As another example, the data storage device 102 may correspond to a memory card, such as a Secure Digital (SD®) card, a microSD® card, a miniSD™ card (trademarks of SD-3C LLC, Wilmington, Delaware),
20 a MultiMediaCard™ (MMC™) card (trademark of JEDEC Solid State Technology Association, Arlington, Virginia), or a CompactFlash® (CF) card (trademark of SanDisk Corporation, Milpitas, California). Alternatively, the data storage device 102 may be removable from the access device 180 (i.e., “removably” coupled to the access device 180). As an example, the data storage device 102 may be removably coupled to
25 the access device 180 in accordance with a removable universal serial bus (USB) configuration.

The data storage device 102 may operate in compliance with an industry specification. For example, the data storage device 102 may include a SSD and may be configured to communicate with the access device 180 using a small computer system interface
30 (SCSI)-type protocol, such as a serial attached SCSI (SAS) protocol. As other examples, the data storage device 102 may be configured to communicate with the access device 180 using a NVM Express (NVMe) protocol or a serial advanced

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technology attachment (SATA) protocol. In other examples, the data storage device 102 may operate in compliance with a JEDEC eMMC specification, a JEDEC Universal Flash Storage (UFS) specification, one or more other specifications, or a combination thereof, and may be configured to communicate using one or more protocols, such as an
5 eMMC protocol, a universal flash storage (UFS) protocol, a universal serial bus (USB) protocol, and/or another protocol, as illustrative, non-limiting examples.

The access device 180 may include a memory interface (not shown) and may be configured to communicate with the data storage device 102 via the memory interface to read data from and write data to the memory device 103 of the data storage device 102.
10 For example, the access device 180 may be configured to communicate with the data storage device 102 using a SAS, SATA, or NVMe protocol. As other examples, the access device 180 may operate in compliance with a Joint Electron Devices Engineering Council (JEDEC) industry specification, such as a Universal Flash Storage (UFS) Access Controller Interface specification. The access device 180 may communicate
15 with the memory device 103 in accordance with any other suitable communication protocol.

The access device 180 may include a processor and a memory. The memory may be configured to store data and/or instructions that may be executable by the processor. The memory may be a single memory or may include multiple memories, such as one or
20 more non-volatile memories, one or more volatile memories, or a combination thereof. The access device 180 may issue one or more commands to the data storage device 102, such as one or more requests to erase data, read data from, or write data to the memory device 103 of the data storage device 102. For example, the access device 180 may be configured to provide data, such as data 182, to be stored at the memory device 103 or
25 to request data to be read from the memory device 103. The access device 180 may include a mobile telephone, a computer (e.g., a laptop, a tablet, or a notebook computer), a music player, a video player, a gaming device or console, an electronic book reader, a personal digital assistant (PDA), a portable navigation device, a computer, such as a laptop computer or notebook computer, a network computer, a
30 server, any other electronic device, or any combination thereof, as illustrative, non-limiting examples.

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The memory device 103 of the data storage device 102 may include one or more memory dies (e.g., one memory die, two memory dies, eight memory dies, or another number of memory dies). The memory device 103 includes a memory 104, such as a non-volatile memory of storage elements included in a memory die of the memory
5 device 103. For example, the memory 104 may include a flash memory, such as a NAND flash memory, or a resistive memory, such as a resistive random access memory (ReRAM), as illustrative, non-limiting examples. In some implementations, the memory 104 may include or correspond to a memory die of the memory device 103. The memory 104 may have a three-dimensional (3D) memory configuration. As an
10 example, the memory 104 may have a 3D vertical bit line (VBL) configuration. In a particular implementation, the memory 104 is a non-volatile memory having a 3D memory configuration that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate. Alternatively, the memory 104 may have another configuration, such as a two-
15 dimensional (2D) memory configuration or a non-monolithic 3D memory configuration (e.g., a stacked die 3D memory configuration).

Although the data storage device 102 is illustrated as including the memory device 103, in other implementations the data storage device 102 may include multiple memory devices that may be configured in a similar manner as described with respect to the
20 memory device 103. For example, the data storage device 102 may include multiple memory devices, each memory device including one or more packages of memory dies, each package of memory dies including one or more memories such as the memory 104. Data striping and error recovery as described with respect to pages of the memory 104 may be extended to include data striping and error recovery across multiple dies, across
25 multiple packages, across multiple memory devices, or any combination thereof.

The memory 104 may include one or more blocks, such as a NAND flash erase group of storage elements. Each storage element of the memory 104 may be programmable to a state (e.g., a threshold voltage in a flash configuration or a resistive state in a resistive memory configuration) that indicates one or more values. Each block of the memory
30 104 may include one or more word lines. Each word line may include one or more pages, such as one or more physical pages. In some implementations, each page may be configured to store a codeword. A word line may be configurable to operate as a single-

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level-cell (SLC) word line, as a multi-level-cell (MLC) word line, or as a tri-level-cell (TLC) word line, as illustrative, non-limiting examples.

The memory device 103 may include support circuitry, such as read/write circuitry 105, to support operation of one or more memory dies of the memory device 103. Although
5 depicted as a single component, the read/write circuitry 105 may be divided into separate components of the memory device 103, such as read circuitry and write circuitry. The read/write circuitry 105 may be external to the one or more dies of the memory device 103. Alternatively, one or more individual memory dies of the memory device 103 may include corresponding read/write circuitry that is operable to read data
10 from and/or write data to storage elements within the individual memory die independent of any other read and/or write operations at any of the other memory dies.

The controller 120 is coupled to the memory device 103 via a bus, an interface (e.g., interface circuitry), another structure, or a combination thereof. For example, the bus may include one or more channels to enable the controller 120 to communicate with a
15 single memory die of the memory device. As another example, the bus may include multiple distinct channels to enable the controller 120 to communicate with each memory die of the memory device 103 in parallel with, and independently of, communication with other memory dies of the memory device 103.

The controller 120 is configured to receive data and instructions from the access device
20 180 and to send data to the access device 180. For example, the controller 120 may send data to the access device 180 via the first interface 124, and the controller 120 may receive data from the access device 180 via the first interface 124. The controller 120 is configured to send data and commands to the memory 104 and to receive data from the memory 104. For example, the controller 120 is configured to send data and a write
25 command to cause the memory 104 to store data to a specified address of the memory 104. The write command may specify a physical address of a portion of the memory 104 (e.g., a physical address of a word line of the memory 104) that is to store the data. The controller 120 may also be configured to send data and commands to the memory 104 associated with background scanning operations, garbage collection operations,
30 and/or wear leveling operations, etc., as illustrative, non-limiting examples. The controller 120 is configured to send a read command to the memory 104 to access data

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from a specified address of the memory 104. The read command may specify the physical address of a portion of the memory 104 (e.g., a physical address of a word line of the memory 104).

The memory device 103 may also include a temperature sensor 112. For example, the temperature sensor will 112 may be configured to measure a temperature and may be configured to provide an indication of the measured temperature to the controller 120, such as a read temperature 162. For example, the temperature sensor 112 may be responsive to one or more commands 160, such as a command to measure temperature. The memory device 103 may include a single temperature sensor 112, or may include multiple temperatures sensors. For example, in an implementation with a memory device 103 that includes multiple memory dies, each of the multiple memory dies may include a separate temperature sensor 112 such as described with reference to FIG. 8. Each of the temperature sensors 112 may be independently polled by the controller 120 to provide a respective temperature 162 for the associated memory die.

The memory 104 is illustrated as including representative data 106. For example, the data 106 may include encoded data, such as an ECC codeword, that is written to one or more word lines in one or more blocks of the memory 104. The memory 104 may also store a write temperature 108 associated with the data 106. For example, the write temperature 108 may indicate a temperature measurement corresponding to the memory device 103 at a time the data 106 was written to the memory 104. For example, the write temperature 108 may be determined currently with, prior to, or following programming of the data 106 to the memory 104. The write temperature 108 may be stored in a block or word line as metadata in the block header or the word line header.

The memory 104 also includes a refresh flag 110 associated with the data 106. As discussed in further detail below, the refresh flag 110 may indicate the data 106 was stored when a temperature at the memory 104 was in an abnormal temperature range. The refresh flag 110 may be accessed by the controller 120 to identify the data 106 as a target for refresh when the temperature of the memory 104 falls below a particular threshold temperature.

The controller 120 includes a temperature based adjuster 122, a marked data list 126, an ECC engine 170, a temperature history 130, and data structure (e.g., a table 148) that

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associates temperature differences to read voltage parameters. The ECC engine 170 is configured to receive data to be stored to the memory 104 and to generate a codeword. For example, the ECC engine 170 may include an encoder configured to encode data using an ECC scheme, such as a Reed Solomon encoder, a Bose-Chaudhuri-

5 Hocquenghem (BCH) encoder, a low-density parity check (LDPC) encoder, a Turbo Code encoder, an encoder configured to encode one or more other ECC encoding schemes, or any combination thereof. The ECC engine 170 may include one or more decoders configured to decode data read from the memory 104 to detect and correct, up to an error correction capability of the ECC scheme, any bit errors that may be present
10 in the data.

The temperature based adjuster 122 is configured to perform one or more operations to adjust for differences between write temperatures and read temperatures of data written into and/or read from the memory 104. For example, the temperature based adjuster 122 includes a comparator 132 configured to compare a measured temperature 140 to
15 one or more thresholds, illustrated as a first threshold 142 and a second threshold 144. For example, when the measured temperature 140 corresponds to a temperature at the time of writing data to the memory 104, such as a temperature retrieved from the temperature sensor 122 in response to receiving the data 106 at the controller 120 to be written to the memory device 103, in response to the comparator 132 determining that
20 the measured temperature 140 exceeds the first threshold 132, the abnormal temperature engine 134 may be activated.

The abnormal temperature engine 134 may be configured to perform one or more operations associated with writing data to the memory 104 when a temperature of the memory 104 is in an abnormal range. For example, the abnormal temperature engine
25 134 may be responsive to the comparator 132 to add the refresh flag 110 to be stored at the memory 104 in conjunction with the data 106, to store an indication of the data 106 to the marked data list 126, to initiate one or more other actions, or any combination thereof. For example, the one or more other actions that may be initiated by the abnormal temperature engine 134 may correspond to designating that the data to be
30 stored needs to be encoded using a higher number of parity bits at the ECC engine 170 than data that is stored when the temperature is not in the abnormal temperature range. Alternatively, or in addition, the abnormal temperature engine 134 may cause data to be

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stored in the memory 104 in a single level cell (SLC) mode instead of a multilevel cell (MLC) mode, with multiple copies of the data rather than a single copy, and/or with a slower and more reliable trim, e.g. an increased number of program pulses, a reduced programming voltage step size, or one or more other adjustments to cause programming
5 to be more reliable than during normal operation.

The trim adjuster 136 may be configured to adjust one or more parameters used during writing data to or reading data from the memory 104. For example, the trim adjuster 136 may be configured to retrieve one or more offset values from the table 128 based on the difference between a temperature that the data is written to the memory 104 and a
10 temperature at which the data is to be read from the memory 104. For example, when the controller 120 receives the request from the access device 180 to read the data 106, the controller 120 may retrieve the write temperature 108 from the memory 104 and may further instruct the temperature sensor 112 to perform a measurement operation and to provide the read temperature 162 to the controller 120. The trim adjuster 136
15 may be configured to use a difference between the read temperature 162 and the write temperature 108 to determine an index into the table 128. For example, a temperature difference (illustrated as $\Delta T1$) may correspond to a first change in read voltages 152 ($\Delta VR1$). Different amounts of temperature difference may correspond to different amounts of read voltage offset values that may be retrieved from the table 128. The
20 trim adjuster 136 may be configured to adjust a default value of one or more trim parameters based on offset values retrieved from table 128 and to provide the adjusted values to the memory device 103 for use during data retrieval from memory 104.

The description above refers to a change in read parameters. For programming parameters (i.e. for changing the programming trim), the trim adjuster may change for
25 example the programming pulse step size or width, the starting programming voltage or the verify levels. This may be done as a function of the programming temperature.

In response to the comparator 132 determining that a measured temperature 140 has reduced from being a higher than the first threshold 142 to being less than or equal to the second threshold 144, the comparator 132 may indicate to the controller 120 that
30 marked data is to be refreshed (e.g., the second threshold 144 may be equal to the first threshold 142 or may be less than the first threshold 142). For example, the controller

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120 may access the marked data list 126 and, for each entry in the marked data list 126, the controller 120 may instruct a data read of data corresponding to the entry from the memory 104 and a subsequent data write of the data to the memory 104. The controller 120 may cause the ECC engine 170 to perform a data error correction operation to
5 correct one or more errors that may occur in the data prior to storing the data back to the memory 104 at the lower temperature.

The range adjuster 138 may be configured to adjust one or more temperature thresholds, such as the first threshold 142 and the second threshold 144, based on the temperature history 130. For example, when the temperature history 130 indicates that a “normal”
10 historical operating temperature range of the data storage device 102 has increased since setting the first threshold 142, the range adjuster 138 may adjust a value of the first threshold 142. Similarly, the range adjuster 138 may adjust one or more other temperature thresholds based on a history of the temperature measurements associated with the memory device 103. An example of range adjustment is described with
15 reference to FIG. 2.

By performing one or more adjustments based on the difference between a write temperature and a read temperature of data stored at the memory 104, based on whether a write temperature is outside of a normal temperature range, or based on one or more other temperature related factors, an accuracy of reading data from the memory 104
20 may be increased. As a result, data correction provided by the ECC engine 170 may be enhanced, enabling a less powerful ECC engine to be used to accomplish an equivalent amount of data correction. Alternatively, or in addition, an increased error correction capability and therefore an increased useful life of the data storage device 102 may be obtained.

25 Referring to FIG. 2, an example 200 of performing temperature range adjustment is depicted. For example, a first graph 202 may indicate a distribution of historical temperature measures 230 associated with storage of data or retrieval of data from the memory device 103 of FIG. 1. As illustrated, the historical temperature measures 230 may be considered an “older” set of historical temperature measures as compared to a
30 “newer” (e.g., more recent) set of historical temperature measures 232. Based on the older historical temperature measures 230, three or more temperature ranges may be

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determined, such as a first temperature range 220, a second temperature range 222, and a third temperature range 224.

For example, the first temperature range 220 may correspond to a “normal” temperature range. The second temperature range 222 may correspond to an “abnormal”

5 temperature range of temperatures that exceed a highest temperature of the first temperature range 220. The third temperature range 224 may be considered an “abnormal” temperature range of temperatures that are less than the first temperature of the first temperature range 220.

The first temperature range 220 may have an upper boundary indicated by a first
10 threshold 210. For example, the first threshold 210 may correspond to the first threshold of FIG. 1. A second threshold 212 is also illustrated, which may correspond to the second threshold 144 of FIG. 1. Temperatures exceeding the first threshold 210 may be considered to be in the “abnormal” temperature range indicated by the second temperature range 220. The second temperature range 220 may have an upper bound
15 216, beyond which reliability of the data storage device 102 may be jeopardized. For example, design of the data storage device 102 may be determined to satisfy performance based metrics when operating at a temperature between the upper bound 216 and a lower bound 218. A third threshold 214 may indicate a boundary between the first temperature range 220 and the third temperature range 224.

20 In response to the range adjustment 250 determining that the distribution of newer historical temperature measures 232 includes a portion of measurements, the range adjuster 138 may adjust one or more of the thresholds 210 – 214. For example, as depicted in the second graph 204, the range adjustment 250 may result in the first threshold 210 being increased to a first updated threshold 260. The first updated
25 threshold 260 may be positioned such that a particular percentage of the newer historical temperature measures 232 are at lower temperatures than the first updated threshold 260. For example, the first updated threshold 260 may be selected so that one percent, two percent, one-half of a percent, 10 percent, or any other portion of the newer historical temperature measures 232 exceed the first updated threshold 260.

30 The second updated threshold 262 may also be adjusted. For example, an offset amount that is applied to the first threshold 210 to generate the first updated threshold 260 may

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also be applied to the second threshold 212 to generate the second updated threshold 262. Alternatively, one or more or other techniques may be used to determine the second updated threshold 262, such as by selecting the second updated threshold 262 based on a proportion of the new historical measurement data 232 being greater than the
5 second updated threshold 262.

Increasing the first updated threshold 260 may decrease the second temperature range 222 to form a second updated temperature range 272. The first temperature range 220 may be updated to form the first updated temperature range 270 that spans from the first updated threshold 260 to a third updated threshold 264. For example, as illustrated, the
10 first temperature range 220 may be shifted based on the shift of the first threshold 210 to the updated first threshold 260. Thus, a temperature difference between the first updated threshold 260 and the third updated threshold 264 may be equal to a temperature difference between the first threshold 210 and the third threshold 214.

The third temperature range 224 may be adjusted to form the updated third temperature
15 range 274. For example, the lower bound 218 may remain unadjusted, and the updated third temperature range 274 may span between the lower bound 202 and the third updated threshold 264.

Because temperature effects on data storage and retrieval may be primarily based on a temperature difference between write temperatures and read temperatures, by adjusting
20 the temperature ranges 220 – 224 based on a recent history of historical temperature measures, a proportion of data write and/or data reads occurring in the abnormal temperature range(s) may be reduced, resulting in a higher performance and lower error rates as compared to operation using the unadjusted temperature ranges 220 – 224.

FIG. 3 depicts an example 300 of an implementation that may be used in the data
25 storage device 102 of FIG. 1. An adjusted read voltage may be generated by or based on a sum of a default value of the read voltage 301 and an offset retrieved from an offset table 302. For example, in the offset table 302 may correspond to the table 128 of FIG. 1. The offset table 302 includes multiple columns, each column corresponding to a respective read temperature range. The offset table 302 also includes a number of rows,
30 each row corresponding to a respective write temperature range.

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An example of temperature ranges that may be used as the read temperature ranges and the write temperature ranges is depicted in a range table 304. For example, range 0 may span from a temperature of -25 degrees (e.g., degrees Celsius) to a temperature of 0 degrees. Range 1 may correspond to a temperature in the range from one degree to 25
5 degrees. Range 2 may correspond to a temperature between 26 and 50 degrees. Range 3 may correspond to a temperature from 51 degrees to 75 degrees. Range 4 may correspond to a temperature from 76 degrees to 100 degrees.

As illustrated, the offset table 302 omits values for entries that correspond to matching temperature ranges and read temperature ranges. For example, an entry of the offset
10 table 302 corresponding to a read temperature in range 1 and a write temperature in range 1 includes a value "N/A", meaning that the entry may be omitted from the table, may be empty of data, or may include zero values (e.g., zero offset to the default value 301). Other entries of the offset table 302 include offset values that may be negative values or may be positive values. When the read temperature range corresponds to a
15 lower temperature range than the write temperature range, the offset stored in the table entries may have negative values, such as Offset_Neg_1. Similarly, for table entries where the write temperature range exceeds the read temperature range, values in the table entries may be positive, such as Offset_Pos_1.

As illustrated, for five temperature ranges, a total of four negative offset values and four
20 positive offset values may be used. Thus, a reduced amount of data may be used to adjust for differences in read temperature ranges using a relatively small amount of offset data as compared to including a distinct offset value for each temperature difference. Although the offset table 302 is illustrated as having a table format, in other implementations the values of Offset_Pos_1-4 and Offset_Neg_1-4 may be stored in a
25 data structure having a non-table format and may be selectively accessed based on differences between the read temperature range and the write temperature range.

FIG. 4 illustrates an example 400 of the memory device 103 of FIG. 1 after the controller 120 has closed partially written open blocks in response to programming temperature changes exceeding a threshold amount. For example, data written to the
30 memory device 103 may be striped across multiple dies including a first die 402 and a second die 404. The first die 402 may include a first plane 410 and a second plane 412,

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and the second die 404 may include a first plane 414 and a second plane 416. Each of the planes 410 – 416 may include multiple strings, illustrated as string 0, string 1, string 2 and string 3. Each string may correspond to a physical page and may be sized to include a sufficient number of storage elements of the memory 104 to store a sector of data, such as an ECC codeword. Each plane 410-416 is illustrated as including a single
5 representative block having 24 word lines and that may be operated as a 4-block “metablock” by the controller. Although a single block is illustrated for each plane 410-416, it should be understood that each plane 410-416 may have any number of blocks.

Data may be stored to the memory device 103 according to an order of page writes indicated as page numbers within the respective planes 410 - 416. For example, a first
10 page of data (“page 0”) may be written to string 0 of the first plane 410 of the first die 402. A second page of data may be written to a first string of the second plane 412 of the first die 402. A third page of data may be written to a first string of the first plane 414 of the second die 404, and a fourth page of data may be written to a first string of
15 the second plane 416 of the second die 404.

As data is received from the access device 180 to be stored at the memory device 103, the controller 120 may monitor a temperature and compare a change in temperature to a block variation threshold. For example, in response to detecting a temperature change that exceeds a block variation threshold after writing data to a block, such as a the
20 illustrated block of the second plane 416 of the second die 404 that includes the data storing page 327, the controller 120 may be configured to close the block to prevent further write operations to an unused portion of the block (or of the multiple blocks when operated as a metablock). For example, each block may initially include all erased word lines, and as data is received, the word lines may be written as illustrated in
25 FIG. 4, until page 327 is written to the memory. Upon writing page 327, a temperature measurement associated with page 327 may exceed a temperature measurement associated with writing page 0 to the memory 103 by more than a block variation threshold. In response to detecting the temperature change between writing page 327 and writing page 0 has exceeded the block variation threshold, the controller 120 may
30 be configured to write dummy data to pages labeled 344 – 359 to form a boundary that isolates the last written valid data of each block, illustrated as pages 328 – 343, from erased word lines that remain unwritten after closing the block.

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By writing the dummy data to the boundary word lines, an enhanced data retention may be maintained upon closing the block. By closing the block when the temperature variation has exceeded the threshold, reading data from the block may be accomplished using a common set of read parameters, without having to adjust read parameters for
5 different word lines of the block. Thus, by constraining a write temperature range for data written to the blocks, a parameter adjustment range for data read from the block may be reduced.

FIG. 5 depicts another example of closing one or more blocks in response to the temperature variation within the block exceeding a particular amount. The example 500
10 differs from the example 400 in that the controller 130 does not write dummy data at the boundary following the last valid data written to the memory 103. Although closing the block according to the example 500 may be performed more quickly than the example 400 because less data is written (i.e., the dummy data is omitted), an improved data retention and reduced error rate may be obtained in the example 400 by use of the
15 dummy data.

FIG. 6 depicts an example of a system 600 that may be implemented in the data storage device 102 of FIG. 1. For example, the system 600 includes the memory device 103 and the controller 120 of FIG. 1. The controller 120 includes a time and temperature group manager 602 that is configured to access a data structure 604, such as a table or
20 array that associates indicators of groups of data to memory access parameters associated with the groups of data. For example, a group of data 620 labeled group “N” may be associated with a first set of access parameters 630, such as a first set of read voltage parameters, a first set of write voltage parameters, a first set of erase parameters, or combination thereof. A second group indicator 622 is labeled group “N+1” and is
25 associated with a second set of memory access parameters 632.

The time and temperature group manager 602 may be configured to maintain a group indication pointer 604 that indicates a current group to be used as storage data to the memory device 103. For example, when the group indication pointer 640 points to group indicator N 620, data received from the access device 180 to be stored in the
30 memory device 103 may be associated with group N and the first set of parameters 630 may be used for data write and data retrieval at the memory device 103. The time and

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temperature group manager 602 may be configured to update the group indication pointer 640 to point to a next group based on detecting one or more events.

For example, a group may have a time threshold 606 that is compared against a time measurement (e.g., a current time). In response to the current time exceeding the
5 current group time threshold 606, the time and temperature group manager 602 may cause a new group to be generated by a new group generator 610. Alternatively, or in addition, an upper and/or lower temperature range of the current group may be indicated based on a current group temperature threshold 608. For example, when the current group is created, a measured temperature of the memory device 103 may be obtained
10 and used to generate a current group temperature threshold 608. For example, the current group temperature threshold 608 may be used to constrain an amount of temperature variation that occurs while data is written. For example, the current group may be constrained to a particular temperature range, such as a 20 degree range that is centered on a write temperature for the group.

15 To illustrate, when a new group is created, a temperature T_{new} of the memory device 103 may be measured. An upper temperature T_{hi} for the group may be computed as $T_{\text{hi}} = T_{\text{new}} + 10$, and a lower temperature T_{lo} for the group may be computed as $T_{\text{lo}} = T_{\text{new}} - 10$. The current group temperature threshold 608 may include multiple elements (e.g., a vector) including T_{lo} and T_{hi} . In this case, the current group
20 temperature threshold is “exceeded” when a measured temperature is greater than T_{hi} or when the measured temperature is less than T_{lo} . In other implementations, the current group temperature threshold 608 may represent a difference threshold, such as 10 degrees, and may be “exceeded” when an absolute value of a difference between a measured temp T_{meas} and T_{new} (e.g., $|T_{\text{meas}} - T_{\text{new}}|$) is greater than the difference
25 threshold.

The new group generator 610 may be configured to populate a next group indicator and a next set of memory access parameters in the data structure 604. For example, when the current group is group N 620 and the current group time threshold 606 or the current group temperature threshold 608 is exceeded, the time and temperature group manager
30 602 may cause the new group generator 610 to generate the new group indicator N+1

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622 and to determine the second memory access parameters 632 associated with group N+1.

During operation, the group indication pointer 640 may point to the first group indicator 620. Data that is received at the controller 120 to be written to the memory device 103 may be associated with time data and temperature data. For example, first data 650 may be received, associated with first time data 652 and first temperature data 654. For example, the first time data 652 may correspond to a chronological time, a count of memory accesses or write/erase cycles, a memory health metric, a count of power cycles, or some other indicator of time passage or memory usage. The first temperature data 654 may be received from a temperature sensor of the memory device 103, such as the temperature sensor 112 of FIG. 1. The time and temperature group manager 602 may compare the first time data 652 to the current group time threshold 606 and compare the first temperature data 654 to the current group temperature threshold 608. In response to determining that the first time data 652 does not exceed the current group time threshold 606 and that the first temperature data 654 does not exceed the current group temperature threshold 608, the time and group temperature manager 602 may associate the first data 650 with the current group N, and may provide the first access memory parameter 630 to the memory device 103 for storage of the first data 650.

After storing the first data 650, the controller 610 may receive second data 660 associated with second time data 662 and second temperature data 664. Although the second time data 662 may not exceed the current group time threshold 606, the second temperature data 664 may exceed the current group temperature threshold 608.

In response to determining that the second temperature data 664 exceeds the current group temperature data 608, the time and temperature group manager 602 may generate a new group N+1, may generate the second group indicator 662, may determine the second memory access parameters 632, and may provide the second memory access parameters 632 to the memory device 103 for storing the second data 660 to the memory device 103. In addition, the time and temperature group manager 602 may update the group indication pointer 640 to point to the second group indication 662.

Another method that may be used for deciding whether to open a new time and temperature tag (e.g., create a new group with a new group indicator) is that whenever

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new data is programmed (e.g., a new block) then the block may be read with the read parameters associated with the current time & temperature tag. In case the BER measured for the read result does not fit to the BER indicated by the time & temperature tag, then a new time & temperature group may be created and the current block may be
5 associated with the new group. For example, in cases where there was a power drop at the data storage device, and when the memory is powered up again, the data storage device may not know how much time has elapsed. Thus, the controller may be configured to check whether the parameters associated the last time & temperature group/tag fit the newly programmed block.

10 By constraining the group associated with data to be within a common time range and also within a common temperature range, an applicability of the memory access parameters associated with the group may be maintained. For example, a variation of data characteristics of stored memory device 103 may remain relatively constrained such that the memory access parameters associated with the group may enable reliable
15 reading and writing of data using the memory access parameters for the group. Adjustment of the memory access parameters, such as due to device usage or in response to temperature variation of the data storage device, may be performed by adjustment of the memory access parameters associated with the groups as opposed to adjustment of memory access parameters for individual data accesses to the memory
20 device 103. This may be done by calibrating the parameters on representative pages of the group, instead of calibrating them on each page within the group, thus saving time and reducing maintenance complexity. The updating of the parameters of the different time and temperature groups may be done as maintenance operations performed in the background. Alternatively, the updating of parameters may be triggered by some event
25 in the foreground (e.g. high BER observed during a host read).

FIG. 7 is a block diagram of another illustrative example of the data storage device of FIG. 1. FIG. 7 illustrates a data storage device 700 that includes the memory device 103 that is coupled to the controller 120. The memory device 103 and the controller 120 may include or correspond to the memory device 103 and the controller 120 of FIG.
30 1.

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The controller 120 may include the ECC engine 170 and the temperature based adjuster 122. The controller 120 may be configured to read multiple codewords of data from the memory device 103. For example, the controller 120 may be configured to read a first codeword 702, a second codeword 704, and a third codeword 706 from the memory device 103. In other implementations, more than three codewords or fewer than three codewords may be read from the memory device 103.

The controller 120 may be configured to determine an error rate associated with reading the multiple codewords of data. For example, the ECC engine 170 of the controller 120 may be configured to determine a first error rate (e.g., a first bit error rate (BER)) associated with reading the first codeword 702, a second error rate associated with reading the second codeword 704, and a third error rate associated with reading the third codeword 706. The controller 120 may be configured to maintain determined error rates as history of error rates data 708 that includes multiple error rates (e.g., multiple BERs). For example, the ECC engine 170 of the controller 120 may be configured to maintain the history of error rates data 708 (e.g., in a controller memory) that includes a first error rate 710 (e.g., BER 1) and an n-th error rate 712 (e.g., BER n). The number n of error rates included in the history of error rates data 708 may correspond to the number of codewords read from the memory device 103 during a particular operation (or set of operations).

The temperature based adjuster 122 of the controller 120 may be configured to compare the error rate to a threshold error rate for a threshold number of codewords. For example, the temperature based adjuster 122 may include a comparator 718 that is configured to compare one or more error rates from the history of error rates data 708 to an error rate threshold 714. In a particular implementation, the error rate threshold 714 is less than a threshold correctable error rate of the ECC engine 170. In response to determining that error rates exceed the error rate threshold 714 for a number of sequential codewords that exceeds a number of codewords threshold 716, the temperature based adjuster 122 may initiate the temperature compensation operation 136. To illustrate, the number of codewords threshold 716 may be three, and in response to detecting that the first error rate 710 (corresponding to the first codeword 702), a second error rate (corresponding to the second codeword 704), and the n-th error rate 712 (corresponding to the third codeword 706) each exceed the error rate threshold

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714, the temperature based adjuster 122 may initiate the temperature compensation operation 136. The temperature compensation operation may cause one or more memory access parameters (such as the read voltage 164 of FIG. 1) to be modified based on a temperature difference between a first temperature associated with writing the multiple codewords 702-706 to the memory device 103 (e.g., the first temperature is associated with a first time period, the first time period includes a write operation of the multiple codewords 702-706 to the memory 104), and a second temperature associated with reading the multiple codewords 702-706 from the memory device 103 (e.g., the second temperature is associated with a second time period, the second time period includes a read operation of multiple codewords 702-706 from the memory 104).

During operation, the controller 120 may read multiple codewords including the first codeword 702, the second codeword 704, and the third codeword 706 from the memory device 103. The controller 120 (e.g., the ECC engine 170) may detect error rates associated with the codewords 702-706. The error rates may be included in the history of error rates data 708. The controller 120 (e.g., the temperature based adjuster 122) may compare the history of error rates data 708 to the error rate threshold 714. In response to detecting that error rates exceed the error rate threshold 714 for a number of sequential codewords that exceeds the number of codewords threshold 716, the controller 120 may initiate the temperature compensation operation 136 that modifies one or more memory access parameters based on a temperature difference between a first temperature associated with writing the multiple codewords 702-706 to the memory device 103 and a second temperature associated with reading the multiple codewords 702-706 from the memory device 103.

FIG. 8 is a diagram illustrating a particular example of a configuration of a memory device of the data storage device of FIG. 1. FIG. 8 illustrates a data storage device 800 that includes the memory device 103. The memory device 103 may include or correspond to the memory device 103 of FIG. 1.

The memory device 103 includes a stack 820 of memory dies. The stack 820 may include multiple memory dies, such as a first memory die 802, a second memory die 804, an i-th memory die 806, and an n-th memory die 808. In other implementations, the stack 820 may include more than n or fewer than n memory dies. In a particular

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implementation, the first memory die 802 is a top die of the stack 820, the n-th memory die 808 is a bottom memory die of the stack 820, and other memory dies such as the second memory die 804 and the i-th memory die 806 are “central” memory dies of the stack 820. As used herein, central memory dies refer to memory dies that are neither
5 the top memory die nor the bottom memory die of the stack 820, such as to dies in a center of a stack, e.g., die 3 in a 5-die stack or dies 4 and 5 in an 8-die stack.

Each memory die of the stack 820 may include a corresponding temperature sensor. For example, the first memory die 802 may include a first temperature sensor 812, the second memory die 804 may include a second temperature sensor 814, the i-th memory
10 die 806 may include an i-th temperature sensor 816, and the n-th memory die 808 may include an n-th temperature sensor 818. Each temperature sensor of the temperature sensors 812-818 may be configured to generate an indicator of a temperature of the corresponding memory die. For example, the first temperature sensor 812 may be configured to generate a first indicator 832 (T1) of a first temperature of the first
15 memory die 802, the second temperature sensor 814 may be configured to generate a second indicator 834 (T2) of a second temperature of the second memory die 804, the i-th temperature sensor 816 may be configured to generate a third indicator 836 (T3) of a third temperature of the i-th memory die 806, and the n-th temperature sensor 818 may be configured to generate a fourth indicator 838 (T4) of a fourth temperature of the n-th
20 memory die 808. The memory device 103 may be configured to provide the indicators 832-838 to the controller for processing.

The controller may be configured to receive multiple indicators from the memory device 103 and to determine an average based on the multiple indicators. For example, the controller may be configured to receive the first indicator 832 of the first
25 temperature from the first temperature sensor 812 and the third indicator 836 of the third temperature from the i-th temperature sensor 816. The controller may be configured to determine an average temperature 840 of the first temperature and the third temperature. In this manner, the average temperature may be determined based on a temperature of a non-center memory die (e.g., the first memory die 802) and a central memory die (e.g.,
30 the i-th memory die 806). Because the first memory die 802 is the coolest and the central die (e.g., the i-th memory die 806) is the hottest, the average temperature 840 may be representative of a range of temperatures of memory dies in the stack 820.

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In some implementations, the average temperature 840 may be further based on indications (e.g., the second indication 834, the n-th indication 838, or both) of temperatures of other memory dies. As non-limiting examples, the average temperature 840 may be determined based on the first indicator 832 and the second indicator 834, the n-th indicator 838 and the second indicator 834, the n-th indicator 838 and the i-th indicator 836, or some other combination of two or more of the indicators 832-838. The average temperature 840 may include or correspond to a mean temperature, a weighted mean temperature, a median temperature, a mode of the temperatures, or another statistical measure of central accuracy. The controller may be further configured to determine a temperature range associated with a memory access based on the average temperature 840. In other implementations, the memory device 103 may be configured to perform the above-described actions of the controller. For example, the memory device 103 may determine the average temperature 840 and a temperature range of the stack 820 based on the average temperature 840.

During operation, temperature sensors of memory dies of the stack 820 may generate indications of a temperature of a corresponding memory die. For example, the first temperature sensor 812 may generate the first indicator 832 of the first temperature of the first memory die 802, the second temperature sensor 814 may generate the second indicator 834 of the second temperature of the second memory die 804, the i-th temperature sensor 816 may generate the third indicator 836 of the third temperature of the i-th memory die 806, and the n-th temperature sensor 818 may generate the fourth indicator 838 of the fourth temperature of the n-th memory die 808. The controller (e.g., the controller 120 of FIG. 1) may receive indicators from the memory device 103 and may determine the average temperature 840. For example, the controller may receive the first indicator 832 of the first temperature and the i-th indicator 836 of the third temperature and the controller may determine the average temperature 840 for the first and third temperatures. The controller may determine a temperature range associated with a memory access based on the average temperature 840. In another implementation, the memory device 103 may determine the temperature range and the average temperature 840, and the memory device 103 may send an indication of the temperature range to the controller.

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FIG. 9 is a flow diagram of a particular example of a method 900 of refreshing data. The method 900 may be performed at a data storage device that includes a controller and a non-volatile memory. For example, the method 900 may be performed by the data storage device 102 of FIG. 1.

- 5 The method 900 includes, at 902, marking data stored at the non-volatile memory for refresh in response to determining that a first measured temperature associated with writing the data to the non-volatile memory exceeds a first threshold. For example, the temperature-based adjuster 122 of FIG. 1 may determine that the write temperature 108 (e.g., a first measured temperature associated with writing the data 106 to the memory
- 10 104) exceeds the first threshold 142. In this example, in response to determine that the write temperature 108 exceeds the first threshold 142, the temperature-based adjuster 122 may mark the data 106 by storing the refresh flag 110. Alternatively or in addition, the temperature-based adjuster 122 may store an indicator (or an identifier) of the data 106 in the marked data list 126.
- 15 The method 900 includes, at 904, refreshing the marked data in response to determining that a second measured temperature associated with the non-volatile memory is below a second threshold. For example, the temperature-based adjuster 122 of FIG. 1 may receive the measured temperature 140 (e.g., the second measure temperature) from the temperature sensor 112. In this example, the comparator 132 may compare the measure
- 20 temperature 140 to the second threshold 144. If a value of the measured temperature 140 is below a value of the second threshold 144, the temperature-based adjuster 122 may cause the marked data to be refreshed. To illustrate, if the value of the measured temperature 140 is below a value of the second threshold 144, the controller 120 may access the marked data list 126 to identify marked data. The controller 120 may also
- 25 initiate data refresh operations, such as by sending the command 160 to cause the data 106 to be refreshed.

FIG. 10 is a flow diagram of a particular example of a method 1000 of temperature-based control. The method 1000 may be performed at a data storage device that includes a controller and a non-volatile memory. For example, the method 1000 may be

30 performed by the data storage device 102 of FIG. 1.

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The method 1000 includes, at 1002, writing data to a block of the non-volatile memory. For example, the data 106 of FIG. 1 may be written to a particular block of the memory 104.

The method 1000 also includes, at 1004, in response to detecting a temperature change
5 that exceeds a block variation threshold after writing the data to the block, closing the block. For example, the temperature-based adjuster 122 may detect a temperature change (e.g., based on the measured temperature 140 and the temperature history 130). The comparator 132 may determine whether the temperature change exceeds a threshold. In response to determining that the temperature change exceeds a threshold,
10 the controller 120 may close the block, such as described with reference to FIGs. 4-5. Closing the block may prevent write operations to an unused portion of the block. In some implementations, the controller 120 may write dummy data to a word line of the block prior to closing the block.

FIG. 11 is a flow diagram of another particular example of a method 1100 of
15 temperature-based control. The method 1100 may be performed at a data storage device that includes a controller and a non-volatile memory. For example, the method 1100 may be performed by the data storage device 102 of FIG. 1.

The method 1100 includes, at 1102, associating first data that is stored in the non-volatile memory with a first group indicator, and, at 1104, associating first memory
20 access parameter values with the first group indicator. For example, the time and temperature group manager 602 of FIG. 6 may associate the first data 650 with the first group 620. The time and temperature group manager 602 may also associate the first parameters 630 with the first group 620.

The method 1100 also includes, at 1106, in response to detecting a temperature change
25 that exceeds a group temperature threshold associated with the first group indicator, associating second data to be stored in the non-volatile memory with a second group indicator, and, at 1108, associating second memory access parameters with the second group indicator. For example, the time and temperature group manager 602 of FIG. 6 may detect a temperature change (e.g., by comparing the first temperature data 654 and
30 the second temperature data 664 to a first stored temperature for the first group 620). If the temperature change exceeds the current group temperature threshold 608, the time

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and temperature group manager 602 may generate a new group (e.g., the second group 622) and may associate the second data 660 with the second group 622. The time and temperature group manager 602 may also associate the second parameters 632 with the second group 622.

- 5 In a particular implementation, the time and temperature group manager 602 may store the group indicator pointer 640 which may indicate a group indicator (e.g., an indicator of the first group 620 or an indicator of the second group 622) to be associated with data (e.g., data received from the access device 180) that is to be written to the non-volatile memory. In this particular implementation, in response to detecting the temperature
10 change, the time and temperature group manager 602 may update the group indicator pointer 640 to indicate the indicator of the second group 622.

FIG. 12 is a flow diagram of another particular example of a method 1200 of determining a read voltage value. The method 1200 may be performed at a data storage device that includes a controller and a non-volatile memory. For example, the method
15 1200 may be performed by the data storage device 102 of FIG. 1.

The method 1200 may include, at 1202, determining a read voltage offset value based on data structure that maps read voltage offset values to differences between write temperatures and read temperatures. For example, the data structure may include the table 128 and temperature-based adjuster 122 may perform a lookup operation to read
20 the table 128 to determine a read voltage offset value, such as the first read voltage offset value 152, that corresponds to a particular temperature difference, such as the first temperature difference 150.

In a particular implementation, each entry of the table is accessible according to a write temperature range and a read temperature range. In this particular implementation, the
25 table omits read voltage offset values for entries that correspond to matching write temperature ranges and read temperature ranges. For example, an offset value can be determined from the offset table 302 based on a write temperature range and a read temperature range. Further, the offset table 302 omits read voltage offset values for table entries that correspond to matching write temperature ranges and read temperature
30 ranges.

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The method 1200 may also include, at 1204, determining an adjusted value of a read voltage associated with reading data from the non-volatile memory. The adjusted value determined based on a default value of the read voltage and based on the read voltage offset value. For example, the trim adjuster 136 may use the read voltage offset value
5 determined from the table 128 and a default value of the read voltage (e.g., the default value 301 of FIG. 3) to determine the adjusted value of the read voltage.

FIG. 13 is a flow diagram of another particular example of a method 1300 of temperature-based control. The method 1300 may be performed at a data storage device that includes a controller and a non-volatile memory. For example, the method 1300
10 may be performed by the data storage device 102 of FIG. 1.

The method 1300 includes, at 1302, reading multiple codewords of data from the non-volatile memory. For example, as illustrated in FIG. 7, the controller 120 may read multiple codewords, such as the first codeword 702, the second codeword 704 and the third codeword 706 from the memory device 103.

15 The method 1300 also includes, at 1304, in response to detecting an error rate exceeding a threshold error rate for a threshold number of the codewords, initiating a temperature compensation operation that modifies one or more memory access parameters based on a temperature difference between a first temperature and a second temperature. For example, the error correction coding (ECC) engine 180 may generate the history of
20 error rates data 708. In this example, the temperature-based adjuster 122 may compare the history of error rates data 708 to the error rate threshold 714 and to the number of codewords threshold 716. In a particular implementation, the threshold error rate is less than a threshold correctable error rate of the ECC engine 180. In response to detecting that an error rate exceeds a threshold error rate for a threshold number of the codewords,
25 the temperature-based adjuster 122 initiates a temperature compensation operation 136. The temperature compensation operation 136 may cause one or more memory access parameters (such as the read voltage 164 of FIG. 1) to be modified based on a temperature difference between a first temperature associated with writing the multiple codewords to the non-volatile memory and a second temperature associated with
30 reading the multiple codewords from the non-volatile memory.

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FIG. 14 is a flow diagram of another particular example of a method 1400 of determining a temperature range. The method 1400 may be performed at a data storage device that includes a controller and a non-volatile memory. For example, the method 1400 may be performed by the data storage device 102 of FIG. 1.

5 The method 1400 includes, at 1402, receiving a first indicator of a first temperature from a first temperature sensor of a first die of the non-volatile memory. For example, the memory device 103 may include a stack 820 of memory die as in FIG. 8. In this example, the first memory die 802 may include the first temperature sensor 812 which may generate and send the first indication 832, which indicates a temperature of the first
10 memory die 802.

The method 1400 includes, at 1404, receiving a second indicator of a second temperature from a second temperature sensor of a second die of the non-volatile memory. For example, the second memory die may correspond to the i-th memory die 806 that includes the i-th temperature sensor 816. The i-th temperature sensor 816 may
15 generate and send the i-th indication 836, which indicates a temperature of the i-th memory die 806. In this example, the stack 820 may also include other memory dies, one or more of which may include another temperature sensor. To illustrate, the stack 820 in FIG. 8 includes one or more memory dies stacked between the first memory die 802 and the i-th memory die 806, each of which may include a temperature sensor. The
20 stack 820 includes one or more other dies, such the n-th memory die 808, which includes the nth temperature sensor 818. Thus, the first memory die 802 and the i-th memory die 804 may represent different portions of the stack 820. For example, in FIG. 8, the first memory die 802 is the top die of the stack 820 and the i-th memory die 804 is a central die (e.g., a memory die that is neither the top memory die nor the bottom
25 memory die of the stack 820).

The method 1400 also includes, at 1406, determining a temperature range based on an average of the first temperature and the second temperature. For example, the controller 120 or the memory device 103 may determine the average temperature 840 based on the first indication 832 of the first temperature and based on the i-th indication 836 of the
30 second temperature. In some implementations, the average temperature 840 may be further based on indications (such as the second indication 834, the nth indication 838,

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or both) of temperatures of other memory dies. The average temperature 840 may include or correspond to a mean temperature, a weighted mean temperature, a median temperature, a mode of the temperatures, or another statistical measure of central tendency. The average temperature may be associated with a memory access, such as
5 indicating a temperature condition prior to, during, or upon completion of reading data from the memory 104 or writing data to the memory 104.

Although the controller 120 and certain other components described herein are illustrated as block components and described in general terms, such components may include one or more microprocessors, state machines, and/or other circuits configured to
10 enable the data storage device 102 (or one or more components thereof) to perform operations described herein. Components described herein may be operationally coupled to one another using one or more nodes, one or more buses (e.g., data buses and/or control buses), one or more other structures, or a combination thereof. One or more components described herein may include one or more physical components, such
15 as hardware controllers, state machines, logic circuits, one or more other structures, or a combination thereof, to enable the data storage device 102 to perform one or more operations described herein.

Alternatively or in addition, one or more aspects of the data storage device 102 may be implemented using a microprocessor or microcontroller programmed (e.g., by executing
20 instructions) to perform one or more operations described herein, such as one or more operations of the methods 900-1400. In a particular embodiment, the data storage device 102 includes a processor executing instructions (e.g., firmware) retrieved from the memory device 103. Alternatively or in addition, instructions that are executed by the processor may be retrieved from memory separate from the memory device 103,
25 such as at a read-only memory (ROM) that is external to the memory device 103.

It should be appreciated that one or more operations described herein as being performed by the controller 120 may be performed at the memory device 103. As an illustrative example, in-memory ECC operations (e.g., encoding operations and/or decoding operations) may be performed at the memory device 103 alternatively or in
30 addition to performing such operations at the controller 120.

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To further illustrate, the data storage device 102 may be configured to be coupled to the access device 180 as embedded memory, such as in connection with an embedded MultiMedia Card (eMMC®) (trademark of JEDEC Solid State Technology Association, Arlington, Virginia) configuration, as an illustrative example. The data storage device
5 102 may correspond to an eMMC device. As another example, the data storage device 102 may correspond to a memory card, such as a Secure Digital (SD®) card, a microSD® card, a miniSD™ card (trademarks of SD-3C LLC, Wilmington, Delaware), a MultiMediaCard™ (MMC™) card (trademark of JEDEC Solid State Technology Association, Arlington, Virginia), or a CompactFlash® (CF) card (trademark of
10 SanDisk Corporation, Milpitas, California). The data storage device 102 may operate in compliance with a JEDEC industry specification. For example, the data storage device 102 may operate in compliance with a JEDEC eMMC specification, a JEDEC Universal Flash Storage (UFS) specification, one or more other specifications, or a combination thereof.

15 The memory device 103 may include a three-dimensional (3D) memory, such as a resistive random access memory (ReRAM), a flash memory (e.g., a NAND memory, a NOR memory, a single-level cell (SLC) flash memory, a multi-level cell (MLC) flash memory, a divided bit-line NOR (DINOR) memory, an AND memory, a high capacitive coupling ratio (HiCR) device, an asymmetrical contactless transistor (ACT) device, or
20 another flash memory), an erasable programmable read-only memory (EPROM), an electrically-erasable programmable read-only memory (EEPROM), a read-only memory (ROM), a one-time programmable memory (OTP), or a combination thereof.

Alternatively or in addition, the memory device 103 may include another type of memory. In a particular embodiment, the data storage device 102 is indirectly coupled
25 to an access device (e.g., the access device 180) via a network. For example, the data storage device 102 may be a network-attached storage (NAS) device or a component (e.g., a solid-state drive (SSD) component) of a data center storage system, an enterprise storage system, or a storage area network. The memory device 103 may include a semiconductor memory device.

30 Semiconductor memory devices include volatile memory devices, such as dynamic random access memory (“DRAM”) or static random access memory (“SRAM”) devices, non-volatile memory devices, such as resistive random access memory

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(“ReRAM”), magnetoresistive random access memory (“MRAM”), electrically erasable programmable read only memory (“EEPROM”), flash memory (which can also be considered a subset of EEPROM), ferroelectric random access memory (“FRAM”), and other semiconductor elements capable of storing information. Each type of memory device may have different configurations. For example, flash memory devices may be configured in a NAND or a NOR configuration.

The memory devices can be formed from passive and/or active elements, in any combinations. By way of non-limiting example, passive semiconductor memory elements include ReRAM device elements, which in some embodiments include a resistivity switching storage element, such as an anti-fuse, phase change material, etc., and optionally a steering element, such as a diode, etc. Further by way of non-limiting example, active semiconductor memory elements include EEPROM and flash memory device elements, which in some embodiments include elements containing a charge region, such as a floating gate, conductive nanoparticles, or a charge storage dielectric material.

Multiple memory elements may be configured so that they are connected in series or so that each element is individually accessible. By way of non-limiting example, flash memory devices in a NAND configuration (NAND memory) typically contain memory elements connected in series. A NAND memory array may be configured so that the array is composed of multiple strings of memory in which a string is composed of multiple memory elements sharing a single bit line and accessed as a group.

Alternatively, memory elements may be configured so that each element is individually accessible, e.g., a NOR memory array. NAND and NOR memory configurations are exemplary, and memory elements may be otherwise configured.

The semiconductor memory elements located within and/or over a substrate may be arranged in two or three dimensions, such as a two dimensional memory structure or a three dimensional memory structure. In a two dimensional memory structure, the semiconductor memory elements are arranged in a single plane or a single memory device level. Typically, in a two dimensional memory structure, memory elements are arranged in a plane (e.g., in an x-z direction plane) which extends substantially parallel to a major surface of a substrate that supports the memory elements. The substrate may

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be a wafer over or in which the layer of the memory elements are formed or it may be a carrier substrate which is attached to the memory elements after they are formed. As a non-limiting example, the substrate may include a semiconductor such as silicon.

The memory elements may be arranged in the single memory device level in an ordered
5 array, such as in a plurality of rows and/or columns. However, the memory elements may be arrayed in non-regular or non-orthogonal configurations. The memory elements may each have two or more electrodes or contact lines, such as bit lines and word lines.

A three dimensional memory array is arranged so that memory elements occupy multiple planes or multiple memory device levels, thereby forming a structure in three
10 dimensions (i.e., in the x, y and z directions, where the y direction is substantially perpendicular and the x and z directions are substantially parallel to the major surface of the substrate). As a non-limiting example, a three dimensional memory structure may be vertically arranged as a stack of multiple two dimensional memory device levels. As another non-limiting example, a three dimensional memory array may be arranged as
15 multiple vertical columns (e.g., columns extending substantially perpendicular to the major surface of the substrate, i.e., in the y direction) with each column having multiple memory elements in each column. The columns may be arranged in a two dimensional configuration, e.g., in an x-z plane, resulting in a three dimensional arrangement of memory elements with elements on multiple vertically stacked memory planes. Other
20 configurations of memory elements in three dimensions can also constitute a three dimensional memory array.

By way of non-limiting example, in a three dimensional NAND memory array, the memory elements may be coupled together to form a NAND string within a single horizontal (e.g., x-z) memory device levels. Alternatively, the memory elements may
25 be coupled together to form a vertical NAND string that traverses across multiple horizontal memory device levels. Other three dimensional configurations can be envisioned wherein some NAND strings contain memory elements in a single memory level while other strings contain memory elements which span through multiple memory levels. Three dimensional memory arrays may also be designed in a NOR
30 configuration and in a ReRAM configuration.

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Typically, in a monolithic three dimensional memory array, one or more memory device levels are formed above a single substrate. Optionally, the monolithic three dimensional memory array may also have one or more memory layers at least partially within the single substrate. As a non-limiting example, the substrate may include a semiconductor
5 such as silicon. In a monolithic three dimensional array, the layers constituting each memory device level of the array are typically formed on the layers of the underlying memory device levels of the array. However, layers of adjacent memory device levels of a monolithic three dimensional memory array may be shared or have intervening layers between memory device levels.

10 Alternatively, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device having multiple layers of memory. For example, non-monolithic stacked memories can be constructed by forming memory levels on separate substrates and then stacking the memory levels atop each other. The substrates may be thinned or removed from the memory device levels before stacking,
15 but as the memory device levels are initially formed over separate substrates, the resulting memory arrays are not monolithic three dimensional memory arrays. Further, multiple two dimensional memory arrays or three dimensional memory arrays (monolithic or non-monolithic) may be formed on separate chips and then packaged together to form a stacked-chip memory device.

20 Associated circuitry is typically required for operation of the memory elements and for communication with the memory elements. As non-limiting examples, memory devices may have circuitry used for controlling and driving memory elements to accomplish functions such as programming and reading. This associated circuitry may be on the same substrate as the memory elements and/or on a separate substrate. For example, a
25 controller for memory read-write operations may be located on a separate controller chip and/or on the same substrate as the memory elements.

One of skill in the art will recognize that this disclosure is not limited to the two dimensional and three dimensional exemplary structures described but cover all relevant memory structures within the spirit and scope of the disclosure as described herein and
30 as understood by one of skill in the art. The illustrations of the embodiments described herein are intended to provide a general understanding of the various embodiments.

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Other embodiments may be utilized and derived from the disclosure, such that structural and logical substitutions and changes may be made without departing from the scope of the disclosure. This disclosure is intended to cover any and all subsequent adaptations or variations of various embodiments. Those of skill in the art will recognize that such
5 modifications are within the scope of the present disclosure.

The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, that fall within the scope of the present disclosure. Thus, to the maximum extent allowed by law, the scope of the present disclosure is to be determined
10 by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

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WHAT IS CLAIMED IS:

1. A device comprising:
a memory; and
a controller coupled to the memory, the controller configured to mark data for refresh in
5 response to determining that a first measured temperature associated with writing the
data to the memory exceeds a first threshold, the controller further configured to refresh
the marked data in response to determining that a second measured temperature
associated with the memory is below a second threshold.
2. The device of claim 1, wherein the controller is configured to mark the data by
10 adding an indication of the data to a marked data list.
3. The device of claim 2, wherein the controller is configured to access the marked data
list and to initiate a data refresh operation in response to detecting that the second
measured temperature is below the second threshold.
4. The device of claim 1, further comprising a temperature sensor configured to
15 indicate the first measured temperature and the second measured temperature to the
controller.
5. A device comprising:
a memory; and
a controller coupled to the memory, the controller configured to write data to a block of
20 the memory and, in response to detecting a temperature change that exceeds a block
variation threshold after writing the data to the block, to close the block to additional
write operations to an unused portion of the block.
6. The device of claim 5, wherein the controller is configured to write dummy data to a
word line of the block prior to closing the block.
- 25 7. A device comprising:
a memory; and

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a controller coupled to the memory, the controller configured to associate first data that is stored in the memory with a first group indicator and to associate first memory access parameter values with the first group indicator, wherein in response to detecting a temperature change that exceeds a group temperature threshold associated with the first group indicator, the controller is configured to associate second data to be stored in the memory with a second group indicator and to associate second memory access parameter values with the second group indicator, the second memory access parameter values different from the first memory access parameter values.

8. The device of claim 7, wherein the controller is configured to maintain a group indicator pointer indicating a group indicator to be associated with data to be written to the memory, and wherein in response to detecting the temperature change, the controller is configured to update the group indicator pointer to indicate the second group indicator.

9. A device comprising:
a memory; and
a controller coupled to the memory, the controller configured to store a default value of a read voltage and to determine an adjusted read voltage to read data from the memory, the adjusted read voltage determined based on the default value and based on a data structure that maps read voltage offset values to differences between write temperatures and read temperatures.

10. The device of claim 9, wherein the data structure includes a table and wherein each entry of the table is accessible according to a write temperature range and a read temperature range.

11. The device of claim 9, wherein the table omits read voltage offset values for entries that correspond to matching write temperature ranges and read temperature ranges.

12. A device comprising:
a memory; and
a controller coupled to the memory, the controller configured to read multiple codewords of data from the memory and, in response to detecting an error rate

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exceeding a threshold error rate for a threshold number of the codewords, to initiate a temperature compensation operation that modifies one or more memory access parameters based on a temperature difference between a first temperature and a second temperature.

- 5 13. The device of claim 12, wherein the first temperature is associated with a first time period, the first time period includes a write operation of multiple codewords to the memory, and the second temperature is associated with a second time period, the second time period includes a read operation of multiple codewords from the memory.

- 10 14. The device of claim 12, further comprising an error correction coding (ECC) engine, and wherein the threshold error rate is less than a threshold correctable error rate of the ECC engine.

- 15 15. A device comprising:
a memory including:
a first memory die that includes a first temperature sensor; and
15 a second memory die that includes a second temperature sensor; and
a controller coupled to the memory, the controller configured to receive a first indicator of a first temperature from the first temperature sensor and a second indicator of a second temperature from the second temperature sensor, wherein the controller is configured to determine a temperature range based on an average of the first
20 temperature and the second temperature.

16. The device of claim 15, wherein the memory includes a stack of memory dies, wherein the first memory die is a top die of the stack and wherein the second memory die is a central die of the stack.

17. A method comprising:
25 at a data storage device that includes a controller coupled to a non-volatile memory, performing:
marking data stored at the non-volatile memory for refresh in response to determining that a first measured temperature associated with writing the data to the non-volatile memory exceeds a first threshold; and

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refreshing the marked data in response to determining that a second measured temperature associated with the non-volatile memory is below a second threshold.

18. The method of claim 17, wherein marking the data comprises adding an indication of the data to a marked data list.

- 5 19. The method of claim 18, further comprising, after marking the data:
accessing the marked data list; and
in response to detecting that the second measured temperature is below the second threshold, initiating data refresh operations.

20. A method comprising:
10 at a data storage device that includes a controller coupled to a non-volatile memory, performing:
writing data to a block of the non-volatile memory; and
in response to detecting a temperature change that exceeds a block variation threshold after writing the data to the block, closing the block.

- 15 21. The method of claim 20, further comprising writing dummy data to a word line of the block prior to closing the block.

22. The method of claim 20, wherein closing the block prevents write operations to an unused portion of the block.

23. A method comprising:
20 at a data storage device that includes a controller coupled to a non-volatile memory, performing:
associating first data that is stored in the non-volatile memory with a first group indicator;
associating first memory access parameter values with the first group indicator;
25 in response to detecting a temperature change that exceeds a group temperature threshold associated with the first group indicator:

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associating second data to be stored in the non-volatile memory with a second group indicator; and

associating second memory access parameters with the second group indicator.

24. The method of claim 23, further comprising:

- 5 storing a group indicator pointer indicating a group indicator to be associated with data that is to be written to the non-volatile memory; and
in response to detecting the temperature change, updating the group indicator pointer to indicate the second group indicator.

25. A method comprising:

- 10 at a data storage device that includes a controller coupled to a non-volatile memory, performing:
determining a read voltage offset value based on data structure that maps read voltage offset values to differences between write temperatures and read temperatures; and
determining an adjusted value of a read voltage associated with reading data from the
15 non-volatile memory, the adjusted value determined based on a default value of the read voltage and based on the read voltage offset value.

26. The method of claim 25, wherein the data structure includes a table and wherein each entry of the table is accessible according to a write temperature range and a read temperature range.

- 20 27. The method of claim 26, wherein the table omits read voltage offset values for entries that correspond to matching write temperature ranges and read temperature ranges.

28. A method comprising:

- at a data storage device that includes a controller coupled to a non-volatile memory,
25 performing:
reading multiple codewords of data from the non-volatile memory; and
in response to detecting an error rate exceeding a threshold error rate for a threshold number of the codewords, initiating a temperature compensation operation that modifies

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one or more memory access parameters based on a temperature difference between a first temperature and a second temperature.

29. The method of claim 28, wherein the first temperature is associated with a first time period, the first time period includes a write operation of multiple codewords to the memory, and the second temperature is associated with a second time period, the second time period includes a read operation of the multiple codewords from the memory.

30. The method of claim 28, wherein the threshold error rate is less than a threshold correctable error rate of an error correction coding (ECC) engine of the data storage device.

31. A method comprising:
at a data storage device that includes a controller coupled to a non-volatile memory, performing
receiving a first indicator of a first temperature from a first temperature sensor of a first die of the non-volatile memory;
receiving a second indicator of a second temperature from a second temperature sensor of a second die of the non-volatile memory; and
determining a temperature range based on an average of the first temperature and the second temperature.

32. The method of claim 31, wherein the non-volatile memory includes a stack of memory dies, wherein the first die is a top die of the stack and wherein the second die is a central die of the stack.

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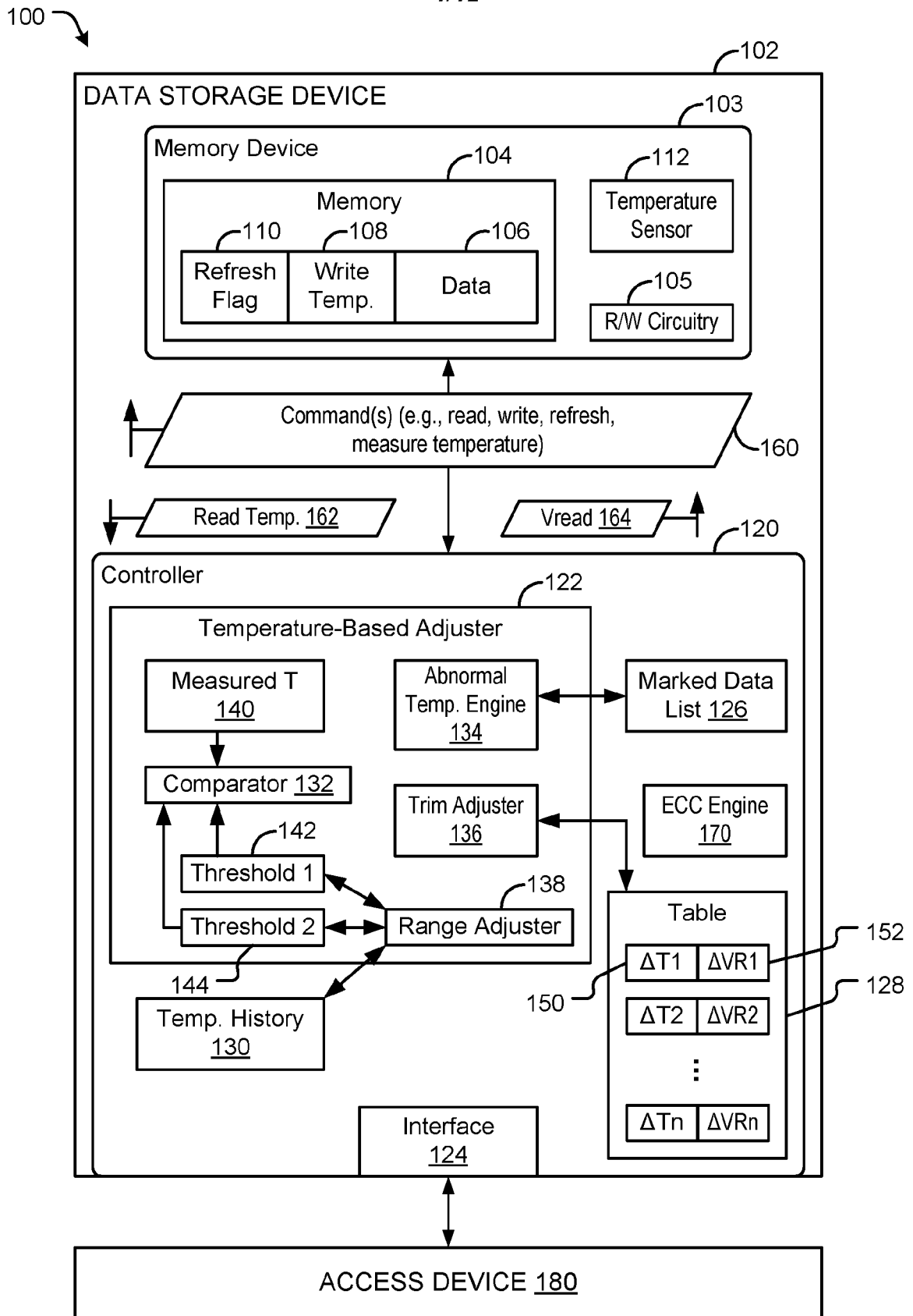
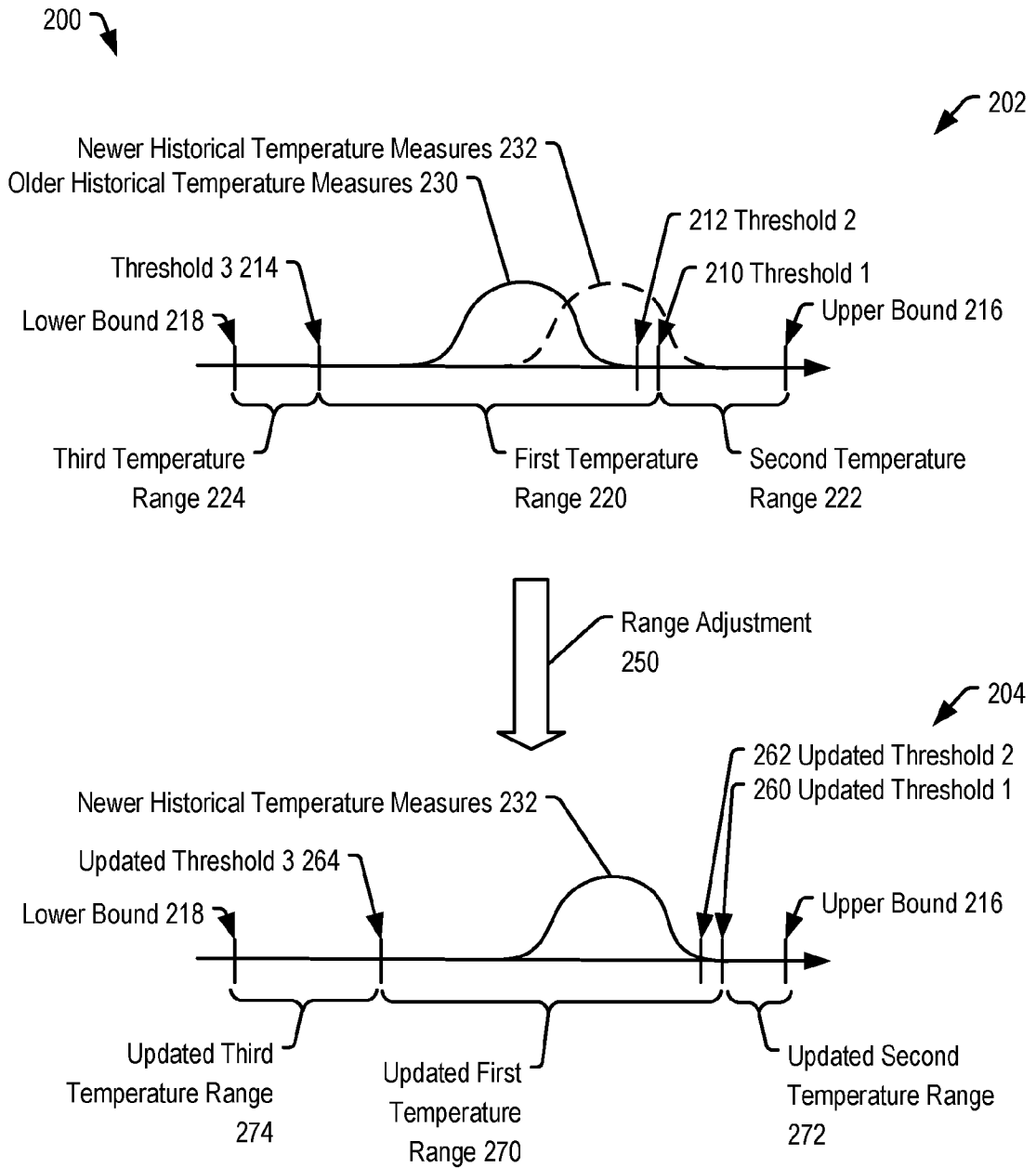


FIG. 1

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**FIG. 2**

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300 

Default Value of a Read
Voltage 301

 302 Offset Table

		Read Temperature Range				
		0	1	2	3	4
Write Temperature Range	0	N/A	Offset_Neg_1	Offset_Neg_2	Offset_Neg_3	Offset_Neg_4
	1	Offset_Pos_1	N/A	Offset_Neg_1	Offset_Neg_2	Offset_Neg_3
	2	Offset_Pos_2	Offset_Pos_1	N/A	Offset_Neg_1	Offset_Neg_2
	3	Offset_Pos_3	Offset_Pos_2	Offset_Pos_1	N/A	Offset_Neg_1
	4	Offset_Pos_4	Offset_Pos_3	Offset_Pos_2	Offset_Pos_1	N/A

 304 Range Table

Range	Temperature
0	-25 to 0
1	1 to 25
2	26 to 50
3	51 to 75
4	76 to 100

FIG. 3

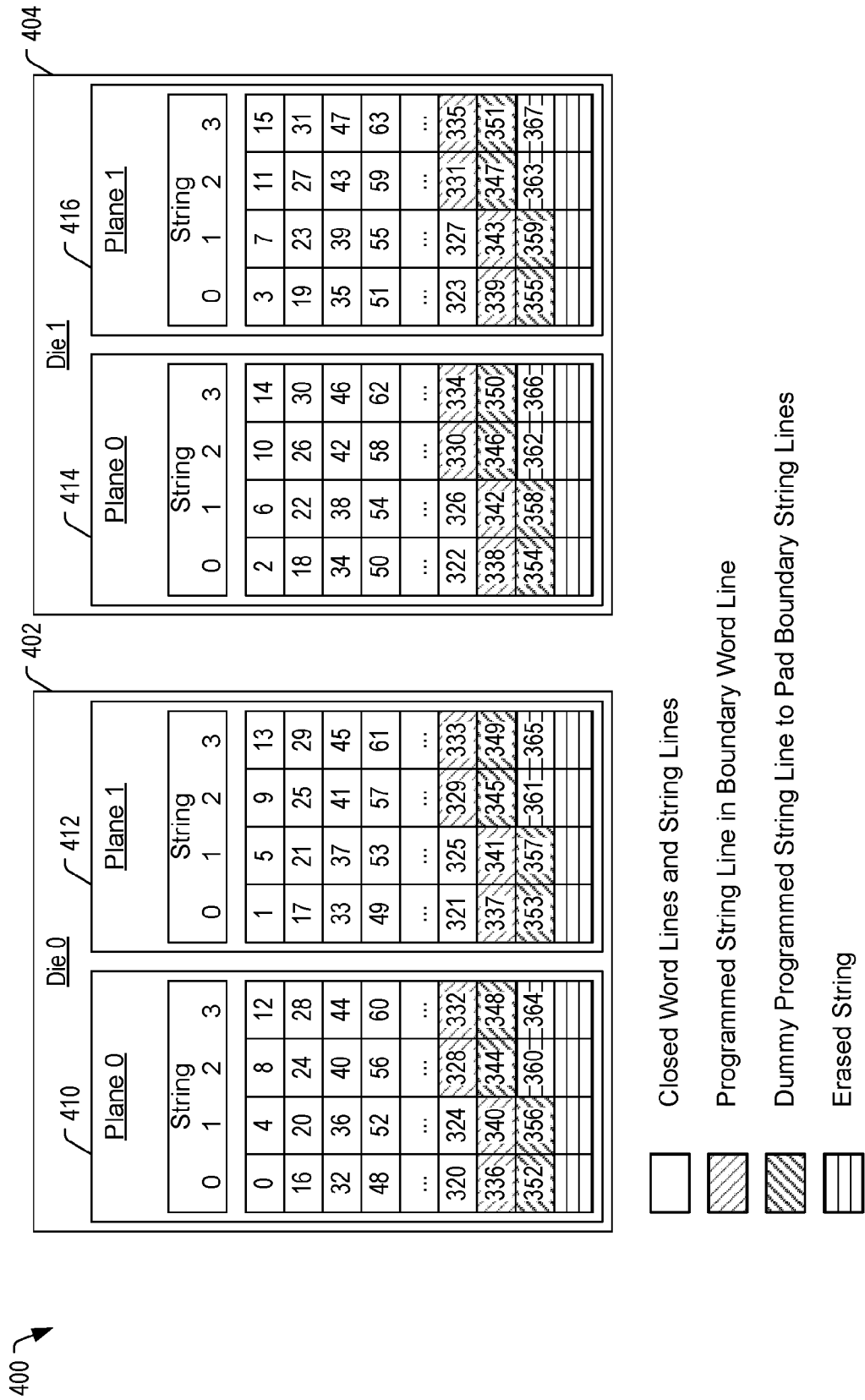


FIG. 4

500 ↗

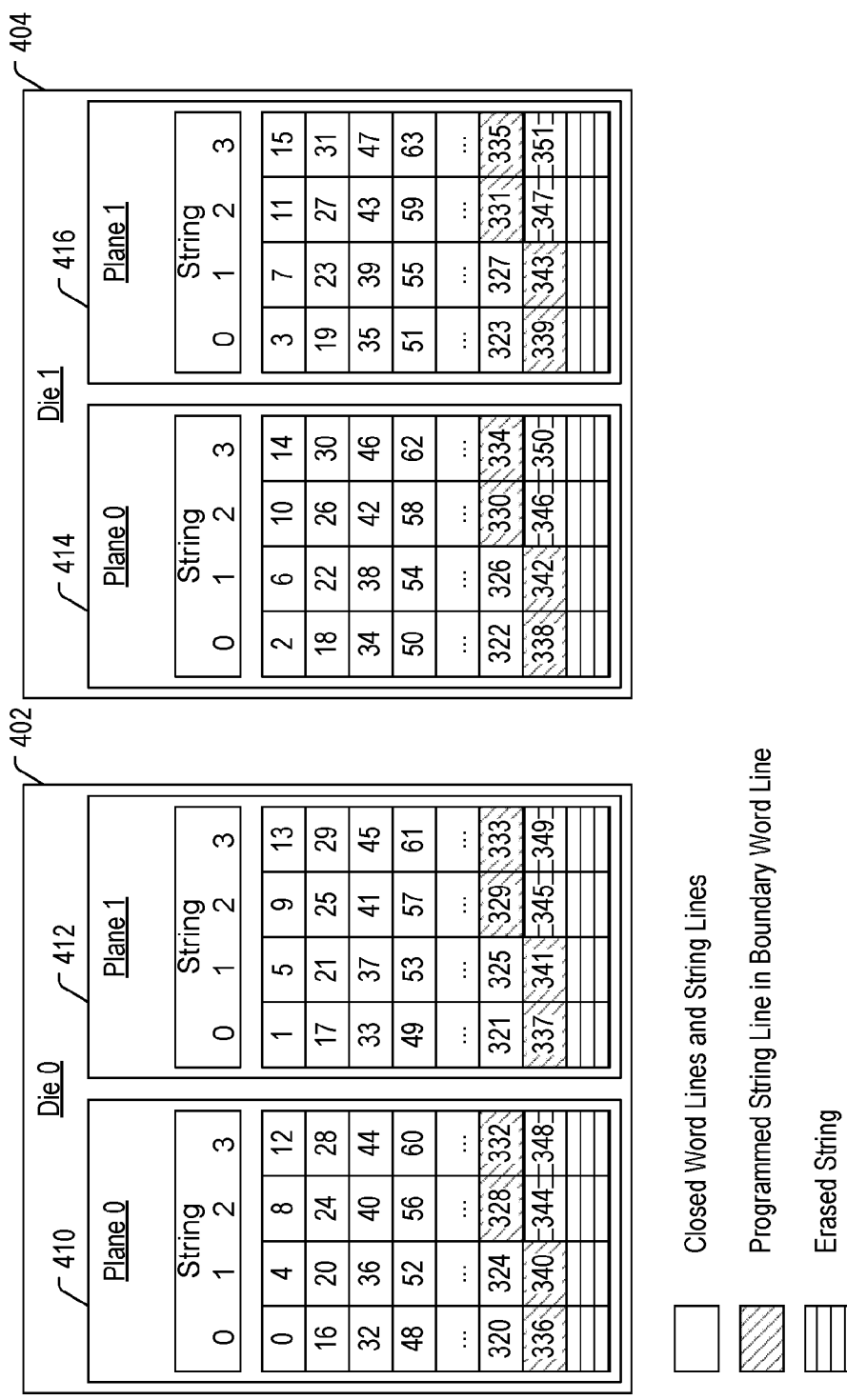


FIG. 5

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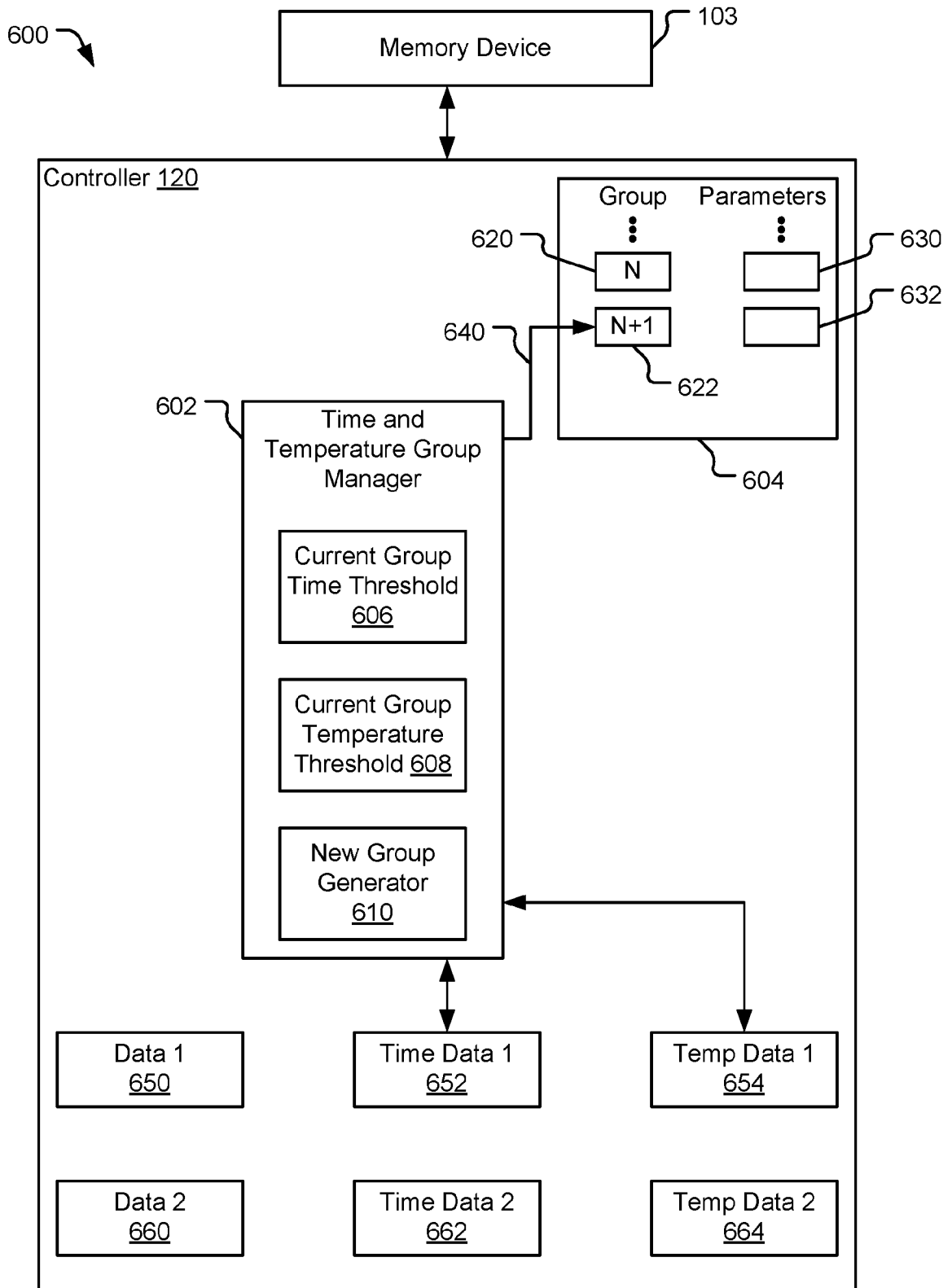
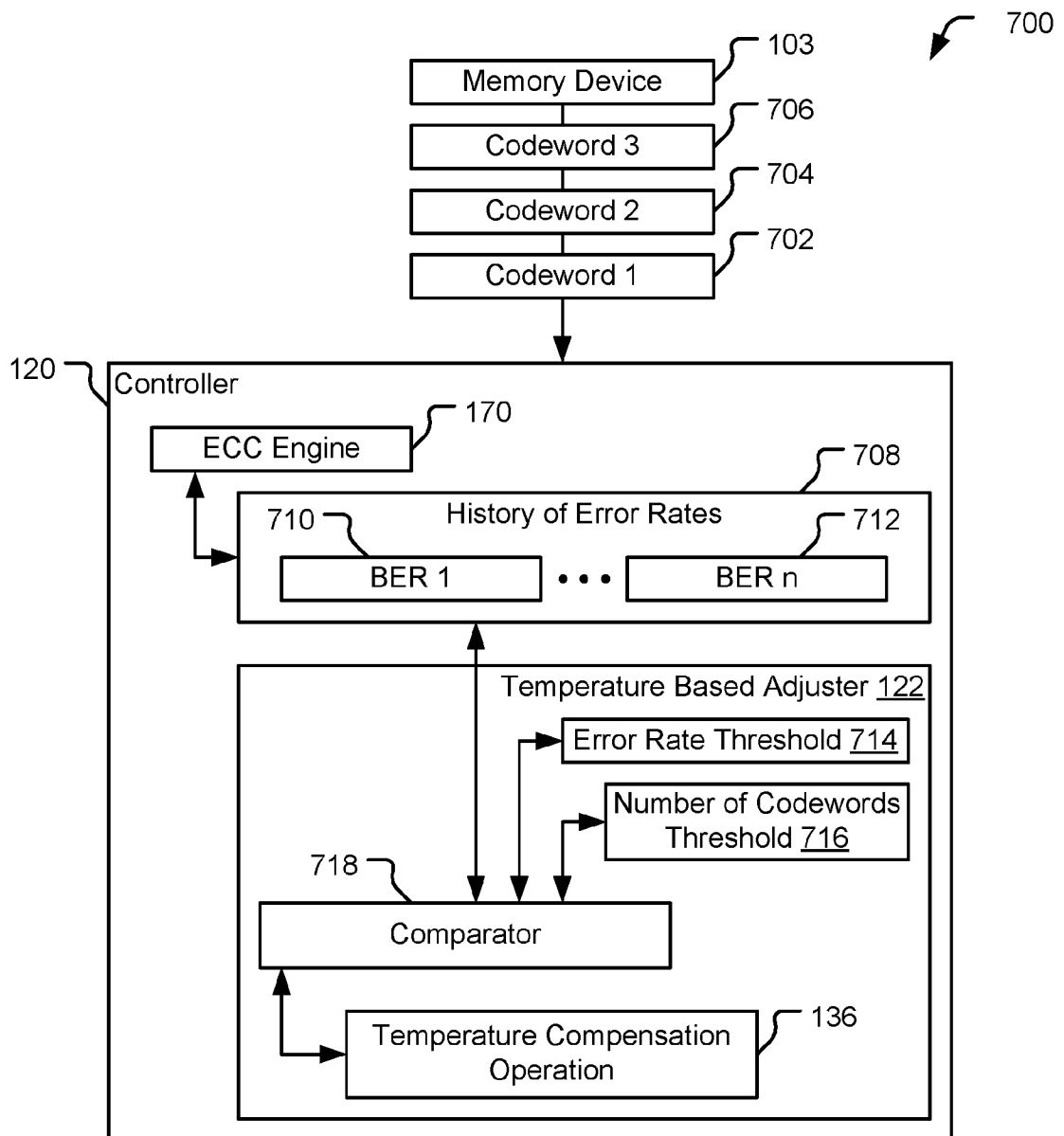
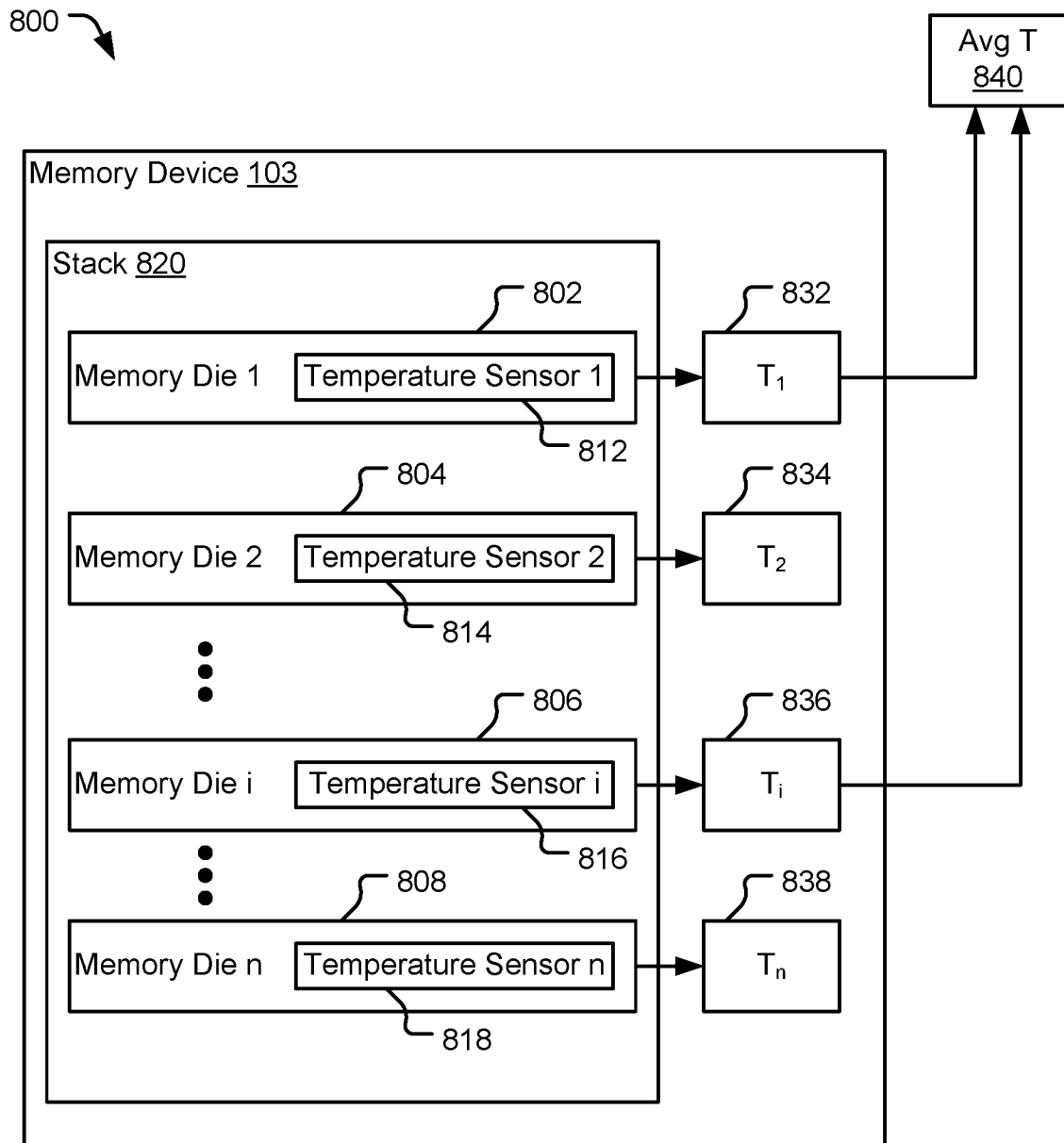


FIG. 6

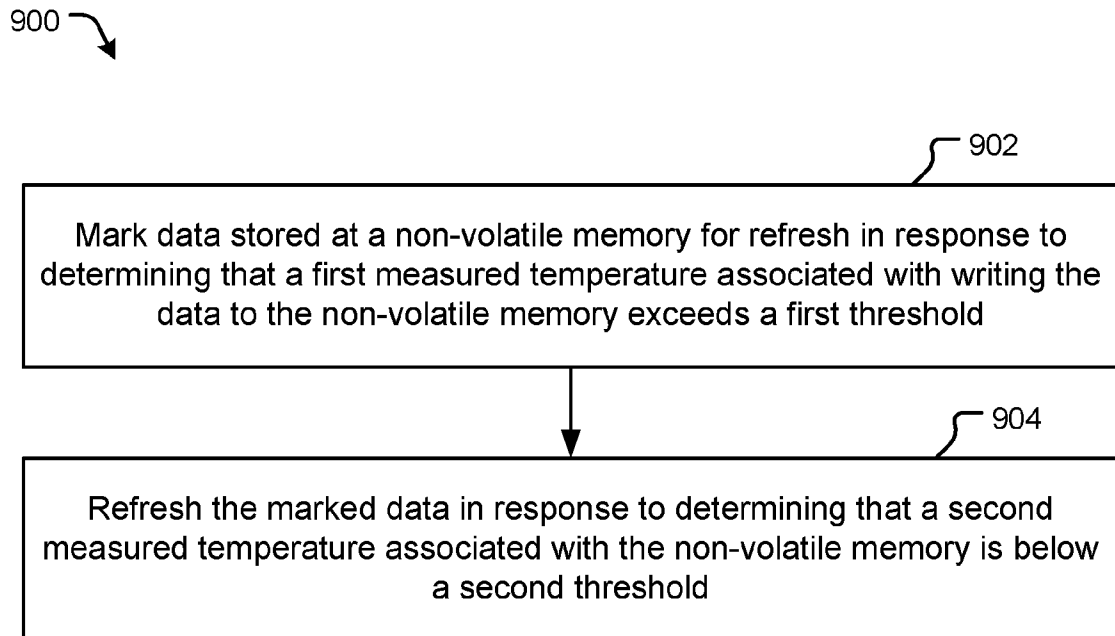
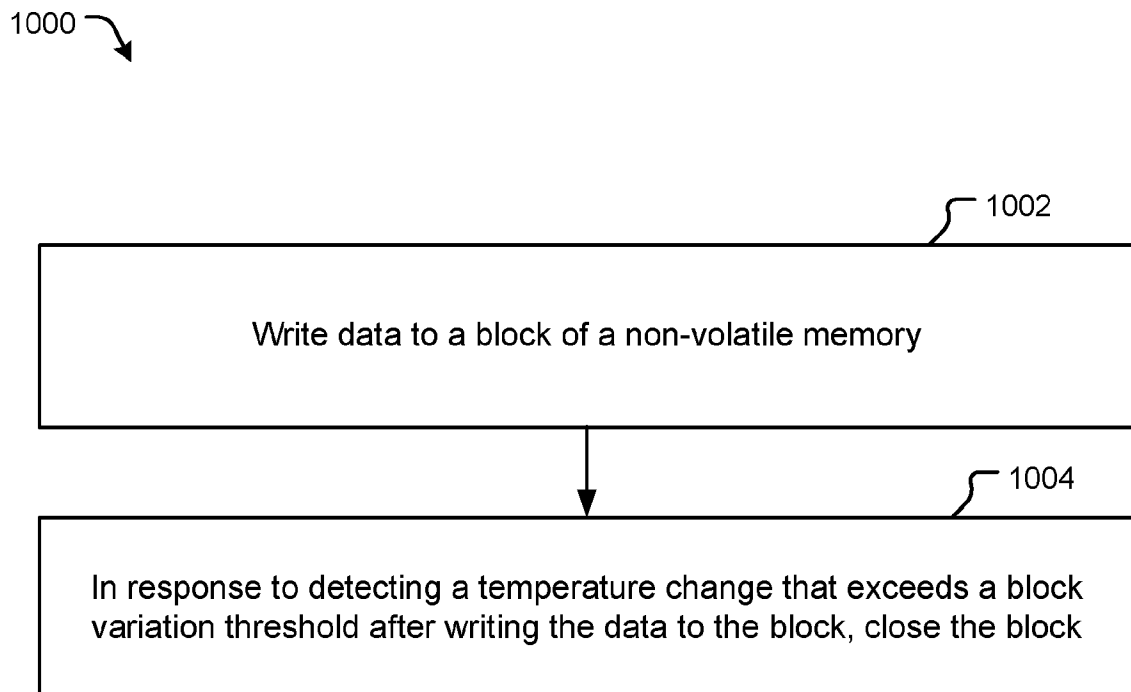
7/12

**FIG. 7**

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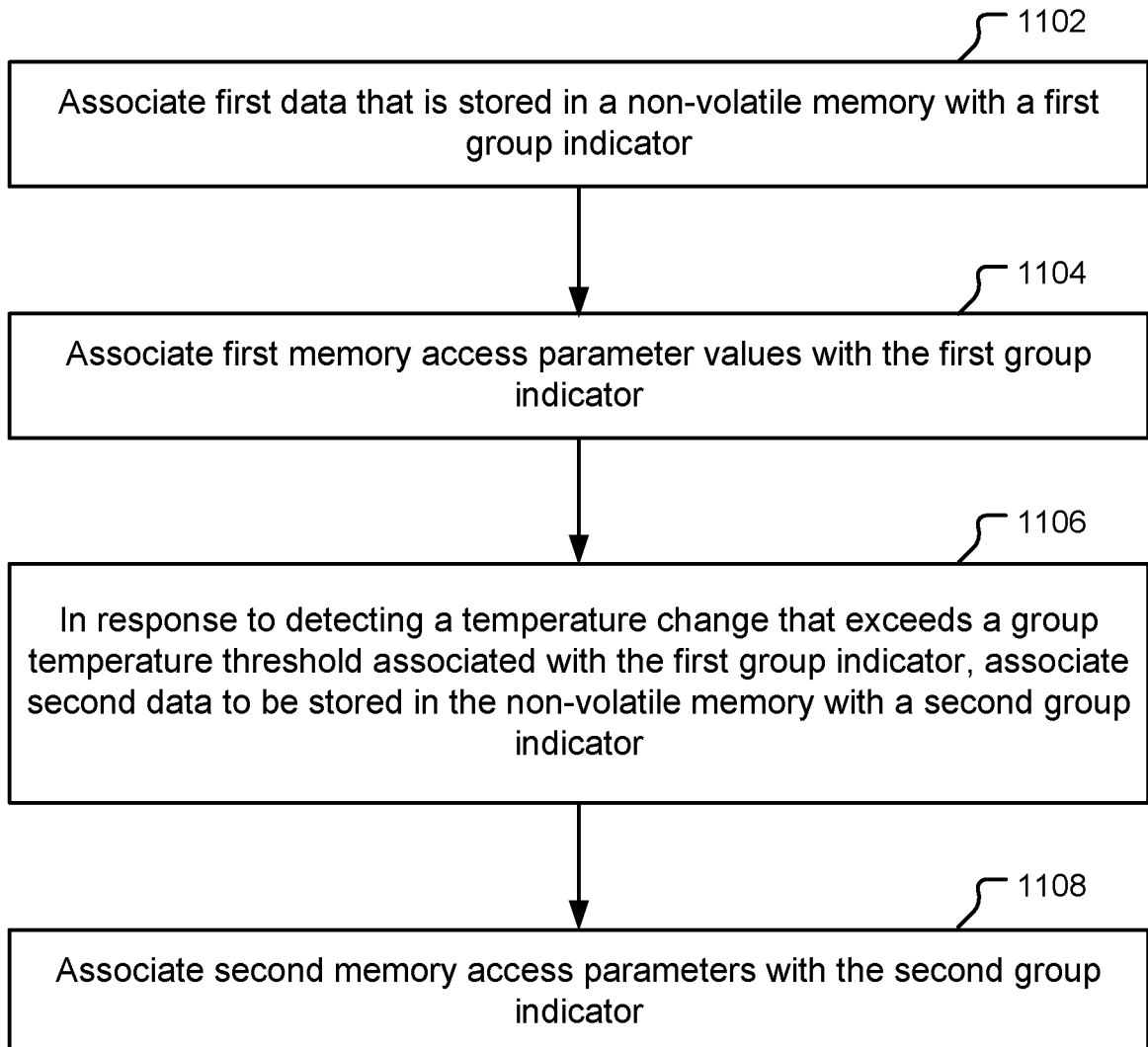
**FIG. 8**

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**FIG. 9****FIG. 10**

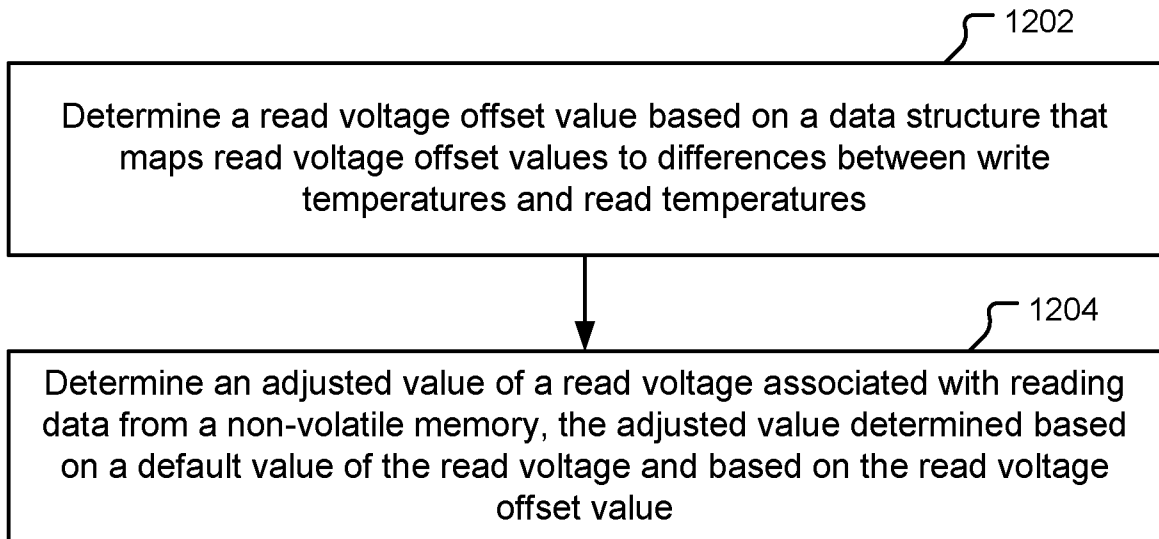
10/12

1100 ↘

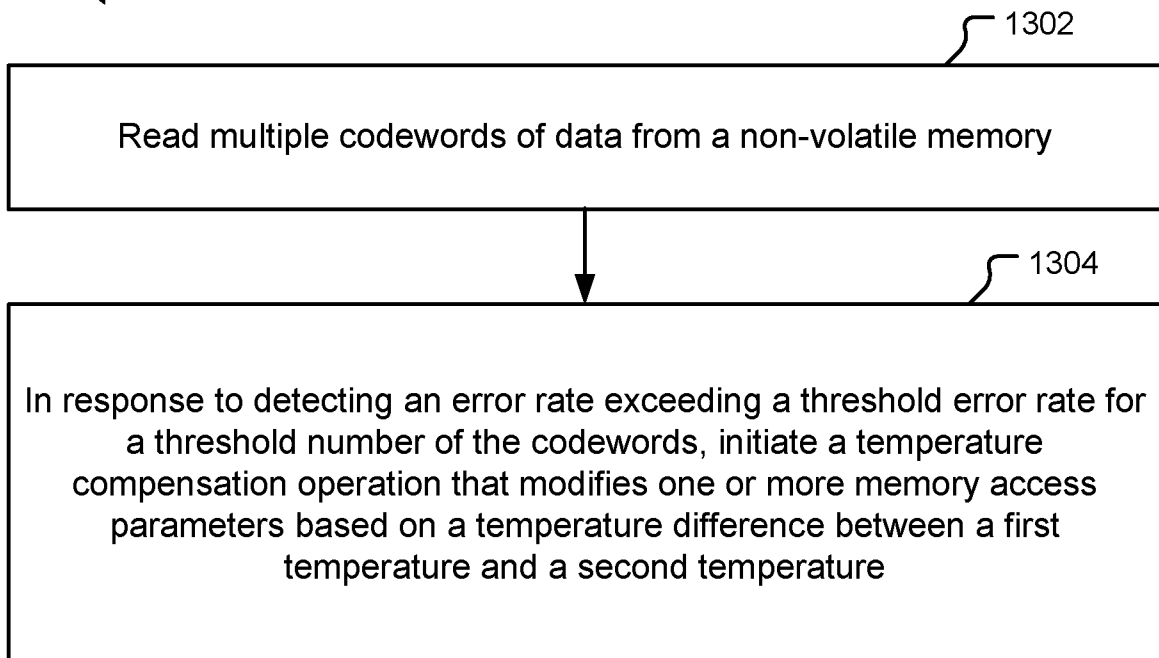
**FIG. 11**

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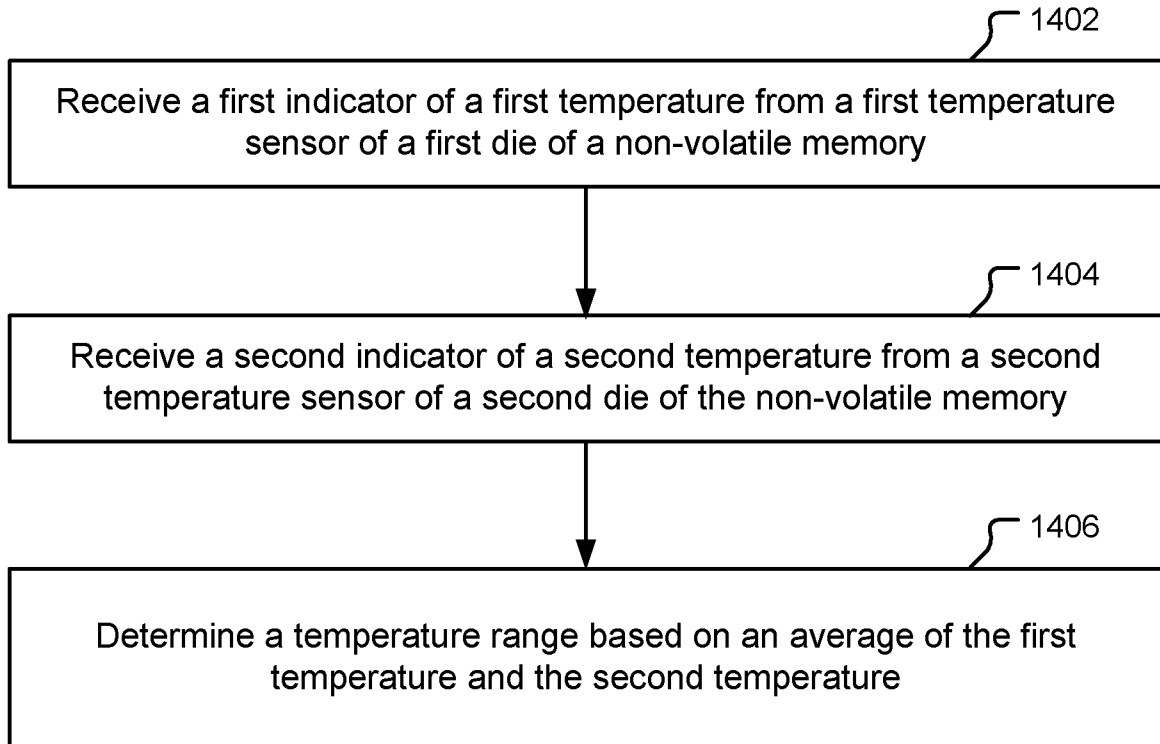
1200 ↘

**FIG. 12**

1300 ↘

**FIG. 13**

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1400 **FIG. 14**

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/019612

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C7/04 G11C11/56 G11C16/10 G11C16/26 G11C16/34
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, COMPENDEX, INSPEC, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/145521 A1 (AOKI YASUNOBU [JP] ET AL) 16 June 2011 (2011-06-16) paragraphs [0070] - [0075], [0079] - [0090], [0101] - [0121]; figures 5,7,8 -----	1-4, 17-19
A	US 2012/134213 A1 (CHOI YOON HEE [KR] ET AL) 31 May 2012 (2012-05-31) abstract figures 3,5A -----	1-4, 17-19

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

9 May 2017

Date of mailing of the international search report

14/07/2017

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
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Authorized officer

Havard, Corinne

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/019612

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-4, 17-19

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 17-19

Data marking for refresh when the writing occurs at high temperature and execution of the refresh when the temperature decreases

2. claims: 5, 6, 20-22

Closing of a block seeing too high temperature variations during write

3. claims: 7, 8, 23, 24

Change of memory access parameters when the temperature varies outside a range associated with first memory access parameter values

4. claims: 9-11, 25-27

Read voltage adjusting based on differences between write and read temperatures

5. claims: 12-14, 28-30

Use of temperature compensated memory (read) access parameters when the error rate is higher than a threshold

6. claims: 15, 16, 31, 32

Determination of a temperature of a memory based on an average of values given by temperature sensors on memory dies

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2017/019612

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2011145521 A1	16-06-2011	JP 5554974 B2	23-07-2014
		JP 2011123703 A	23-06-2011
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US 2012134213 A1	31-05-2012	CN 102479550 A	30-05-2012
		DE 102011087105 A1	06-06-2012
		JP 6022153 B2	09-11-2016
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		KR 20120056424 A	04-06-2012
		US 2012134213 A1	31-05-2012
		US 2014169101 A1	19-06-2014
