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(54) Title: SOLAR CELL SURFACE PASSIVATION USING PHOTO-ANNEAL

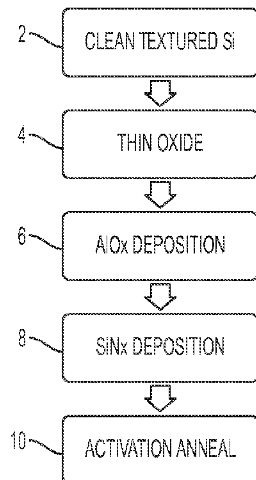

FIG. 1

(57) Abstract: A surface of a silicon substrate is passivated. A silicon oxide layer is formed on a first surface of a silicon substrate. An aluminum oxide layer is formed on the silicon oxide layer. A hydrogenated amorphous silicon nitride layer is formed on the aluminum oxide layer. A high intensity light source illuminates the silicon surface, the silicon oxide layer, the aluminum oxide layer, and the hydrogenated amorphous silicon nitride layer.

WO 2016/019396 A2

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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SOLAR CELL SURFACE PASSIVATION USING PHOTO-ANNEAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application claims the benefit of U.S. provisional patent application 62/032,414 filed on Aug. 1, 2014, which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[002] The present disclosure relates in general to the fields of solar photovoltaic (PV) cells, and more particularly to surface passivation for solar cells.

BACKGROUND

[003] As solar photovoltaic technology is adopted as an energy generation solution on an increasingly widespread scale, improvements relating to solar cell efficiency and fabrication are required. Generally, solar cell structures often include passivation surfaces – for example frontside or light receiving (sunnyside) surface passivation and backside surface passivation opposite the frontside. Manufacturing cost and conversion efficiency factors are driving solar cell semiconductor absorbers ever thinner in thickness and larger in area. Thin semiconductor absorbers and corresponding thin semiconductor absorber solar cell structure aspects/components have increased fragility and are more sensitive to temperature and mechanical processing, thus, complicating and introducing challenges in the processing of these thin absorber based solar cells – particularly relating to high temperature processing.

[004] The performance of semiconductor crystalline silicon based devices such as solar cells strongly depends on minority carrier recombination in the bulk as well as surface regions of the cell. Consequently, for these devices reducing the surface recombination is of utmost importance. Surface recombination effects are becoming progressively more important as silicon semiconductor device dimensions such as the solar cell wafer thicknesses are reduced. Surface passivation may be used to reduce surface recombination. The surface passivation of silicon using amorphous films based on hydrogenated silicon compounds has been the subject of intense research in recent years, particularly for solar cell applications. Stability is one of the key

requirements of frontside passivation films to help guarantee stable power performance over the lifespan (e.g., greater than 25 years) of solar cells in the field, along with high quality surface passivation as measured by surface recombination velocity. Passivation using amorphous aluminum oxide and a silicon nitride stack have been shown to achieve high quality passivation and have demonstrated low surface recombination velocity. However, these passivation schemes using aluminum oxide and a silicon nitride stack showing improved passivation rely on a thermal anneal carried out at higher temperatures, for example a high temperature rapid thermal anneal (e.g., at a temperature greater than 800°C for a period of five seconds) which may damage or impair temperature sensitive solar cells and solar cell structural features.

BRIEF SUMMARY OF THE INVENTION

[005] Therefore, a need has arisen for improved surface passivation processes that provide increased passivation quality at lower processing temperatures. In accordance with the disclosed subject matter, surface passivation processes surface passivation processes are provided which may substantially eliminate or reduces disadvantage and deficiencies associated with previously surface passivation processes.

[006] According to one aspect of the disclosed subject matter, a method for passivating a silicon surface is provided. A silicon oxide layer is formed on a first surface of a silicon substrate. An aluminum oxide layer is formed on the silicon oxide layer. A hydrogenated amorphous silicon nitride layer is formed on the aluminum oxide layer. A high intensity light source illuminates the silicon surface, the silicon oxide layer, the aluminum oxide layer, and the hydrogenated amorphous silicon nitride layer.

[007] These and other aspects of the disclosed subject matter, as well as additional novel features, will be apparent from the description provided herein. The intent of this summary is not to be a comprehensive description of the claimed subject matter, but rather to provide a short overview of some of the subject matter's functionality. Other systems, methods, features and advantages here provided will become apparent to one with skill in the art upon examination of the following FIGUREs and detailed description. It is intended that all such additional systems, methods, features and

advantages that are included within this description, be within the scope of any claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[008] The features, natures, and advantages of the disclosed subject matter may become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference numerals indicate like features and wherein:

[009] **Fig. 1** is a process flow for passivating the surface of a silicon substrate;

[010] **Fig. 2** is a cross-sectional diagram of a passivated silicon substrate consistent with the passivation process of **Fig. 1**;

[011] **Fig. 3** is a process flow for passivating the surface of a silicon substrate;

[012] **Fig. 4** is a graph of relative solar cell open circuit voltage V_{oc} vs. light exposure time;

[013] **Fig. 5** is a graph showing the spectrum of different light sources; and

[014] **Fig. 6** is a graph showing the solar radiation spectrum.

DETAILED DESCRIPTION

[015] The following description is not to be taken in a limiting sense, but is made for the purpose of describing the general principles of the present disclosure. The scope of the present disclosure should be determined with reference to the claims. Exemplary embodiments of the present disclosure are illustrated in the drawings, like aspects and identifiers being used to refer to like and corresponding parts of the various drawings.

[016] And although the present disclosure is described with reference to specific embodiments and components, such as a back contact back junction (BCBJ) silicon solar cell, one skilled in the art could apply the principles discussed herein to other solar cell structures solar cell semiconductor materials (e.g., GaAs, other compound III-V materials, etc.), solar cell structures (e.g., front contact or back contact front junction), fabrication processes (e.g., various deposition and diffusion methods and materials), as well as alternative technical areas and/or embodiments without undue experimentation.

[017] Fabrication methods and structures are provided for the passivation of solar cells. A photo-anneal improves surface passivation quality and potentially eliminates

a higher temperature anneal. Methods are described for achieving high-quality, reduced recombination passivation on silicon surfaces by utilizing photo-anneal processes to improve and stabilize the passivation that is needed for high performance solar cells. Processes steps may include growth and/or deposition of a passivation stack (e.g., hydrogenated amorphous silicon nitride on thin aluminum oxide on silicon oxide), and final post-annealing. Process steps such as appropriate surface preparation and cleaning of the silicon substrate prior to or integrated with the growth and/or deposition of the passivation stack may also be utilized. These processes are able to achieve stable surface recombination velocities that are equivalent to or lower than known results without a need for the formation of a front surface field.

[018] **Fig. 1** is a process flow showing a passivation method which may be applied to smooth, rough, or textured surfaces of a surface of a silicon substrate. In step **2** the surface of a silicon substrate is cleaned. In step **4** a silicon oxide thin film (e.g., having a thickness in the range of 1-3 nm and in some instances having a thickness in the narrower range of 1-2 nm) is formed on the clean surface of the silicon substrate (e.g., at a temperature less than 50°C). In step **6** aluminum oxide (e.g., having a thickness in the range of 1-50 nm and in some instances having a thickness in the narrower range of 20-30 nm) is deposited on the chemical oxide thin film (e.g., with deposition temperatures in the range of 100-500°C and in some instances in the narrower range 150-200°C). In step **8** a hydrogenated amorphous silicon nitride thin film (e.g., having a thickness in the range of 10-200 nm and in some instances having a thickness in the narrower range of 50-80 nm) is deposited on the aluminum oxide (e.g., with deposition temperatures in the range of 100-500°C and in some instances in the narrower range 250-350°C). In step **10** a photo-anneal illuminates a high intensity light source on the silicon surface and passivation stack (e.g., at temperatures less than 500°C and in some instances in the narrower range of less than 380°C) which activates and stabilizes the passivation of the silicon surface of the substrate.

[019] **Fig. 2** is a representative cross-sectional diagram of a passivated silicon substrate consistent with the passivation process of **Fig. 1**. Thin oxide layer **14** is formed on silicon substrate **12**. Aluminum oxide layer **16** (AlO_X) is formed on thin oxide layer **14** and silicon nitride layer **18** (SiN_X) is formed on aluminum oxide layer **16**.

[020] The thin silicon oxide layer may be a chemical oxide having a thickness in the range of 1-3 nm and as thin as 1-2 nm which may be formed in clean dry air with UV

light exposure creating an ozone gas on a hydrofluoric acid HF cleaned silicon surface (e.g., cleaned using an HF dip) at room temperature. In another embodiment, the oxide layer may be formed using a wet chemistry step, for example using a heated hydrogen peroxide solution process.

[021] Then an aluminum oxide film having a thickness less than 50 nm may be deposited in an inline or batch/cluster tool (e.g., deposited using plasma enhanced chemical vapor deposition PECVD, atmospheric pressure chemical vapor deposition APCVD, or atomic layer deposition ALD). In one embodiment, the aluminum oxide may be formed by: introducing a clean silicon substrate with chemical oxide into a plasma enhanced chemical vapor deposition chamber; then deposition of 1-40 nm thick aluminum oxide film at temperatures of 100-500°C using tri-methyl aluminum (TMA), N_2O or O_2, and N_2 gas precursors with the aluminum oxide deposition conditions tuned to obtain a refractive index between 1.50 to 1.70 and in some instances in the narrower range of 1.58-1.60.

[022] The hydrogenated amorphous silicon nitride thin film having a thickness less than 200 nm may also be deposited using an inline or batch/cluster tool (e.g., deposited using plasma enhanced chemical vapor deposition PECVD, low pressure chemical vapor deposition LPCVD, or atomic layer deposition ALD). In one embodiment, the hydrogenated amorphous silicon nitride thin film may be formed by: introducing the silicon substrate with aluminum oxide into a plasma enhanced chemical vapor deposition chamber; then deposition of 10-200 nm thick amorphous silicon nitride film at temperatures of 100-500°C using SiH_4, Si_2H_6, NH_3, H_2, and N_2 gas precursors with the silicon nitride deposition conditions tuned to obtain a refractive index between 1.86-2.10. In consideration with other factors, the hydrogenated amorphous silicon nitride may be deposited at a temperature equal to or higher than the aluminum oxide deposition temperature and lower than 500°C to assist in obtaining ultra-low surface recombination velocities.

[023] The photo-anneal/stabilization step may be performed by exposing the passivation stack (e.g., thin silicon oxide, aluminum oxide, and hydrogenated amorphous silicon nitride thin film) and silicon substrate to a high intensity light source to provide low surface recombination velocities (e.g., low surface recombination velocities less than 10 cm/sec.) and in some instances ultra-low recombination surface velocities (e.g., ultra-low surface recombination velocities less than 5 cm/sec.). In one embodiment, the photo-anneal is performed in a separate

inline or batch type tool. Alternatively, for example consistent with **Fig. 1**, the photo-anneal may be a part of the silicon nitride deposition tool (e.g., a plasma enhanced chemical vapor deposition chamber) which may also be used for the deposition of aluminum oxide – in other words a single tool used for the deposition of aluminum oxide and silicon nitride and the photo-anneal process. The photo-anneal process may be carried out using metal-halide lamps, with or without UV filters, or alternatively using tungsten-halogen lamps or mercury-vapor lamps. In one embodiment, photo-anneal may be performed after a thermal activation anneal, for example a thermal activation anneal at temperature below 500°C and in some instances below 380°C, which may also be performed in the same tool as the deposition of aluminum oxide and silicon nitride and the photo-anneal process.

[024] In one embodiment, the need for an additional end-of-the-line high temperature sun exposure anneal may be eliminated and a high cell efficiency with full light induced degradation LID mitigation effects achieved by performing the post-passivation anneal in, for example, a tungsten-halogen lamp-heated furnace (e.g., an in-line furnace using tungsten halogen lamp heating). In addition to reducing and/or eliminating the need for an additional end-of-the-line high temperature sun exposure anneal, this method also lowers the effective post-passivation deposition anneal temperature due to the concurrent photochemical effects of intense visible and IR photons from the tungsten-halogen lamp source — a benefit particularly advantageous for temperature sensitive solar cells and solar cell structure materials. The AlO_x interface charge formation involves a thin interfacial silicon oxide layer which plays an important role in formation of the negative fixed charge density. Light exposure of the passivated surface increases fixed charge in the AlO_x and reduces surface recombination thus providing improved passivation. In order to take full advantage of these potential benefits, the sunnyside of the solar cell must be exposed to or "see" the tungsten-halogen lamp source (like seeing the sun source). **Fig. 5** is a graph showing the spectrum of different light sources. **Fig. 6** is a graph showing the solar radiation spectrum. As shown in the graphs of **Figs. 5** and **6**, the typical radiation spectrum of a tungsten-halogen lamp source closely matches that of the sunlight (note a tungsten-halogen lamp source has less UV content as compared to sunlight).

[025] The light for photochemical anneal may be primarily in the visible range (400 nm to 800 nm) as well as the near IR range (800 nm to about 2000 nm wavelength range) – for example a 4100 K halogen lamp. The near-IR range (800 nm – 2000 nm)

has selective photochemical absorption lines for water molecules (and OH – hydroxyl groups), as indicated by the notches in the solar spectrum. Some activation of the embedded hydroxyl groups may cause the passivation improvement (and efficiency increase) with end-of-the-line sun exposure.

[026] In one embodiment, the photo-anneal may be performed in vacuum or N_2, H_2, NH_3 or forming gas (N_2+H_2) ambient for approximately 1-120 minutes at or above the temperature of deposition of amorphous silicon nitride thin film (e.g., 100-500°C) to produce ultra-low surface recombination velocities. In another embodiment, for example in the case of a thermal anneal after deposition of the passivation stack which may utilized before or concurrent with a photo-anneal.

[027] **Fig. 3** is a process flow showing a passivation method which may be applied to smooth, rough, or textured surfaces of a silicon surface similar to **Fig. 1**. In step **20** the surface of a silicon substrate is cleaned. In step **22** a chemical oxide thin film (e.g., having a thickness in the range of 1-3 nm) is formed on the clean surface of the silicon substrate. In step **24** aluminum oxide (e.g., having a thickness in the range of 1-40 nm) is deposited on the chemical oxide thin film (e.g., with deposition temperatures in the range of 100-500°C). In step **26** a hydrogenated amorphous silicon nitride thin film (e.g., having a thickness in the range of 10-200 nm) is deposited on the aluminum oxide (e.g., with deposition temperatures in the range of 100-500°C). In step **28** a thermal anneal step at temperature below 500°C and in some instances below 380°C. In step **30** a photo-anneal illuminates a high intensity light source on the silicon surface and passivation stack (e.g., at temperatures less than 500°C and in some instances in the narrower range of less than 380°C) which activates and stabilizes the passivation of the silicon surface of the substrate. In step **30**, as described above, a photo-anneal may be performed at or above the deposition temperature of the amorphous silicon nitride thin film.

[028] In one embodiment, the high intensity light (e.g., greater than twice the intensity of the sun or two sun) may be applied for a short duration, for example applied less than 20 minutes (e.g., between 30 seconds and 20 minutes), to produce high quality passivation - for example, a light intensity 2.5 times from a metal-halide lamp with a UV filter (or in some instances a tungsten-halogen lamp) at an intensity 2.5 times sun (2.5 sun) applied for ten minutes. The light source intensity and time period, as well as light source wavelength, may be adjusted to achieve high quality passivation. **Fig. 4** is a graph showing relative solar cell open circuit voltage V_{oc} vs.

light exposure time where “reference lower intensity” is one sun and “high intensity” is two suns. As shown in the graph of **Fig. 4**, high intensity lamps may increase processing throughput.

[029] In another embodiment, a passivated substrate is formed using a silicon substrate with either p or n type substrate doping and a diffused sub-surface layer of the other doping type, n or p respectively, then the passivated stack is formed on the top side (sunny side or light receiving side) of the silicon substrate, and then the structure is post-annealed by illumination of ta high intensity light source at temperatures less than 500°C and in some instances in the narrower range of less than 380°C.

[030] In operation, the photo-annealing methods described herein, for example using tungsten-halogen-lamp-heated furnace, for post passivation stack deposition photo-anneal provide some or all of the following benefits: elimination of an additional end-of-the-line sun exposure process step; reduction of both the temperature and time of passivation material deposition anneal process; improvement of the solar cell open circuit voltage V_{oc} and cell efficiency; and improved LID resistance.

[031] The foregoing description of the exemplary embodiments is provided to enable any person skilled in the art to make or use the claimed subject matter. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the innovative faculty. Thus, the claimed subject matter is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

CLAIMS

What is claimed is:

1. A method for passivating a silicon surface, comprising:

   forming a silicon oxide layer on a first surface of a silicon substrate;

   forming an aluminum oxide layer on said silicon oxide layer;

   forming a hydrogenated amorphous silicon nitride layer on said aluminum oxide layer;

   illuminating said silicon surface and said silicon oxide layer, said aluminum oxide layer, and said hydrogenated amorphous silicon nitride layer with a high intensity light source.

2. The method for passivating a silicon surface of Claim 1, further comprising cleaning said first surface of said silicon substrate before forming said oxide layer.

3. The method for passivating a silicon surface of Claim 2, wherein said step of cleaning said first surface of said silicon substrate before forming said silicon oxide layer uses an HF dip.

4. The method for passivating a silicon surface of Claim 1, wherein said silicon oxide layer is formed by applying UV light to said first surface of said silicon substrate.

5. The method for passivating a silicon surface of Claim 1, wherein said silicon oxide layer is a chemical silicon oxide layer.

6. The method for passivating a silicon surface of Claim 5, wherein said chemical silicon oxide layer has a thickness in the range of 1 to 3 nanometers.

7. The method for passivating a silicon surface of Claim 1, wherein said aluminum oxide layer has a thickness in the range of 1 to 40 nanometers.

8. The method for passivating a silicon surface of Claim 1, wherein said aluminum oxide layer has a refractive index in the range of 1.50 to 1.70.

9. The method for passivating a silicon surface of Claim 1, wherein said hydrogenated amorphous silicon nitride layer has a thickness in the range of 10 to 200 nanometers.

10. The method for passivating a silicon surface of Claim 1, wherein said hydrogenated amorphous silicon nitride layer has a refractive index in the range of 1.86 to 2.10.

11. The method for passivating a silicon surface of Claim 1, further comprising performing a thermal activation anneal before said photo-annealing.

12. The method for passivating a silicon surface of Claim 12, wherein said thermal activation anneal is performed at a temperature below 380°C.

13. The method for passivating a silicon surface of Claim 1, wherein said photo-annealing is performed in vacuum or N_2, H_2, NH_3 or forming gas (N_2+H_2) ambient for approximately 1-120 minutes.

14. The method for passivating a silicon surface of Claim 1, wherein said photo-annealing is performed at a temperature below 380°C.

15. The method for passivating a silicon surface of Claim 1, wherein said high intensity light source is a metal-halide lamp.

16. The method for passivating a silicon surface of Claim 1, wherein said high intensity light source is a tungsten-halogen lamp.

17. The method for passivating a silicon surface of Claim 1, wherein said high intensity light source is a mercury-vapor lamp.

18. The method for passivating a silicon surface of Claim 1, wherein said high intensity light source is twice the intensity of the sun and is applied for a time period less than 20 minutes.

19. A method for passivating a silicon surface, comprising:

forming a chemical silicon oxide layer having a thickness in the range of 1 to nanometers on a clean first surface of a silicon substrate by applying UV light to said clean first surface;

depositing an aluminum oxide layer having a thickness in the range of 1 to 40 nanometers and a refractive index in the range of 1.50 and 1.70 on said chemical silicon oxide layer at a deposition temperature less than 500°C;

depositing a hydrogenated amorphous silicon nitride layer having a thickness in the range of 10 to 200 nanometers and a refractive index in the range of 1.86 to 2.10 on said aluminum oxide layer at a deposition temperature less than 500°C;

illuminating said silicon surface and said silicon oxide layer, said aluminum oxide layer, and said hydrogenated amorphous silicon nitride layer with a high intensity light source having a light intensity at least twice the intensity of the sun and for time period less than 20 minutes at a temperature less than 380°C.

20. The method for passivating a silicon surface of Claim 19, further comprising performing a thermal activation anneal at a temperature below 380°C before said photo-annealing.

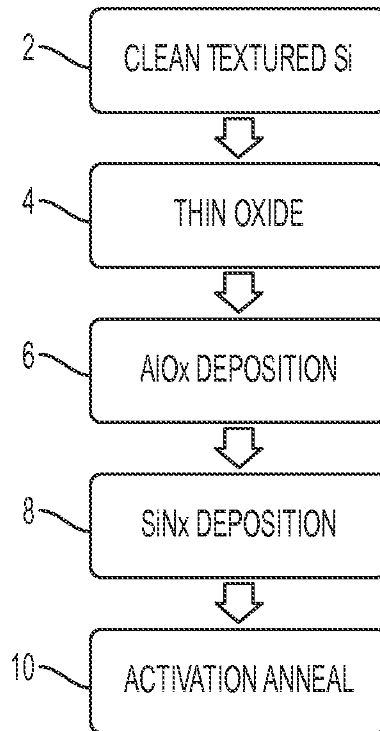

FIG. 1

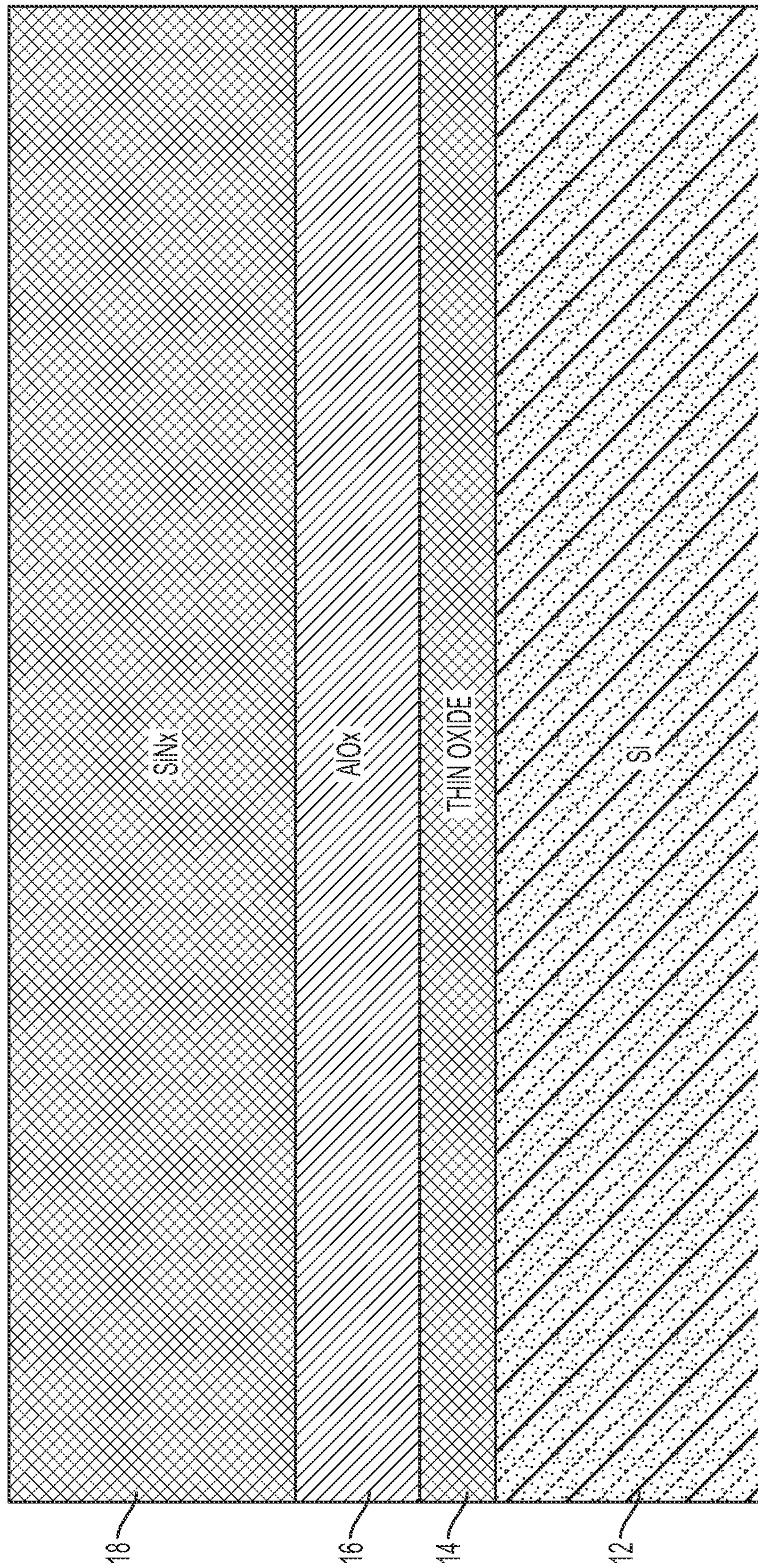

FIG. 2

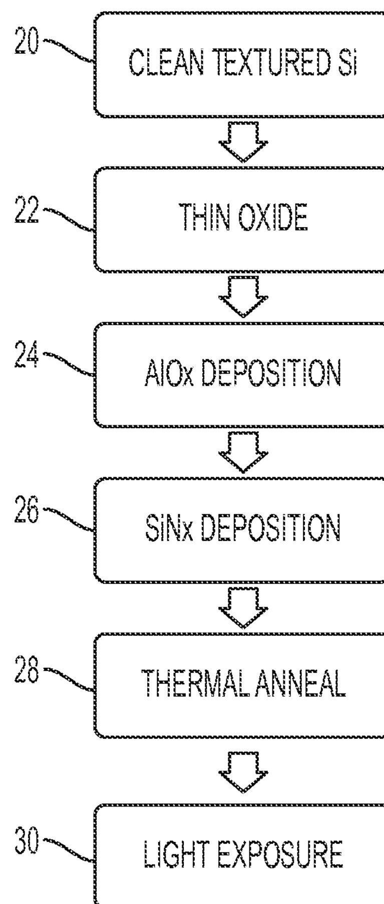

FIG. 3

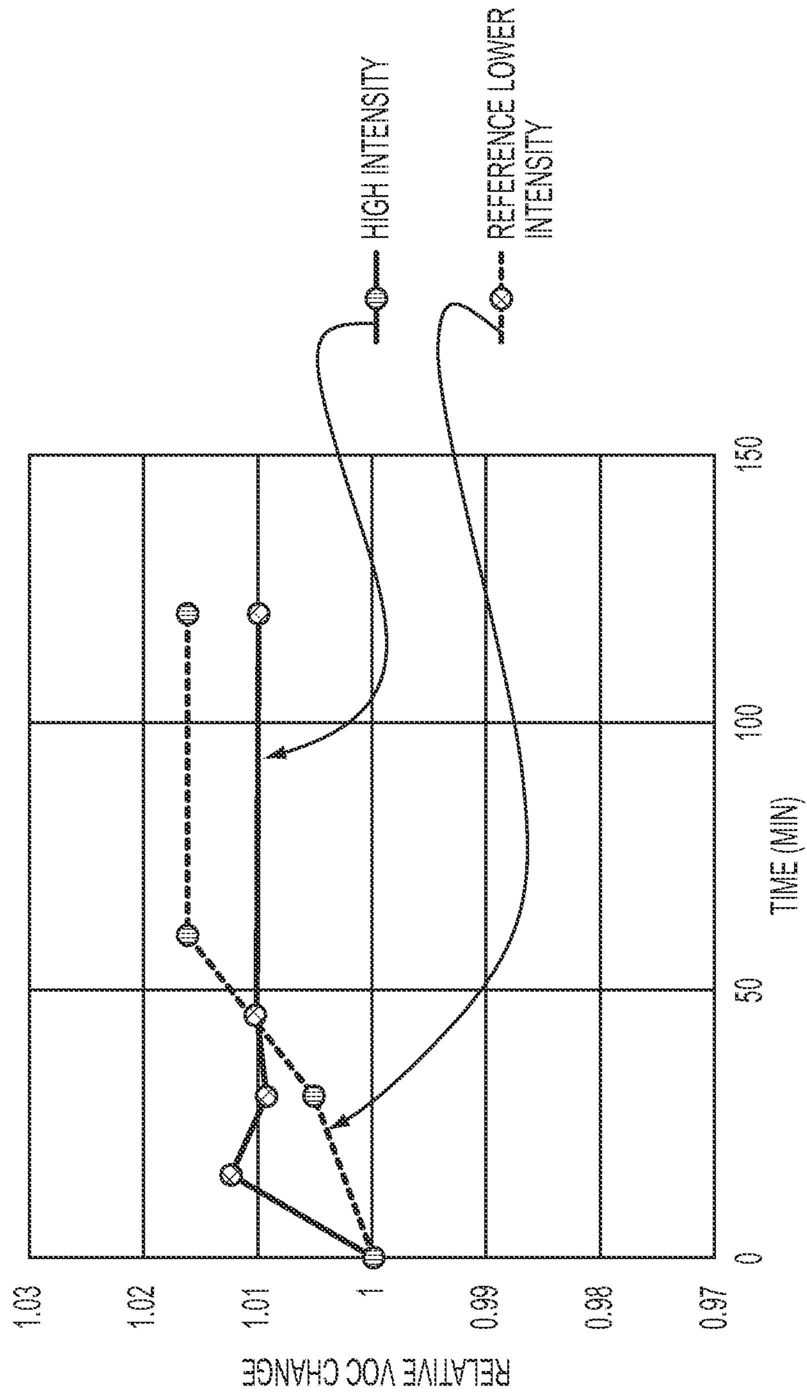

FIG. 4

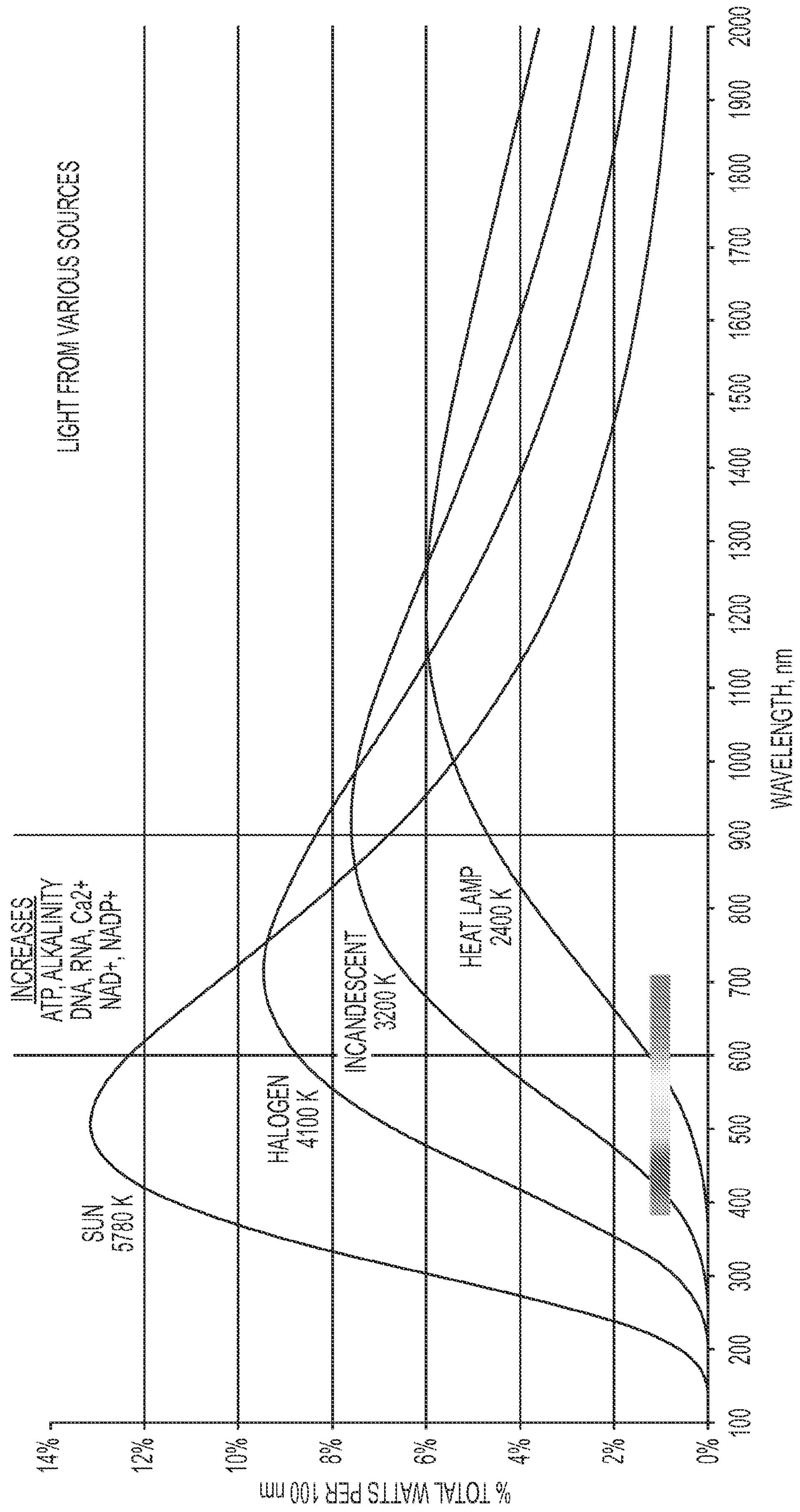

FIG. 5

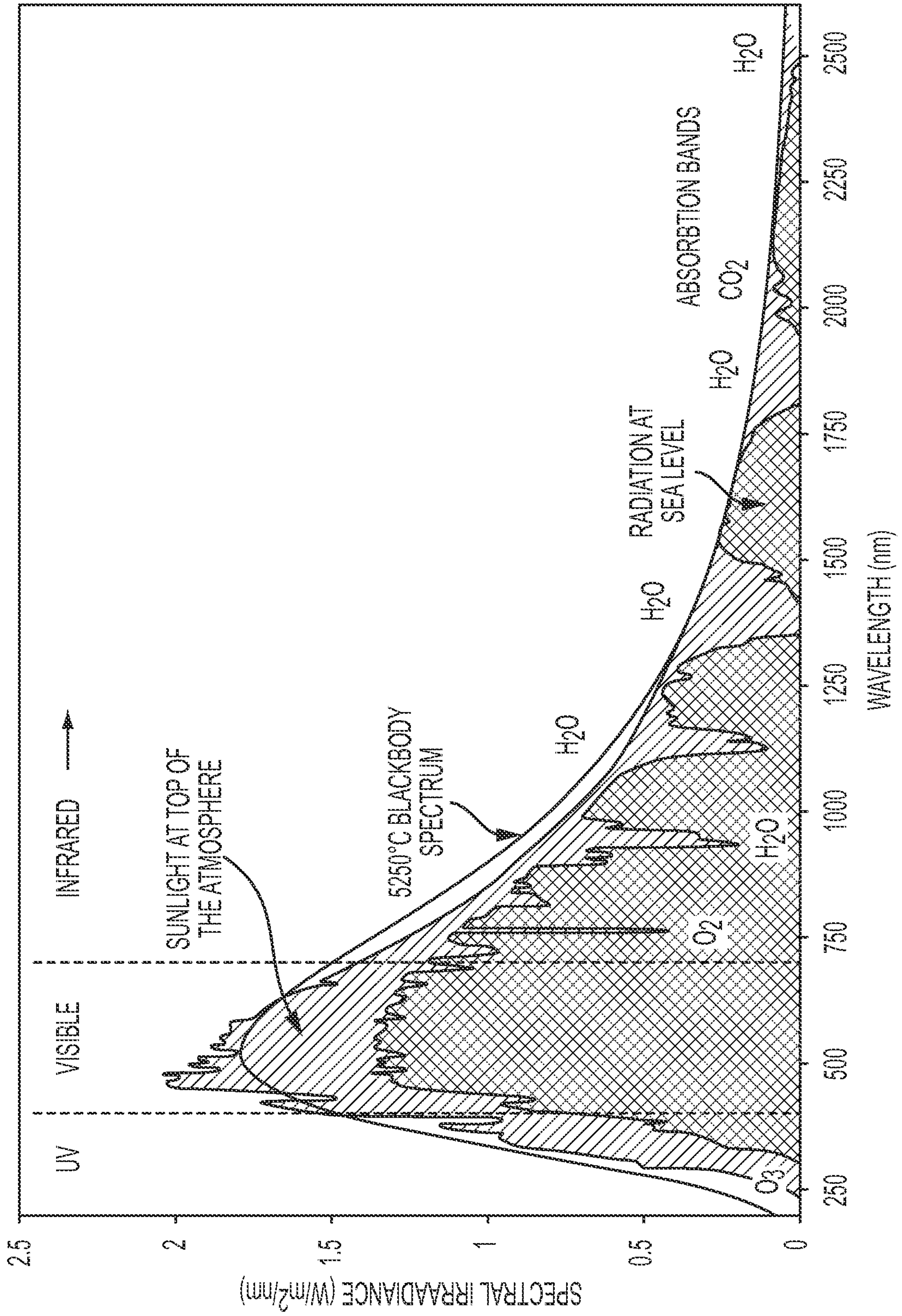

FIG. 6