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ENCODING AND STORAGE APPARATUS FOR TRAFFIC MEASURING

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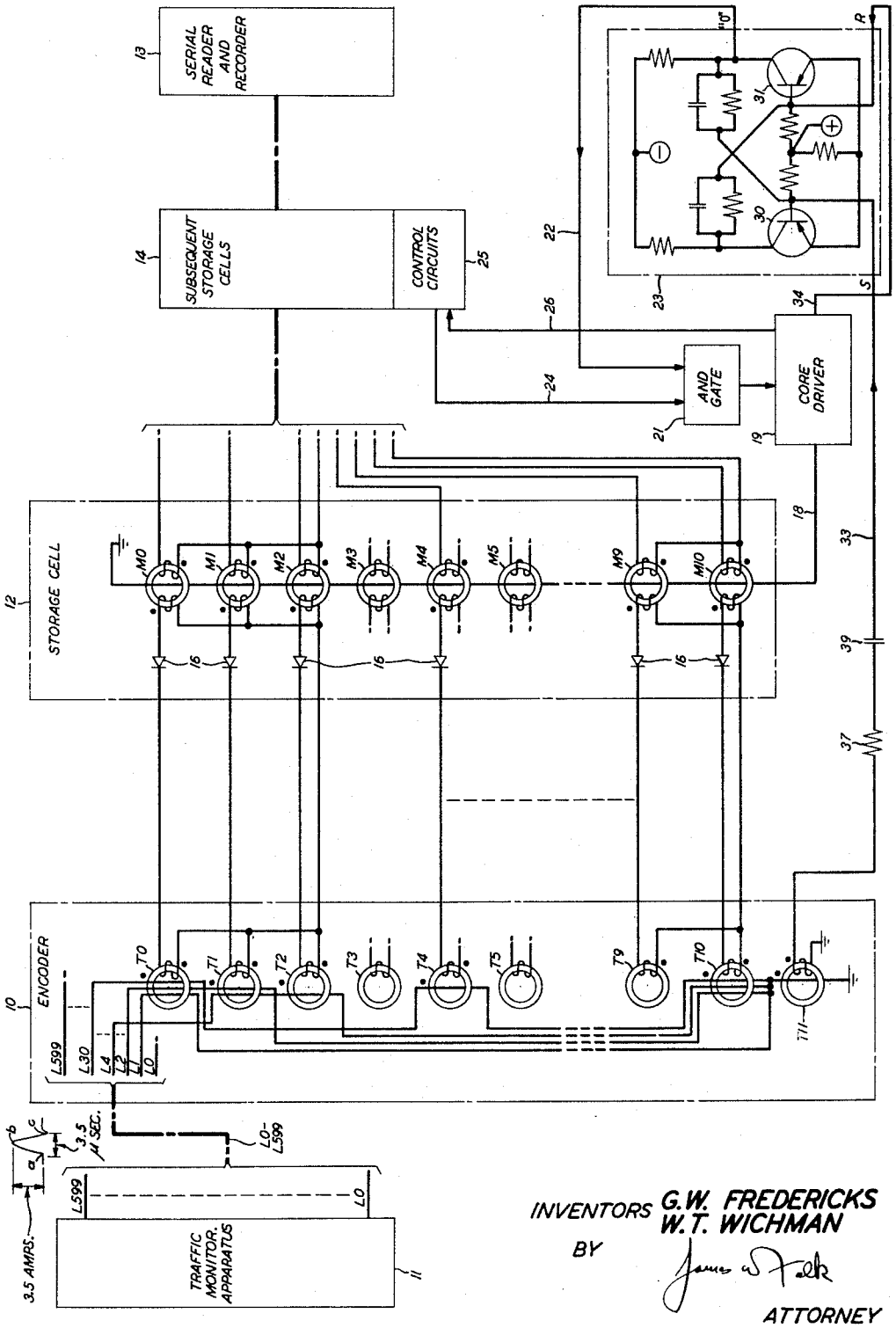

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ENCODING AND STORAGE APPARATUS FOR TRAFFIC MEASURING

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This invention relates to traffic measuring apparatus and, particularly, to encoding and storage apparatus to be included in traffic measuring apparatus.

Generally, statistical data for purposes of traffic studies is initially accumulated in a form which is identifiable on an immediate basis as relevant to a plurality of units of equipment to be studied. For example, such data normally appears as electrically indistinguishable pulse indications directed from traffic monitoring circuits along particular control leads which are peculiarly identified with either an individual one or a group of selected ones of the plurality of units of equipment. However, as each of the pulse indications so directed have a finite duration, it becomes evident that the information represented thereby is lost and not available for traffic studies unless such indications are either immediately recorded or processed.

Heretofore, the general practice has been to connect an individual mechanical counter device or other equally cumbersome apparatus to a control lead emanating from a traffic monitoring circuit individually associated with each individual one or a group of selected ones of the plurality of units of equipment to be studied; each counter device was thereupon operative to count and record the individual pulse indications directed along the control lead. The shortcomings in this manner of accumulating statistical data are obvious as considerable time and effort must be expended by human agents in compiling, interpreting, and indexing such data. The effort required to perform such operations necessarily limits the amount of statistical data which can be accumulated. Further, the need of employing human agents for such operations not only increases the cost of the individual traffic study but also provides a major source of error therein. Priorly, an indexing of statistical data involved the translation thereof by human agents to a notational form which could thereafter be processed by automatic data processing machines. For example, statistical data was generally converted to perforations appearing on individual cards or a continuous tape. Accordingly, to avoid such shortcomings, present day traffic monitoring circuits include an encoder or translator device for providing statistical data in a notational form which is recordable on a storage medium for later processing by automatic data processing equipment. Therefore, the translator or encoder device in present day traffic monitoring circuits translates statistical data to a notational form directly processable by automatic data processing equipment while necessarily eliminating the need of employing human agents and the accompanying expense attached theerto.

The desirability of recording statistical data on a storage medium for later processing at a centralized location is predicated upon the large cost of automatic data processing equipment and the nonfeasibility of providing one such equipment at each accumulating station. Accordingly, the recording of accumulated statistical data on a storage medium provides that such data may be later processed at a convenient time by an automatic data processing equipment which is shared by a plurality of accumulating stations.

It is evident, however, that statistical data which is

directed from the traffic monitoring circuit as electrically indistinguishable pulse indications cannot be directly recorded on a storage medium but must be identified according to its source or origin, i.e., converted to an equivalent code notation peculiarly designating such source or origin, and recorded as such on the final storage medium. For example, in the D. H. Barnes patent application Serial No. 1,602, filed on even date herewith, now Patent No. 3,099,819, an encoder or translator device is interposed between a monitoring circuit and buffer storage cells connected to a final recording arrangement. The encoder operates to identify each pulse indication directed thereto from a traffic monitoring circuit according to the particular lead along which it appears, by providing an equivalent binary code notation particularly designating the unit of equipment which is peculiarly identified with the particular lead. Accordingly, it is this equivalent binary code notation which is recorded on the final storage medium to be processed as such by the automatic data processing equipment.

It is generally known that the operation of an information transfer circuit to which statistical data is transferred from a next previous information circuit must be temporarily delayed or inhibited until the transfer process has been completed. The delayed operation of a subsequent information circuit is necessary to avoid a mutilation of the statistical data. For example, in the above-identified D. H. Barnes patent, statistical data is directed from the encoder device as an equivalent reflected binary code notation designating a particular one of the units of equipment being monitored and stored in parallel in the first storage cell included in a buffer storage unit. The buffer storage unit therein disclosed comprises a plurality of tandemly arranged storage cells which are asynchronously operated by control logic circuitry whereby each binary code notation stored in the first storage cell thereof is automatically transferred through succeeding cells to a last vacant one of the storage cells. The logic circuitry associated with the buffer storage unit must therefore be inhibited during that time in which statistical data received as pulse indications is being translated by the encoder device to an equivalent binary code notation and is being stored in the first buffer storage cell.

Accordingly, an object of this invention is to provide delay apparatus to temporarily inhibit information transfer circuits until such time that statistical data has been completely transferred thereto whereby mutilation of such data during the transfer process is avoided.

Another object of this invention is to provide delay apparatus which is simple and economical in construction and yet operative to provide sufficient delay whereby statistical data may be directed between successive information handling circuits without mutilation.

A further object of this invention is to provide delay apparatus to be used in conjunction with encoder devices employing transformer cores.

These and other objects of this invention are achieved in one illustrative embodiment comprising an encoder device to be employed in conjunction with traffice monitoring apparatus for translating statistical data directed thereto as high current electrically indistinguishable pulse indications to equivalent binary code notations; in accordance with our invention the encoder is operative to provide an essential time delay in the operation of a next subsequent information transfer circuit to which such notations are directed to insure nonmutilation of such data during the transfer process. To effect such results, the encoder is responsive to the leading edge of each pulse indication directed thereto to perform the translation and transfer an equivalent binary code notation in parallel

to the subsequent information transfer or storage circuit which is normally maintained in a quiescent state; the encoder device is, thereupon, responsive to the trailing edge of each pulse indication to direct a triggering pulse to the control circuitry for initiating the reading of the information out of the subsequent storage circuit only after the transfer into the storage circuit has been completed. Accordingly, the encoder provides an essential time delay in the read out operation of the subsequent information storage circuit to insure that each equivalent binary code notation directed thereto is not mutilated during the transfer process.

According to one specific embodiment of this invention, the encoder device is essentially a translator which comprises a plurality of transformer cores each having an output winding thereon. A plurality of input leads, which are peculiarly identified with particular units of equipments for which statistical data is desired and along which pulse indications are directed from a traffic monitoring circuit, are selectively threaded on a sing'e-turn basis through certain of the transformer cores in accordance with an equivalent reflected binary code. Accordingly, upon the appearance of the leading edge of a pluse indication along a particular one of the input leads, a resultant magnetic flux is produced in only those transformer cores through which such lead is threaded whereby the information represented thereby is translated and directed in parallel as an equivalent binary code notation to the subsequent information transfer circuit. A transformer trigger core is also included in the encoder device through which each of the input leads is threaded. The output winding of the trigger core, however, is directed to a control circuit by which the subsequent information transfer circuit is controlled, such control circuit being responsive to the voltage induced thereacross by the magnetic flux change resulting from the trailing edge of the pulse indication. Accordingly, a delay is provided to the subsequent information transfer circuit which is sufficient to insure that an equivalent binary code notation has been transferred thereto by the encoder. Accordingly, the subsequent information transfer circuit can only be operated upon the completed operation of the encoder.

Accordingly, a feature of this invention relates to the provision of an encoder which is discriminating with respect to the leading edge of a pulse indication directed thereto to convert such indication to an equivalent binary code notation.

Another feature of this invention relates to an encoder and control apparatus which are discriminating with respect to the trailing edge of each pulse indication directed thereto to serve as a source of control or triggering pulses.

It is a further feature of this invention that the encoder comprises a plurality of transformer cores by means of which information is translated and applied to storage elements, such as magnetic cores having stable remanent magnetic states, in a subsequent storage stage in response to the leading edge of applied pulses and further comprises a trigger transformer core and associated control circuitry by means of which the information can be read out of the subsequent storage stage only in response to the trailing edge of the applied pulses.

Other objects, features, and advantages of this invention will become apparent from a consideration of the following detailed description in conjunction with the single figure which shows an illustrative embodiment of the invention employed in conjunction with traffic measuring apparatus.

Referring now particularly to the single figure, an encoder **10** is illustrated as comprising a plurality of transformer cores **T0** through **T11**; the encoder **10** is operative on a one-at-a-time basis to recognize and convert to equivalent binary code notations the pulse indications directed thereto on a time basis along the input leads **L0** through **L599** from the traffic monitoring apparatus **11**. The traffic monitoring apparatus **11**, illustrated in block representation, may advantageously comprise the traffic monitoring circuit which is fully disclosed in the copending patent application Lamneck-Wichman, Serial No. 1604, filed on even date herewith, now Patent No. 3,115,549, issued December 24, 1963. The traffic monitoring apparatus as disclosed in the above-identified Lamneck-Wichman patent is operative on a fixed basis to monitor a plurality of units of equipment and to selectively direct pulse indications denoting the appearances of predetermined conditions on a time basis along particular ones of a plurality of input leads peculiarly identified therewith. Accordingly, each pulse indication directed from the traffic monitoring apparatus of the above-identified Lamneck-Wichman patent is recognizable as relating to the particular unit of equipment which is peculiarly identified with that one of the input leads **L0** through **L599** along which it appears. As illustrated, the pulse indications provided along particular ones of the input leads **L0** through **L599** have a peak positive current excursion of approximately 3½ amperes and are of approximately 3.5-microsecond duration. As hereinafter employed, the leading edge of the pulse indication refers to the current build-up thereof along the portion *a–b* of the illustrated pulse; the trailing edge of the pulse indication refers to the current decrease thereof along the portion *b–c* of the illustrated pulse.

Each of the input leads **L0** through **L599** is selectively threaded on a single-turn basis through or in by-pass of each of the transformer cores **T0** through **T11**. With respect to each of the transformer cores **T0** through **T9**, each of the input leads **L0** through **L599** is threaded in accordance with an equivalent reflected binary or Gray code notation of a decimal number which is arbitrarily assigned to the unit of equipment which is peculiarly identified therewith; each transformer core corresponds to an information bit slot in the equivalent binary code notation, a threaded core representing a "1," a by-passed core representing a "0." To provide for parity checking, the leads **L0** through **L599** are selectively threaded through the transformer core **T10** so that each equivalent binary code notation directed from the encoder **10** contains an odd number of binary ones. The remaining transformer core **T11**, which is hereinafter to be referred to as the trigger core, is threaded by each of the leads **L0** through **L599**; the trigger core **T11** is, therefore, responsive to pulse indications directed along each of the input leads **L0** through **L599** through the encoder **10**. The transformer cores **T0** through **T10**, on the other hand, are responsive only to pulse indications directed along those of the input leads **L0** through **L599** which are selectively threaded therethrough. Each of the input leads **L0** through **L599** is threaded through the encoder **10** to ground.

The portion of the encoder **10** comprising the transformer cores **T0** through **T10** operates on the principle of a "ring" translator of the type disclosed in the T. L. Dimond Patent 2,614,176, issued on October 14, 1952, and, also, in the above-identified D. H. Barnes patent. Accordingly, input pulses are directed to the encoder **10** from the traffic monitoring apparatus **11** on a time basis to avoid the mutilation of the statistical data represented thereby during the translation process. In the present embodiment, the permissible long term rate at which pulse indications can be directed to the encoder **10** for translation to an equivalent binary code notation and storage as such in a storage cell **12**, hereinafter described, is limited to the rate of operation of the serial reader and recorder **13** in reading out the equivalent binary code notation stored in the storage cells and in serially recording the read-out information on a final storage medium. The rate at which pulses can be directed to encoder **10** is also limited by the number of storage cells **12** and **14** provided. As described in the above-identified D. H. Barnes patent, the buffer storage unit provides a backlog

or a temporary store of the equivalent binary code notations directed from the encoder **10** to increase the apparent rate of operation of the serial reader recorder **13**.

To facilitate an understanding of the operation of the encoder **10**, a dot convention is employed with respect to input leads L0 through L599 and with respect to the output windings provided to each of the transformer cores T0 through T10 and the trigger core T11. Assume that a pulse indication has been directed from the traffic monitoring apparatus along input lead L30. This pulse indication is, thereupon, directed along the lead L30 as selectively threaded through the transformer cores T0, T4, T10 and the trigger core T11; the threading or by-passing a transformer core being indicative of a binary one or a binary zero, respectively, in the corresponding information bit slot in the equivalent binary code notation. As illustrated, during the leading edge of the pulse indication, there is a build-up or increase in the magnitude of current flow along the lead L30 from the traffic monitoring apparatus 11 to ground. Accordingly, a build-up or increase of clockwise magnetic flux occurs in each transformer core T0 through T10 through which the input lead L30 is selectively threaded, i.e., the transformer cores T0, T4, T10; and the trigger core T11 during the leading edge of the pulse indication, i.e., the portion *a–b* of the illustrated pulse. In response thereto, current flow is induced in each of the output windings provided to the transformer cores T0, T4, T10 and the trigger core T11, in a manner well known in the art, as a result of a positive voltage appearing at the dotted terminals thereof.

The direction of induced current flow, therefore, in each of the output windings of the transformer cores T0, T4 and T10 is from the dotted terminal thereof and through the input windings of corresponding square-loop magnetic storage cores M0, M4 and M10, respectively, of the first storage cell **12** in the low impedance direction of the isolation diodes **16**. This induced current flowing through the input windings of the magnetic cores M0, M4 and M10 of the storage cell **12** is operative to produce a magnetic flux of sufficient magnitude to switch or set each of the magnetic cores, in a manner well known in the art, to store a binary one in the corresponding information bit slots of the equivalent binary code notation. The remaining magnetic cores, i.e., M1 through M3 and M5 through M9, remain in an unset condition to indicate a binary zero in the corresponding information bit slots of the equivalent binary code notation. It is evident that each pulse indication directed along one of the input leads L0 through L599 to the encoder **10** is encoded or converted to an equivalent binary code notation, and stored in parallel in the storage cell **12**.

During the trailing edge of the pulse indication directed along the input lead L30, i.e., the portion *b–c* of the illustrated pulse, there is a decay or decrease of current flow therealong and a decreasing magnetic flux change occurs in the transformer cores T0, T4, T10 and the trigger core T11. This decrease of current flow along the input lead L30 results in the appearance of a negative voltage at the dotted terminals of each of the output windings to the transformer cores T0, T4, T10 and the trigger core T11. The negative voltage and resultant reverse currents induced thereby in the output windings of the transformer cores T0, T4 and T10 are effectively inhibited by the isolation diodes **16** from disturbing the equivalent binary code notation which has been stored in the storage cell **12**. However, with respect to the trigger core T11, the encoder **10** in accordance with our invention makes effective use of the negative voltage developed thereby for controlling the essential delay in the transfer of the stored information from the storage cell **12** to the subsequent storage cells **14**.

The bistable device **23** may advantageously comprise a conventional Eccles-Jordan type bistable transistor circuit, commonly known as a flip-flop circuit, and a detailed description of the operation thereof is not deemed necessary. A complete description of the operation of a transistor bistable circuit herein employed may be had by reference to Section 10.6.1, pages 324–338 of "Transistor Circuit Engineering," editored by Richard F. Shea and published by John Wiley and Sons, Incorporated, November 1957. The bistable device **23**, as illustrated, comprises a pair of p-n-p transistor devices **30** and **31** which are adapted for bistable operation. The bistable device **23** is adapted to be set and reset by negative pulses applied along lead **33** to the set terminal S and along lead **34** to the reset terminal R, respectively, which are electrically integral with the base electrodes of the transistors **30** and **31**, respectively. The set terminal S is connected by the lead **33** to the dotted terminal of the output winding of the trigger core T11 included in the encoder **10** through the resistor **37** and the capacitor **39**.

Threaded through each of the remanent magnetic cores M of the storage cell **12** is a drive lead **18** to which read-out pulses are applied from a core driver circuit **19**. The core driver circuit may advantageously comprise a transistor blocking oscillator, as fully disclosed in the above-mentioned Barnes patent. The core driver circuit **19** provides the desired read-out pulse to the drive lead **18** to reset the magnetic cores M of the storage cell **12**, and thus transfer the information to the subsequent storage cells **14** in response to an input signal applied to it from an AND gate circuit **21**. The AND gate **21**, which is also disclosed more fully in the Barnes patent, receives a first enabling signal along a lead **22** from a flip-flop circuit **23** associated with the storage cell **12** and controlled by the encoder **10** in accordance with our invention, as more fully discussed below, and a second enabling signal along a lead **24** from the control circuits **25** associated with the next storage cell **14**. The second enabling signal, as more fully discussed in the Barnes patent, advises the AND gate **21** that the subsequent storage cell **14** is vacant and can therefore receive the information presently being stored in storage cell **12** by operation of the encoder circuit **10**.

The core driver **19** is activated by an input signal from the AND gate **21** only when the AND gate is fully enabled by the presence of both enabling signals, described above, and at the time of the receipt of the second of the two signals.

It may also be noted that the core driver **19** has an output lead **26** which immediately ofter the reading out of the information from the storage cell **12** sets a flip-flop in the subsequent control circuits **25** to indicate information storage in the next subsequent storage cell **14** and thus prevent an enabling signal from being present on the lead **24**.

The peculiar operation of the trigger core T11 of the encoder **10**, in accordance with our invention, may now be detailed. It is to be noted, particularly, that the output winding provided to the trigger core T11 is opposite in polarity with respect to those output windings provided to the remaining transformer cores T0 through T10 of the encoder **10**. When the core driver **19** has completed a read-out operation with respect to the magnetic cores M0 through M10 of the storage cell **12**, a pulse of negative polarity is directed to the reset terminal R of the bistable device **23** along the lead **34**. As mentioned above when the flip-flop **23** is reset, an enabling potential is not applied along the lead **22** and the AND gate **21** is inhibited. The bistable device **23** may be conveniently considered as a memory device to indicate the storage condition of the storage cell **12**. For example, during such time that the storage cell **12** is vacant or in a nonstorage condition, the bistable device **23** is reset. This is obvious as the storage cell **12** is placed in a nonstorage condition upon the completed operation of the core driver **19** which is also operative to direct a negative pulse along the lead **34** to the reset terminal R of the flip-flop **23**.

At this time each of the magnetic cores M0 through M10 is in a reset condition. Assume now that the above-identified pulse indication appears along the lead L30 as threaded through the encoder 10. During the leading edge of this pulse indication, a resultant positive voltage appears at the dotted terminal of the output windings of the transformer cores T0, T4, T10 and the trigger core T11, and the equivalent binary code notation is stored in parallel in the storage cell 12, as hereinabove described. The resultant positive voltage appearing at the dotted terminal of the output winding of the trigger core T11 during this time is applied at the set terminal S of the bistable device 23 to the base electrode of the transistor 30. However, as the bistable device 23 is in a reset condition whereby the transistor 31 is conducting and the transistor 30 is reverse biased, i.e., the base electrode voltage is positive with respect to the emitter electrode voltage, the only effect of the resultant positive voltage appearing at the dotted terminal of the output winding of the trigger core T11 during the leading edge of the pulse indication is to further reverse bias the transistor device 30. Accordingly, the operational state of the bistable circuit 23 is not transferred and the core driver 19 remains in an unoperated state.

However, upon the pulse indication having reached a maximum positive excursion at the point *b*, as illustrated the encoder 10, including the trigger core T11, is now operative upon a decrease of current flow along the input lead L30, and the accompanying decrease of flux in trigger core T11, during the trailing edge of the pulse indication, to direct a pulse of negative potential from the dotted terminal of the output winding thereof. This negative pulse is effective to transfer or set the operational state of the bistable device 23 to initiate the operation of the core driver 19. Accordingly, the operation of the core driver 19 is sufficiently delayed to insure the transfer and storage in parallel in the storage cell 12 of the equivalent binary code notation directed from the encoder 10. The reset terminal R of the bistable circuit 23 is connected to core driver 19 so that a pulse is applied from the core driver circuit to reset the flip-flop circuit after each read-out operation of the storage cell 12. Accordingly, when the storage cell 12 contains no information and is in condition to receive the next encoded input from the encoder 10, the flip-flop circuit 23 is reset with the transistor 31 normally conducting and the AND gate 21 is not enabled.

Such operation is had by determining the mode of winding of the transformer cores T0 through T10 and the trigger core T11, respectively, so that the equivalent binary code notation is encoded and stored in the storage cell 12 during the leading edge of each pulse indication directed to the encoder 10 and a voltage of proper polarity to set the bistable device 23 is developed across the output winding of the trigger core T11 during the trailing edge thereof. During the trailing edge of each pulse indication, reverse voltages are induced in each of the transformer cores T0 through T10 and the trigger core T11. As hereinabove stated, the reverse currents induced in the output windings provided to the transformer cores T0, T4 and T10 are effectively blocked by the isolation diodes 16, and the equivalent binary code notation stored in the storage cell 12 is not mutilated. However, with respect to the resultant voltage developed across the output winding of the trigger core T11, at this same time, effective use is made thereof to provide a trigger pulse subsequent in time to the completed storage of the equivalent binary code notation in the storage unit 12 to initiate the operation of the core driver 19. Accordingly, the resultant negative voltage appearing at the dotted terminal of the output winding of the trigger core T11 is reflected through the resistor 37 and capacitor 39 along lead 33 to the set terminal S of the bistable device 23 as a momentary negative voltage spike which is sufficient to transfer the operational state thereof.

Upon a transfer of the operational state of the flip-flop circuit 23, an enabling voltage is applied to the AND gate 21 from the output terminal "0" of the flip-flop 23 along the lead 22. Assuming that the subsequent storage cell 14 is vacant and an enabling signal is already present along lead 24, the AND gate 21 is thereupon enabled and transmits a signal to the core driver 19 causing it to apply a drive pulse to the drive lead 18 threading each of the cores M in the storage cell 12, whereby the information in the storage cell 12 is transferred to the next subsequent storage cell 14, as described above.

Upon the core driver 19 being enabled to apply the drive pulse to the drive lead 18, a negative reset pulse is also directed from the core driver 19 at the termination of its drive pulse, to the reset terminal R of the flip-flop circuit 23, which pulse is effective to forward bias the transistor 31. Accordingly the operational state of the flip-flop 23 is switched and an enabling voltage is no longer applied from the output "0" thereof to the AND gate 21. The core driver 19 thereupon remains in its quiescent or normal state until the bistable circuit 23 is again triggered or set by a triggering pulse from the trigger core T11 in the encoder 10, assuming that the subsequent storage cell 14 will also have been cleared of its stored information by that time. The circuit is thus in condition to encode and store the subsequent indication from the traffic monitoring apparatus 11, in the manner hereinbefore described.

It is to be understood that the above-described arrangements are merely illustrative of the application of the principles of our invention. Numerous other arrangements may be devised by those skilled in the art without departing from the spirit and scope of the invention.

What is claimed is:

1. In combination, an encoder comprising a plurality of transformer cores, input means including pulse source means and a plurality of wires threading said transformer cores in accordance with the desired code of said encoder, storage means comprising a plurality of storage devices, means including an output winding on each of said transformer cores for transferring information from said encoder to said storage devices in response to the leading edge of a pulse applied to said plurality of wires by said pulse source means, means for transferring information out of said storage means, and variable delay means responsive to said pulse for preventing operation of said transfer means until after transfer of said information from said encoder to said storage devices has been completed, said delay means including an additional transformer core in said encoder, means effectively threading each of said plurality of wires through said additional transformer core, and means including an output winding on said additional transformer core for enabling said transfer means only on the trailing edge of said pulse applied to said plurality of wires by said pulse source means.

2. In combination, an encoder comprising a plurality of transformer cores, input means including pulse source means and a plurality of wires threading said transformer cores in accordance with the desired code of said encoder, a storage cell comprising a plurality of magnetic cores having stable states of remanent magnetization, there being one said remanent magnetic core for each said transformer core, means including an output winding on each of said transformer cores for setting the state of magnetization of said remanent magnetic cores in response to the leading edge of a pulse applied to said plurality of wires by said pulse source means, means for reading said information from said storage cell comprising means for resetting the state of magnetization of said remanent magnetic cores, and variable delay means responsive to said pulse for preventing operation of said reading means until after completion of the setting of said remanent magnetic cores, said delay means including

an additional transformer core in said encoder, means effectively threading each of said plurality of wires through said additional transformer core, and means including an output winding on said additional transformer core and means connecting said output winding on said additional transformer core to said reading means for enabling said reading means only on the trailing edge of said pulse applied to said plurality of wires by said pulse source means.

3. The combination as set forth in claim 2 wherein said means for enabling said winding means only on the trailing edge of said pulse further comprises a bistable flip-flop circuit, means for normally maintaining said flip-flop circuit in a first state, and means for switching the state of said flip-flop circuit in response to said trailing edges of said pulse.

4. In combination, an encoder comprising a plurality of transformer cores, input means including pulse source means and a plurality of wires threading said transformer cores in accordance with the desired code of said encoder, storage means comprising a plurality of storage devices, means including an output winding on each of said transformer cores for transferring information from said encoder to said storage devices in response to the leading edge of a pulse applied to said plurality of wires by said pulse source means, said output windings and said wires threading said transformer cores being in a first phase relationship, means for transferring information out of said storage means, and variable delay means responsive to said pulse for preventing operation of said transfer means until after transfer of said information from said encoder to said storage devices has been completed, said delay means including an additional transformer core in said encoder, means effectively threading each of said plurality of wires through said additional transformer core, and means including an output winding on said additional transformer core for enabling said transfer means only on the trailing edge of said pulse applied to said plurality of wires by said pulse source means, said output winding on said additional transformer core being in the opposite phase relationship to said plurality of wires effectively threading said additional transformer core.

5. The combination as set forth in claim 4 wherein said storage devices comprise remanent magnetic cores having two states of remanent magnetization, there being one such remanent magnetic core for each said first mentioned transformer cores in said encoder.

6. The combination as set forth in claim 5 wherein said transfer means further includes means for switching the state of said remanent magnetic cores, bistable means connected to said switching means, means for normally maintaining said bistable means in a first state, and means for shifting said bistable means to its second state in response to said trailing edge of said pulse.

7. In a traffic measuring apparatus, an encoder, means for directing a pulse indication to said encoder, said encoder including means responsive to the leading edge of said pulse indication to encode an equivalent binary code notation, information transfer means for receiving said equivalent binary notation, means for controlling said information transfer means, and variable delay means including means responsive to the trailing edge of said pulse indication for operating said control means whereby said control means is only operated upon said equivalent binary notation having been received by said information transfer means.

8. A traffic measuring apparatus comprising an encoder having a plurality of input leads, means for directing statistical data in the form of pulse indications along particular ones of said plurality of input leads, storage means connected to said encoder, said encoder device including means responsive to the leading edge of each of said pulse indications for storing an equivalent binary notation in said storage means, information transfer means connected to said storage means, and variable delay means responsive to the trailing edge of each of said pulse indications for controlling said information transfer means.

9. A traffic measuring apparatus comprising an encoder device having a plurality of input leads, means for directing statistical data in the form of pulse indications along particular ones of said input leads, storage means, said encoder device including means operative upon the appearance of the leading edge of each of said pulse indications to store an equivalent binary notation thereof in said storage means, information transfer means connected to said storage means, bistable means operative in a first state for inhibiting said information transfer means, variable delay means including means operative upon the appearance of the trailing edge of each of said pulse indications to transfer the state of said bistable device whereby said information transfer means becomes operative, and means operative upon each completed operation of said information transfer means to reset said bistable means to said first state.

10. In a traffic measuring apparatus, an encoder having a plurality of input leads, means for directing statistical data in the form of pulse indications along particular ones of said plurality of input leads, said encoder including translation means operative during the leading edge of each pulse indication directed thereto to provide an equivalent binary notation thereof, variable delay means including means operative during the trailing edge of each pulse indication directed thereto for generating a trigger pulse, storage means for receiving said equivalent binary notation directed from said encoder, and means responsive to said trigger pulse for transferring said equivalent binary notation from said storage means.

11. In a traffic monitoring circuit, an encoder comprising a plurality of transformer cores, storage means having a plurality of storage elements corresponding one to each of said transformer cores, diode circuit means connecting corresponding ones of transformer cores and said storage elements, means for selectively threading a plurality of input leads through said plurality of transformer cores, variable delay means including an additional transformer trigger core in said encoder device threaded by each of said input leads, means for directing statistical data in the form of pulse indications along particular ones of said input leads whereby an equivalent coded notation thereof is stored in said storage means, information transfer means connected to said storage means and means connected to said information transfer means responsive to said trigger core for controlling the operation of said information transfer means when said diode circuit means are blocked.

12. In a traffic monitoring circuit a word organized memory comprising a plurality of transformer cores and a trigger core, input leads individually coupled to selective ones of said transformer cores in accordance with a binary code and to said trigger core, means for pulsing a particular one of said plurality of input leads, output windings on said transformer cores and said trigger core, storage means, means including said transformer core output windings for transferring a binary notation to said storage means in response to increasing current flow along said particular lead, information transfer means connected to said storage means, and variable delay means responsive to the voltage developed across said output windings on said trigger core during decreasing current flow along said particular lead for enabling said information transfer means.

13. In a traffic measuring apparatus, a word organized memory comprising a plurality of transformer cores and a trigger core, each of said transformer cores and said trigger core having an output winding, a plurality of control leads inductively coupled to selected ones of said transformer cores and to said trigger core, storage

means connected to said transformer core output windings, means for providing a pulse of current along a particular one of said plurality of control leads, a memory device connected to said output winding of said trigger core, means including said output windings provided to said plurality of transformer cores responsive to increasing current flow along said particular input lead to store a binary code notation in said storage means, variable delay means including said trigger core output winding for switching the memory state of said memory device in response to decreasing current flow along said particular input lead, and information transfer means controlled by said memory device for transferring said notation from said storage means and for switching the state of said memory device upon said transfer from said storage means.

14. In a traffic measuring apparatus, a word organized memory including an encoder portion and a storage portion, said encoder portion comprising a plurality of transformer cores and a trigger core each provided with an output winding, said storage portion comprising a plurality of magnetic cores having stable states of magnetic remanence and each provided with an input winding and a common readout winding, said output winding

provided to each of said transformer cores being connected to the input winding to the corresponding one of said plurality of magnetic cores, a plurality of input leads inductively coupled to selected ones of said plurality of transformer cores in accordance with a binary code and to said trigger core, means for directing a current pulse along a particular one of said input leads to provide a resultant voltage across the output windings of said transformer cores and said trigger core, means including said transformer core output windings for storing an equivalent binary notation in said storage portion, information transfer means connected to said storage portion, and variable delay means including means connected to said trigger core output winding and responsive to the voltage developed across said trigger core output winding upon a decrease of current flow along said particular input lead for controlling the operation of said information transfer means.

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