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(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

(71) Applicant *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-Shinjuku 6-chome, Shinjuku-ku, 160-8366 (JP).

(72) Inventors: **POTTY, Sreenath Narayanan**; Vishnusree, TRA5, Thamalam, Poojappura P.O, Trivandrum 695012 Kerala (IN). **MITTAL, Rajesh**; 2B-501, Akme Encore, Brookfield, Bangalore 560037 Kamataka (IN). **KAWOOSA, Mudasir Shafat**; Naidoori, Gillikadal, Nowshera, Srinagar, Srinagar, Jammu and Kashmir (IN). **SINGHAL, Vivek**; C-401, Springfields Apartments, Sarjapura Road, Bangalore 560102 Karnatakal (IN).

(74) Agents: **DAVIS, Michael A. Jr.** et al.; International Patent Manager, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

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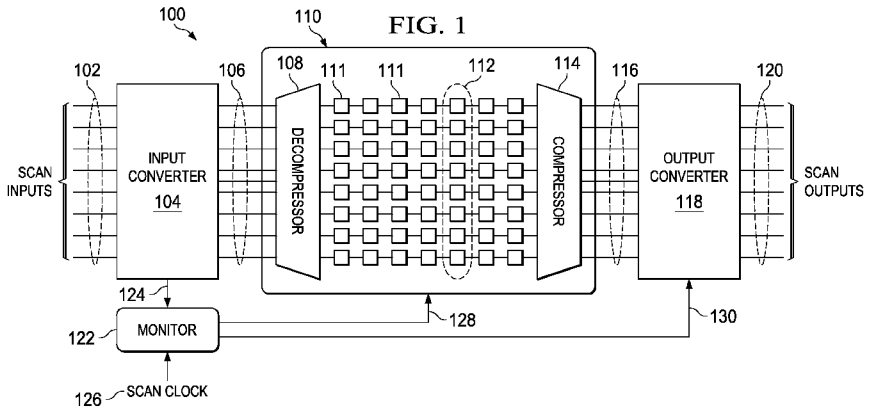
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(54) **Title**: METHOD AND APPARATUS FOR TEST TIME REDUCTION

FIG. 1



(57) **Abstract**: In described examples of a circuit (100) for testing an integrated circuit (IC), the circuit (100) includes an input converter (104) that receives N scan inputs (102) and generates M pseudo scan inputs (106), where M and N are integers. A scan compression architecture (110) is coupled to the input converter (104) and generates P pseudo scan outputs (116) in response to the M pseudo scan inputs (106). An output converter (118) is coupled to the scan compression architecture (110) and generates Q scan outputs (120) in response to the P pseudo scan outputs (116), where P and Q are integers. The input converter (104) receives the N scan inputs (102) at a first frequency and generates the M pseudo scan inputs (106) at a second frequency. The output converter (118) receives the P pseudo scan outputs (116) at the second frequency and generates the Q scan outputs (120) at the first frequency.

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METHOD AND APPARATUS FOR TEST TIME REDUCTION

[0001] This relates to scan testing of semiconductor devices, such as integrated circuits (ICs).

BACKGROUND

[0002] Scan based techniques offer an efficient alternative to achieve high fault coverage compared to the functional pattern based testing. As the design size increases and multi-core SoCs (system-on-chip) becomes essential to drive high speed applications, test data volume and test application time grow unwieldy, even in the highly efficient and balanced scan based designs. So far, scan compression technique is the best technique for test data volume, and for test time reduction during pattern execution of scan inserted designs. Scan compression architecture includes: a decompressor for decompression of a data on an input side; and a compressor for compression of the data on an output side. The decompressor takes scan inputs and expands them spatially into large number of scan chains internally. Each scan chain has multiple scan cells. If more scan inputs are provided to the decompressor, then the expansion will be improved, and the number of scan chains will be larger. Similarly, on the output side of the scan compression architecture, the scan chains are compressed to a small number of scan outputs, which leads to the phenomenon of aliasing. Practically, if more scan outputs are available, then aliasing will be lower, and the scan compression architecture will be more robust. However, in case of a very low cost tester (VLCT), a maximum of 8 scan inputs and 8 scan outputs are supported. According to one known scan technique to comprehend observation of scan chains on scan outputs, the maximum number of scan chains would be 1024 ($N*2^{(M-1)}$, where N is number of scan inputs, and M is number of scan outputs. Each scan chain has 128 scan cells, so the total number of scan cells is 131072 (128*1024). If the number of scan inputs and scan outputs is 9, then the number of scan chains would be 2304, and the number of scan cells in each scan chain would be approximately 57 (128x1024/256*9). Thus, when the number of scan inputs and scan outputs is increased from 8 to 9, the number of scan cells in each scan chain is reduced by approximately 50%, which reduces time for testing by a huge margin. However, VLCT does not support 9 scan inputs and 9 scan outputs.

[0003] In pin-limited devices, such as devices with 5 pins, the number of scan chains required would be 80 ($5*2^{(5-1)}$). Thus, the number of scan cells required in each scan chain would be approximately 1638 (128*1024/80). Accordingly, the test timing would increase substantially. Also, to make VLCT compatible with pin-limited devices, a serializer approach is used. In this approach, at least two shift registers are used per scan input. Therefore, to support the VLCT for the 5 pin device, a total of 10 shift registers are used at the input side. Further, as the data is shifted through two shift registers, a frequency of data shifting in scan cells is reduced by half, which increases the test timing. Also, because only 8 inputs are required, two of these scan inputs from the shift registers would be considered as "do not care" inputs. The shift registers are an additional overhead on the scan system. In an example situation where optimal test timing is achieved at 9 pins, the serializer approach does not allow to support 9 pins for a 5 pin device. Thus, when A pins provide optimal test timing and the device has B pins, the serializer approach does not support A/B, when A is not an integer multiple of B.

SUMMARY

[0004] In described examples, for testing an integrated circuit, a circuit includes an input converter that receives N scan inputs and generates M pseudo scan inputs, where M and N are integers. A scan compression architecture is coupled to the input converter and generates P pseudo scan outputs in response to the M pseudo scan inputs. An output converter is coupled to the scan compression architecture and generates Q scan outputs in response to the P pseudo scan outputs, where P and Q are integers. The input converter receives the N scan inputs at a first frequency and generates the M pseudo scan inputs at a second frequency. The output converter receives the P pseudo scan outputs at the second frequency and generates the Q scan outputs at the first frequency.

[0005] In an example method of testing an integrated circuit, N scan inputs are received at a first frequency, and M pseudo scan inputs are generated at a second frequency from N scan inputs. P pseudo scan outputs are generated at the second frequency from M pseudo scan inputs, and Q scan outputs are generated at the first frequency from M pseudo scan outputs. A ratio of the first frequency and the second frequency is equal to a ratio of M and N and to a ratio of P and Q, where N, M, P and Q are integers.

[0006] In another described example, a computing device includes a master device and a slave device coupled to the master device. The master device operates at N bits per clock cycle, and

the slave device operates at M bits per clock cycle. A converter coupled to the master device and the slave device. During a write operation, the converter receives N bits from the master device at every clock cycle and stores bits received from the master device. The converter provides M bits to the slave device when a number of bits stored in the converter is equal to or more than M.

BRIEF DESCRIPTION OF THE VIEWS OF DRAWINGS

[0007] FIG. 1 is a schematic of a circuit for testing an integrated circuit (IC).

[0008] FIG. 2 is a table of parameters of a circuit for testing an integrated circuit (IC), as a function of scan clock.

[0009] FIG. 3(a) and FIG. 3(b) illustrate fractional data packing in a circuit for testing an integrated circuit (IC).

[0010] FIG. 4 is a timing diagram of a circuit for testing an integrated circuit (IC).

[0011] FIG. 5 is a schematic of a circuit for testing an integrated circuit (IC).

[0012] FIG. 6(a) and FIG. 6(b) illustrate fractional data packing in a circuit for testing an integrated circuit (IC).

[0013] FIG. 7 is a timing diagram of a circuit for testing an integrated circuit (IC).

[0014] FIG. 8 illustrates a computing device.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0015] FIG. 1 is a schematic of a circuit 100 for testing an integrated circuit (IC). The circuit 100 includes an input converter 104. The input converter 104 receives N scan inputs 102 from a tester (not shown in FIG. 1), where N is an integer. Examples of some testers may include a very low cost tester (VLCT) or high-end testers. The input converter 104 generates M pseudo scan inputs 106, where M is an integer. In an embodiment, the input converter 104 is a FIFO (first-in first-out) buffer. A scan compression architecture 110 is coupled to the input converter 104. The scan compression architecture 110 receives M pseudo scan inputs 106 and generates P pseudo scan outputs 116 in response to the M pseudo scan inputs 106. The scan compression architecture 110 includes a decompressor 108, multiple scan chains 112 and a compressor 114. The decompressor 108 is coupled to the input converter 104 and receives M pseudo scan inputs 106. The decompressor 108 is coupled to the scan chains 112. Each of the scan chains 112 includes multiple scan cells, such as scan cell 111. The compressor 114 is coupled to scan chains 112. The compressor 114 generates P pseudo scan outputs 116, where P is an integer. An output converter 118 is coupled to the compressor 114. The output converter 118 receives the P pseudo scan

outputs 116 and generates Q scan outputs 120, where Q is an integer. In an embodiment, the output converter 118 is a FIFO (first-in first-out) buffer. The circuit 100 includes a monitor 122. The monitor 122 receives a status signal 124 from the input converter 104 and also receives a scan clock 126. The monitor 122 generates an internal clock 128 and an enable signal 130. The internal clock 128 is provided to the scan compression architecture 110. The output converter 118 receives the enable signal 130 from the monitor 122. The circuit 100 may include one or more additional components, which are not discussed here for simplicity of the description.

[0016] In operation of the circuit 100 of FIG. 1, the input converter 104 receives the N scan inputs 102 and generates the M pseudo scan inputs 106. The scan compression architecture 110 receives the M pseudo scan inputs 106 and generates the P pseudo scan outputs 116. The decompressor 108 receives the M pseudo scan inputs 106 and generates multiple core scan inputs in response to the M pseudo scan inputs 106. The core scan inputs are provided to the scan chains 112. Each of the scan chains 112 includes the scan cells, such as scan cell 111. Each scan cell 111 shifts a core scan input of the core scan inputs at a frequency of the internal clock 128. The scan chains 112 generate multiple core scan outputs in response to the core scan inputs received by the scan chains 112. The compressor 114 receives the core scan outputs and generates P pseudo scan outputs 116 in response to the core scan outputs. The output converter 118 receives the P pseudo scan outputs 116 and generates Q scan outputs 120. The input converter 104 receives the N scan inputs 102 at a first frequency and generates the M pseudo scan inputs 106 at a second frequency. The output converter 118 receives the P pseudo scan outputs 116 at the second frequency and generates the Q scan outputs 120 at the first frequency. The ratio of the first frequency and the second frequency is equal to a ratio of M and N and to a ratio of P and Q. The monitor 122 receives the scan clock 126 and generates the internal clock 128. The frequency of the internal clock 128 is equal to the second frequency. The scan chains 112 are driven by the internal clock 128.

[0017] The input converter 104 receives N scan inputs 102 at every scan clock 126. The input converter 104 is configured to store the N scan inputs 102 and generates M pseudo scan inputs 106 when a number of scan inputs 102 stored in the input converter 104, at the beginning of a scan clock, is equal to or more than M. In an embodiment, when N is equal to 8, and M is equal to 9, the input converter 104 receives 8 scan inputs 102 in a first scan clock. Because 8 is less than M, the input converter 104 does not generate M pseudo scan inputs 106 in the first scan

clock. These 8 scan inputs 102 are stored in the input converter 104. In the next scan clock (which is the second scan clock): (a) the input converter 104 receives another 8 scan inputs 102; and (b) the total number of scan inputs 102 stored in the input converter 104, at the beginning of the second scan clock, is more than M. Thus, the input converter 104 generates 9 pseudo scan inputs 106 in the second scan clock and the number of remaining scan inputs stored in the input converter 104 is 7 (16-9 = 7). This process is called fractional data packing and is further explained later in the description with the help of FIG. 2 and FIG. 3. The monitor 122 receives the status signal 124 from the input converter 104. The status signal 124 updates the monitor 122 about the number of scan inputs stored in the input converter 104 at a beginning of every scan clock. For example, in the embodiment explained above, the status signal 124 would update the monitor 122 that 8 scan inputs are stored in the input converter 104 at the beginning of the first scan clock, and 16 scan inputs are stored in the input converter 104 at the beginning of the second scan clock. The monitor 122 is configured to discontinue the internal clock 128 to the scan compression architecture 110 when the number of scan inputs stored in the input converter 104, at the beginning of a scan clock, is less than M. Thus, the shifting of core scan inputs in the scan cells is stopped when the number of scan inputs stored in the input converter 104 at the beginning of a scan clock is less than M.

[0018] The output converter 118 generates Q scan outputs at every scan clock 126 other than the first scan clock. In an embodiment, when N is equal to 8, and M is equal to 9, the input converter 104 receives 8 scan inputs 102 in a first scan clock. Because 8 is less than M, the input converter 104 does not generate M pseudo scan inputs 106 in the first scan clock. These 8 scan inputs 102 are stored in the input converter 104, and the output converter 118 does not receive any input in the first scan clock. In the next scan clock (which is the second scan clock), the input converter 104 receives another 8 scan inputs 102, and the total number of scan inputs stored in the input converter 104 is more than M. Thus, the input converter 104 generates 9 pseudo scan inputs 106 in the second scan clock. When P is equal to 9, and Q is equal to 8, the scan compression architecture 110 receives 9 pseudo scan inputs 106 and generates 9 pseudo scan outputs 116. The output converter 118 receives the 9 pseudo scan outputs 116 and generates 8 scan outputs 120. One (1) pseudo scan output is stored in the output converter 118. In the third scan clock, the output converter 118 receives the 9 pseudo scan outputs 116 and generates 8 scan outputs 120. A total of 2 pseudo scan outputs are then stored in the output converter 118.

Similarly, after 9 scan clocks, a total of 8 pseudo scan outputs are stored in the output converter 118. In the 10^{th} scan clock, the output converter 118 generates 8 scan outputs 120, and the number of pseudo scan outputs stored in the output converter 118 is zero. The output converter 118 receives the enable signal 130 from the monitor 122. The enable signal 130 is configured to disable the storage of pseudo scan outputs in the output converter 118 when a number of pseudo scan outputs stored in the output converter 118, at the beginning of a scan clock, is less than Q. In one embodiment, the enable signal 130 is configured to disable the storage of pseudo scan outputs in the output converter 118 when no pseudo scan outputs are received by the output converter 118. In one embodiment: (a) a storage depth of the input converter 104 is K bits, where K is an integer, and K is greater than or equal to 2N; and (b) a storage depth of the output converter 118 is L bits, where L is an integer, and L is greater than or equal to 2P.

[0019] The circuit 100 is adaptable to all devices irrespective of the number of pins. Thus, when A pins provide optimal test timing, and a device or an integrated circuit to be tested is of B pins, the circuit 100 does not require A to be an integer multiple of B. Also, the problem of "do not care" inputs does not arise in circuit 100. The test timing required in circuit 100 is substantially reduced, as compared to a conventional technique.

[0020] FIG. 2 is a table 200 that shows parameters of a circuit, for testing an integrated circuit (IC), as a function of scan clock. The table 200 is explained with the help of circuit 100 of FIG. 1, when N is 8, M is 9, P is 9, and Q is 8. Row 1 shows the scan clock 126 received by the circuit 100. For example, only 12 scan clocks are represented in table 200. Row 2 shows a number of scan inputs (similar to scan inputs 102) stored in the input converter 104 at the end of a scan clock. The input converter 104 is configured to store the N scan inputs 102 and generates M pseudo scan inputs 106 when a number of scan inputs stored in the input converter 104, at the beginning of a scan clock, is equal to or more than M. When N is equal to 8, and M is equal to 9, the input converter 104 receives 8 scan inputs 102 at scan clock 1. Because 8 is less than M, the input converter 104 does not generate M pseudo scan inputs 106 in the first scan clock (scan clock 1). These 8 scan inputs 102 are stored in the input converter 104. In the next scan clock (which is scan clock 2), the input converter 104 receives another 8 scan inputs 102, and the total number of scan inputs stored in the input converter 104 at the beginning of scan clock 2 is more than M. Thus, the input converter 104 generates 9 pseudo scan inputs 106 at scan clock 2, and the number of remaining scan inputs stored in the input converter 104 at the end of scan clock 2

is 7 (16-9 = 7) as shown in Row 2 (below scan clock 2). This process is called fractional data packing, because a fraction of scan inputs received at the scan clock 2 is sent as part of pseudo scan inputs. Similarly, at scan clock 3, a next set of 8 scan inputs 102 are received at the input converter 104. The total number of scan inputs stored in the input converter 104 at the beginning of scan clock 3 is (7+8=15), which is more than M. Thus, the input converter 104 generates 9 pseudo scan inputs 106 in the third scan clock, and the number of remaining scan inputs stored in the input converter 104 at the end of third scan clock is 6 (15-9 = 6) as shown in Row 2 (below scan clock 3). Similarly, at scan clock 9, a set of 8 scan inputs 102 are received at the input converter 104. The total number of scan inputs stored in the input converter 104 is (1+8=9), which is equal to M. Thus, the input converter 104 generates 9 pseudo scan inputs 106 in the ninth scan clock (scan clock 9), and the number of remaining scan inputs stored in the input converter 104 at the end of ninth scan clock is 0 (9-9 = 0) as shown in Row 2 (below scan clock 9). At scan clock 10, the input converter 104 receives another set of 8 scan inputs 102, which become stored in the input converter 104.

[0021] At scan clock 2, the internal clock 128 to the scan compression architecture 110 is enabled as 9 pseudo scan inputs 106 are received from the input converter 104, as shown in Row 3 (below scan clock 2). The monitor 122 continues to provide internal clock 128 to the scan compression architecture 110, so long as the number of scan inputs stored in the input converter 104 at the beginning of a scan clock is equal to or more than M. The monitor 122 discontinues the internal clock 128 to the scan compression architecture 110 when the number of scan inputs stored in the input converter 104 is less than M, as shown in the table 200 at scan clock 10 in Row 3. At scan clock 10, the input converter 104 receives another set of 8 scan inputs 102, which become stored in the input converter 104. Because 8 is less than M (M=9), the input converter 104 does not generate M pseudo scan inputs 106 in the tenth scan clock (scan clock 10). Accordingly, the monitor 122 discontinues the internal clock 128 to the scan compression architecture 110 at scan clock 10 (illustrated as 0 in Row 3 below scan clock 10).

[0022] As the internal clock 128 is provided to the scan compression architecture 110 at scan clock 2, the scan compression architecture 110 generates 9 pseudo scan outputs 116 in response to the 9 pseudo scan inputs 106 received from the input converter 104. The output converter 118 generates Q scan outputs 120 when the number of pseudo scan outputs stored in the output converter 118 at the beginning of a scan clock is more than or equal to Q. At the beginning of

scan clock 2, the 9 pseudo scan outputs 116 are received and stored in the output converter 118. As Q is 8, and the number of pseudo scan outputs stored in the output converter 118 is 9, the output converter 118 generates 8 scan outputs 120, and the number of remaining pseudo scan outputs stored in the output converter 118 at the end of scan clock 2 is 1 (9-8 = 1) as shown in Row 4 (below scan clock 2). At scan clock 3, next set of 9 pseudo scan outputs 116 are received at the output converter 118. The total number of pseudo scan outputs stored in the output converter 118 is (1+9=10), which is more than Q. Thus, the output converter 118 generates 8 scan outputs 120 in the third scan clock, and the number of remaining pseudo scan outputs stored in the output converter 118 at the end of third scan clock is 2 (10-8 = 2) as shown in Row 4 (below scan clock 3). Similarly, at scan clock 9, a set of 9 pseudo scan outputs 116 are received at the output converter 118. The total number of pseudo scan outputs stored in the output converter 118 is (7+9=16), which is more than Q. Thus, the output converter 118 generates 8 scan outputs 120 in the ninth scan clock (scan clock 9), and the number of remaining pseudo scan outputs stored in the output converter 118 at the end of ninth scan clock is 8 (16-8 = 8) as shown in Row 4 (below scan clock 9). At scan clock 10, the input converter 104 does not generate pseudo scan inputs 106, and the internal clock 128 to the scan compression architecture 110 is also disabled. However, the output converter 118 has 8 pseudo scan outputs stored, which is equal to Q, and therefore generates 8 scan outputs 120 at the scan clock 10, and the number of remaining pseudo scan outputs stored in the output converter 118 at the end of scan clock 10 is 0 (8-8=0) as shown in Row 4 (below scan clock 10). Row 5 shows the enable signal 130, which is received by the output converter 118 from the monitor 122. The enable signal 130 is configured to disable the storage of pseudo scan outputs in the output converter 118 when the number of pseudo scan outputs 116 stored in the output converter 118 at the beginning of a scan clock is less than Q. The enable signal 130 is similar to the internal clock 128. When the monitor 122 discontinues the internal clock 128, the enable signal 130 to the output converter 118 is also disabled.

[0023] FIG. 3(a) and FIG. 3(b) illustrate fractional data packing in a circuit for testing an integrated circuit (IC). For example, the fractional data packing is illustrated with the help of circuit 100 in FIG. 1, when N is equal to 8, and M is equal to 9. FIG. 3(a) is a table that shows the scan inputs received at the input converter 104 for scan clocks 308 (scan clock 1 to scan clock 11). The 8 scan inputs are shown in column 302 as S0 to S7. A column 304 shows the

values of scan inputs received at scan clock 1. Similarly, column 306 represents the values of scan inputs received at scan clock 2. FIG. 3(b) is a table that shows the pseudo scan inputs generated by the input converter 104 in response to the received scan inputs of FIG. 3(a) for scan clocks 308 (scan clock 1 to scan clock 11). A column 312 represents the 9 pseudo scan inputs as PS0 to PS8. As shown in column 314, no pseudo scan inputs are generated at scan clock 1. Because the input converter 104 receives 8 scan inputs at scan clock 1, and 8 is less than M (=9), the input converter 104 does not generate pseudo scan inputs in the scan clock 1. At scan clock 2, the input converter 104 generates 9 pseudo scan inputs shown in column 316. The 9 pseudo scan inputs generated at scan clock 2 include: (a) the 8 scan inputs received at the input converter 104 at scan clock 1; and (b) 1 scan input received at the input converter 104 at scan clock 2. Similarly, the 9 pseudo scan inputs generated at scan clock 3 (shown in column 318) include: (a) 7 scan inputs received at the input converter 104 at scan clock 2; and (b) 2 scan inputs received at scan clock 3. This process is called fractional data packing, because a fraction of scan inputs received at the scan clock 2 is sent as part of pseudo scan inputs at the scan clock 2 . For simplicity of description, the values of scan inputs and pseudo scan inputs are same in FIG. 3(a) and FIG. 3(b) respectively. However, in an embodiment, the input converter 104 processes the scan inputs and generates different values of pseudo scan inputs. The 9 pseudo scan inputs generated at scan clock 8 (shown in column 320) include: (a) 2 scan inputs received at the input converter 104 at scan clock 7; and (b) 7 scan inputs received at scan clock 8. Also, the 9 pseudo scan inputs generated at scan clock 9 (shown in column 322) include: (a) 1 scan input received at the input converter 104 at scan clock 8; and (b) 8 scan inputs received at scan clock 9. At scan clock 10, the input converter 104 receives another set of 8 scan inputs, which become stored in the input converter 104 (column 309). However, 8 scan inputs at scan clock 10 is less than M (=9), so the input converter 104 does not generate pseudo scan inputs in the scan clock 10 (shown in column 324). The values of scan inputs and pseudo scan inputs of FIG. 3(a) and FIG. 3(b) are for example purposes.

[0024] FIG. 4 is a timing diagram of a circuit for testing an integrated circuit (IC). For example, the timing diagram is illustrated with the help of the circuit 100 in FIG. 1, when N is equal to 8, M is equal to 9, P is equal to 9, and Q is equal to 8. The timing diagram shows scan inputs 102 received at every scan clock 126. Each block represented in FIG. 4, such as block 102a and 102b, represents multiple scan inputs. Each block, such as block 102a and 102b, is a set

of bits that represents multiple scan inputs. When N is equal to 8, each block represents 8 scan inputs. Thus, 8 scan inputs are received at every scan clock 126. At the first scan clock, no pseudo scan inputs 106 are generated because the number of scan inputs stored in the input converter 104 is less than 9. At the second scan clock, the number of scan inputs stored in the input converter 104 is more than 9, so that 9 pseudo scan inputs 106 are generated at second scan clock. The internal clock 128 is enabled when 9 pseudo scan inputs 106 are received from the input converter 104. The monitor 122 continues to provide internal clock 128 to the scan compression architecture 110, so long as the number of scan inputs stored in the input converter 104 at the beginning of a scan clock is more than M. The monitor 122 discontinues the internal clock 128 to the scan compression architecture 110 when the number of scan inputs stored in the input converter 104 is less than M, as shown in FIG. 4 at scan clock 10 represented as XXX. At scan clock 10, the input converter 104 receives another set of 8 scan inputs, which become stored in the input converter 104. Because 8 is less than M (M=9), the input converter 104 does not generate M pseudo scan inputs 106 in the tenth scan clock (scan clock 10). Accordingly, the monitor 122 discontinues the internal clock 128 to the scan compression architecture 110 at scan clock 10. The values of scan inputs 102 and pseudo scan inputs 106 represented in FIG. 4 are according to an example embodiment.

[0025] As the internal clock 128 is provided to the scan compression architecture 110 at scan clock 2, the scan compression architecture 110 generates 9 pseudo scan outputs 116 in response to the 9 pseudo scan inputs 106 received from the input converter 104. The output converter 118 generates Q scan outputs 120 when the number of pseudo scan outputs stored in the output converter 118 at the beginning of a scan clock is more than or equal to Q. At the beginning of scan clock 2, the 9 pseudo scan outputs 116 are received and stored in the output converter 118. As Q is 8, and the number of pseudo scan outputs stored in the output converter 118 is 9, the output converter 118 generates 8 scan outputs 120. As described above, no pseudo scan inputs 106 are generated at scan clock 10, so no pseudo scan outputs 116 are generated at scan clock 10 represented as XXX. However, the output converter 118 continues to generate scan outputs 120 at all scan clocks. The output converter 118 has 8 pseudo scan outputs stored at the scan clock 10, which is equal to Q, and therefore generates 8 scan outputs 120. The values of scan inputs 102, pseudo scan inputs 106, pseudo scan outputs 116 and scan outputs 120 represented in FIG. 4 are according to an example embodiment. In at least one embodiment, the scan outputs 120 will

be different from the scan inputs 102.

[0026] FIG. 5 is a schematic of a circuit 500 for testing an integrated circuit (IC). The circuit 500 includes an input converter 504. The input converter 504 receives N scan inputs 502 from a tester (not shown in FIG. 5), where N is an integer. In one of the embodiments, the input converter 504 receives multiple scan inputs from the tester. For the purpose of illustration, N is 8, and the scan inputs 502 are shown as S0 to S7. Examples of some testers may include a very low cost tester (VLCT) or high-end testers. The input converter 504 generates M pseudo scan inputs 506, where M is an integer. For the purpose of illustration, M is 9, and the pseudo scan inputs 506 are shown as PS0 to PS8. The input converter 504 further includes a logic unit 505, which is configured to process a set of scan inputs of the N scan inputs 502 and generate a set of pseudo scan inputs 506 of the M pseudo scan inputs 506. In one embodiment, the logic unit 505 is configured to process scan inputs S0 to S7 and generates pseudo scan inputs PS0 to PS7. The input converter 504 includes multiple multiplexers and multiple flip-flops coupled together and configured to generate pseudo scan input PS8. In one embodiment, the input converter 504 includes 7 multiplexers (M1-M7), and each multiplexer of the 7 multiplexer receives a scan input of the scan inputs S1-S7 as a first input. The input converter 504 includes eight flip-flops arranged serially, and each flip-flop is coupled to a second input of a multiplexer. Each multiplexer receives an enable signal 530 from a monitor 522. A first flip-flop of the eight flip-flops receives scan input S0, and a last flip-flop of the eight flip-flops generates pseudo scan input PS8. In another embodiment, a combination of sequential devices is used for generating one or more pseudo scan inputs.

[0027] A scan compression architecture 510 is coupled to the input converter 504. The scan compression architecture 510 receives M pseudo scan inputs 506 and generates P pseudo scan outputs 516 in response to the M pseudo scan inputs 506. In an embodiment, the scan compression architecture 510 receives 9 pseudo scan inputs 506 and generates 9 pseudo scan outputs 516 in response to the 9 pseudo scan inputs 506. The scan compression architecture 510 includes a decompressor 508, multiple scan chains 512 and a compressor 514. The decompressor 508 is coupled to the input converter 504 and receives M pseudo scan inputs 506. The decompressor 508 is coupled to the scan chains 512. Each of the scan chains 512 includes multiple scan cells, such as scan cells 511. The compressor 514 is coupled to the scan chains 512. The compressor 514 generates P pseudo scan outputs 516, where P is an integer. An output

converter 518 is coupled to the compressor 514. The output converter 518 receives the P pseudo scan outputs 516 and generates Q scan outputs 520, where Q is an integer. In the illustrated embodiment, P is 9, and Q is 8. Thus, the output converter 518 receives the 9 pseudo scan outputs 516 and generates 8 scan outputs 520. In one embodiment, the output converter 518 includes multiple multiplexers and multiple flip-flops coupled together and configured to generate Q scan outputs. In one embodiment, the output converter 518 includes 8 multiplexers, and each multiplexer of the 8 multiplexers receives a pseudo scan output of the 9 pseudo scan outputs as a first input. The output converter 518 includes eight flip-flops arranged serially, and an output of each flip-flop is coupled to a second input of a multiplexer. Each multiplexer receives the enable signal 530 from the monitor 522. A first flip-flop of the eight flip-flops receives one pseudo scan output. In another embodiment, a combination of sequential devices is used in the output converter 518 to generate one or more scan outputs. In one embodiment: (a) a storage depth of the input converter 504 is K bits, where K is an integer, and K is greater than or equal to 2N; and (b) a storage depth of the output converter 518 is L bits, where L is an integer, and L is greater than or equal to 2P.

[0028] The circuit 500 includes the monitor 522. The monitor 522 receives a status signal 524 from the input converter 504 and also receives a scan clock 526. The monitor 522 generates an internal clock 528 and an enable signal 530. The internal clock 528 is provided to the scan compression architecture 510. The output converter 518 receives the enable signal 530 from the monitor 522. The circuit 500 may include one or more additional components, which are not discussed here for simplicity of the description.

[0029] For ease of understanding, the operation of FIG. 5 is explained when N is equal to 8, M is equal to 9, P is equal to 9, and Q is equal to 8. The input converter 504 receives the 8 scan inputs 502 and generates the 9 pseudo scan inputs 506. The scan compression architecture 510 receives the 9 pseudo scan inputs 506 and generates the 9 pseudo scan outputs 516. The decompressor 508 receives the 9 pseudo scan inputs 506 and generates multiple core scan inputs in response to the 9 pseudo scan inputs 506. The core scan inputs are provided to the scan chains 512. Each scan cell 511 shifts a core scan input of the core scan inputs at a frequency of the internal clock 528. The scan chains 512 generate multiple core scan outputs in response to the core scan inputs received by the scan chains 512. The compressor 514 receives the core scan outputs and generates 9 pseudo scan outputs 516 in response to the core scan outputs. The output

converter 518 receives the 9 pseudo scan outputs 516 and generates 8 scan outputs 520. The input converter 504 receives the 8 scan inputs 502 at a first frequency and generates the 9 pseudo scan inputs 506 at a second frequency, and the output converter 518 receives the 9 pseudo scan outputs 516 at the second frequency and generates the 8 scan outputs 520 at the first frequency. The ratio of the first frequency and the second frequency is equal to a ratio of M and N and to a ratio of P and Q. The monitor 522 receives the scan clock 526 and generates the internal clock 528. A frequency of the internal clock 528 is equal to the second frequency. The scan chains 512 are driven by the internal clock 528 at the second frequency.

[0030] The input converter 504 receives N scan inputs at every scan clock 526. The input converter 504 is configured to store the 8 scan inputs 502 and generates 9 pseudo scan inputs 506 when a number of scan inputs stored in the input converter 504, at the beginning of a scan clock, is equal to or more than 9. The input converter 504 receives 8 scan inputs 502 in a first scan clock. Because 8 is less than M, the input converter 504 does not generate M pseudo scan inputs 506 in the first scan clock. The first flip-flop of the eight flip-flops receives scan input S0, and the rest of the scan inputs are provided to the first input of each multiplexer of the seven multiplexers. For example, multiplexer M1 receives scan input S1, and multiplexer M7 receives scan input S7. In the next scan clock (which is the second scan clock), the input converter 504 receives another 8 scan inputs 502. These scan inputs are provided as S0-S7 to the input converter 504. The logic unit 505 processes these scan inputs S0-S7 and generates eight pseudo scan inputs PS0-PS7. In one embodiment, the logic unit 505 is a buffer, so the values of pseudo scan inputs are same as scan inputs. The monitor 522 provides an enable signal to the multiplexers, and a scan input (S7) received in the first scan clock is shifted through the flip-flops to generate the pseudo scan input PS8. Thus, the input converter 504 generates 9 pseudo scan inputs in the second scan clock. Similarly, at a third scan clock, the input converter 504 receives another 8 scan inputs. These scan inputs are provided as S0-S7 to the input converter 504. The logic unit 505 processes these scan inputs (S0-S7) and generates eight pseudo scan inputs PS0-PS7. The monitor 522 provides an enable signal to the multiplexers, and a scan input (S6) received in the first scan clock is shifted through the flip-flops to generate the pseudo scan input PS8. Thus, the input converter 504 generates 9 pseudo scan inputs 506 in the third scan clock. This process is called fractional data packing and is further explained later in the description with the help of FIG. 6(a) and FIG. 6(b). The monitor 522 receives the status signal

524 from the input converter 504. The status signal 524 updates the monitor 522 about the number of scan inputs stored in the input converter 504 at the inputs of the multiplexers at the beginning of every scan clock. For example, in the embodiment explained above, the status signal 524 would update the monitor 522 that 8 scan inputs are stored in the input converter 504 at the beginning of first scan clock, and 16 scan inputs are stored in the input converter 504 at the beginning of the second scan clock. The monitor 522 is configured to discontinue the internal clock 528 to the scan compression architecture 510 when the number of scan inputs stored in the input converter 504, at the beginning of a scan clock, is less than M. Thus, the shifting of core scan inputs in the scan cells is stopped when the number of scan inputs stored in the input converter 504, at the beginning of a scan clock, is less than M. At the ninth scan clock, the eight scan inputs and a scan input (S0) stored in the first scan clock together form the 9 pseudo scan inputs that are provided to the scan compression architecture 510. At the tenth scan clock, a new set of 8 scan inputs 502 is received at the input converter 504. Because 8 is less than M, the input converter 504 does not generate M pseudo scan inputs 506 in the tenth scan clock. The first flip-flop of the eight flip-flops receives scan input S0, and the rest of the scan inputs are provided to the first input of each multiplexer of the seven multiplexers. For example, multiplexer M1 receives scan input S1, and multiplexer M7 receives scan input S7.

[0031] The output converter 518 generates 8 scan outputs 520 at every scan clock 526 other than the first scan clock. The input converter 504 receives 8 scan inputs 502 in the first scan clock. Because 8 is less than M, the input converter 504 does not generate M pseudo scan inputs 506 in the first scan clock. These 8 scan inputs are stored in the input converter 504, and the output converter 518 does not receive any input in the first scan clock. In the next scan clock (which is the second scan clock), the input converter 504 receives another 8 scan inputs 502. The input converter 504 generates 9 pseudo scan inputs 506 in the second scan clock. The scan compression architecture 510 receives 9 pseudo scan inputs 506 and generates 9 pseudo scan outputs 516. The output converter 518 receives the 9 pseudo scan outputs 516. One pseudo scan output of the 9 pseudo scan output is provided to a flip-flop of the eight flip-flops arranged serially. This pseudo scan output is stored in first flip-flop in the eight flip-flops arranged in a serial manner. The other eight pseudo scan outputs of the 9 pseudo scan outputs 516 are provided to the eight multiplexers. The monitor 522 provides the enable signal 530 to the eight multiplexers, and the multiplexers generate the eight scan outputs 520. In the third clock cycle,

when the 9 pseudo scan outputs 516 are received at the output converter 518, one pseudo scan output of the 9 pseudo scan output is provided to a flip-flop of the eight flip-flops arranged serially. The previously stored pseudo scan output is moved to the next flip-flop (which is the second flip-flop) on receiving the scan clock. The other eight pseudo scan outputs of the 9 pseudo scan outputs are provided to the eight multiplexers. The monitor 522 provides the enable signal 530 to the eight multiplexers, and the multiplexers generate the eight scan outputs 520. Thus, with each scan clock, a new pseudo scan output is stored in the flip-flop chain, and the previously stored pseudo scan outputs in the flip-flops are shifted. Therefore, after 9 scan clocks, the eight flip-flops would get occupied by the pseudo scan outputs. Because, at the tenth scan clock, the pseudo scan inputs 506 are not generated at the input converter 504, the data in the eight flip-flops is made available to the eight multiplexers, and the multiplexers generate the eight scan outputs 520.

[0032] FIG. 6(a) and FIG. 6(b) illustrate fractional data packing in a circuit for testing an integrated circuit (IC). For example, the fractional data packing is illustrated with the help of circuit 500 in FIG. 5, when N is equal to 8, and M is equal to 9. FIG. 6(a) is a table that shows the scan inputs received at the input converter 504 for scan clocks 608 (scan clock 1 to scan clock 18). The 8 scan inputs are shown in column 602 as S0 to S7. A column 604 shows the values of scan inputs received at scan clock 1. Similarly, column 606 represents the values of scan inputs received at scan clock 2. FIG. 6(b) is a table that shows the pseudo scan inputs generated by the input converter 504 in response to the received scan inputs of FIG. 6(a) for scan clocks 608 (scan clock 1 to scan clock 18). A column 612 represents the 9 pseudo scan inputs as PS0 to PS8. As shown in column 614, no pseudo scan inputs are generated at scan clock 1. Because the input converter 504 receives 8 scan inputs at scan clock 1, and 8 is less than M (=9), the input converter 504 does not generate pseudo scan inputs in the scan clock 1. These scan inputs are stored in the flip-flop and multiplexer arrangement discussed in FIG. 5, and each of these scan input is shifted out as a pseudo scan input with each scan clock. At scan clock 2, the input converter 504 generates 9 pseudo scan inputs shown in column 616. The 9 pseudo scan inputs generated at scan clock 2 include: (a) the 8 scan inputs received at the input converter 504 at scan clock 2; and (b) 1 scan input received at the input converter 504 at scan clock 1. Similarly, the 9 pseudo scan inputs generated at scan clock 3 (shown in column 618) include: (a) 8 scan inputs received at the input converter 504 at scan clock 2; and (b) 1 scan input

received at scan clock 1. The pseudo scan input PS8 over a span of 9 scan clocks represents the scan inputs received at the input converter 504 at scan clock 1 (illustrated as 615). This process is called fractional data packing, because a fraction of scan inputs received at the scan clock 1 is sent as part of pseudo scan inputs. For simplicity of description, the values of scan inputs and pseudo scan inputs are same in FIG. 6(a) and FIG. 6(b) respectively. However, in an embodiment, the input converter 504 processes the scan inputs and generates different values of pseudo scan inputs. The 9 pseudo scan inputs generated at scan clock 8 (shown in column 620) include: (a) 8 scan inputs received at the input converter 504 at scan clock 7; and (b) 1 scan input received at scan clock 1. Also, the 9 pseudo scan inputs generated at scan clock 9 (shown in column 622) include: (a) 8 scan inputs received at the input converter 504 at scan clock 8; and (b) 1 scan input received at scan clock 1. At scan clock 10, the input converter 504 receives another set of 8 scan inputs, which become stored in the input converter 504 (column 609) in the flip-flops and multiplexer arrangement discussed in FIG. 5. However, 8 scan inputs at scan clock 10 is less than M (=9), so the input converter 504 does not generate pseudo scan inputs in the scan clock 10 (shown in column 624).

[0033] FIG. 7 is a timing diagram of a circuit for testing an integrated circuit (IC). For example, the timing diagram is illustrated with the help of the circuit 500 in FIG. 5, when N is equal to 8, M is equal to 9, P is equal to 9, and Q is equal to 8. The timing diagram shows scan inputs 502 received at every scan clock 526. Each block represented in FIG. 4, such as block 502a and 502b, represents multiple scan inputs. Each block, such as block 502a and 502b, is a set of bits that represents multiple scan inputs. When N is equal to 8, each block represents 8 scan inputs. Thus, 8 scan inputs are received at every scan clock 526. At the first scan clock, no pseudo scan inputs 506 are generated, because the number of scan inputs stored in the input converter 504 is less than 9. These 8 scan inputs received at first scan clock become stored in the input converter 504 in the flip-flops and multiplexer arrangement discussed in FIG. 5. At the second scan clock, the input converter 504 receives next set of 8 scan inputs, and the number of scan inputs stored in the input converter 504 is 16 at the beginning of scan clock 2. Thus, 9 pseudo scan inputs are generated by the input converter 504. The internal clock 528 is enabled when 9 pseudo scan inputs are received from the input converter 504. The monitor 522 continues to provide internal clock 528 to the scan compression architecture 510, so long as the number of scan inputs stored in the input converter 504 at a beginning of a scan clock is equal to or more

than M. The monitor 522 discontinues the internal clock 528 to the scan compression architecture 510 when the number of scan inputs stored in the input converter 504 is less than M, as shown in FIG. 7 at scan clock 10 represented as XXX. At scan clock 10, the input converter 504 receives another set of 8 scan inputs, which become stored in the input converter 504. Because 8 is less than M (M=9), the input converter 504 does not generate M pseudo scan inputs in the tenth scan clock (scan clock 10). Accordingly, the monitor 522 discontinues the internal clock 528 to the scan compression architecture 510 at scan clock 10. The values of scan inputs and pseudo scan inputs represented in FIG. 4 are according to an example embodiment.

[0034] As the internal clock 528 is provided to the scan compression architecture 510 at scan clock 2, the scan compression architecture 510 generates 9 pseudo scan outputs 516 in response to the 9 pseudo scan inputs received from the input converter 504. The output converter 518 generates Q scan outputs when the number of pseudo scan outputs stored in the output converter 518 at the beginning of a scan clock is more than or equal to Q. At the beginning of scan clock 2, the 9 pseudo scan outputs 516 are received and stored in the output converter 518. As Q is 8, and the number of pseudo scan outputs stored in the output converter 518 is 9, the output converter 518 generates 8 scan outputs 520 and stores 1 pseudo scan output. As shown in the figure, the scan output 520 generated at the second scan clock is same as the scan input 502 received at the second scan clock. Similarly, at the beginning of scan clock 3, the 9 pseudo scan outputs 516 are received and stored in the output converter 518. The output converter 518 generates 8 scan outputs 520 and stores 1 pseudo scan output. As shown in the figure, the scan output 520 generated at the third scan clock is same as the scan input 502 received at the third scan clock. Thus, at the end of third scan clock, the output converter stores 2 pseudo scan outputs. As discussed in FIG. 5, the pseudo scan outputs are stored in flip-flops arranged in a serial manner. With each scan clock, a new pseudo scan output is stored in the flip-flop chain, and the previously stored pseudo scan outputs in the flip-flops are shifted in the flip-flop chain. As described above, no pseudo scan inputs are generated at scan clock 10, so no pseudo scan outputs 516 are generated at scan clock 10 represented as XXX. However, the output converter 518 continues to generate scan outputs 520 at scan clock 10. The pseudo scan outputs stored in the flip-flop chain are made available to the multiplexers, and the multiplexers generate the eight scan outputs at the scan clock 10. As shown in the figure, the scan output 520 generated at the tenth scan clock is same as the scan input 502 received at the first scan clock. For ease of

understanding, the values of scan inputs and scan outputs are shown same in FIG. 7. However, in an embodiment, the circuit 500 processes the scan inputs and generates different values of scan outputs.

[0035] FIG. 8 illustrates a computing device 800 according to an embodiment. The computing device 800 is, or is an integrated circuit incorporated into, a server farm, a computing device with hard-drive, a video recorder, a bluetooth device, a remote control, a keyboard, a global navigation satellite system, a mobile communication device (such as a mobile phone), a personal digital assistant, a personal computer, or any other type of electronic system.

[0036] In some embodiments, the computing device 800 can be one of, but is not limited to, a microcontroller, a microprocessor or a system-on-chip (SoC). The computing device 800 includes master devices, such as master device 802a, 802b and 802c. For example, the master device can be a processing unit, such as a CPU (central processing unit), a CISC-type (complex instruction set computer) CPU, RISC-type CPU (reduced instruction set computer), or a digital signal processor (DSP). A converter 804 is coupled to at least one master device of the master devices. A slave device 812 is coupled to the converter 804. In one embodiment, multiple slave devices are coupled to the converter 804. For example, the slave device 812 can be a memory, a pre-processor, a passive storage device or a logic unit. The converter 804 is bidirectionally coupled to the slave device 812 through the data path 806. The converter 804 also sends write enable signal 808 and read enable signal 810 to the slave device 812. The converter 804 is analogous to the input converter 104 of FIG. 1 or input converter 504 of FIG. 5, in operation. In an embodiment, the converter 804 is analogous to the output converter 118 or the output converter 518 in operation.

[0037] In operation of the computing device 800 of FIG. 8, the master devices operate at N bits per clock cycle. For example, a master device 802a operates at 24 bits per clock cycle. Thus, data is read by the master device 802a at a rate of 24 bits/clock, and the data is written by the master device 802a at a rate of 24bits/clock. The slave device 812 operates at M bits per clock cycle. A write operation is defined as the master device 802a writing a data in the slave device 812, and a read operation is defined as the master device 802a reading the data from the slave device 812. During write operation, the converter 804 receives the data from the master device 802a at the rate of N bits per clock cycle. However, the slave device 812 operates at M bits per clock cycle. Therefore, the converter 804 temporarily stores the data received from the master device 802a

and provides M bits to the slave device 812 through the data path 806 when a number of bits stored in the converter 804 is equal to or more than M. The converter 804 also sends the write enable signal 808 to the slave device 812 at every clock cycle when the number of bits stored in the converter 804 is equal to or more than M. The write enable signal 808 indicates to the slave device 812 that the data on the data path 806 is a valid data. For ease of understanding, the write operation is now explained with the help of an example in which the master device 802a operates at 24 bits per clock cycle, and the slave device 812 operates at 32 bits per clock cycle. The converter 804 receives data from the master device 802a at a rate of 24 bits per clock cycle. Because the slave device 812 operates at 32 bits per clock cycle, the data from the master device 802a cannot be written directly to the slave device 812. Therefore, the converter 804 temporarily stores the data received from the master device 802a and provides 32 bits to the slave device 812 through the data path 806 when a number of bits stored in the converter 804 is equal to or more than 32. In a first clock cycle, the converter 804 would receive 24 bits of data. Also, because it is less than 32, the converter 804 would store these 24 bits of data. In the second clock cycle, the converter 804 would receive another 24 bits of data. Thus, 48 bits of data is stored in the converter 804 at the beginning of the second clock cycle, which is more than M. Thus, at the second clock cycle, the converter 804 would provide 32 bits of data to the slave device 812. The total number of bits stored in the converter 804 at the end of second clock cycle is 16 (48-32 = 16). At the third clock cycle, the converter 804 would receive another 24 bits of data. Thus, 40 (16+24=40) bits of data is stored in the converter 804 at the beginning of the third clock cycle, which is more than M. Thus, at the third clock cycle, the converter 804 would provide 32 bits of data to the slave device 812. The total number of bits stored in the converter 804 at the end of third clock cycle is 8 (40-32 = 8). Also, the converter 804 sends write enable signal 808 to the slave device 812 at every clock cycle when the number of bits stored in the converter 804 at the beginning of a clock cycle, is equal to or more than M.

[0038] This ensures that memory is not wasted. Also, the ratio of the operating speed of master device 802a and the slave device 812 (M and N) is not required to be an integer. The converter 804 provides fractional packing of data received from the master device 802a and transferring to the slave device 812. Similarly, during the read operation, the converter supports transfer of data from the slave device 812 to the master device 802a. The converter 804 sends the read enable signal 810 to the slave device 812 at every clock cycle when it is reading data from the slave

device 812. When the master device 802a operates at 24 bits per clock cycle, the slave device 812 operates at 32 bits per clock cycle. During read operation, the converter 804 receives data from the slave device 812 at a rate of 32 bits per clock cycle. Because the master device 802a operates at 24 bits per clock cycle, the data from the slave device 812 cannot be written directly to the master device 802a. In a first clock cycle, the converter 804 would receive 32 bits of data from the slave device 812, and these bits are stored in the converter 804. The converter 804 would provide 24 bits of data to the master device 802a and store the remaining 8 bits (32-24=8bits) of data. In the second clock cycle, the converter 804 would receive another 32 bits of data from the slave device 812. Thus, 42 bits of data is stored in the converter 804 at the beginning of the second clock cycle, which is more than N. At the second clock cycle, the converter 804 would provide 24 bits of data to the master device 802a. The total number of bits stored in the converter 804 at the end of second clock cycle is 18 (42-24 = 18).

[0039] The term "circuit" means at least either a single component or a multiplicity of passive or active components, which are connected together to provide a desired function. The term "signal" means at least one current, voltage, charge, data or other signal.

[0040] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A circuit comprising:

an input converter configured to receive N scan inputs and configured to generate M pseudo scan inputs, where M and N are integers;

a scan compression architecture coupled to the input converter and configured to generate P pseudo scan outputs in response to the M pseudo scan inputs; and

an output converter coupled to the scan compression architecture and configured to generate Q scan outputs in response to the P pseudo scan outputs, wherein P and Q are integers, and the input converter receives the N scan inputs at a first frequency and generates the M pseudo scan inputs at a second frequency, and the output converter receives the P pseudo scan outputs at the second frequency and generates the Q scan outputs at the first frequency.

2. The circuit of claim 1, wherein a ratio of the first frequency and the second frequency is equal to a ratio of M and N and to a ratio of P and Q.

3. The circuit of claim 1 further comprising a monitor configured to receive a scan clock and generate an internal clock, wherein the scan compression architecture is configured to be driven by the internal clock at the second frequency.

4. The circuit of claim 1, wherein the input converter is configured to receive the N scan inputs at every scan clock and configured to generate the M pseudo scan inputs at the second frequency.

5. The circuit of claim 1, wherein the input converter and the output converter are configured to store the N scan inputs and the P pseudo scan outputs respectively.

6. The circuit of claim 1, wherein the monitor is configured to receive a status signal from the input converter, the status signal configured to update the monitor on a number of scan inputs stored in the input converter at a beginning of every scan clock.

7. The circuit of claim 1, wherein the monitor is configured to discontinue the internal clock to the scan compression architecture when the number of scan inputs stored in the input converter, at the beginning of the scan clock, is less than M.

8. The circuit of claim 1, wherein the output converter is configured to receive an enable signal from the monitor, the enable signal configured to disable the storage of pseudo scan outputs in the output converter when the pseudo scan outputs are not received in the output

converter.

9. The circuit of claim 1, wherein the scan compression architecture further comprises:

a decompressor coupled to the input converter and configured to receive the M pseudo scan inputs;

a compressor coupled to the decompressor and configured to generate the P pseudo scan outputs; and

a plurality of scan chains coupled between the decompressor and the compressor, wherein each scan chain of the plurality of scan chains comprises a plurality of scan cells.

10. The circuit of claim 1, wherein the plurality of scan chains is driven by the internal clock.

11. The circuit of claim 1, wherein the decompressor is configured to generate a plurality of core scan inputs in response to the M pseudo scan inputs.

12. The circuit of claim 1, wherein the plurality of scan chains is configured to receive the plurality of core scan inputs, and wherein each scan cell of the plurality of scan cells is configured to shift a core scan input of the plurality of core scan inputs at the second frequency.

13. The circuit of claim 1, wherein the plurality of scan chains is configured to generate a plurality of core scan outputs in response to the plurality of core scan inputs.

14. The circuit of claim 1, wherein the compressor is configured to generate the P pseudo scan outputs in response to the plurality of core scan outputs.

15. The circuit of claim 1, wherein: a storage depth of the input converter is K bits, where K is an integer, and K is greater than or equal to 2N; and a storage depth of the output converter is L bits, wherein L is an integer, and L is greater than or equal to 2P.

16. A method of testing comprising:

receiving N scan inputs at a first frequency;

generating M pseudo scan inputs at a second frequency from N scan inputs;

generating P pseudo scan outputs at the second frequency from M pseudo scan inputs; and

generating Q scan outputs at the first frequency from M pseudo scan outputs, wherein a ratio of the first frequency and the second frequency is equal to a ratio of M and N and to a ratio of P and Q, where N, M, P and Q are integers.

17. The method of claim 16 further comprising receiving N scan inputs at every scan clock, generating M pseudo scan inputs at the second frequency, storing the N scan inputs, and

generating M pseudo scan inputs when a number of scan inputs stored in the input converter is equal to or more than M.

18. The method of claim 16 further comprising receiving P pseudo scan outputs at the second frequency, generating Q scan outputs at every scan clock, storing the P pseudo scan outputs, and generating the Q scan outputs when a number of pseudo scan outputs stored in the output converter is equal to or more than Q.

19. A computing device comprising:

a master device configured to operate at N bits per clock cycle;

a slave device coupled to the master device and configured to operate at M bits per clock cycle; and

a converter coupled to the master device and the slave device, wherein the converter, during a write operation, is configured to: receive N bits from the master device at every clock cycle; store bits received from the master device; and provide M bits to the slave device when a number of bits stored in the converter is equal to or more than M.

20. The computing device of claim 19, wherein the converter is configured to provide a write enable signal to the slave device at every clock cycle during the write operation.

21. The computing device of claim 19, wherein the converter, during a read operation is configured to: receive M bits from the slave device at every clock cycle; store bits received from the slave device; and provide N bits to the master device when a number of bits stored in the converter is equal to or more than N.

22. The computing device of claim 19, wherein the converter is configured to provide a read enable signal to the slave device at every clock cycle during the read operation.

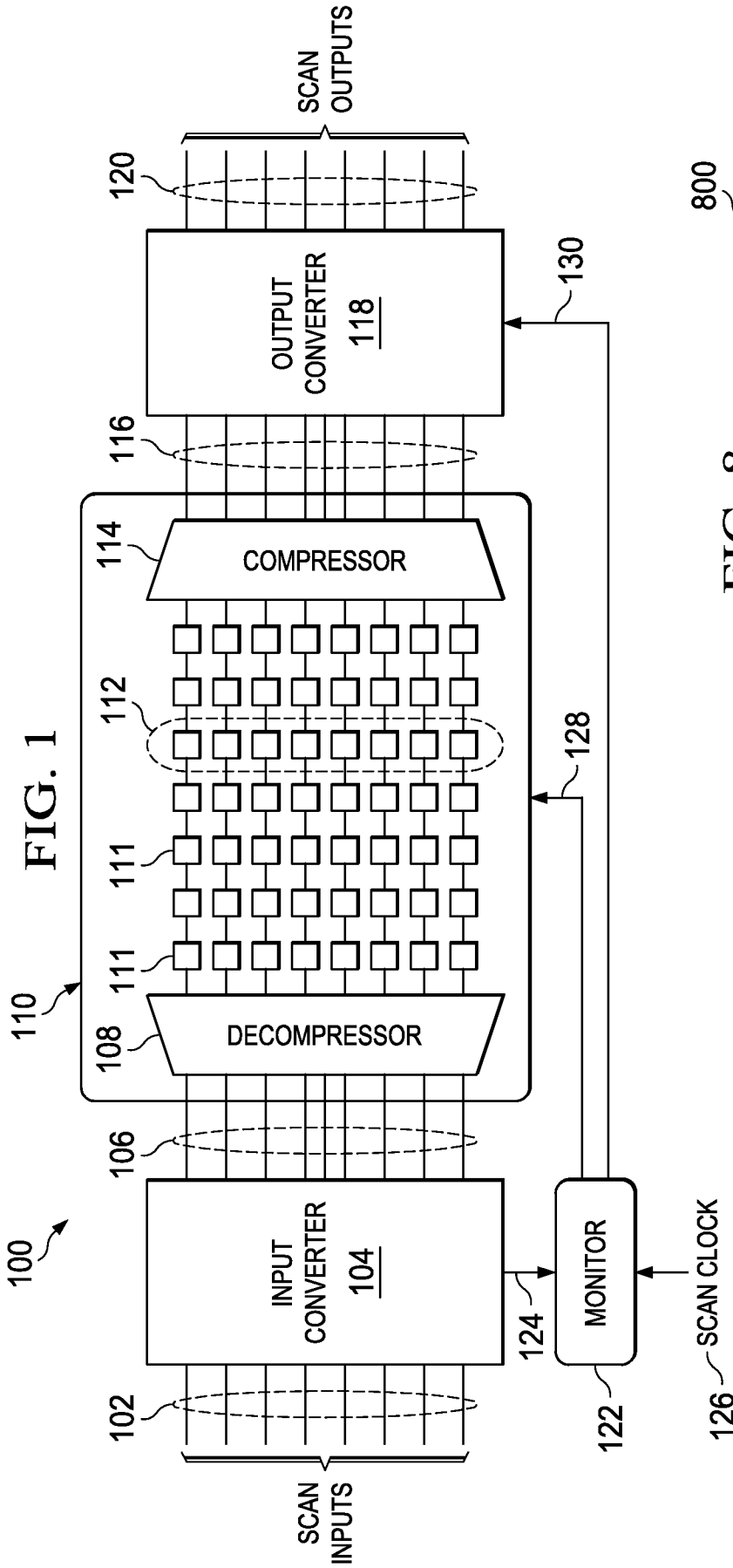

SCAN OUTPUTS
120
OUTPUT CONVERTER 118
130
116
114
COMPRESSOR
112
111
111
110
108
DECOMPRESSOR
128
106
100
INPUT CONVERTER 104
124
MONITOR
SCAN CLOCK
102
122
126
SCAN INPUTS

FIG. 1

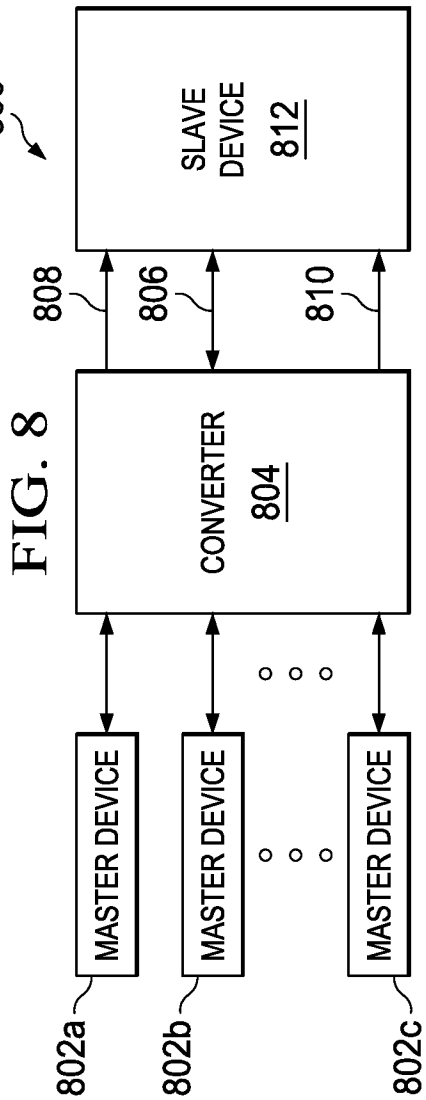

800
SLAVE DEVICE 812
808
806
810
CONVERTER 804
MASTER DEVICE
MASTER DEVICE
MASTER DEVICE
802a
802b
802c

FIG. 8

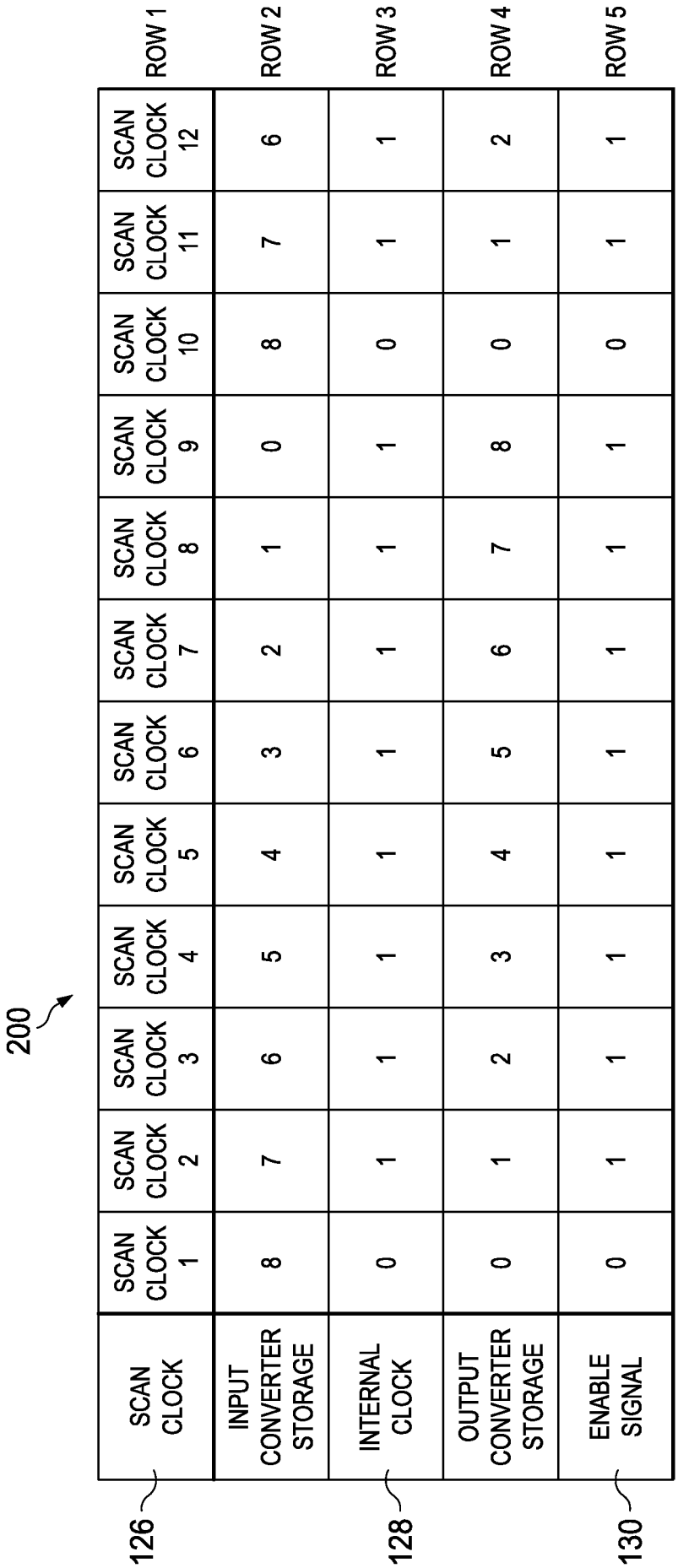
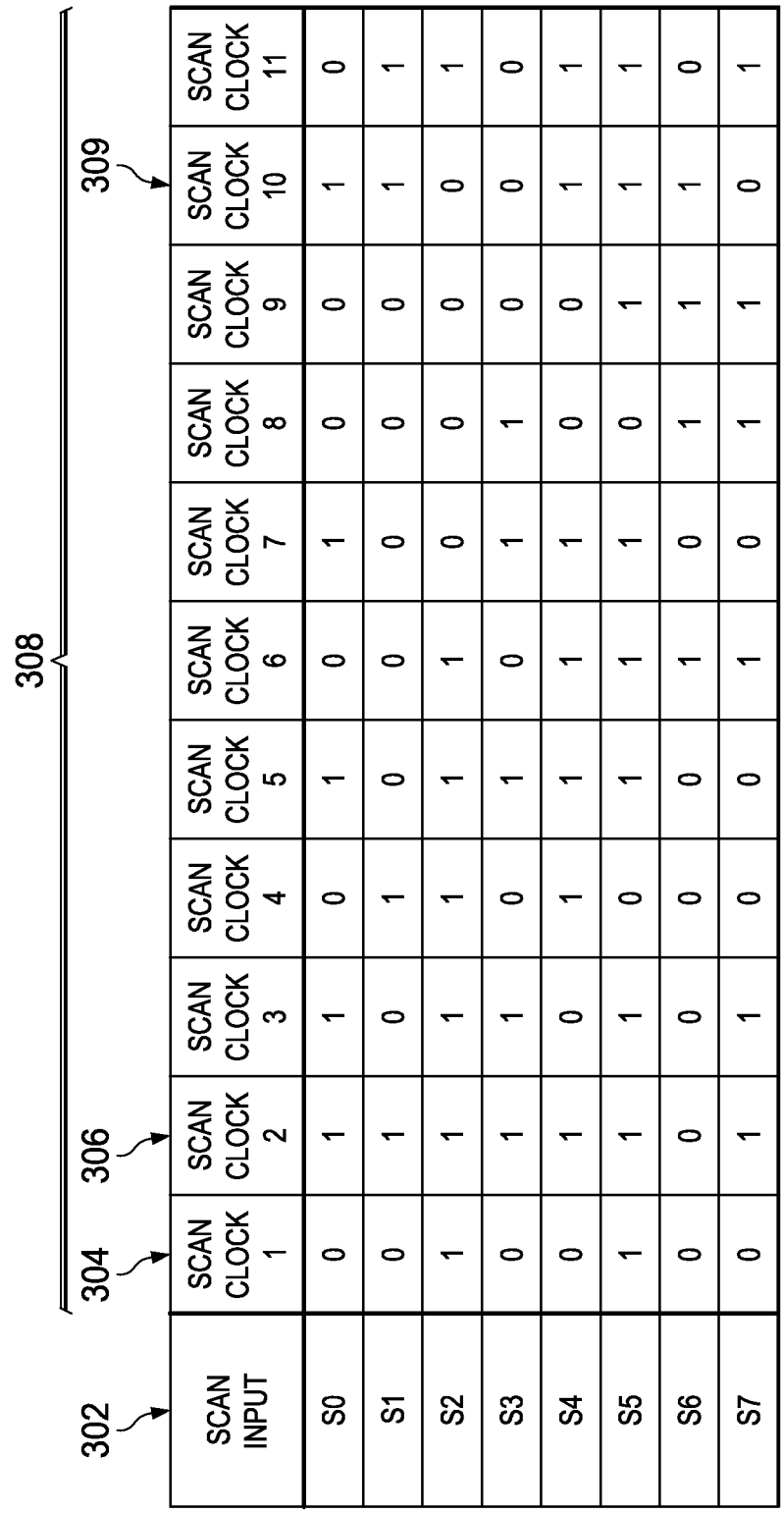
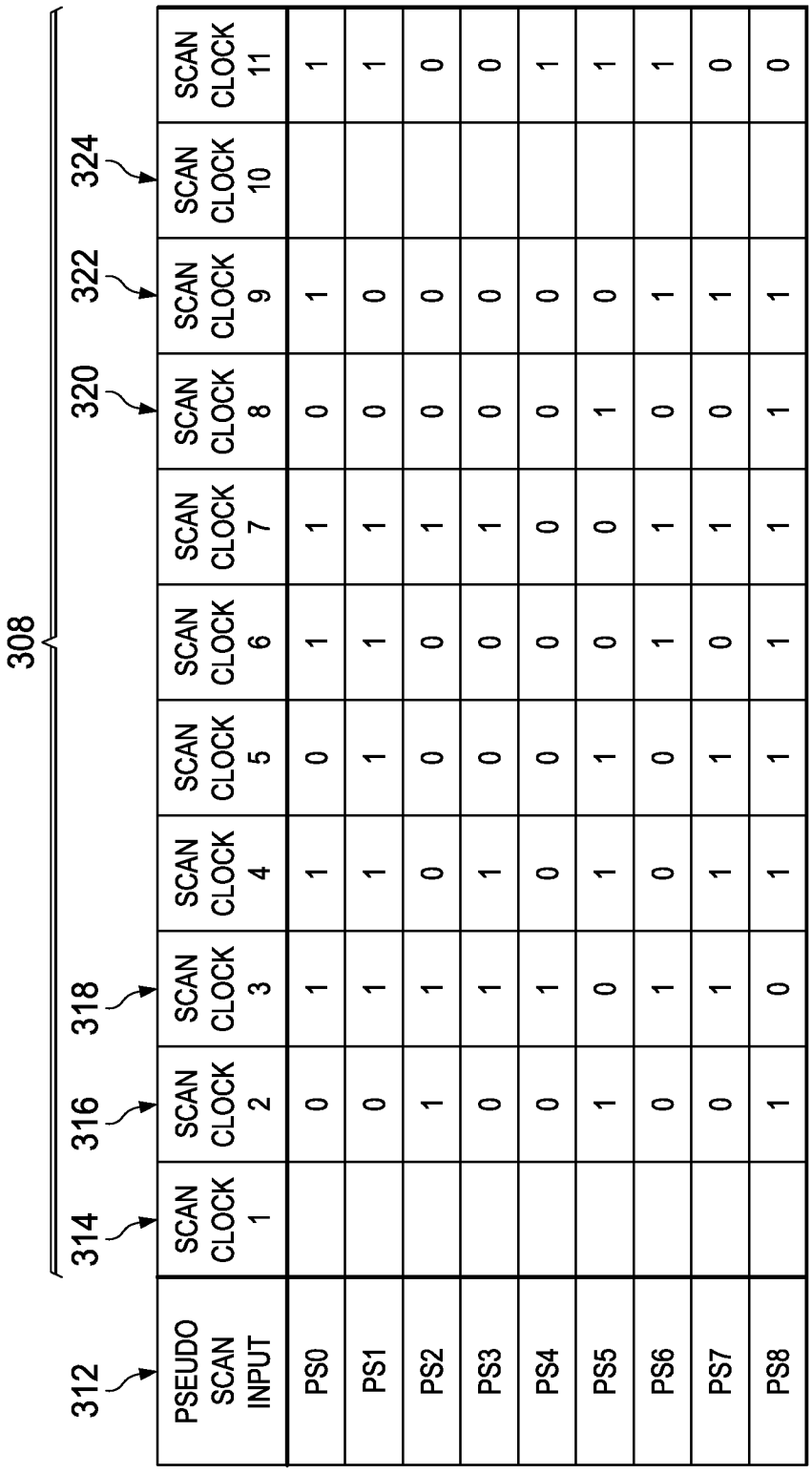

200
126
128
130
SCAN CLOCK
INPUT CONVERTER STORAGE
INTERNAL CLOCK
OUTPUT CONVERTER STORAGE
ENABLE SIGNAL
SCAN CLOCK 1
SCAN CLOCK 2
SCAN CLOCK 3
SCAN CLOCK 4
SCAN CLOCK 5
SCAN CLOCK 6
SCAN CLOCK 7
SCAN CLOCK 8
SCAN CLOCK 9
SCAN CLOCK 10
SCAN CLOCK 11
SCAN CLOCK 12
ROW 1
8 7 6 5 4 3 2 1 0 8 7 6
0 1 1 1 1 1 1 1 1 0 1 1
0 1 2 3 4 5 6 7 8 0 1 2
0 1 1 1 1 1 1 1 1 0 1 1
ROW 2
ROW 3
ROW 4
ROW 5

FIG. 2



SCAN INPUT	SCAN CLOCK 1	SCAN CLOCK 2	SCAN CLOCK 3	SCAN CLOCK 4	SCAN CLOCK 5	SCAN CLOCK 6	SCAN CLOCK 7	SCAN CLOCK 8	SCAN CLOCK 9	SCAN CLOCK 10	SCAN CLOCK 11
S0	0	1	1	0	1	0	1	0	0	1	0
S1	0	1	0	1	0	0	0	0	0	1	1
S2	1	1	1	1	1	1	0	0	0	0	1
S3	0	1	1	0	1	0	1	1	0	0	0
S4	0	1	0	1	1	1	1	0	0	1	1
S5	1	1	1	0	1	1	1	0	1	1	1
S6	0	0	0	0	0	1	0	1	1	1	0
S7	0	1	1	0	0	1	0	1	1	0	1

FIG. 3(a)



PSEUDO SCAN INPUT	SCAN CLOCK 1	SCAN CLOCK 2	SCAN CLOCK 3	SCAN CLOCK 4	SCAN CLOCK 5	SCAN CLOCK 6	SCAN CLOCK 7	SCAN CLOCK 8	SCAN CLOCK 9	SCAN CLOCK 10	SCAN CLOCK 11
PS0		0	1	1	0	1	1	0	1		1
PS1		0	1	1	1	1	1	0	0		1
PS2		1	1	0	0	0	1	0	0		0
PS3		0	1	1	0	0	1	0	0		0
PS4		0	1	0	0	0	0	0	0		1
PS5		1	0	1	1	0	0	1	0		1
PS6		0	1	0	0	1	1	0	1		1
PS7		0	1	1	1	0	1	0	1		0
PS8		1	0	1	1	1	1	1	1		0

FIG. 3(b)

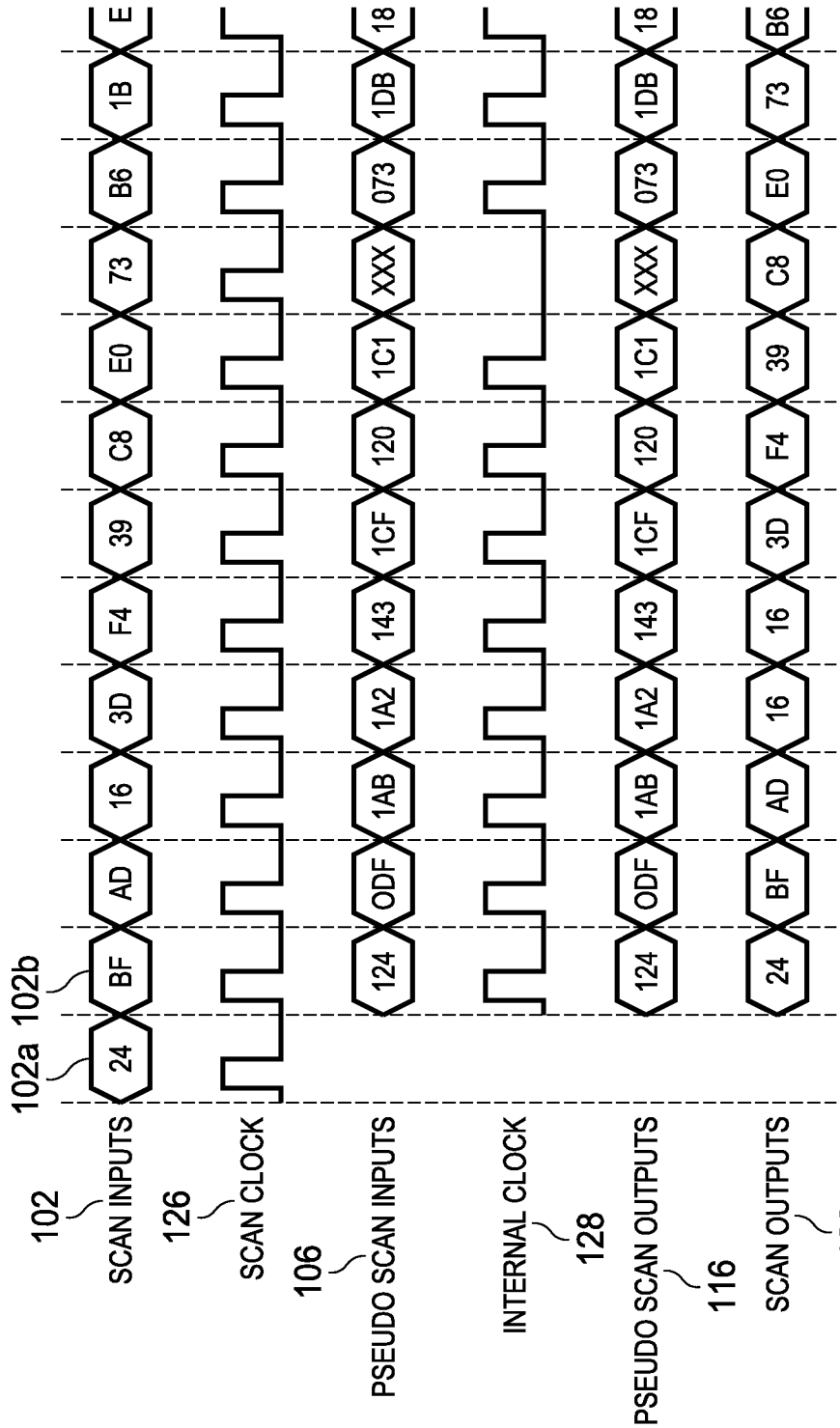

102
SCAN INPUTS
102a
102b
24
BF
AD
16
3D
F4
39
C8
E0
73
B6
1B
E
126
SCAN CLOCK
106
PSEUDO SCAN INPUTS
124
ODF
1AB
1A2
143
1CF
120
1C1
XXX
073
1DB
18
INTERNAL CLOCK
128
PSEUDO SCAN OUTPUTS
116
SCAN OUTPUTS
120
24
BF
AD
16
16
3D
F4
39
C8
E0
73
B6

FIG. 4

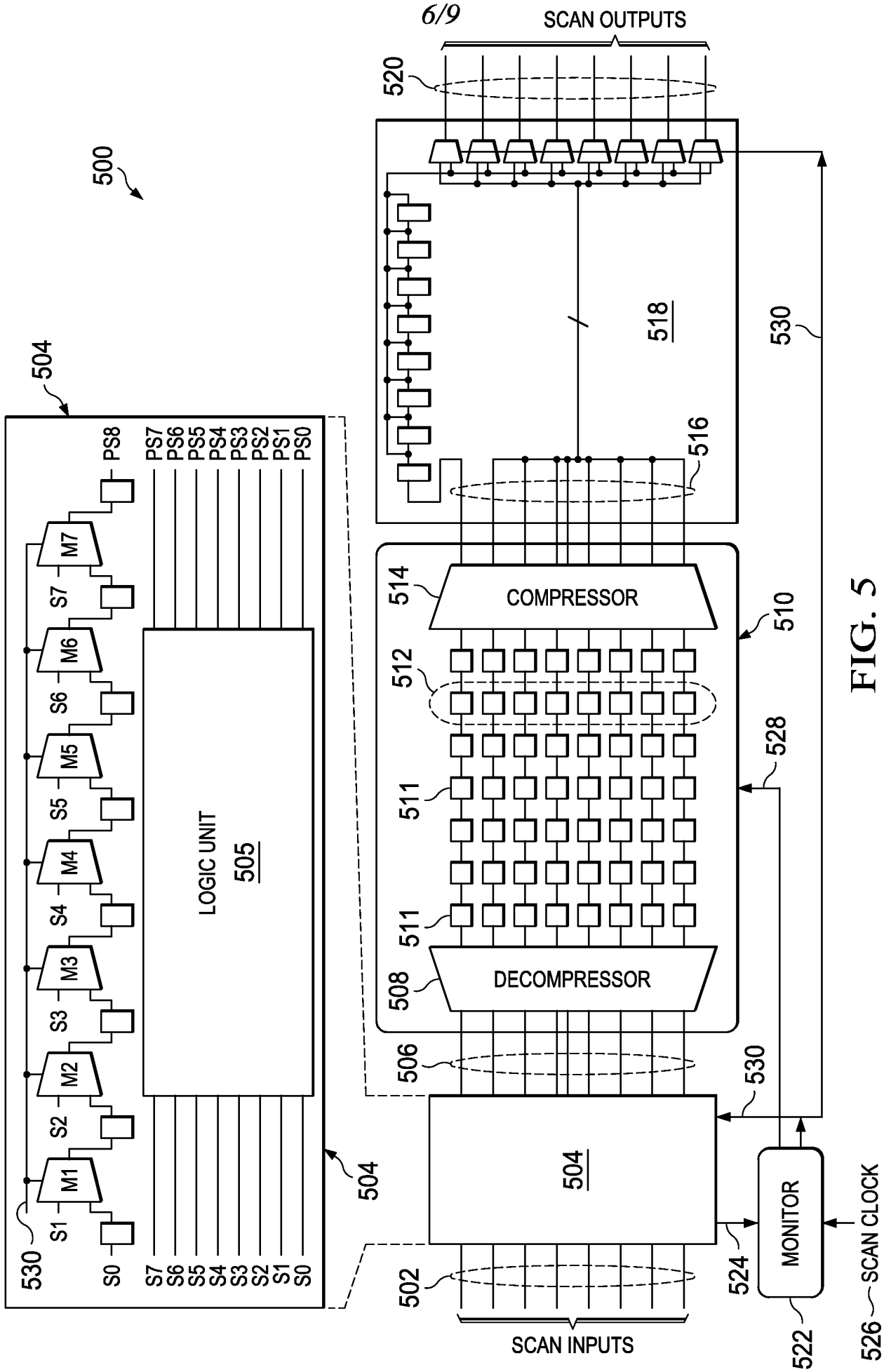
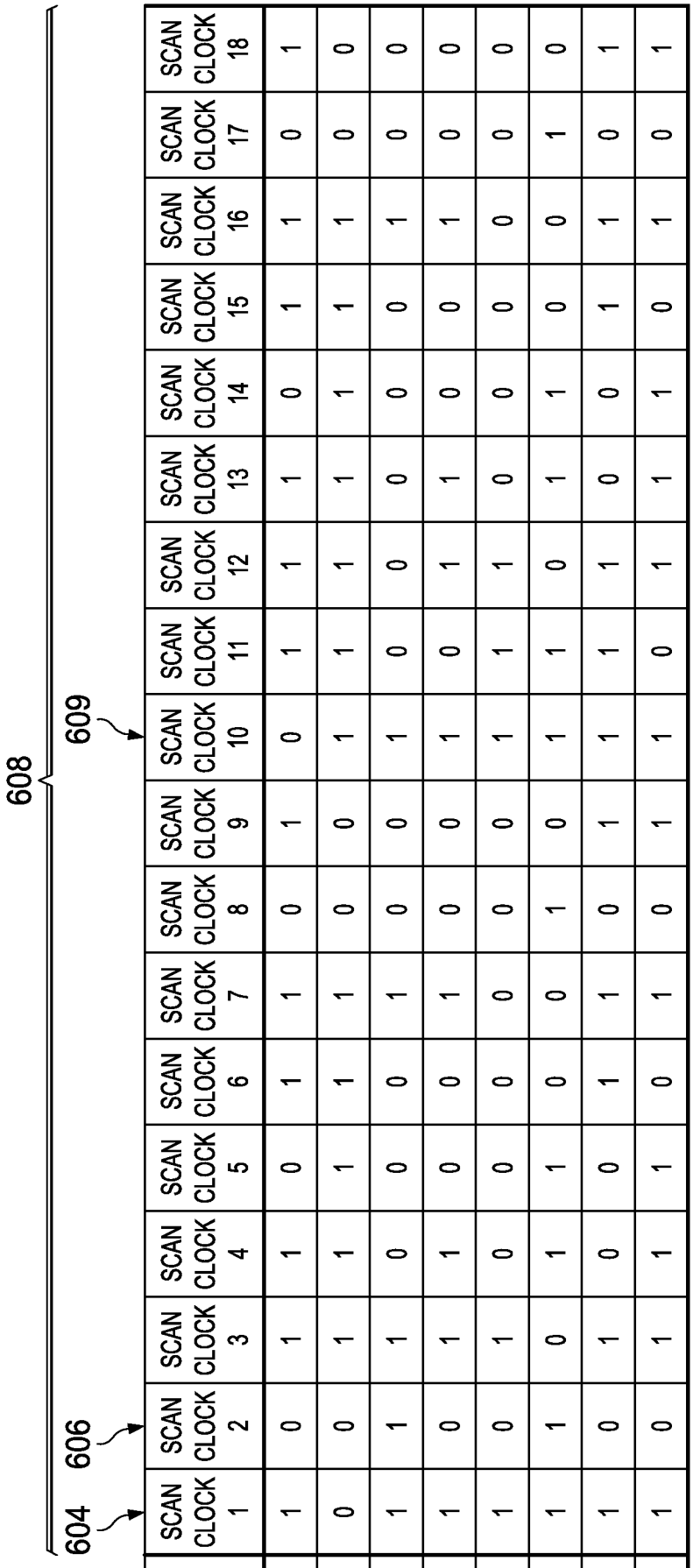
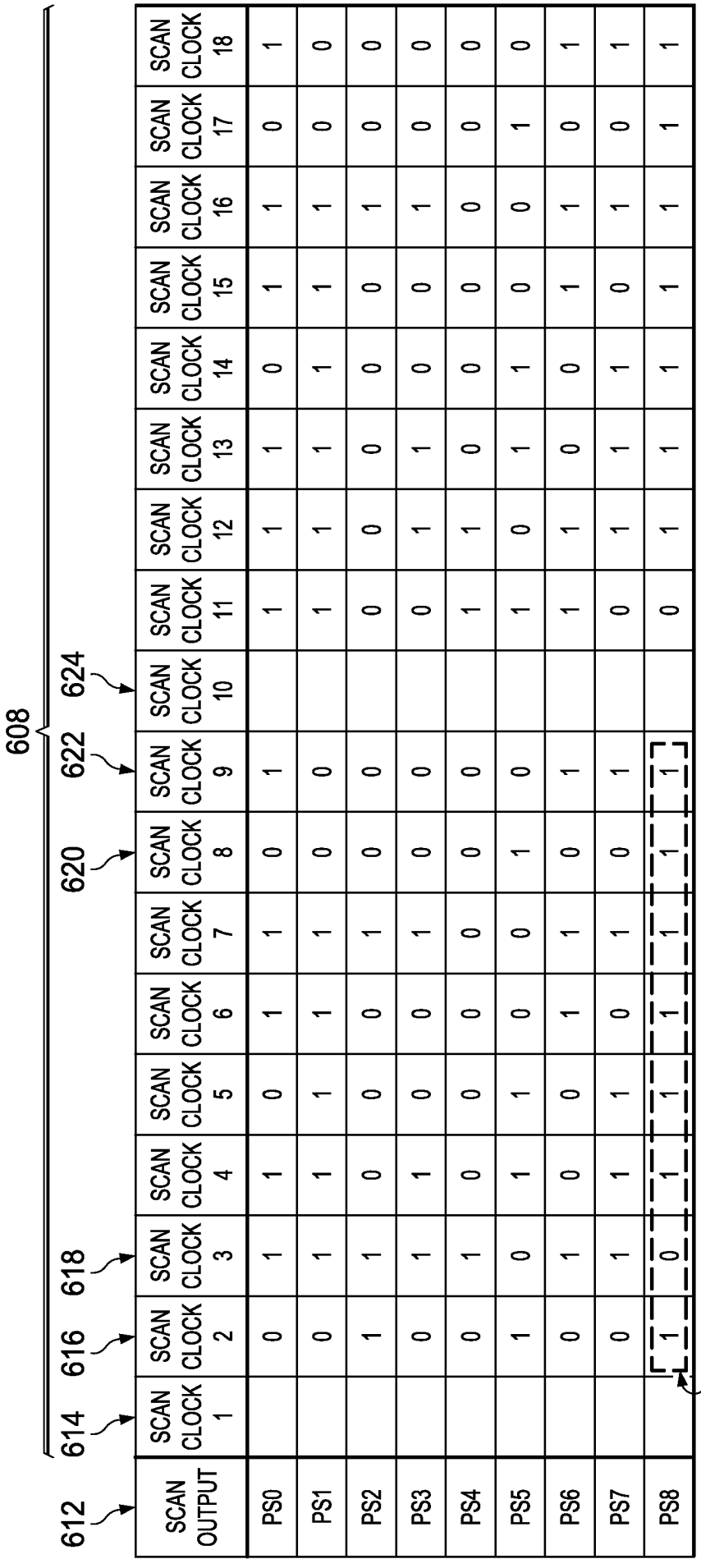

SCAN OUTPUTS
520
500
504
518
530
516
514
COMPRESSOR
510
512
528
511
511
508
DECOMPRESSOR
506
530
504
PS8
PS7
PS6
PS5
PS4
PS3
PS2
PS1
PS0
M7
M6
M5
M4
M3
M2
M1
S7
S6
S5
S4
S3
S2
S1
S0
LOGIC UNIT
505
530
504
502
524
MONITOR
SCAN CLOCK
522
526
SCAN INPUTS

FIG. 5



SCAN INPUT	SCAN CLOCK 1	SCAN CLOCK 2	SCAN CLOCK 3	SCAN CLOCK 4	SCAN CLOCK 5	SCAN CLOCK 6	SCAN CLOCK 7	SCAN CLOCK 8	SCAN CLOCK 9	SCAN CLOCK 10	SCAN CLOCK 11	SCAN CLOCK 12	SCAN CLOCK 13	SCAN CLOCK 14	SCAN CLOCK 15	SCAN CLOCK 16	SCAN CLOCK 17	SCAN CLOCK 18
S0	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1	1	0	1
S1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0	0
S2	1	1	1	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0
S3	1	0	1	1	0	0	1	0	0	1	0	1	1	0	0	1	0	0
S4	1	0	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
S5	1	1	0	1	1	0	0	1	0	1	1	0	1	1	0	0	1	0
S6	1	0	1	0	0	1	1	0	1	1	1	1	0	0	1	1	0	1
S7	1	0	1	1	1	0	1	0	1	1	0	1	1	1	0	1	0	1

FIG. 6(a)



SCAN OUTPUT	SCAN CLOCK 1	SCAN CLOCK 2	SCAN CLOCK 3	SCAN CLOCK 4	SCAN CLOCK 5	SCAN CLOCK 6	SCAN CLOCK 7	SCAN CLOCK 8	SCAN CLOCK 9	SCAN CLOCK 10	SCAN CLOCK 11	SCAN CLOCK 12	SCAN CLOCK 13	SCAN CLOCK 14	SCAN CLOCK 15	SCAN CLOCK 16	SCAN CLOCK 17	SCAN CLOCK 18
PS0		0	1	1	0	1	1	0	1		1	1	1	0	1	1	0	1
PS1		0	1	1	1	1	1	0	0		1	1	1	1	1	1	0	0
PS2		1	1	0	0	0	1	0	0		0	0	0	0	0	1	0	0
PS3		0	1	1	0	0	1	0	0		0	1	1	0	0	1	0	0
PS4		0	1	0	0	0	0	0	0		1	1	0	0	0	0	0	0
PS5		1	0	1	1	0	0	1	0		1	0	1	1	0	0	1	0
PS6		0	1	0	0	1	1	0	1		1	1	0	0	1	1	0	1
PS7		0	1	1	1	0	1	0	1		0	1	1	1	0	1	0	1
PS8		1	0	1	1	1	1	1	1		0	1	1	1	1	1	1	1

FIG. 6(b)

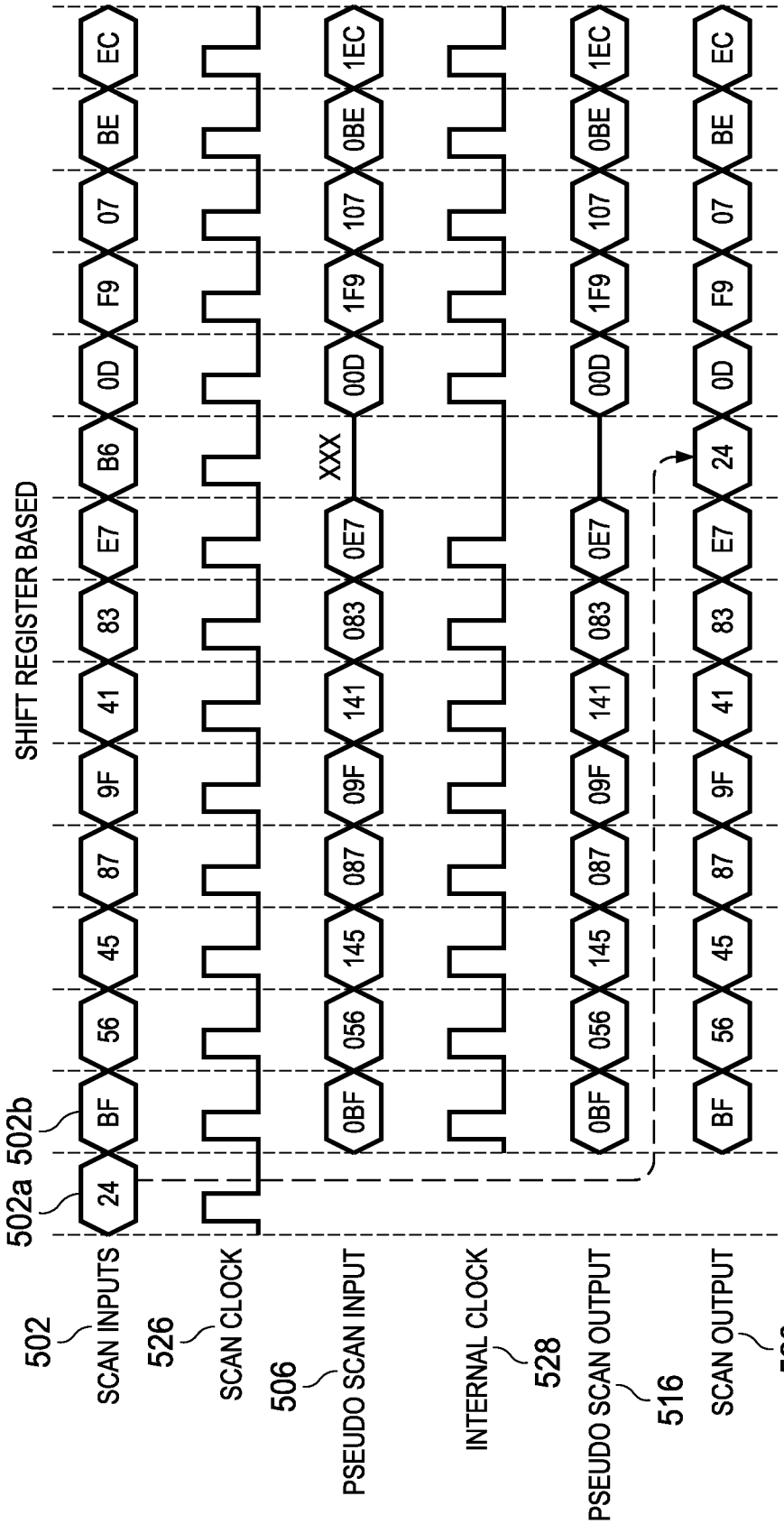

SHIFT REGISTER BASED
502a
502b
24
BF
56
45
87
9F
41
83
E7
B6
0D
F9
07
BE
EC
0BF
056
145
087
09F
141
083
0E7
XXX
00D
1F9
107
0BE
1EC
502
SCAN INPUTS
526
SCAN CLOCK
506
PSEUDO SCAN INPUT
528
INTERNAL CLOCK
516
PSEUDO SCAN OUTPUT
520
SCAN OUTPUT

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/029996

A. CLASSIFICATION OF SUBJECT MATTER

G01R 31/3177 *(200.01)*
G06F 11/25 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G01R 31/00, 31/28, 31/317, 31/3177, G06F 11/00, 11/07, 11/16, 11/22, 11/25

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/0289369 A1 (LEE HEON-HEE) 24.11.2011	1-22
A	US 2013/0159800 A1 (TEXAS INSTRUMENTS INCORPORATED) 20.06.2013	1-22
A	US 2008/0222470 A1 (TOMOKI SATOI et. al.) 11.09.2008	1-22

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 August 2015 (20.08.2015)	27 August 2015 (27.08.2015)

Name and mailing address of the ISA/RU:
Federal Institute of Industrial Property,
Berezhkovskaya nab., 30-1, Moscow, G-59,
GSP-3, Russia, 125993
Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37

Authorized officer

M. Bryleva

Telephone No. 8 499 240 25 91