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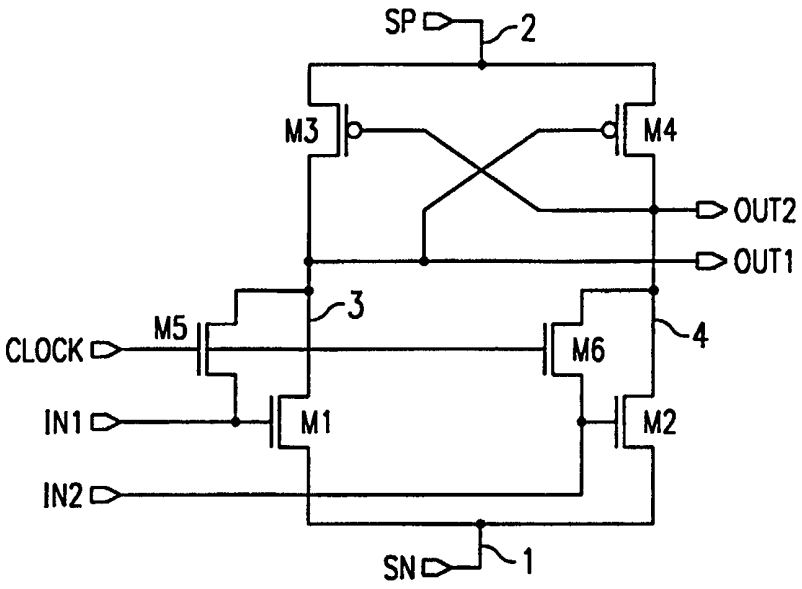
(57) Abstract

First and second currents can be compared and an output generated at first and second output nodes (3) and (4). First, the first and second output nodes (3) and (4) are calibrated such that the first output node (3) reaches a first real equilibrium voltage and the second output node (4) reaches a second real equilibrium voltage. The first real equilibrium voltage is not necessarily equal to the second real equilibrium voltage. At the active edge of a clock signal, the difference between the first and second currents can be amplified by causing the voltage at the first output node (3) to become lower than the voltage at the second output node (4) when the first current is greater than the second current. On the other hand, the voltage at the first output node (3) becomes higher than the voltage at the second output node (4) when the first current is less than the second current. With some modifications including at least one more switch, voltage comparisons can similarly be achieved.



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Self-Calibrating Self-Regenerative Comparator Circuit and Method

FIELD OF THE INVENTION

The present invention relates generally to electrical circuits and more particularly to a self-calibrating self-regenerative comparator circuit and method.

BACKGROUND OF THE INVENTION

Analog circuits rely very often on the matching of transistors. Unfortunately, with the advent of smaller feature size technology, the spread on several transistor parameters becomes more pronounced. As an example, transistors fabricated in Silicon on Insulator (SOI) show unwanted "kink" effects, which can be seen as a change in transistor's parameters with time, mostly depending on the transistor's operational history. In this case, even if the circuit is tuned at fabrication, the transistor operation may be affected over time.

One way to cope with these mismatch problems is to layout very large transistor pairs when good matching is required. This solution is only gained at the expense of larger area and input capacitance. Another popular method is to have a self-calibrating mechanism whereby the errors get canceled using input capacitors (which take up the error), and an Operational Transconductance Amplifier (OTA). This input stage in then often followed by a self-regenerative amplification stage, generating rail-to-rail digital output(s).

Several prior patents relating to problems similar to those addressed by the present invention have issued. For example, U.S. Patent No. 5,568,438 discloses offset auto zeroing for reducing the access time of a RAM cell. In this patent, the auto zeroing

stage is not self-regenerative. The circuit disclosed in U.S. Patent No. 5,237,533 has similar merits and is not self-regenerative either. U.S. Patent No. 5,300,839 discloses a circuit that overcomes the threshold voltage mismatch of a differential pair of transistors at the input of a sense-amplifier.

SUMMARY OF THE INVENTION

In one aspect, the present invention discloses a comparator building block that includes a positive feedback and a negative feedback mechanism. The negative feedback mechanism is stronger by construction, and can be enabled and disabled by switches. For example, when the switches are in the conductive state, the comparator is forced in a self-calibration mode where finally no current flows through the switches, even if there are substantial mismatches in the transistors constituting the comparator.

This mismatch tolerant comparator building block can perform current comparisons. For example, when combined with two capacitors and one or more switches, the comparator can perform rail-to-rail voltage comparisons with offset errors more than ten times lower than the threshold voltage mismatch of the pairs of transistors defining the comparator. Advantageously, in the same way a high tolerance to all other mismatches of the transistors is obtained. In one application, a sense-amplifier for memory cell read out can be constructed with mismatch insensitivity by including two cascode transistors between the memory bit-lines and the comparator building block.

In the preferred embodiment of the present invention, a self-calibration comparator stage and a self-regenerative digitizing stage are merged into one stage operating with two phases. In a first phase, self-calibration is performed. In the second phase, a self-regenerative amplification process amplifies the initial signal difference up to a desired level, e.g. the digital rail-to-rail level. Mismatches in transistor's parameters are allowed since their effects are cancelled by the self-calibration principle. Voltages and currents can be compared with improved precision.

In one specific embodiment, the present invention can be implemented with six transistors. The first transistor has a current path coupled between a first supply voltage (e.g., ground) and a first switching node. The second transistor has a current path coupled between the first supply voltage node and a second switching node. In this embodiment, the third transistor is coupled between a second supply voltage node and the first switching node and the fourth transistor between the second supply voltage node and the second switching node. These two transistors are cross-coupled. The fifth transistor has a current path coupled between the first switching node and the control terminal of the first transistor and the sixth transistor has a current path being coupled between the second switching node and control terminal of the second transistor. The control terminal of the sixth transistor is coupled to the control terminal of the fifth transistor.

The present invention is advantageous compared to prior art circuits that use an OTA stage. Since the slower OTA stage is avoided, faster self-regeneration can be achieved. In addition, the basic comparator building block requires only six small area transistors, keeping the occupied transistor area small.

BRIEF DESCRIPTION OF THE DRAWINGS

The above features of the present invention will be more clearly understood from consideration of the following descriptions in connection with accompanying drawings in which:

Figure 1 is a preferred embodiment building block of the comparator having six transistors;

Figure 2 is a voltage comparator using the building block of Figure 1 and including de-coupling capacitors and three switches;

Figure 3 is a timing diagram showing the voltages versus time as a result of a spice simulation;

Figure 4 shows an alternative voltage comparator that includes one switch and two resistors;

Figure 5 depicts a current comparator with two cascode transistors;

Figure 6 is an extension of the six-transistor system with two more transistors acting as internal cascodes making the basic building block contain eight transistors;

Figure 7 is a post amplifier that can be used with any of the comparators of the present invention; and

Figure 8 is a block diagram of a memory device that includes sense amplifiers that utilize the present invention.

DETAILED DESCRIPTION

The making and use of the presently preferred embodiments are discussed below in detail. However, it should be appreciated that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

The present invention will now be described with respect to specific examples. The detailed explanation is limited to a description of a circuit based on CMOS transistors. The person skilled in the art can easily convert the given circuits to BiCMOS or bipolar circuits. For sake of simplicity, the explanation is also limited to the case where the positive feedback is due to PMOS transistors, and negative feedback to NMOS transistors. The designer skilled in the art can easily swap the role of the NMOS and the PMOS transistor, in the same basic way any design with complementary transistors can be "flipped up side down".

Referring first to Figure 1, the basic building block of the preferred embodiment of the present invention is illustrated. The circuit is coupled between a negative supply node 1 (labeled SN) and a positive supply node 2 (labeled SP). For example, negative supply node 1 (SN) can be connected to ground (Gnd) and positive supply node 2 (SP) can be connected to the V_{cc} supply (e.g., 5V, 3.3V or 2.5V relative to Gnd). This arrangement is sufficient for most applications.

In some embodiments, however, one or both of nodes 1 (SN) and 2 (SP) can also be connected to a current source (not shown), which will then tune the current consumption of the circuit. The current level will also affect the g_m of transistors M1-

M4, and hence influence the comparator speed and thermal noise equivalent input level. For most applications, however, a direct connection of nodes 1 (SN) and 2 (SP) to the power supply lines will suffice, and by tuning the W/L (width to length) ratios of transistors M1-M4 with enough consideration, sufficient precision on the current consumption can be obtained.

Another reason to drive one or both of the supply nodes SN and SP would be to allow a power down mode of the comparator, thereby lowering power consumption. This technique is commonly used for comparators that serve as sense amplifiers in memory devices, such as DRAMs.

In order to simplify the explanation of the preferred embodiments, the following discussion assumes that the positive supply node 2 (SP) and the negative supply node 1 (SN) are connected to the V_{cc} and Gnd, respectively.

In the preferred embodiment, transistors M1 and M2 are n-channel MOS (metal oxide semiconductor) transistors that have their sources coupled to the negative supply node 1 (SN). The drain nodes of these transistors M1 and M2 are coupled to the switching nodes 3 and 4 of the comparator. In this example, these nodes 3 and 4 serve as the output terminals Out1 and Out2, respectively. In this configuration, the transistors M1 and M2 each have a current path, e.g., through the channel, between the negative supply node 1 (SN) and the respective switching node 3 or 4. When a component includes a current path coupled between two nodes, it is understood that other components may also be coupled in series. One example of this will be described below with respect to Figure 6.

Transistor M5 and M6 are n-channel MOS transistors that act as switches to allow the gates of transistors M1 and M2 to be coupled to their own drain nodes 3 and 4. The impedance delivered by transistors M1 and M2 is ($g_{01} + g_{m1}$) when M5 and M6 are conducting (and M1 and M2 are then configured as "diodes"), and g_{01} when switches M5 and M6 are non-conducting (and M1 and M2 configured as current sources). As is very well known in the art, the parameters g_{01} and g_{m1} are the output conductance and the transconductance parameters of transistor M1. In this nomenclature, the parameter g_{0x} is the g_0 of transistor MX.

Transistors M3 and M4 are p-channel MOS transistors that have their sources coupled to the positive power supply 2 (SP), and their drains coupled to the switch nodes 3 and 4, respectively. The gates of these transistors M3 and M4 are cross-coupled. That is, the gate of transistor M3 is coupled to the drain of transistor M4 (at node 4), and the gate of transistor M4 is coupled to the drain of transistor M3 (at node 3). This configuration adds to the impedance of the switching nodes with $g_{03} - g_{m3}$. During operation, transistors M1 to M4 typically operate in saturation. In this case, each transistor has an impedance g_0 that is much smaller than its impedance g_m. Therefore, for the sake of simplicity, the g_0's will be neglected in the following analysis.

When switches M5 and M6 are conducting, the total impedance on nodes 3 and 4 (from the combination of the six transistors M1-M6) is g_{m1}-g_{m3}. When the switches M5 and M6 are non-conductive, the total impedance is $-g_{m3}$. Taking the sum of all capacitance in each switching node 3 and 4 as C_{sw}, the time behavior of the system can be calculated. With positive impedance of the switching nodes 3 and 4, a typical exponential decay behavior to a stable equilibrium end point is found. If the voltage at

node 3 is referred to as V_3 and the voltage at node 4 is referred to as V_4, then it follows that:

$$V_4 - V_3 = (V_4 - V_3)_{at\ t=t_1}\, e^{-\frac{g_{m1}-g_{m3}}{C_{sw}}(t-t_1)}$$

The period of time when M5 and M6 are conducting is a resetting phase, and as will be explained later on, can also be a self-calibration phase. The end voltage at both switching nodes 3 and 4 is somewhere between the two supply voltages SP and SN. In the situation where the set up is fully symmetric (i.e., M1 matches M2 in all aspects and M3 matches M4 in all aspects), the end voltage of switching node 3 is exactly equal to the end voltage of switching node 4 (except for the thermal noise difference). When the circuit is not fully symmetric, however, the voltage at node 3 may differ from that at node 4.

When M5 and M6 are non-conducting, an explosive situation is created due to positive feedback. The value over time can be characterized as:

$$V_4 - V_3 = (V_4 - V_3)_{at\ t=t_2}\, e^{+\frac{g_{m3}}{C_{sw}}(t-t_2)}$$

A small deviation in the voltages V_3 and V_4 at time t_2 (the situation at the completion of the reset phase) will be amplified exponentially with time. Several ways to induce a deviation from the equilibrium state will be taught below. Other methods could also be used.

For the resetting to take place, the transconductance g_{m1} is preferably larger than the transconductance g_{m3}. As a rule of thumb, it is preferable that transistors M1 and M2 have more than twice as much g_m as transistors M3 and M4 (e.g., $g_{m1} > 2g_{m3}$). In fact, by increasing the W/L's (width to length ratios) of transistors M1 and M2, the resetting time

is reduced. By keeping the capacitance C_{sw} as low as possible, resetting time and amplification speed are enhanced.

There are cases when the transistor pair M1 and M2 or the transistor pair M3 and M4 do not match. For example, this may occur because the two transistors in the pair have different threshold voltages, different width-to-length ratios (W/L), and/or a difference in another transistor parameter(s). In any of these cases, it is likely that an asymmetric system will be obtained.

However, as long as negative feedback in the reset cycle is maintained (e.g., when M5 and M6 are conducting), an exponential decay behavior to a stable end situation will be established. Similarly, when positive feedback in the amplification cycle is maintained (with M5 and M6 non-conducting), an exponential explosion behavior will still be present.

The stable end situation in an asymmetric situation such as this differs from the end situation of the symmetric situation in the fact that the reached equilibrium state has two different voltages on switching nodes 3 and 4, and that two different currents flow through the drains of transistors M1 and M2.

When no signal is applied to the inputs (terminals In1 and In2 in Figure 1), the switching of transistors M5 and M6 from the conductive to the non-conductive state, induces no deviation from the asymmetric equilibrium state. When equilibrium has been reached and transistors M5 and M6 are still conducting, the voltage on the gates of transistors M1 and M2 remain at a fixed level and no current flows through transistors M5 and M6. Since no current is flowing, these transistors M5 and M6 can as well be

brought into the non-conductive state, without change. The equilibrium is maintained. However, a stable situation has been transformed into a meta-stable situation.

In other words, with this construction, the circuit evolves during resetting to the "real" equilibrium state, even though it is created from an asymmetric construction. In this context, the term "real equilibrium" is defined to mean that the switching direction from that point depends essentially on the externally applied input signal(s) and on the thermal noise and not on the matching of the transistor pairs.

For this reason the first phase can be referred to as a "self-calibration phase" rather than a "reset phase". This asymmetry is in contrast from most other existing regenerative stages where the same voltage on internal switching nodes is enforced by a switch or pass-transistor. In the symmetric situation the existing solution works well. In an asymmetric situation, however, the system does not work as well since the real equilibrium state is not reached. When switching to the regenerative phase, a certain switching direction is then always encouraged. So, the comparator has then an offset roughly in proportion to the mismatch, or to the sum of all mismatches.

The system of Figure 1 can serve as a current (or voltage) comparator. By applying a current difference into the input terminals In1 and In2 just after the clock transition from high to low, a switching direction can be induced. The current difference will change the bias on the gates of transistors M1 and M2 differently, thereby inducing the switching direction.

When enough time is left for the amplification, the output terminals Out1 and Out2 (e.g., nodes 3 and 4) will reach quite different voltages (at least a much larger difference than the difference at equilibrium originating from the mismatches). A post

amplifier (not shown in Figure 1, see Figure 7) can force the output to clear digital levels. Symmetrical impedance loading, e.g., same capacitive and resistive load, of the switching nodes 3 and 4 is thereby advised for good operation. The post amplifier can be either synchronous or asynchronous. In most cases, however, it is suitable to form the post amplifier from two schmitt triggers and an RS flip-flop as shown in Figure 7. For low loading of the switching nodes 3 and 4, voltage followers can be used, speeding up the operation if required.

Similarly, if the current difference is applied during reset, and removed during regeneration, switching is also obtained. Fortunately, the switching direction is the same, whether the current had been applied before or after the falling edge of the clock. From simulation, however, it seems that the effect of applying the current difference just after the negative clock edge gives a stronger switching tendency. Therefore, it is preferred (but not required) to start to apply the current difference more or less concurrent with the falling edge of the clock.

The circuit of Figure 2 shows a method to compare two voltages V1 and V2 using the principles of the present invention. Three switches 10, 11 and 12 are included in this circuit. Two capacitors C1 and C2 serve to de-couple the DC voltage from the comparator (transistors M1-M6) and to de-couple the equilibrium mismatch of the comparator from the inputs V1 and V2.

As shown in the figure, switch 11 has a current path (when conductive) between input node V1 and a first plate of capacitor C1. Similarly, switch 12 has a current path (when conductive) between input node V2 and a first plate of capacitor C2. The switch 10 has a current path (when conductive) between the first plate of capacitor C1 and the

first plate of capacitor C2. In the preferred embodiment, switches 10, 11 and 12 are n-channel (or p-channel) MOS transistors, although many other switches could alternatively be used. Signal ClockN, coupled to the control input of switch 10, is the inverse of the signal Clock, coupled to the control inputs of switches 11 and 12.

In another example, the circuit could be built with switches 11 and 12 as NMOS transistors, switch 10 as a PMOS transistor, and all of the gates commonly tied to Clock. This configuration is not preferred, however, since it limits the input range of the comparator. Other configurations are also possible. Since, simplifying a switch into a transistor (and when it can be done) is generally known in the state of the art, no further detailed will be provided herein.

To understand the operation of the circuit of Figure 2, assume that input nodes V1 and V2 carry different voltages. During the self-calibration phase, nodes 13 and 14 carry the input voltages V1 and V2 since switches 11 and 12 are conducting. During this same period, nodes 3 and 4 are allowed to converge to an equilibrium state, possibly with different voltages due to mismatches.

At the falling edge of the clock, nodes 13 and 14 are forced to the same voltage by switch 10, implying that the previous voltage difference is superimposed on the present existing voltages on the gates of M1 and M2. During this transition, current will flow through transistor 10, the direction of current flow being determined by which voltage V1 or V2 is greater. The switching is started in a direction induced by the sign of the voltage difference between V1 and V2. At this time, input terminals V1 and V2 are disconnected since switches 11 and 12 are non-conductive during that period.

The capacitance of capacitors C1 and C2 can be chosen to have a value on the same order of magnitude as the gate capacitance of transistors M1 and M2, typically between a few fF (femtofarads) and several pf (picofarads). Preferably, the capacitance of capacitor C1 is substantially equal to that of capacitor C2. When the capacitances C1 and C2 are on the same order of magnitude as the gate capacitances, a sufficiently high voltage signal value is transferred without significant loading on the switching nodes 3 and 4 during the self-calibration phase. Choosing a larger W/L for transistors M1 and M2 can compensate for this loading. As an example, capacitors C1 and C2 can be implemented with MOS transistors that are configured as capacitors.

Figure 3 illustrates some curves showing the node voltages as a function of time. These curves were derived from a spice based simulation of a circuit using 0.6 micron CMOS technology and operating at V_{cc} = 5V. In this simulation, all transistors have the minimum gate length (0.6 micron). The transistors serving as switches 10, 11 and 12, as well as transistors M5 and M6, have the minimum transistor width (0.8 micron). Transistors M1 and M2 have a 4 micron width while transistors M3 and M4 have a 2 micron width.

Curve 20 shows the clock signal. Curves 21 and 22 are the voltages on input nodes V1 and V2, respectively. Curves 23 and 24 are the voltages on nodes 13 and 14, respectively. Curves 25 and 26 are the gate voltages on nodes 15 and 16, respectively. Curves 27 and 28 are the voltages on output nodes 3 and 4 respectively, when the circuit is simulated without mismatches. Curves 29 and 30 are the voltages on the same output nodes 3 and 4 when the circuit is simulated with a threshold voltage (ΔVt) mismatch of 110 mV on transistor M2 compared with transistor M1. During self-calibration it is clear

that the equilibrium voltages are not the same in the case of mismatch. The mismatch of 110 mV does not give a considerable change in switching speed, even when sensing (see the voltage values of curves 21 and 22) only 20 mV.

The proper operation of this comparator has been verified for a large number mismatches in several of the key parameters of the transistors in Figure 2. From these tests it is discovered that input voltage differences smaller than one tenth of the mismatch in threshold voltage can be compared without problems.

Figure 4 shows an alternative embodiment whereby switches 11 and 12 have been eliminated. Switch 10 remains. In this circuit, the switches 11 and 12 have been replaced by two (preferably substantially equal) resistors R1 and R2. The voltage difference between V1 and V2 will now be enforced on nodes 13 and 14 with a time constant on the order of about R1.C1. Depending on the application's timing requirements, the maximum value of R1 can be calculated.

The resistors R1 and R2 can be formed from a CMOS transistor (either n-channel or p-channel) operating in its linear regime. For example, the transistor could have its gate tied to Vcc or Gnd (or somewhere in between). This can limit the input common mode swing to a certain extent, as is known to a person ordinary skilled in the art. In some applications, the sources generating V1 and V2 contain their own output resistances, in which case this resistor set up can be favored over the set up of Figure 2. In other cases, resistors R1 and R2 can be implemented by a diffusion region or a layer of doped polysilicon.

Figure 5 teaches one way to extend the current comparing capability. There are several applications whereby currents (I1, I2) acting on relatively large capacitors (C3,

C4) are to be compared. In these cases, the scheme of Figure 5 could be used. This scheme is useful, for example, in memory sense-amplifiers, where the bit-lines represent relatively large capacitance values. Also in optical receiver systems, the capacitors C3 and C4 can represent the input photo-diode(s) and can be large as compared to the sum of the capacitance on the switching nodes 3 and 4.

In this embodiment, two cascode transistors M9 and M10 de-couple the high capacitive nodes 43 and 44 (with their respective capacitances C3 and C4). Four current-biases Ib form the biasing environment of the cascode transistors M9 and M10. What remains is the current difference which is passed through M9 and M10 (biased by Vbias) to the low capacitive nodes 41 and 42.

During self calibration, the error voltage difference due to transistor mismatches in transistors M1 to M6 will be build up on the nodes 41 (coupled to node 3 through transistor M5 during that period) and 42 (coupled to node 4 through transistor M6). This transient is relatively fast because these nodes are low capacitive nodes by construction. The g_m of M9 and M10 are chosen such that enough bandwidth is available to pass sufficiently fast the incoming current I2 and I1 to these nodes 42 and 41. After the falling edge of the clock, the current difference will induce a steep change of voltage on the gates of transistors M1 and M2, inducing the switching direction.

The current biases Ib can be made with transistors as is known in the art of electronics. These biases are preferentially made with degeneration, a technique known by the person skilled in the art, in order to lower the mismatch effects due to these sources. This degeneration technique is also known to lower the injected noise of a current source.

Cascode transistors M9 and M10 can have some mismatch and this will not affect the passage of current into the nodes 41 and 42. When the current bias Ib required to bias M9 and M10 is low as compared to the currents flowing through M3 and M4 during self calibration, then it is possible to leave out the two lower positioned current sources Ib in Figure 5. The bias current can then be drained by the system formed by transistors M1 to M6. However, the designer should then verify good operation.

Sense-amplifier designers working on memory read out systems should appreciate this set-up since the bit-lines (located at nodes 43 and 44) are clamped by the low impedance input of the cascodes, giving only little voltage changes during sensing, which induces less interference between bit-lines of neighboring columns. The larger voltage output changes obtained on nodes 41 and 42 form the input to a self-calibrated, fast self-regenerative amplification system. The designer skilled in the art can add some extra transistors to restore the measured digital value in the RAM cell (after being read out).

The lower current biases Ib in Figure 5 can be omitted (simplifying the circuit) when the current biasing the cascode transistors M9 and M10 is small compared to the currents flowing through transistors M1 and M2 at equilibrium. The upper current sources Ib are preferred for every sense-amplifier, and should operate during the reading operation of a row of cells.

Figure 8 illustrates an example of a DRAM circuit that uses a sense amplifier of the present invention. A row decoder 63, an array of memory cells 60, and a row of sense amplifiers (including 61 and 62) of the present invention are utilized for row readout. As examples, the voltage comparator set-up from Figure 4 or the cascode version from Figure 6 (discussed below) can serve to retrieve the digital-state from the

memory cell. The sense amplifier could alternatively be used with other types of memory cells such as SRAMs or non-volatile memories (e.g., EPROMs, EEPROMs, flash, ROMs, or others).

The cycle utilizes at least a self-calibration phase and an evaluation phase. At the transient between these two phases, the row of interest is selected. The voltage difference induced by the small charge coming from the selected memory cell determines the direction of switching of the sense-amplifier. When using a set-up similar to the one from Figure 4, it is sufficient to omit the resistors R1 and R2 (e.g., choose R1 = 0 and R2 = 0) since the bitlines become floating during the evaluation phase.

It is also recommended that the bitlines be precharged during the self-calibration phase, for example to halfway between the power supply levels SP and SN. Precharging when using the set-up from Figure 6 is recommended up to a voltage a few times 10 mV (up to a maximally a few hundred mV) higher than the voltage which would be present at the bitlines (Bit and BitN) reached in steady state during self calibration situation. This precharging should take place before or at the start of the calibration phase. A person skilled in the art of sense amplifiers can easily include presetting transistors and their driving cock signal.

Figure 6 is an extension of the present invention whereby two transistors M7 and M8 are added to the self-calibration and self-regenerative stages to enhance speed. Transistors M7 and M8 act as cascode transistors. In addition to switching nodes 3 and 4, two extra switching nodes 51 and 52 are now included. During self-regeneration, nodes 3 and 4 have a relatively low voltage change, whereas nodes 51 and 52 show a larger voltage difference. The designer can decide whether to use this type of set-up in a

particular application. A somewhat higher speed can be obtained, during self-calibration and/or self-regeneration but an extra biasing voltage Vbias and extra transistors M7 and M8 are also required. When having a power supply of only 1.5 V not much (voltage) room is left for this cascoding stage, making the design more critical.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a first transistor having a current path and a control terminal, the current path being coupled between a first supply voltage node and a first switching node;

a second transistor having a current path and a control terminal, the current path being coupled between the first supply voltage node and a second switching node;

a third transistor having a current path and a control terminal, the current path being coupled between a second supply voltage node and the first switching node, the control terminal being coupled to the second switching node;

a fourth transistor having a current path and a control terminal, the current path being coupled between the second supply voltage node and the second switching node, the control terminal being coupled to the first switching node;

a fifth transistor having a current path and a control terminal, the current path being coupled between the first switching node and the control terminal of the first transistor; and

a sixth transistor having a current path and a control terminal, the current path being coupled between the second switching node and control terminal of the second transistor, the control terminal of the sixth transistor being coupled to the control terminal of the fifth transistor.

2. The circuit of claim 1 wherein the first and second transistors comprise n-channel MOS transistors and wherein the third and fourth transistors comprise p-channel MOS transistors.

3. The circuit of claim 2 wherein the fifth and sixth transistors comprise n-channel MOS transistors.

4. The circuit of claim 1 wherein the first and second supply voltage nodes are each biased with a constant supply voltage, the constant supply voltage at the first supply voltage node being different than the constant supply voltage at the second supply voltage node.

5. The circuit of claim 1 and further comprising:

a first capacitor having a first plate coupled to the control terminal of the first transistor; and

a second capacitor having a first plate coupled to the control terminal of the second transistor.

6. The circuit of claim 5 and further comprising a first switch with a current path coupled between a second plate of the first capacitor and a second plate of the second capacitor.

7. The circuit of claim 6 and further comprising:

a second switch with a current path coupled between a first node and the second plate of the first capacitor; and

a third switch with a current path coupled between a second node and the second plate of the second capacitor.

8. The circuit of claim 6 and further comprising:

a first resistor with a current path coupled between a first node and the second plate of the first capacitor; and

a second resistor with a current path coupled between a second node and the second plate of the second capacitor.

9. The circuit of claim 1 and further comprising:

a first cascode transistor coupled to the control terminal of the first transistor; and

a second cascode transistor coupled to the control terminal of the second transistor.

10. The circuit of claim 9 and further comprising first and second current sources wherein the first cascode transistor has a current path coupled between the control terminal of the first transistor and the first current source, and the second cascode transistor has a current path coupled between the control terminal of the second transistor and the second current source.

11. The circuit of claim 1 and further comprising:

a first cascode transistor coupled between the first switching node and the first transistor; and

a second cascode transistor coupled between the second switching node and the second transistor.

12. A method of comparing a voltage at a first node with a voltage at a second node, the method comprising:

providing first and second output nodes;

calibrating the first and second output nodes such that the first output node reaches a first real equilibrium voltage and the second output node reaches a second real equilibrium voltage, the first real equilibrium voltage not necessarily being equal to the second real equilibrium voltage;

amplifying a voltage difference between a voltage at the first node and a voltage at the second node by causing the voltage at the first output node to become higher than the voltage at the second output node when the voltage and the first node is higher than the voltage at the second node and causing the voltage at the first output node to become lower than the voltage at the second output node when the voltage and the first node is lower than the voltage at the second node.

13. The method of claim 12 wherein the first real equilibrium voltage is higher than the second real equilibrium voltage and wherein the voltage at the first node is lower than the voltage at the second node, and wherein the amplifying step comprises causing the voltage at the first output node to become lower than the voltage at the second output node.

14. The method of claim 12 wherein the first real equilibrium voltage is higher than the second real equilibrium voltage and wherein the voltage at the first node is higher than the voltage at the second node, and wherein the amplifying step comprises causing

the voltage at the first output node to become higher than the voltage at the second output node.

15. A memory device comprising:

a plurality of memory cells disposed in rows and columns;

a plurality of sense amplifiers, each sense amplifier coupled to at least one corresponding column of memory cells, each sense amplifier comprising:

a first transistor having a current path and a control terminal, the current path being coupled between a first supply voltage node and a first switching node;

a second transistor having a current path and a control terminal, the current path being coupled between the first supply voltage node and a second switching node;

a third transistor having a current path and a control terminal, the current path being coupled between a second supply voltage node and the first switching node, the control terminal being coupled to the second switching node;

a fourth transistor having a current path and a control terminal, the current path being coupled between the second supply voltage node and the second switching node, the control terminal being coupled to the first switching node;

a fifth transistor having a current path and a control terminal, the current path being coupled between the first switching node and the control terminal of the first transistor; and

a sixth transistor having a current path and a control terminal, the current path being coupled between the second switching node and control terminal of the second transistor, the control terminal of the sixth transistor being coupled to the control terminal of the fifth transistor.

16. The device of claim 15 wherein the memory cells each comprise a capacitor coupled in series with a pass transistor.

17. The device of claim 15 wherein the memory cells each comprise a non-volatile memory cell.

18. The device of claim 15 wherein the memory cells comprise SRAM cells.

19. The device of claim 15 wherein the sense amplifier further comprises:

a first cascode transistor coupled to the control terminal of the first transistor; and

a second cascode transistor coupled to the control terminal of the second transistor.

20. The device of claim 19 and further comprising first and second current sources wherein the first cascode transistor has a current path coupled between the control terminal of the first transistor and the first current source, and the second cascode transistor has a current path coupled between the control terminal of the second transistor and the second current source.

21. The device of claim 15 wherein each sense amplifier further comprises:

a first capacitor having a first plate coupled to the control terminal of the first transistor;

a second capacitor having a first plate coupled to the control terminal of the second transistor; and

a first switch with a current path coupled between a second plate of the first capacitor and a second plate of the second capacitor.

22. The circuit of claim 21 and further comprising:

a second switch with a current path coupled between a first node and the second plate of the first capacitor; and

a third switch with a current path coupled between a second node and the second plate of the second capacitor.

23. The circuit of claim 21 and further comprising:

a first resistor with a current path coupled between a first node and the second plate of the first capacitor; and

a second resistor with a current path coupled between a second node and the second plate of the second capacitor.

FIG. 1

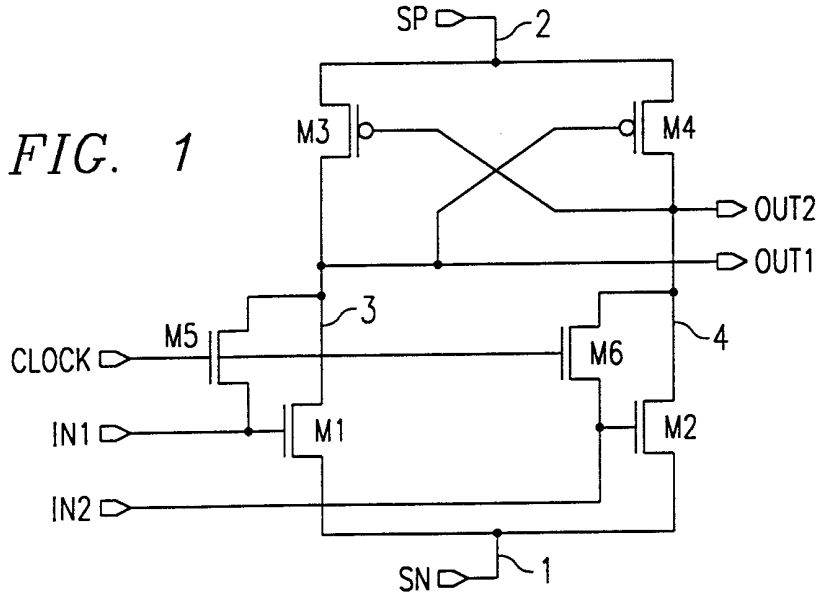
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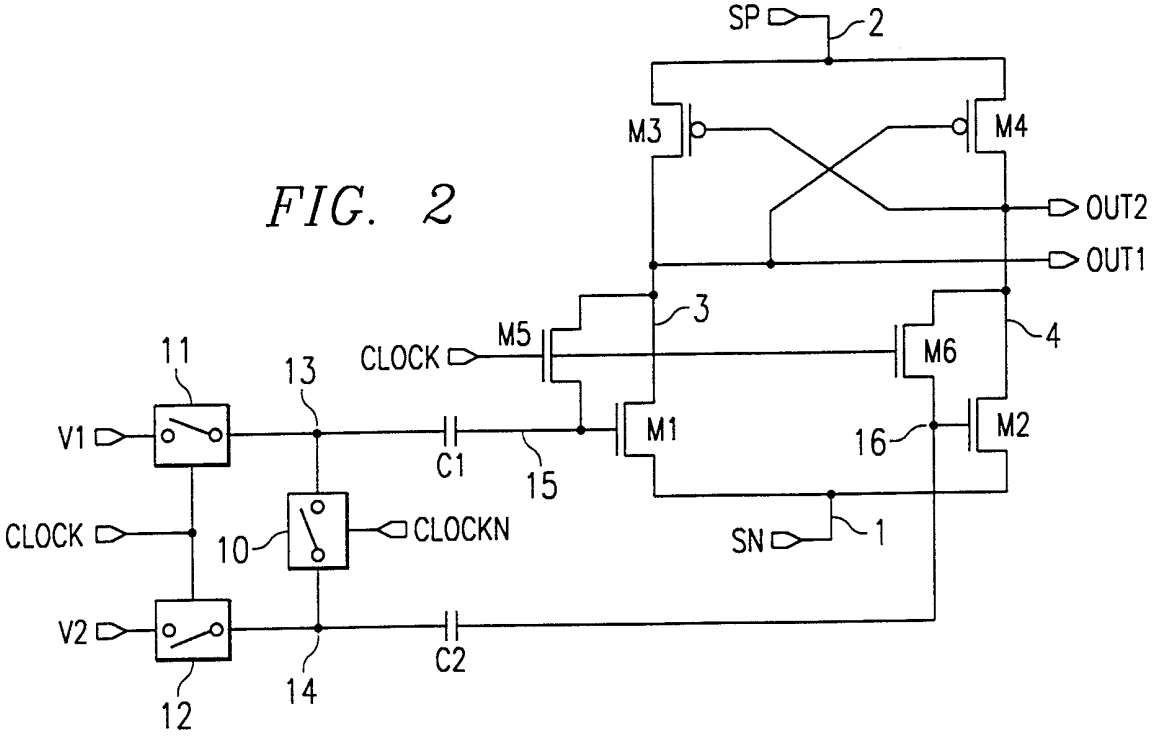
FIG. 2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OUT1
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M5
CLOCK
M6
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M1
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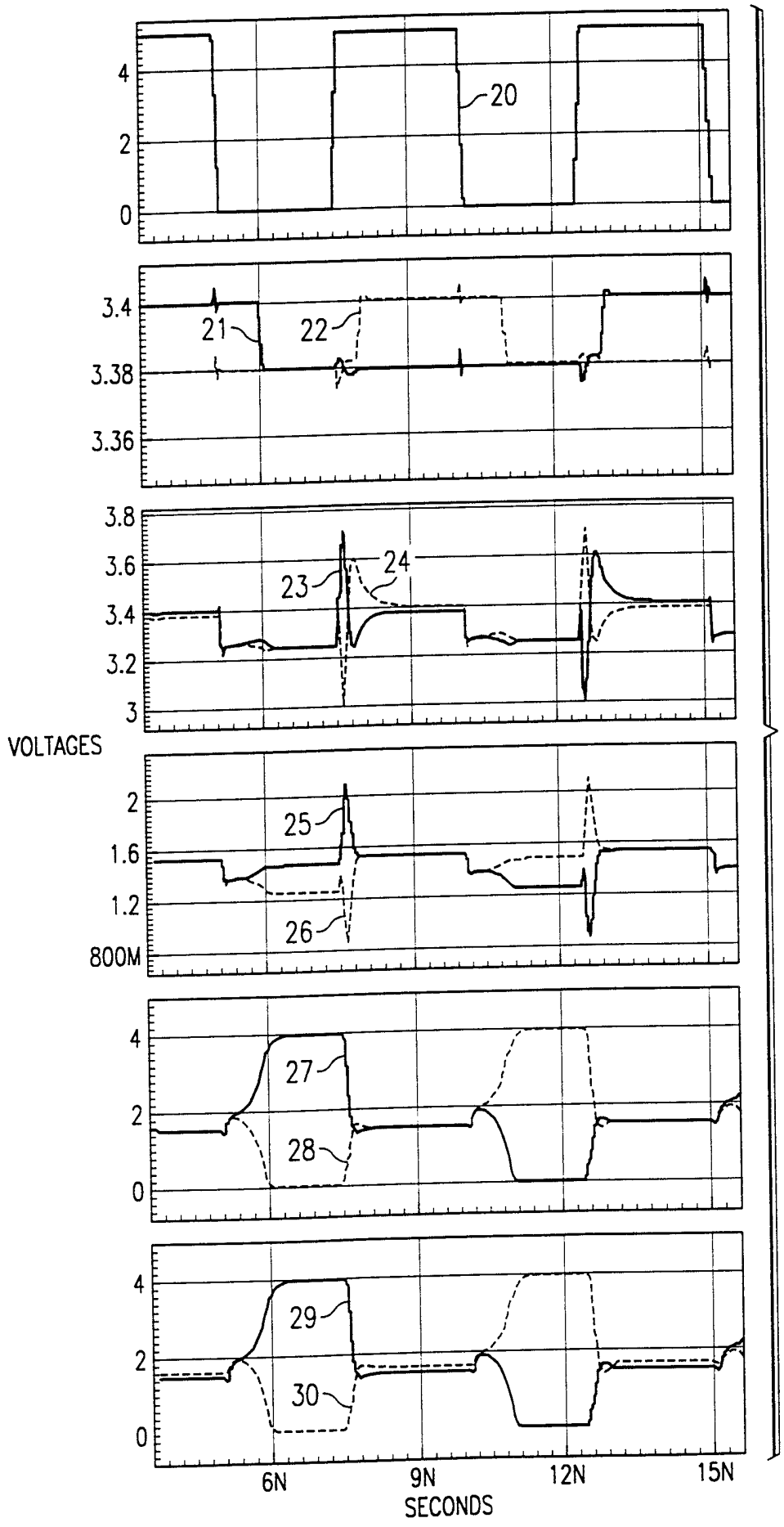
15
CLOCK
10
CLOCKN
SN
1
V2
C2
12
14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3
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1.2
800M
25
26
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30
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9N
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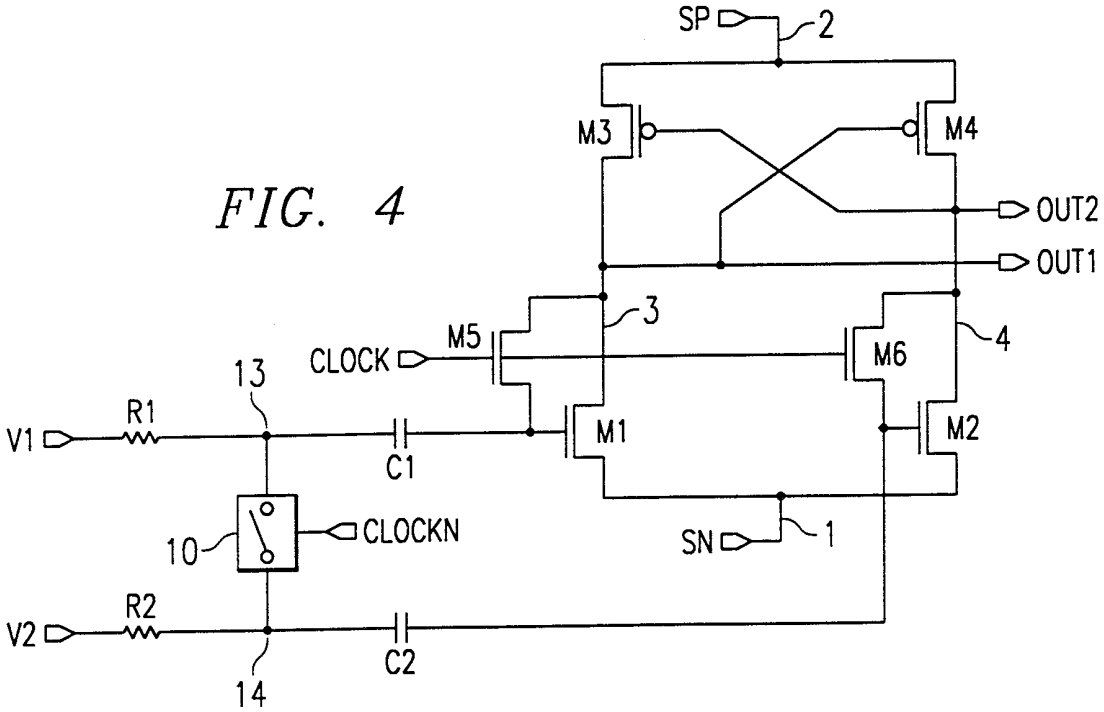
15N
SECONDS

FIG. 3

FIG. 4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M3
M4
OUT2
OUT1
3
M5
CLOCK
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V1
C1
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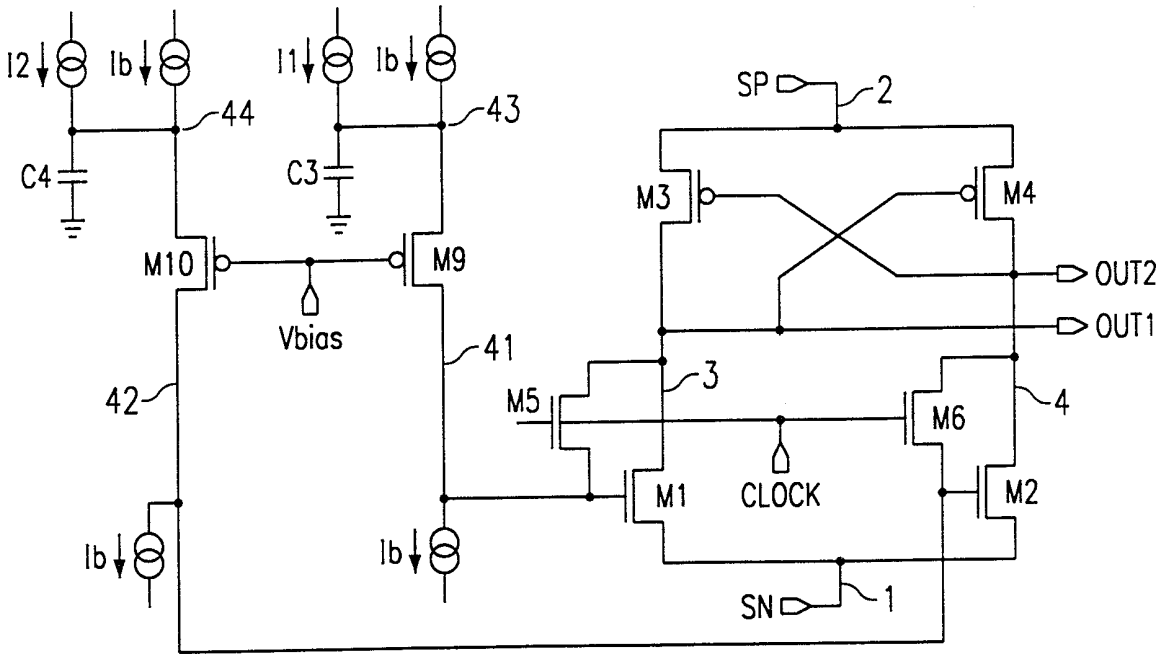
M2
10
CLOCKN
SN
1
R2
V2
C2
14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Ib
I1
Ib
44
43
SP
2
C4
C3
M3
M4
M10
M9
OUT2
OUT1
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M6
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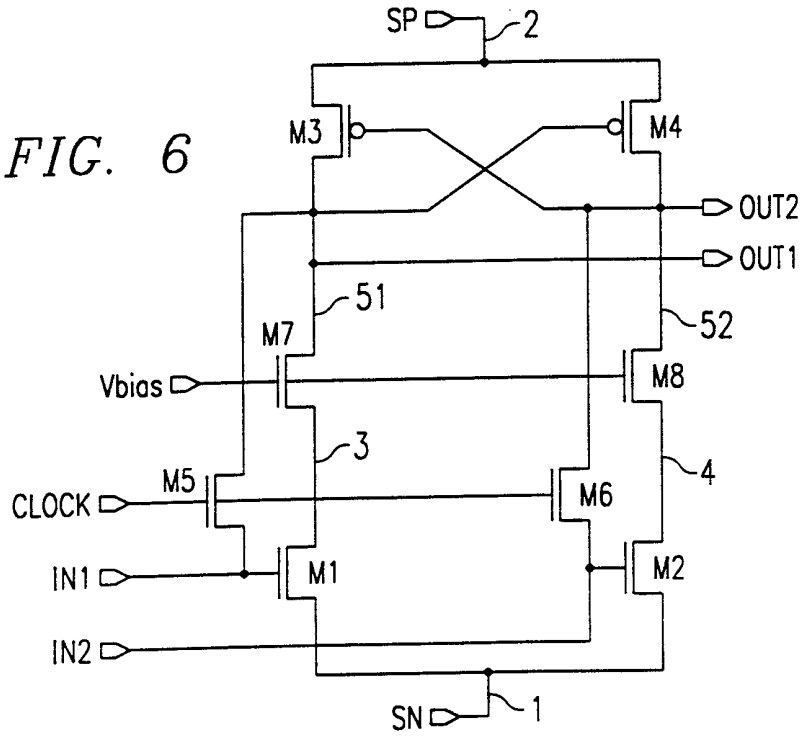
M1
CLOCK
M2
Ib
Ib
SN
1

FIG. 5

FIG. 6



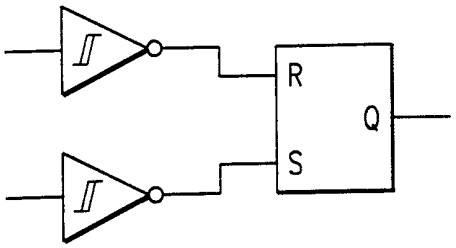


FIG. 7

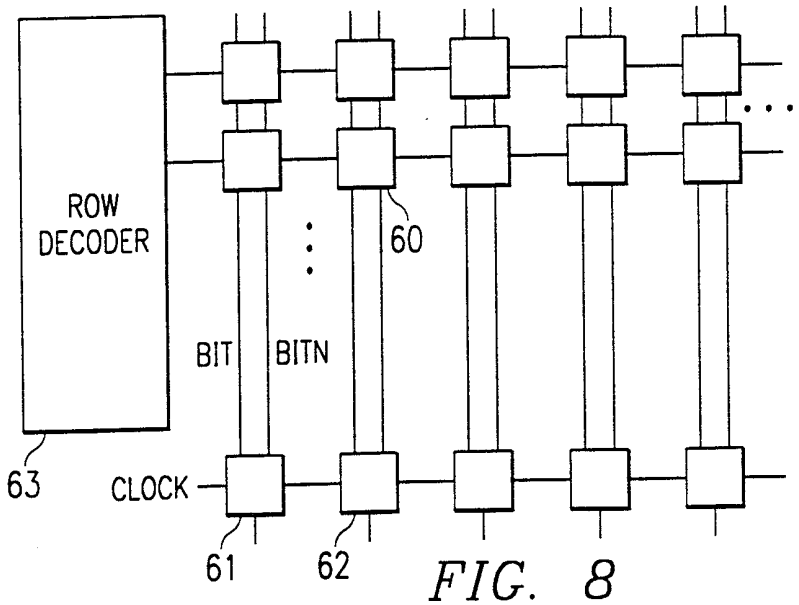


FIG. 8

INTERNATIONAL SEARCH REPORT

Ii ıational Application No
PCT/US 99/03795

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C7/06 H03K3/356

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WATANABE Y ET AL: "OFFSET COMPENSATING BIT-LINE SINSING SCHEME FOR HIGH DENSITY DRAM'S" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 29, no. 1, 1 January 1994 (1994-01-01), pages 9-13, XP000441632 ISSN: 0018-9200 figure 7 ---	1
A	US 5 457 657 A (SUH JEUNG W) 10 October 1995 (1995-10-10) figure 3 ---	1-3
A	US 5 698 998 A (BODENSTAB PAUL R) 16 December 1997 (1997-12-16) -----	1,12,15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 September 1999	14/09/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Czarik, D

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/03795

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5457657 A	10-10-1995	JP 7153270 A	16-06-1995
US 5698998 A	16-12-1997	NONE	