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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventor; and

(71) Applicant: **PENMECHA, Bharat P.** [IN/US]; 5000 W Chandler Blvd., CH-5 -157, Chandler, Arizona 85226 (US).

(72) Inventors: **DUBEY, Manish**; 3662 E Mead Dr, Chandler, Arizona 85249 (US). **DIAS, Rajendra C.**; 14230 South 14th street, Phoenix, Arizona 85048 (US). **BICEN, Baris**; 4693 W. Tara Dr., Chandler, Arizona 85226 (US). **RAORANE, Digvijay**; 875 West pecos road, # 2034, Chandler, Arizona 85225 (US).

(74) Agents: **PERDOK, Monique M.** et al.; Schwegman Lundberg & Woessner, P.A., c/o CPA Global, 900 Second Avenue South, Suite 600, Minneapolis, Minnesota 55402 (US).

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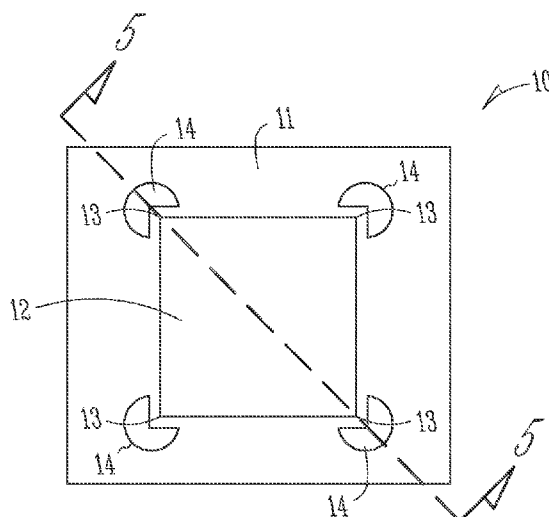


Fig. 2

(57) Abstract: Some example forms relate to an electronic package. The electronic package includes a substrate and a die attached to the substrate. A plurality of supports attached to the substrate adjacent to the die. At least one support in the plurality of supports is positioned adjacent to at least one corner of the die such that the at least one corner of the die is positioned adjacent to the at least one support. Other example forms relate to a method of fabricating an electronic package. The method includes securing a die to a substrate and securing a plurality of supports to the substrate such that at least one support is adjacent to at least one corner of the die.



ELECTRONIC PACKAGE WITH CORNER SUPPORTS

5 **Background**

[0001] Minimizing transistor size in order to keep up with Moore's law continually requires reducing first level interconnect (FLI) pitch and bump size. In addition, using advanced dielectrics has often resulted in utilizing low-k and extremely low-k materials in silicon.

10 **[0002]** The combination of these factors results in higher sensitivity to stress during assembly and thermo-mechanical stress. Therefore, with each new technological advancement, solutions for reducing thermo-mechanical stress become significantly more important.

[0003] With the advent of smaller form factor devices (cellphones, tablets) and their short life expectancy, the reliability requirements for such semiconductor packages has reduced. However, high performance large packages still require good reliability performance because such devices typically have an estimated end life of 5-7 years.

[0004] Reliability related fails for large die products, especially due to wide area inter layer dielectric (ILD) delamination and fillet cracks, have increased due to the use of low-k and ultra-low-k ILD materials. Current server products barely meet existing reliability requirements. In addition, many users of large electronic packages require strong reliability performance, especially in harsher physical environments.

25 **[0005]** FIG. 1 shows ILD delamination 1 that is commonly observed in large die electronic packages 2. This type of ILD delamination 1 in such electronic packages 2 typically occurs due to the stresses that are associated with temperature cycling (TC).

[0006] As shown in FIG. 1, this type of ILD delamination 1 is a well-known reliability fail mechanism that initiates from one of the corners 3 of the electronic package 2. The conventional solution to prevent such fails is by improving the properties of the underfill material. However, improving the

mechanical properties of the underfill comes with compromises on other desirable properties (e.g. flowability and/or cost).

5 [0007] FIG. 1 shows that as the electronic package 2 gets larger, the corners 3 of the electronic package 2 have the highest distance to neutral point DNP, which results in the highest stress being at the corners 3 of the electronic package 2. Therefore, a need exists for a relatively large electronic package that has good reliability performance under a variety of thermal cycling conditions due to reducing the stress on the corners of the relatively large electronic package.

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Brief Description of the Drawings

[0008] FIG. 1 shows ILD delamination that is commonly observed in conventional large die electronic packages.

[0009] FIG. 2 shows a top view of an example electronic package.

15 [0010] FIG. 3 shows a top view of the example electronic package shown in FIG. 2 with different supports.

[0011] FIG. 4 shows a top view of the example electronic package shown in FIG. 2 with different supports.

20 [0012] FIG. 5 shows a schematic cross-sectional view of the example electronic package shown in FIGS. 2-4 taken along line 5-5.

[0013] FIG. 6 shows a top view of another example electronic package.

[0014] FIG. 7 is a flow diagram illustrating an example method of forming an electronic package.

25 [0015] FIG. 8 is a flow diagram illustrating another example method of forming an electronic package.

[0016] FIG. 9 is a block diagram of an electronic apparatus that includes the electronic packages and/or the methods described herein.

Description of Embodiments

30 [0017] The following description and the drawings sufficiently illustrate specific embodiments to enable those skilled in the art to practice them. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Portions and features of some embodiments may be included in, or

substituted for, those of other embodiments. Embodiments set forth in the claims encompass all available equivalents of those claims.

[0018] Orientation terminology, such as “horizontal,” as used in this application is defined with respect to a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term “vertical” refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as “on,” “side” (as in “sidewall”), “higher,” “lower,” “over,” and “under” are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate.

[0019] The electronic packages and methods described herein may address the need for a relatively large electronic package that has good reliability performance under a variety of thermal cycling conditions due to reducing the stress on the corners of the relatively large electronic package. The basic principle is based on addressing the coefficient of thermal expansion mismatch between the die and substrate and their geometries at different temperatures. The proposed solution adds supports at the corners of the die thereby reducing the stress on the die corners.

[0020] FIG. 2 shows a top view of an example electronic package 10. FIG. 3 shows a top view of the example electronic package 10 shown in FIG. 2 with different supports 14. FIG. 4 shows a top view of the example electronic package 10 shown in FIG. 2 with different supports 14. FIG. 5 shows a schematic cross-sectional view of the example electronic package 10 shown in FIGS. 2-4 taken along line 5-5.

[0021] The example electronic package 10 includes a substrate 11 and a die 12 attached to the substrate 11. A plurality of supports 14 is attached to the substrate 11 adjacent to the die 12. At least one support 14 in the plurality of supports 14 is positioned adjacent to at least one corner 13 of the die 12 such that the at least one corner 13 of the die 12 is positioned adjacent to the at least one support 14.

[0022] The addition of a support 14 next to the die 12 corner 13 may reduce the stress on the die 12 corner 13 at high temperatures. FIGS. 2-4 illustrate different types of example supports 14. It should be noted that other types of supports 14 are contemplated and the size and type of support 14 that is

utilized in the electronic package 10 will depend in part on (i) the size and type of die 12; (ii) the size and type of substrate 11; and/or (iii) the size and type of other components on the substrate 11 (among other factors).

[0023] In addition, the supports 14 may be positioned adjacent to one, some or all of the corners 13 of the die 12 in order to reduce stress at the appropriate corners 13 of the die 12. The supports 14 may also all be the same, partially the same, or each support 14 may be different in order to reduce stress at the appropriate corners 13 of the die 12. As shown in FIG. 6, there may also be more than support 14 at one, some, or all of the corners 13 of the die 12.

[0024] The supports 14 may be made of material(s) that are optimized to get the best stress reduction at the appropriate corners 13 of the die 12. In some forms, the material may have a lower CTE (e.g., lower than silicon) to obtain the best performance. The supports 14 may be secured to the substrate 11 with an adhesive or may be soldered to the substrate 11. Other ways of fabricating the supports 14 onto the substrate 11 are contemplated.

[0025] The example electronic package 10 may further include an underfill 15 between the die 12 and the substrate 11. As an example, the underfill 15 may be the same type of underfill between the die 12 and the substrate 11. The supports 14 may be present on the substrate 11 before or after the die 12 is attached to the substrate 11, and before or after the underfill 15 is placed between the die 12 and the substrate 11.

[0026] The electronic packages described herein may reduce stress-related bump cracks and fillet cracks near the corners 13 of the die 12. In addition, reducing these types stress-related bump cracks and fillet cracks may inhibit solder migration in order to improve electronic package reliability (i.e., minimize electrical failures).

[0027] FIG. 7 is a flow diagram illustrating an example method [700] of forming an electronic package 10. The method [700] includes [710] securing a die 12 to a substrate 11 and [720] securing a plurality of supports 14 to the substrate 11 such that at least one support 14 is adjacent to at least one corner 13 of the die 12. One, some or all of the corners 13 of the die 12 may be positioned adjacent to one support 14 (see FIGS. 2-4) or multiple supports 14 (see FIG. 6).

[0028] In some forms, [710] securing a die 12 to a substrate 11 may include adhering the die 12 to the substrate 11 or soldering the die 12 to the

substrate 11. Other forms of attaching the die 12 to the substrate 11 are contemplated.

[0029] In addition, [720] securing a plurality of supports 14 to the substrate 11 may include attaching (e.g., by adhering or soldering) the plurality of supports 14 to the substrate 11. Other forms of attaching the supports 14 to the substrate 11 are contemplated.

[0030] [720] Securing a plurality of supports 14 to the substrate 11 may additionally, or alternatively, include forming the plurality of supports 14 on the substrate 11 (e.g., by etching). Other forms of forming the supports 14 on the substrate 11 are contemplated.

[0031] The method [700] may further include [730] inserting an underfill 15 (see FIG. 5) between the die 12 and the substrate 11. In some forms, the underfill 15 may be inserted before the die 12 is placed on the substrate 11. The manner in which the underfill 15 is inserted between the die 12 and the substrate 11 will depend in part on the size and type of die 12 and substrate 11 as well the type of underfill 15 (among other factors).

[0032] FIG. 8 is a flow diagram illustrating another example method [800] of forming an electronic package 10. The method [800] includes [810] forming a plurality of supports 14 on a substrate 11 and [820] attaching a die 12 to the substrate 11 (as described above) such that at least one support 14 is adjacent to at least one corner 13 of the die 12. One, some or all of the corners 13 of the die 12 may be positioned adjacent to one support 14 (see FIGS. 2-4) or multiple supports 14 (see FIG. 6).

[0033] In some forms, [810] forming the plurality of supports 14 on the substrate 11 may include forming each of the plurality of supports 14 (individually or collectively) into a shape that reduces stress on the corners 13 of the die 12 during operation of the die 12. The supports 14 may also all formed the same, partially the same, or each support 14 may be different in order to reduce stress at the appropriate corners 13 of the die 12.

[0034] The method [800] may further include [830] inserting an underfill 15 (see FIG. 5) between the die 12 and the substrate 11. The manner in which the underfill 15 is inserted between the die 12 and the substrate 11 will depend in part on the size and type of die 12 and substrate 11 as well the type of underfill 15 (among other factors).

[0035] The electronic packages 10 and methods [700], [800] described herein may greatly enhance the reliability performance of large die electronic packages. The electronic packages 10 and methods [700], [800] described herein may add supports 14 at the appropriate corners 13 of the die 12 thereby
5 reducing the stress on the die 12 corners 13.

[0036] FIG. 9 is a block diagram of an electronic apparatus 900 incorporating at least one electronic package 10 and/or method [700], [800] described herein. Electronic apparatus 900 is merely one example of an electronic apparatus in which forms of the electronic packages 10 and/or
10 methods [700], [800] described herein] may be used.

[0037] Examples of an electronic apparatus 900 include, but are not limited to, personal computers, tablet computers, mobile telephones, game devices, MP3 or other digital music players, etc. In this example, electronic apparatus 900 comprises a data processing system that includes a system bus 902
15 to couple the various components of the electronic apparatus 900. System bus 902 provides communications links among the various components of the electronic apparatus 900 and may be implemented as a single bus, as a combination of busses, or in any other suitable manner.

[0038] An electronic assembly 910 that includes any of the electronic
20 packages 10 and/or methods [700], [800] described herein as describe herein may be coupled to system bus 902. The electronic assembly 910 may include any circuit or combination of circuits. In one embodiment, the electronic assembly 910 includes a processor 912 which can be of any type. As used herein, “processor” means any type of computational circuit, such as but not
25 limited to a microprocessor, a microcontroller, a complex instruction set computing (CISC) microprocessor, a reduced instruction set computing (RISC) microprocessor, a very long instruction word (VLIW) microprocessor, a graphics processor, a digital signal processor (DSP), multiple core processor, or any other type of processor or processing circuit.

[0039] Other types of circuits that may be included in electronic
30 assembly 910 are a custom circuit, an application-specific integrated circuit (ASIC), or the like, such as, for example, one or more circuits (such as a communications circuit 914) for use in wireless devices like mobile telephones,

tablet computers, laptop computers, two-way radios, and similar electronic systems. The IC can perform any other type of function.

[0040] The electronic apparatus 900 may also include an external memory 920, which in turn may include one or more memory elements suitable to the particular application, such as a main memory 922 in the form of random access memory (RAM), one or more hard drives 924, and/or one or more drives that handle removable media 926 such as compact disks (CD), flash memory cards, digital video disk (DVD), and the like.

[0041] The electronic apparatus 900 may also include a display device 916, one or more speakers 918, and a keyboard and/or controller 930, which can include a mouse, trackball, touch screen, voice-recognition device, or any other device that permits a system user to input information into and receive information from the electronic apparatus 900.

[0042] To better illustrate the method and apparatuses disclosed herein, a non-limiting list of embodiments is provided herein:

[0043] Example 1 includes an electronic package. The electronic package includes a substrate and a die attached to the substrate. A plurality of supports attached to the substrate adjacent to the die. At least one support in the plurality of supports is positioned adjacent to at least one corner of the die such that the at least one corner of the die is positioned adjacent to the at least one support.

[0044] Example 2 includes the electronic package of example 1, wherein each corner of the die is positioned adjacent to one support.

[0045] Example 3 includes the electronic package of any one of examples 1-2, wherein each corner of the die is positioned adjacent to at least one support.

[0046] Example 4 includes the electronic package of any one of examples 1-3, wherein each support is secured to the substrate with an adhesive.

[0047] Example 5 includes the electronic package of any one of examples 1-4, wherein each support is soldered to the substrate.

[0048] Example 6 includes the electronic package of any one of examples 1-5, wherein each support has a similar shape.

[0049] Example 7 includes the electronic package of any one of examples 1-6, wherein each support is formed of a single material.

[0050] Example 8 includes the electronic package of any one of examples 1-7, and further including an underfill between the die and the substrate.

5 **[0051]** Example 9 includes a method of fabricating an electronic package. The method includes securing a die to a substrate and securing a plurality of supports to the substrate such that at least one support is adjacent to at least one corner of the die.

[0052] Example 10 includes the method of example 9, wherein each corner of the die is positioned adjacent to one support.

10 **[0053]** Example 11 includes the method of any one of examples 9-10, wherein at least one corner of the die is positioned adjacent to a plurality of supports.

[0054] Example 12 includes the method of examples 9-11, wherein securing a die to a substrate includes adhering the die to the substrate.

15 **[0055]** Example 13 includes the method of any one of examples 9-12, wherein securing a die to a substrate includes soldering the die to the substrate.

[0056] Example 14 includes the method of any one of examples 9-13, wherein securing a plurality of supports to the substrate includes attaching the plurality of supports to the substrate.

20 **[0057]** Example 15 includes the method of any one of examples 9-14, wherein securing a plurality of supports to the substrate includes forming the plurality of supports on the substrate.

[0058] Example 16 includes the method of any one of examples 9-15, and further including inserting an underfill between the die and the substrate.

25 **[0059]** Example 17 includes a method of fabricating an electronic package. The method includes forming a plurality of supports on a substrate and attaching a die to the substrate such that at least one support is adjacent to at least one corner of the die.

[0060] Example 18 includes the method of example 17, wherein each corner of the die is positioned adjacent to one support.

30 **[0061]** Example 19 includes the method of any one of examples 17-18, wherein forming the plurality of supports on the substrate includes forming each of the plurality of supports into a shape that reduces stress on the corners of the die during operation of the die.

[0062] Example 20 includes the method of any one of examples 17-19, further comprising inserting an underfill between the die and the substrate.

[0063] This overview is intended to provide non-limiting examples of the present subject matter. It is not intended to provide an exclusive or
5 exhaustive explanation. The detailed description is included to provide further information about the electronic packages and methods.

[0064] The above detailed description includes references to the accompanying drawings, which form a part of the detailed description. The drawings show, by way of illustration, specific embodiments in which the
10 invention can be practiced. These embodiments are also referred to herein as “examples.” Such examples can include elements in addition to those shown or described. However, the present inventors also contemplate examples in which only those elements shown or described are provided. Moreover, the present inventors also contemplate examples using any combination or permutation of
15 those elements shown or described (or one or more aspects thereof), either with respect to a particular example (or one or more aspects thereof), or with respect to other examples (or one or more aspects thereof) shown or described herein.

[0065] In this document, the terms “a” or “an” are used, as is common in patent documents, to include one or more than one, independent of any other
20 instances or usages of “at least one” or “one or more.” In this document, the term “or” is used to refer to a nonexclusive or, such that “A or B” includes “A but not B,” “B but not A,” and “A and B,” unless otherwise indicated. In this document, the terms “including” and “in which” are used as the plain-English equivalents of the respective terms “comprising” and “wherein.” Also, in the
25 following claims, the terms “including” and “comprising” are open-ended, that is, a system, device, article, composition, formulation, or process that includes elements in addition to those listed after such a term in a claim are still deemed to fall within the scope of that claim. Moreover, in the following claims, the terms “first,” “second,” and “third,” etc. are used merely as labels, and are not
30 intended to impose numerical requirements on their objects.

[0066] The above description is intended to be illustrative, and not restrictive. For example, the above-described examples (or one or more aspects thereof) may be used in combination with each other. In addition, the order of the methods described herein may be in any order that permits fabrication of an

electrical interconnect and/or package that includes an electrical interconnect. Other embodiments can be used, such as by one of ordinary skill in the art upon reviewing the above description.

[0067] The Abstract is provided to allow the reader to quickly ascertain
5 the nature of the technical disclosure. It is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

[0068] Also, in the above Detailed Description, various features may be grouped together to streamline the disclosure. This should not be interpreted as intending that an unclaimed disclosed feature is essential to any claim. Rather,
10 inventive subject matter may lie in less than all features of a particular disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment, and it is contemplated that such embodiments can be combined with each other in various combinations or permutations. The scope of the
15 invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

Claims

1. An electronic package comprising:
a substrate;
5 a die attached to the substrate; and
a plurality of supports attached to the substrate adjacent to the die,
wherein at least one support in the plurality of supports is positioned adjacent to
at least one corner of the die.
- 10 2. The electronic package of claim 1, wherein each corner of the die is
positioned adjacent to one support.
3. The electronic package of claim 1, wherein each corner of the die is
positioned adjacent to at least one support.
- 15 4. The electronic package of claim 3, wherein each support is secured to the
substrate with an adhesive.
5. The electronic package of claim 3, wherein each support is soldered to
20 the substrate.
6. The electronic package of claim 3, wherein each support has a similar
shape.
- 25 7. The electronic package of claim 6, wherein each support is formed of a
single material.
8. The electronic package of claim 1, further comprising an underfill
between the die and the substrate.
- 30 9. A method of forming an electronic package comprising:
securing a die to a substrate; and
securing a plurality of supports to the substrate such that at least one
support is adjacent to at least one corner of the die.

10. The method of claim 9, wherein each corner of the die is positioned adjacent to one support.

5 11. The method of claim 9, wherein at least one corner of the die is positioned adjacent to a plurality of supports.

12. The method of claim 9, wherein securing a die to a substrate includes adhering the die to the substrate.

10

13. The method of claim 9, wherein securing a die to a substrate includes soldering the die to the substrate.

14. The method of claim 9, wherein securing a plurality of supports to the
15 substrate includes attaching the plurality of supports to the substrate.

15. The method of claim 9, wherein securing a plurality of supports to the substrate includes forming the plurality of supports on the substrate.

20 16. The method of claim 9, further comprising inserting an underfill between the die and the substrate.

17. A method of forming an electronic package comprising:
forming a plurality of supports on a substrate; and
25 attaching a die to the substrate such that at least one support is adjacent to at least one corner of the die.

18. The method of claim 17, wherein each corner of the die is positioned adjacent to one support.

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19. The method of claim 17, wherein forming the plurality of supports on the substrate includes forming each of the plurality of supports into a shape that reduces stress on the corners of the die during operation of the die.

20. The method of claim 17, further comprising inserting an underfill between the die and the substrate.

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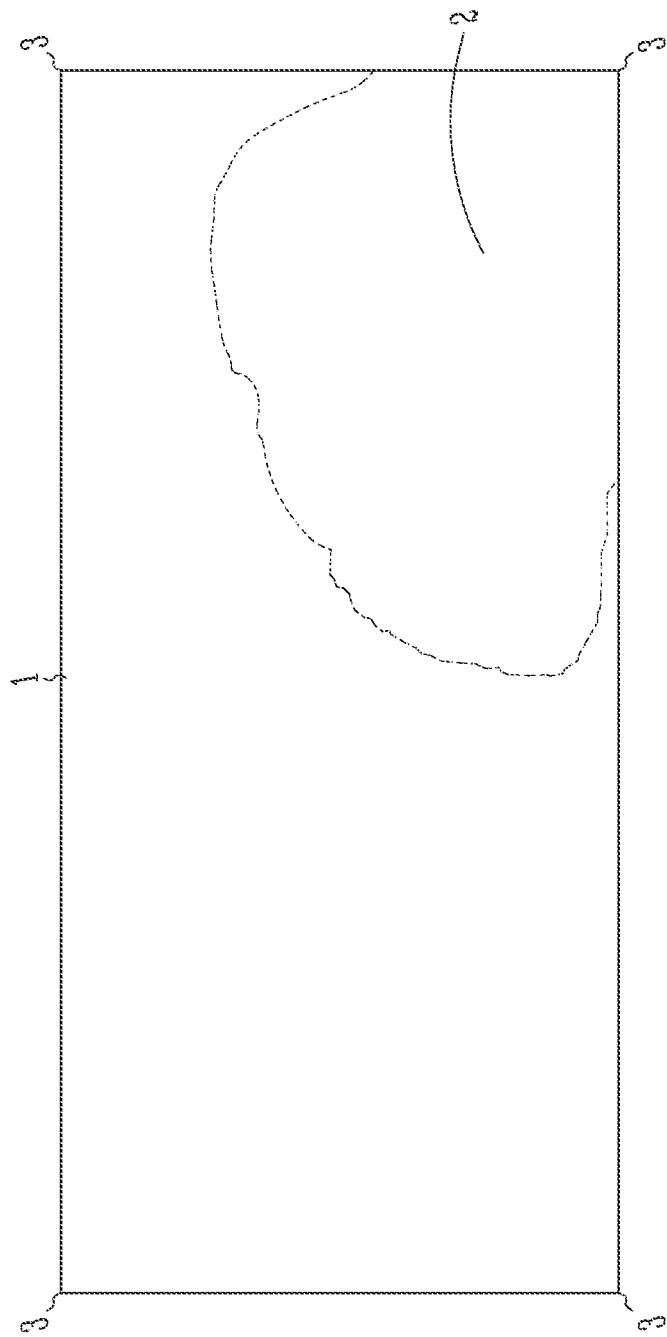


Fig. 1
(Prior Art)

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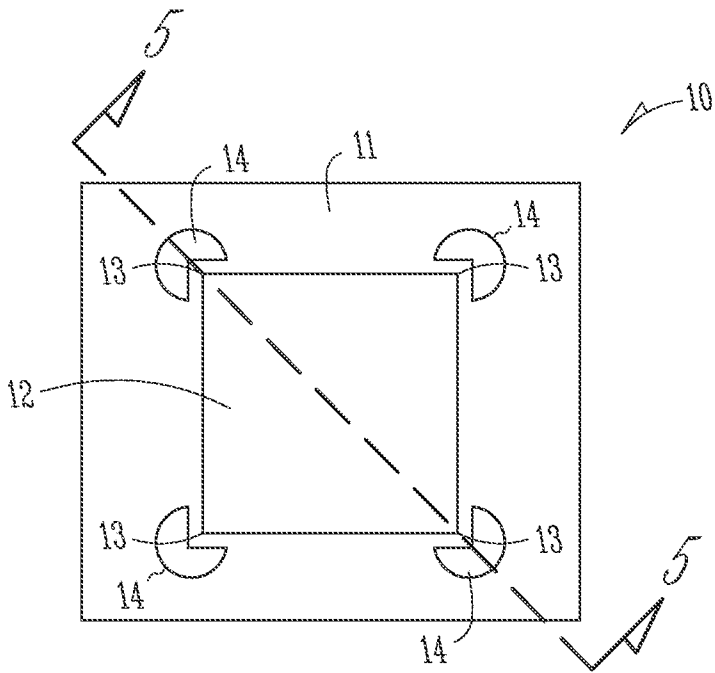


Fig. 2

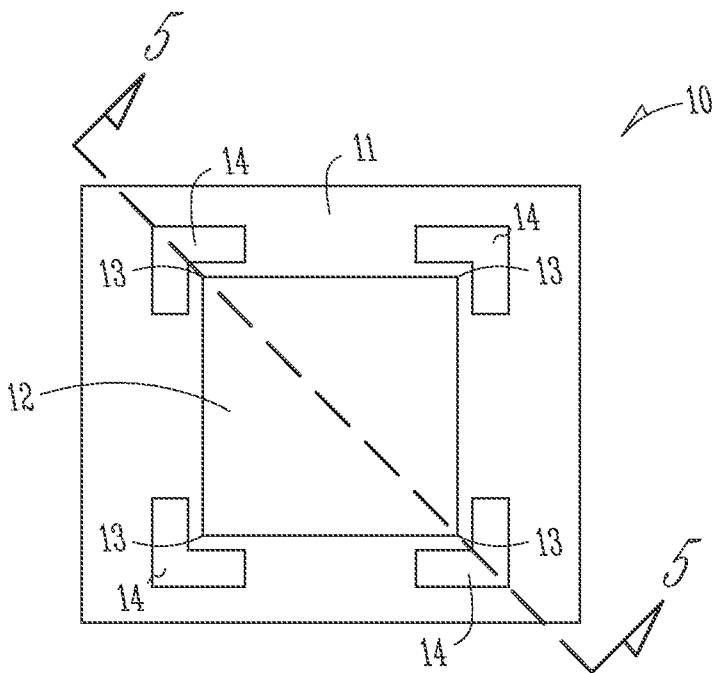


Fig. 3

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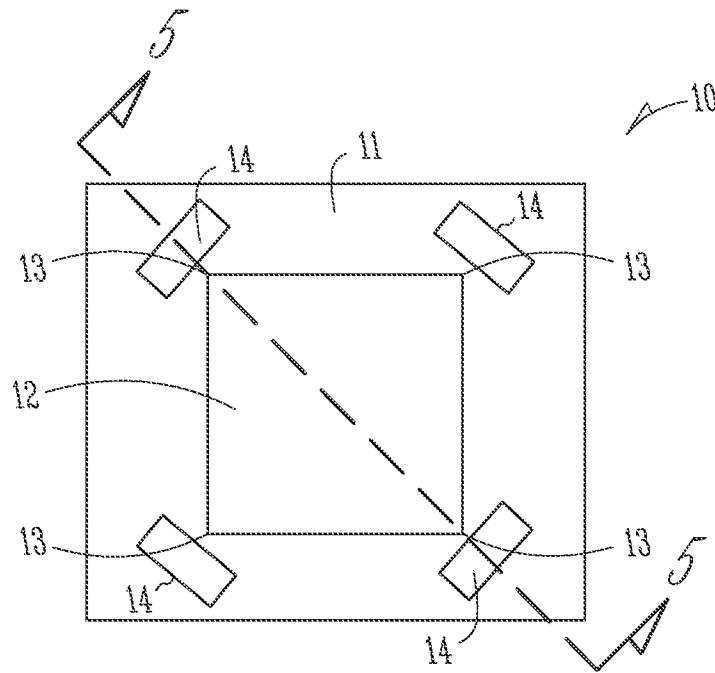


Fig. 4

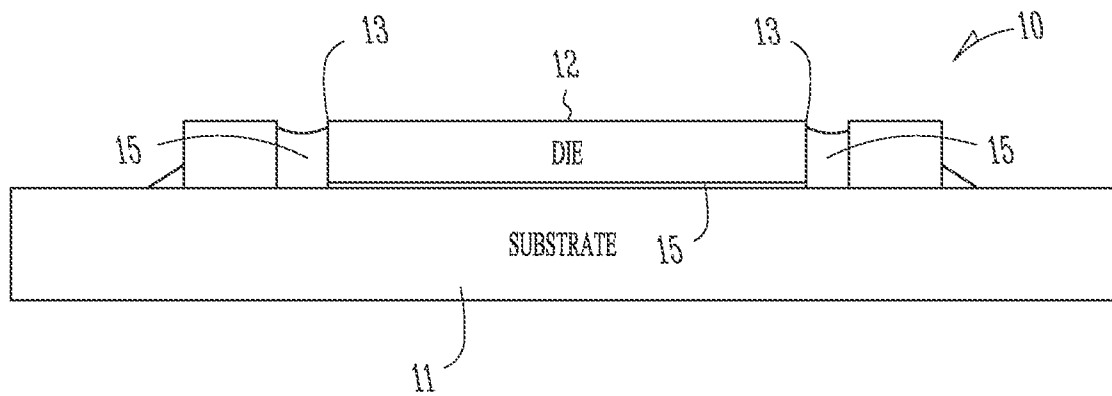


Fig. 5

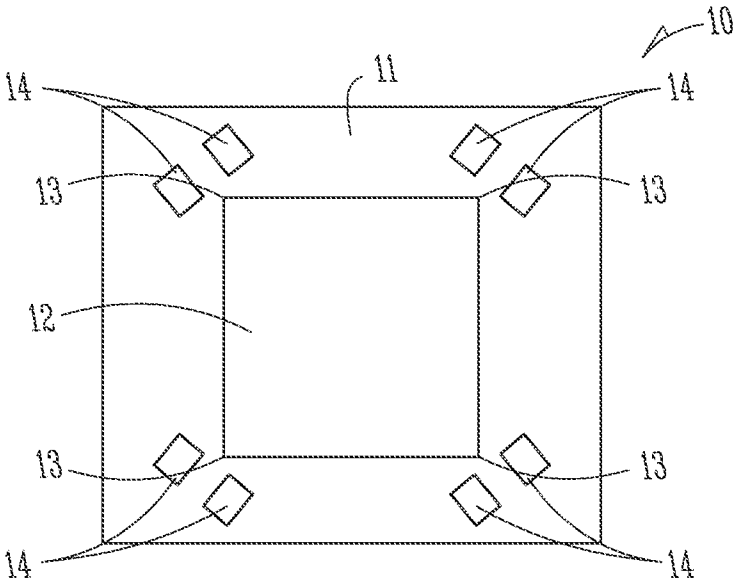
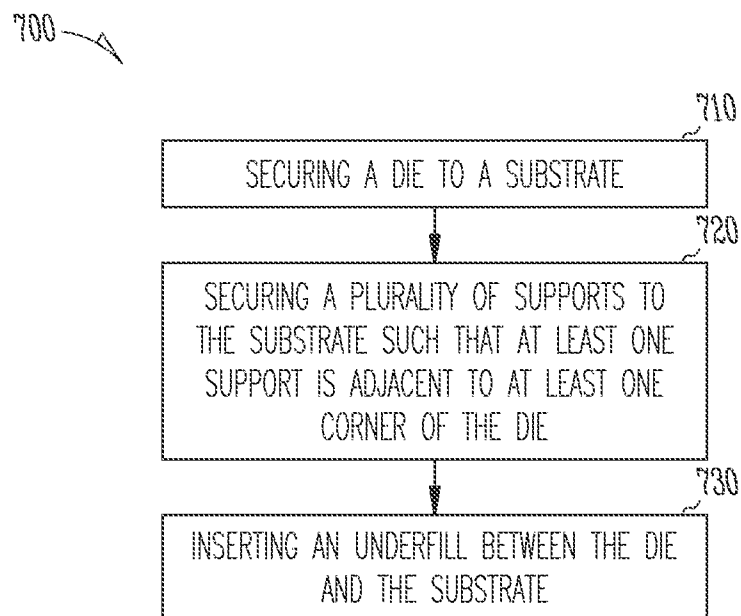
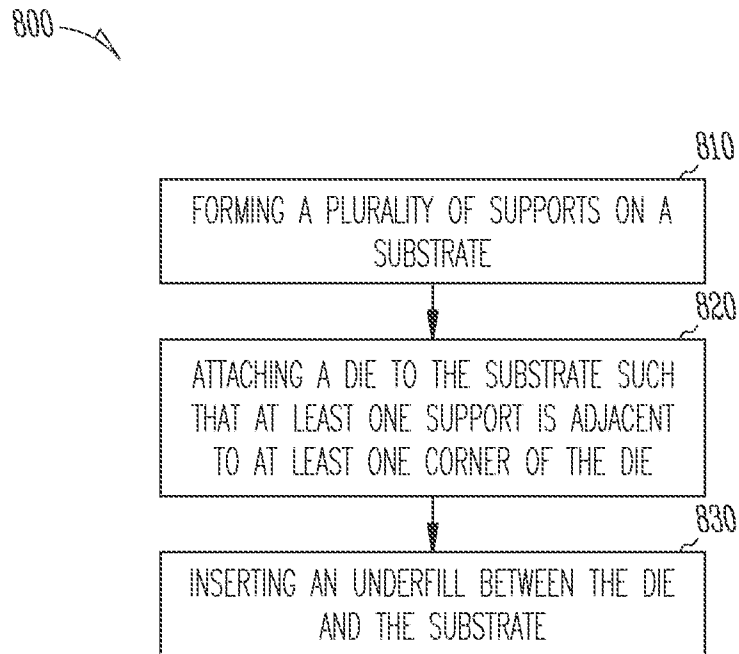


Fig. 6

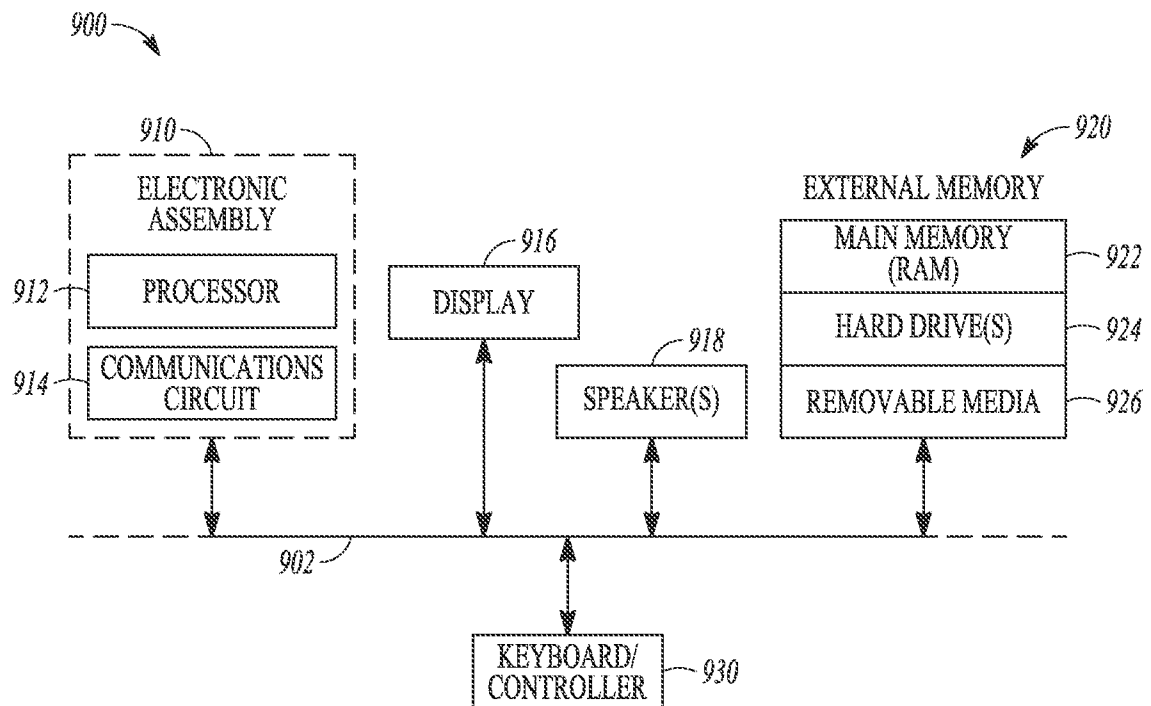
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*Fig. 7*

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*Fig. 8*

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*Fig. 9*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/043405**A. CLASSIFICATION OF SUBJECT MATTER****H01L 23/00(2006.01)i, H01L 21/56(2006.01)i, H01L 23/31(2006.01)i, H01L 23/488(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/00; H01L 21/768; H01L 21/56; H01L 21/46; H01L 23/48; H01L 21/44; H01L 23/31; H01L 23/488

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: substrate, die, pillar, corner, package

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009-0302427 A1 (MICHAEL SU et al.) 10 December 2009 See abstract, paragraphs [0022]-[0042] and figures 1-10.	1-20
A	US 2002-0068417 A1 (WARREN M. FARNWORTH et al.) 06 June 2002 See abstract, paragraphs [0055]-[0065] and figures 8-9.	1-20
A	US 2011-0147895 A1 (XUE BAI et al.) 23 June 2011 See abstract, paragraphs [0030]-[0035] and figure 5.	1-20
A	US 2004-0087061 A1 (QING MA et al.) 06 May 2004 See abstract, paragraph [0031] and figure 4.	1-20
A	US 2005-0200013 A1 (TONY H. HO) 15 September 2005 See abstract, paragraphs [0016]-[0021] and figures 3-4.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

20 October 2016 (20.10.2016)

Date of mailing of the international search report

20 October 2016 (20.10.2016)

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International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



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