

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
8 January 2009 (08.01.2009)

PCT

(10) International Publication Number
WO 2009/006263 A2

(51) International Patent Classification:
H01L 21/28 (2006.01)

[US/US]; 601 McCarthy Boulevard, Milpitas, CA 95035 (US).

(21) International Application Number:
PCT/US2008/068499

(74) Agent: **MAGEN, Burt**; Vierra Magen Marcus & DeNiro, LLP, Suite 2500, 575 Market Street, San Francisco, CA 94105 (US).

(22) International Filing Date: 27 June 2008 (27.06.2008)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/771,137 29 June 2007 (29.06.2007) US

(71) Applicant (for all designated States except US): **SAN-DISK 3D LLC** [US/US]; 601 McCarthy Boulevard, Milpitas, CA 95035 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **HSIA, Kang-Jay** [—/US]; 601 McCarthy Boulevard, Milpitas, CA 95035 (US). **LI, Calvin, K.** [US/US]; 601 McCarthy Boulevard, Milpitas, CA 95035 (US). **PETTI, Christopher, J.**

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

[Continued on next page]

(54) Title: FORMING COMPLIMENTARY METAL FEATURES USING CONFORMAL INSULATOR LAYER

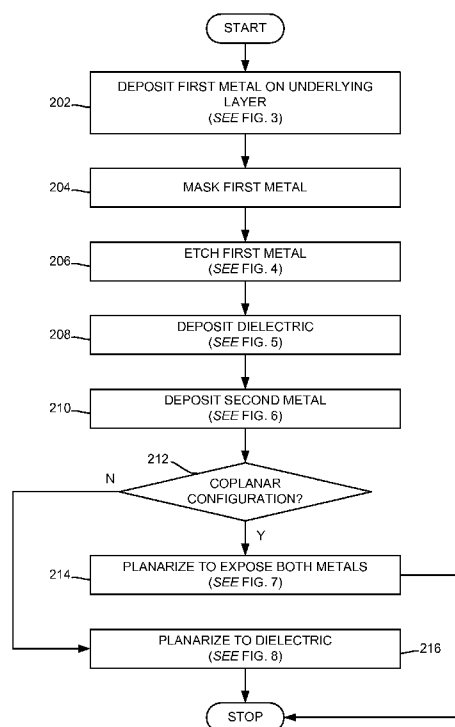


FIG. 2

(57) Abstract: A method is provided to form densely spaced metal lines. A first set of metal lines is formed by etching a first metal layer. A thin dielectric layer is conformally deposited on the first metal lines. A second metal is deposited on the thin dielectric layer, filling gaps between the first metal lines. The second metal layer is planarized to form second metal lines interposed between the first metal lines, coexposing the thin dielectric layer and the second metal layer at a substantially planar surface. In some embodiments, planarization continues to remove the thin dielectric covering tops of the first metal lines, coexposing the first metal lines and the second metal lines, separated by the thin dielectric layer, at a substantially planar surface.



FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL,
NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG,
CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *without international search report and to be republished
upon receipt of that report*

FORMING COMPLIMENTARY METAL FEATURES USING CONFORMAL INSULATOR LAYER

FIELD OF INVENTION

[001] The present invention relates to methods for forming metal features at a tight pitch using both subtractive and damascene methods. Complementary metal patterns may be formed by etching a metal layer, forming a conformal dielectric layer over the etched surface, and then depositing another metal layer.

BACKGROUND OF THE INVENTION

[002] Methods that increase feature density on semiconductor devices within a shrinking footprint are constantly evolving to meet demands for smaller, more powerful electronic devices. However, in some examples, practical considerations may limit how far those methods may evolve. For example, FIG. 1 is an illustrative cross-section of a prior art example of a metal pattern formed on an underlying layer in 45nm processes. As illustrated, in FIG. 1, metal 102 may be formed by well-known method into a pattern on an underlying layer 106. For example, metal 102 can be deposited and etched using standard photolithographic techniques. For clarity, only a portion of an example of the fine metal pattern is illustrated in cross-section. Metal patterns may form any number of features or connective lines. Insulator 104 may be provided to form a barrier between metal lines 108 and 110. Metal lines 108 and 110 may have a width 112 of approximately 45nm and insulator 104 may have a width 114 of approximately 45nm. As such, pitch 116 of the feature is approximately 90nm.

-2-

[003] In some conventional examples, in order to accommodate more densely arranged features, a decrease in pitch is generally required. With conventional methods of fabrication as described above, this would require moving to a more expensive means of fabrication. For example, a more expensive photolithography tool may be required. Thus, it would be desirable to develop methods that increase feature density without increasing the fabrication expense.

[004] Furthermore, as the line width decreases, metal volume of conducting lines also decreases, thus resulting in an increase in resistance of conductive lines. Thus, it may be desirable to develop methods which provide for increased feature density without a commensurate decrease in conductor linewidth. For example, to fit wider conductor lines in the same area, it would be desirable to minimize the width of gaps between them.

SUMMARY OF THE PREFERRED EMBODIMENTS

[005] The present invention is defined by the following claims, and nothing in this section should be taken as a limitation on those claims. In general, the invention is directed to a method to form very dense metal lines.

[006] A first aspect of the invention provides for a method for depositing at least two metal layers on a underlying layer comprising: depositing a first metal layer on the underlying layer; masking the first metal layer such that the first metal layer includes a first masked portion and a first unmasked portion; and etching the first metal layer such that the first unmasked portion is removed to the underlying layer; depositing a first intermediate layer on the first metal layer and on the underlying layer; depositing a second metal layer on the first intermediate layer; and planarizing the second metal layer to

coexpose the first intermediate layer and the second metal layer at a first substantially planar surface.

[007] Another aspect of the invention provides for a method for forming first metal features and second metal features on an underlying layer for use with a semiconductor device, the method comprising: depositing a first metal layer on the underlying layer; masking the first metal layer such that the first metal layer includes a first masked portion and a first unmasked portion wherein the first masked portion and the first unmasked portion correspond to a complementary pattern; etching the first metal layer such that the first unmasked portion is removed to the underlying layer, leaving the first metal features; depositing a first conformal dielectric layer on the first metal layer and on the underlying layer, depositing a second metal layer on the first conformal dielectric layer; and planarizing the second metal layer form the second metal features and to coexpose the second metal features and the first conformal dielectric at a substantially planar surface.

[008] Each of the aspects and embodiments of the invention described herein can be used alone or in combination with one another.

[009] The preferred aspects and embodiments will now be described with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a cross-sectional view of a prior art example of an underlying layer having a metal pattern formed in 45nm processes.

[0011] FIG. 2 is an illustrative flowchart of a method for forming metal lines on an underlying layer in accordance with embodiments of the present invention.

[0012] FIGS. 3-6 are cross-sectional views showing stages in formation of metal lines on underlying layers using methods in accordance with embodiments of the present invention.

[0013] FIG. 7 is a cross-sectional view of metal lines on an underlying layer in accordance with embodiments of the present invention.

[0014] FIG. 8 is a cross-sectional view of metal lines on an underlying layer in accordance with embodiments of the present invention.

[0015] FIG. 9 is a cross-sectional view of metal lines formed according to an embodiment of the present invention used in a monolithic three dimensional memory array.

[0016] FIGS. 10A-C are plan views of metal lines on an underlying layer in accordance with embodiments of the present invention.

[0017] FIG. 11 is a plan view of a connection between a first metal line and a second metal line in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] The present invention will now be described in detail with reference to a few embodiments thereof as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be

apparent, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps and/or structures have not been described in detail in order to not unnecessarily obscure the present invention.

[0019] FIG. 2 is an illustrative flowchart of a method for forming metal lines on an underlying layer in accordance with embodiments of the present invention. FIG. 2 will be discussed in connection with FIGS. 3-8, which are illustrative representations of stages of forming metal lines on underlying layers utilizing methods in accordance with embodiments of the present invention. At a first step 202, a first metal is deposited on an underlying layer. Referring to FIG. 3, in one embodiment first metal layer 302 is deposited on underlying layer 304. As may be appreciated, any number of suitable metal compositions may be deposited on any number of underlying layer compositions using any number of well-known methods without departing from the present invention. Underlying layer 304 is typically a dielectric material such as silicon dioxide. Metal 304 may be tungsten, aluminum, or some other appropriate conductive material. In some embodiments, the thickness of first metal layer 302 is no less than approximately 30nm. In other embodiments, the thickness of first metal layer 302 is no more than approximately 1000nm.

[0020] At a next step 204, the first metal layer is masked using any number of well-known methods. Masking typically provides a fine pattern, for example in a light-sensitive material such as photoresist, on a layer so that subsequent etching will remove the unmasked portion of the masked layer. At a next step 206, first metal layer 302 is etched. As seen in FIG. 4, a resulting pattern after etching may consist of a series of metal features; for example the pattern may include trenches such as trench 404 and lines such as line 408 and line 410. In some embodiments, etching may proceed to underlying layer 304. It may be appreciated that in other embodiments, etching may proceed past an

underlying layer. Etching may be accomplished in any manner well-known in the art without departing from the present invention.

[0021] At a next step 208, dielectric may be conformally deposited onto the tops and sidewalls of the remaining metal layer and the exposed underlying layer. Thus, as shown in FIG. 5, dielectric layer 504 may be conformally deposited on and in contact with the tops and sidewalls of lines 408 and 410 and on exposed sections of underlying layer 304 in accordance with an embodiment of the present invention. Dielectric layer 504 may be deposited in any manner well-known in the art. The thickness of dielectric layer 504 is selected so that trench 404 between metal lines 408 and 410 still has sufficient width, after dielectric layer 504 has been deposited, to allow formation of the next metal lines. In some embodiments, the width of trenches 404 *after* deposition of dielectric layer 504 may be the same, or nearly the same, as the width of first metal lines 408 and 410. Clearly, this requires that the width of trenches 404 *before* deposition of dielectric layer 504 must be wider than the width of metal lines 408 and 410. In some embodiments, dielectric may be selected to provide a diffusion barrier and an adhesion layer. In some embodiments, Si_3N_4 or SiO_2 may be utilized for a dielectric layer.

[0022] At a next step 210, a second metal is deposited on the dielectric layer. As illustrated in FIG. 6, a second metal layer 604 is deposited on and in contact with dielectric layer 504. In some embodiments, the second metal layer is a composition substantially similar to the first metal layer. In other embodiments, the second metal layer is different from the first metal layer. Further, as illustrated in FIG. 6, second metal layer 604 now forms a complementary pattern to the originally masked first metal layer in accordance with an embodiment of the present invention. That is, the second metal layer fills the etched portion of the first metal layer, which corresponds to the originally unmasked portion of the first metal layer. It may be appreciated that

metal compositions selected for deposition may, in some examples, require additional steps or recipes to accommodate chemical and physical properties. In some embodiments, copper or aluminum may be utilized for a second metal layer solely or in combination without departing from present invention. In other embodiments, tungsten may be utilized for a second metal layer. It may be appreciated that use of tungsten for second metal layer deposition may require a conformal adhesion layer before deposition on a dielectric layer. Thus, in some embodiments, a thin adhesion layer such as Ti, TiW, or TiN (solely or in combination) may be conformally deposited on dielectric layer 504 before second metal layer 604 is deposited without departing from the present invention.

[0023] Further, it may be appreciated that although the illustrated metal lines are substantially equal in width, lines may be varied in width to compensate for volumetric differences between first metal layers and second metal layers without departing from the present invention. For example, as noted above, where tungsten is utilized as a second metal layer 604 over dielectric layer 504, an adhesion layer may be required. However, use of a TiN adhesion layer may result in a volumetric change of a second metal layer of tungsten with respect to a first metal layer of tungsten. Thus, in order for metal lines to have similar electrical characteristics, the width of metal lines (*i.e.* second metal layer) may be adjusted to properly compensate for volumetric differences without departing from the present invention.

[0024] Further, it may be appreciated that selection of a metal for a first or second metal layer in accordance with embodiments described herein may be optimized for a particular feature or device connected with the metal layer. For example, some metal-semiconductor connections may create an unintended Schottky device. Thus, where only a single metal is available for conductive lines, some device configurations may not be possible. However, because

present methods provide for selection of a first metal that differs from a second metal in forming conductive lines, device combinations not otherwise possible may be achieved. Thus in some embodiments the first metal layer and the second metal layer are substantially similar while in other embodiments, the first metal layer and the second metal layer are not substantially similar.

[0025] At a next step 212, the method determines whether a coplanar configuration is desired. A coplanar configuration is one in which both metal layers may be contacted from the same side; from above, for example. Alternatively, a non-coplanar configuration is one in which either metal layer may be independently contacted from above and from below. Thus, if the method determines, at a step 212, that a coplanar configuration is required, the method continues to a step 214 to planarize the surface of the structure to coexpose both metals at a substantially planar surface. Planarization may be accomplished in any manner known in the art without departing from the present invention such as: chemical mechanical polishing (CMP) and blanket etchback utilizing wet or dry etch methods. As illustrated in FIG. 7, device 700 includes a surface 720 that has been planarized to expose metal lines 408, 708, and 410 in accordance with an embodiment of the present invention. Further, as illustrated, the portions of dielectric layer 504 that are not removed during planarization are also coexposed at the substantially planar surface and serve to insulate these metal lines from one another. Electrical contact may be made to metal lines 408, 708, and 410 at positions 730, 740, and 750 on the same side of structure 700. In some embodiments, the thickness of the second metal layer is no less than approximately 30nm after planarization. In other embodiments, the thickness of the second metal layer is no more than approximately 1000nm after planarization.

[0026] If the method determines, at a step 212, that a coplanar configuration is not required, the method continues to a step 216 to planarize

the surface of the device, the planarization step stopping on the dielectric 504 and not removing it to expose first metal lines 410 and 408. Planarization may be accomplished in any manner known in the art without departing from the present invention such as CMP and blanket etchback utilizing wet or dry etch methods. As illustrated in FIG. 8, device 800 includes a surface 820 that has been planarized to coexpose dielectric 504 and line 708 at a substantially planar surface in accordance with an embodiment of the present invention. In some embodiments, the thickness of the second metal layer is no less than approximately 30nm after planarization. In other embodiments, the thickness of the second metal layer is no more than approximately 1000nm after planarization. Further, as illustrated, first metal lines 408 and 410 remain shielded by dielectric 504 in this embodiment. Electrical contact may be made to metal line 708 at position 830 above structure 800, while electrical contact can be made to metal lines 408 and 410 at positions 840 and 850 below structure 800.

[0027] Herner et al., US Patent No. 6,952,030, "High-density three-dimensional memory cell," hereby incorporated by reference, describes a monolithic three dimensional memory array including multiple memory levels monolithically formed stacked above a substrate. Each memory level includes a vertically oriented diode disposed between conductors. The diode is preferably a p-i-n diode, having a heavily doped p-type region at one end, a heavily doped n-type region at the other, and an intrinsic region in the middle. Conductors formed according to aspects of the present invention which are contactable from above and below, as in FIG. 8, could be employed in such an array. Turning to FIG. 9, for example, vertically oriented diodes 220 in a first memory level could make electrical contact to first metal lines 408 and 410 from below, while diodes 330 in a second memory level could make electrical contact to second metal lines, such as metal line 708, from above.

[0028] In the embodiments of either FIG. 7 or FIG. 8, after the planarization step, a first plurality of substantially parallel metal lines, formed of the first metal, is interspersed with a second plurality of substantially parallel metal lines, formed of the second metal.

[0029] As noted above, in conventional metal line patterns formed subtractively, in order to accommodate more densely arranged features, a decrease in pitch is generally required. As pitch decreases, metal volume of conducting lines also decreases, thus resulting in an increase in resistance of conductive lines. In general the gap between adjacent lines cannot be too narrow, as very narrow lines are difficult to etch cleanly. Referring to the prior art example of FIG. 1, the width of dielectric 104 may be the same as the width of metal lines 108 and 110, and pitch may be double the width of lines 108 and 110.

[0030] Referring to FIGS. 7 and 8, the width of dielectric layer 504 between adjacent metal lines 408 and 708 is substantially less than the width of metal lines 408 and 708, and pitch is thus substantially less than double the width of lines 408 and 708, allowing for increased density. Therefore, in one embodiment, for a pitch of approximately 250nm, the width of metal lines is in the range of approximately 170-230nm and the width of dielectric is in the range of approximately 20-80nm. In another embodiment, for a pitch of approximately 180nm, the width of metal lines is in the range of approximately 140-166nm and the width of dielectric is in the range of approximately 14-40nm. In another embodiment, for a pitch of approximately 90nm, the width of metal lines is in the range of approximately 70-83nm and the width of dielectric is in the range of approximately 7-20nm. In another embodiment, for a pitch of approximately 72nm, the width of metal lines is in the range of approximately 56-67nm and the width of dielectric is in the range of approximately 5-16nm. In another embodiment, for a pitch of approximately 58nm, the width of metal

lines is in the range of approximately 45-54nm and the width of dielectric is in the range of approximately 4-13nm. In another embodiment, for a pitch of approximately 48nm, the width of metal lines is in the range of approximately 38-44.5nm and the width of dielectric is in the range of approximately 3.5-10nm.

[0031] FIGS. 10A-C are illustrative representations of metal lines on an underlying layer in accordance with embodiments of the present invention. FIG. A is a top view of a portion of a semiconductor device 900 fabricated in accordance with embodiments of the present invention. Further, FIG. 10A corresponds to a top view of FIG. 7 as described above. As illustrated, a number of first metal lines 406, 408, and 410 are insulated from surrounding metal 902 by dielectric 504. As may be appreciated, in this configuration, second metal lines 708 and 706 are shorted together, and must be isolated from each other. Referring to FIG. 10B, etch mask 920 may be applied to device 900 to isolate lines 708 and 706 of second metal 902. In this etching step, the second metal only may be masked and etched, or the first metal and the second metal may both be masked and etched. Etching continues to at least the underlying layer whereupon a conformal dielectric layer may be deposited on all exposed surfaces. Any suitable dielectric layer known in the art may be utilized without departing from the present invention. In some embodiments, Si_3N_4 or SiO_2 may be utilized as a dielectric layer. The device may then be planarized to coexpose the metal lines at a substantially planar surface as illustrated in FIG. 10C. As illustrated, the first set of metal lines such as lines 406, 408, and 410 and second set of metal lines such as line 708 and 706 are surrounded by dielectric 934.

[0032] FIGS. 10A-C also illustrate how the current invention can reduce process cost. Conductors 406, 408, and 410 are patterned at a pitch P. The density of these conductors is therefore $1/P$ lines per unit width. The result in

Fig. 10B has a density of conductor lines of $2/P$ lines per unit width. In a conventional patterning process, this density would require patterning at pitch of $P/2$, which would require processing tools that are twice as capable as those required when using methods of the present invention. An additional mask 920 is required in the example shown, but the pitch of the shapes in mask 920 on Fig. 10B is $2P$. Thus, a conductor density $P/2$ that would normally call for one patterning step with a pitch capability of $P/2$ is fabricated by two patterning steps, one with a capability of P , and one with a capability of $2P$. The cost of the patterning tools is a strong function of their pitch capability. Thus the process of the current invention can be expected to be less expensive than a conventional process.

[0033] FIG. 11 is an illustrative example of a connection 1006 between a first metal line 1002 and a second metal line 708 in accordance with an embodiment of the present invention. As described above, a first set of metal lines may be defined from a first metal layer and a second set of metal lines may be defined from a second metal layer. As may be appreciated, in some embodiments, it may be desirable to connect some portion of the first set of metal lines with some portion of the second set of metal lines. Thus, in some embodiments, a via 1006 may be formed to connect first metal line 1002 with second metal line 708. As may be appreciated, vias may be formed in any manner well-known in the art without departing from the present invention.

[0034] While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. For example, although references to FIGS. 7 and 8 disclose independent coplanar and non-coplanar embodiments, it may be appreciated that those embodiments are not mutually exclusive and may, in some

embodiments, be utilized in combination without departing from the present invention. Although various examples are provided herein, it is intended that these examples be illustrative and not limiting with respect to the invention. Further, the abstract is provided herein for convenience and should not be employed to construe or limit the overall invention, which is expressed in the claims. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

[0035] The foregoing detailed description has described only a few of the many forms that this invention can take. For this reason, this detailed description is intended by way of illustration, and not by way of limitation. It is only the following claims, including all equivalents, which are intended to define the scope of this invention.

WHAT IS CLAIMED IS:

1. A method for depositing at least two metal layers on a underlying layer comprising:
 - depositing a first metal layer on the underlying layer; masking the first metal layer such that the first metal layer includes a first masked portion and a first unmasked portion; and
 - etching the first metal layer such that the first unmasked portion is removed to the underlying layer; depositing a first intermediate layer on the first metal layer and on the underlying layer;
 - depositing a second metal layer on the first intermediate layer; and
 - planarizing the second metal layer to coexpose the first intermediate layer and the second metal layer at a first substantially planar surface.
2. The method of claim 1 wherein the first metal layer is coexposed at the first substantially planar surface with the second metal layer and the intermediate layer.
3. The method of claim 2 further comprising:
 - masking the first metal layer, the second metal layer, and the first intermediate layer such that the first metal layer, the second metal layer, and the first intermediate layer include a third masked portion and a third unmasked portion; and
 - etching the third unmasked portion to the underlying layer;
 - depositing a second intermediate layer on all etched surfaces; and
 - planarizing the second intermediate layer to coexpose the second intermediate layer and the first metal layer at a second substantially planar surface.

-15-

4. The method of claim 4 wherein the first intermediate layer comprises Si_3N_4 or SiO_2 or the second intermediate layer comprises Si_3N_4 or SiO_2 .
5. The method of claim 4 wherein the planarizing is performed by chemical mechanical polishing or etchback.
6. The method of claim 4 further comprising:
electrically connecting a portion of the first metal layer with a portion of the second metal layer.
7. The method of claim 1 further comprising
masking the second metal layer and the first intermediate layer such that the second metal layer and the first intermediate layer include a second masked portion and a second unmasked portion; and
etching the second unmasked portion to the underlying layer;
depositing a second intermediate layer on all etched surfaces; and
planarizing the second intermediate layer to coexpose the second intermediate layer and the first metal layer at a second substantially planar surface.
8. The method of claim 7 wherein the first intermediate layer comprises Si_3N_4 or SiO_2 or the second intermediate layer comprises Si_3N_4 or SiO_2 .
9. The method of claim 7 wherein the planarizing step is performed by chemical mechanical polishing or etchback.
10. The method of claim 1 wherein the first metal layer and the second metal layer are substantially the same composition.

11. The method of claim 1 wherein, after the etching step, the first metal layer is in the form of a plurality of substantially parallel first metal lines.
12. The method of claim 11 wherein, after the planarizing step, the second metal layer is in the form of a plurality of substantially parallel second metal lines, the second metal lines interspersed with first metal lines.
13. The method of claim 1 wherein the first metal layer is a composition selected from the group consisting of tungsten and aluminum.
14. The method of claim 1 wherein the second metal layer is a composition selected from the group consisting of tungsten, aluminum, and copper.
15. The method of claim 14 wherein when the second metal layer is tungsten, the method further comprises:
after the depositing the first intermediate layer, depositing a first conformal adhesion layer on the first intermediate layer.
16. The method of claim 15 wherein the first conformal adhesion layer is selected from the group consisting of: Ti, TiW, and TiN.

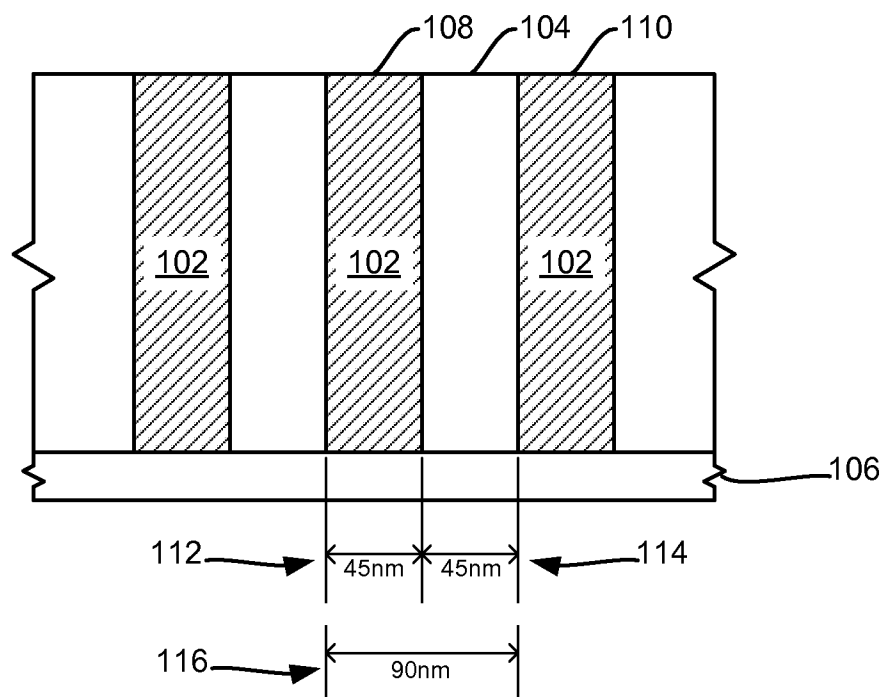


FIG. 1
(PRIOR ART)

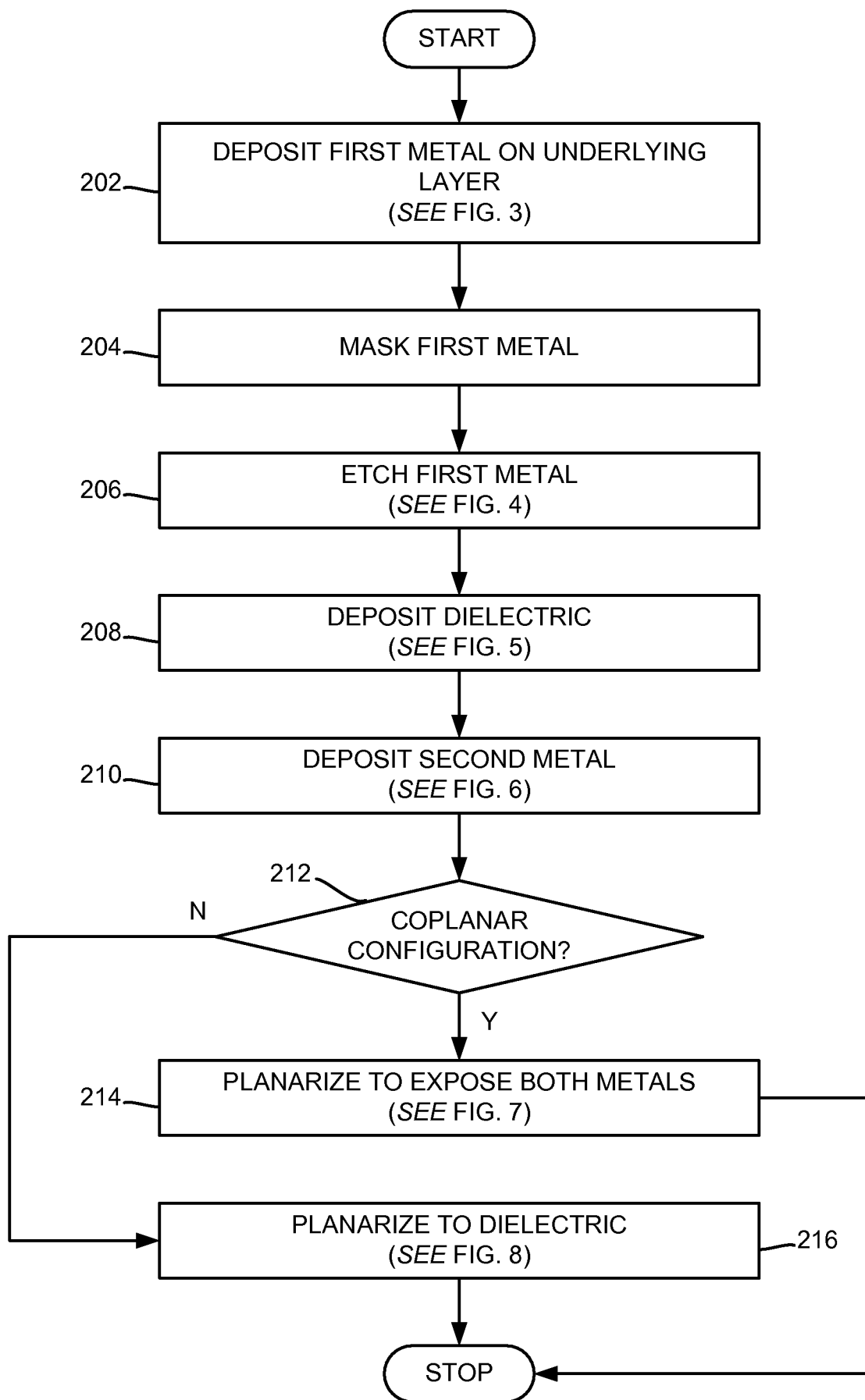


FIG. 2

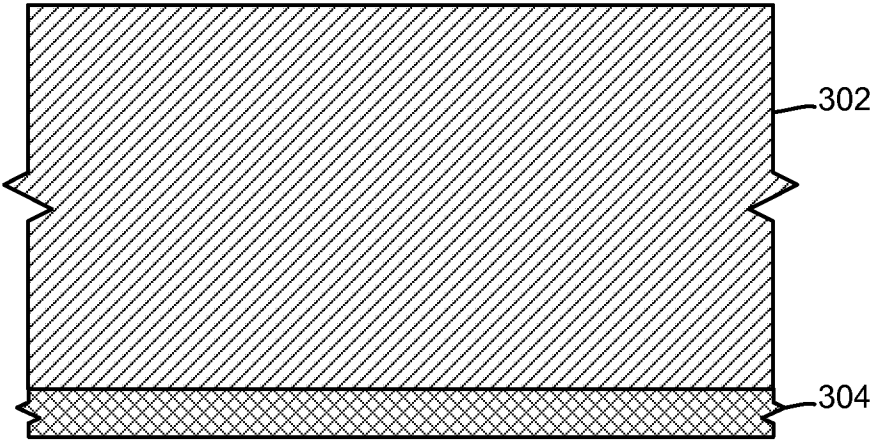


FIG. 3

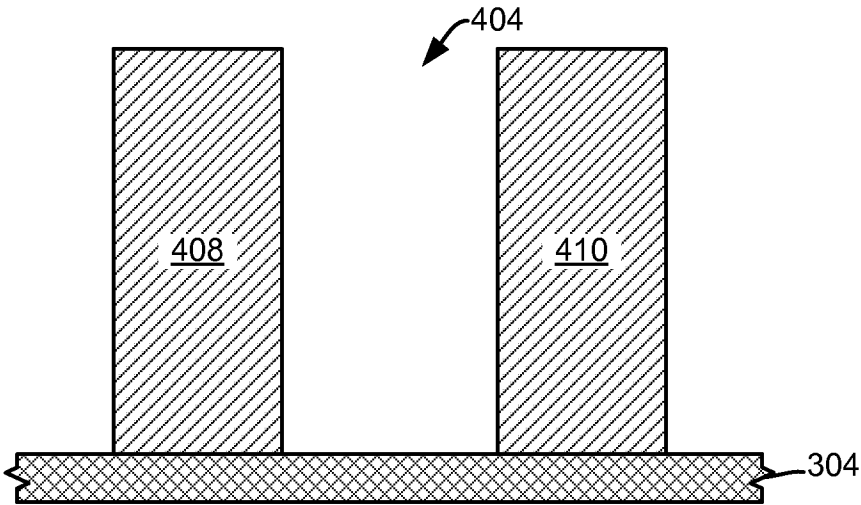


FIG. 4

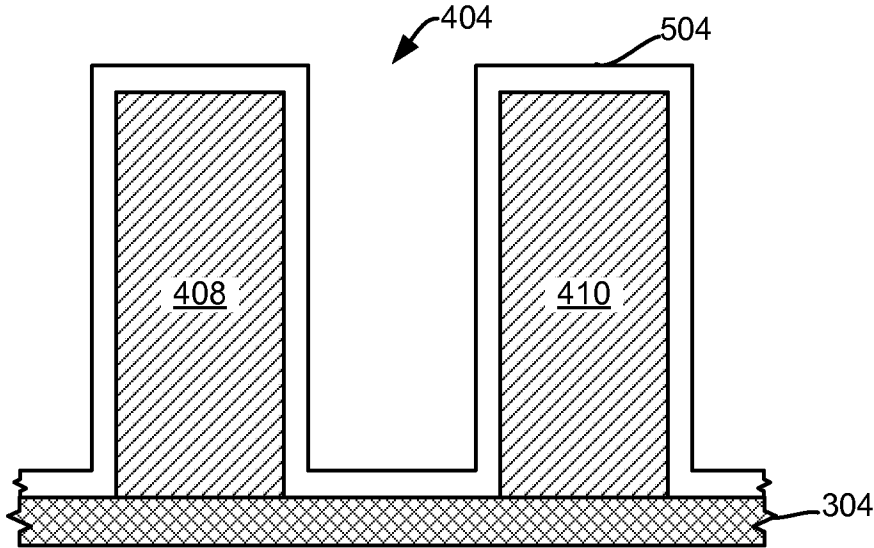


FIG. 5

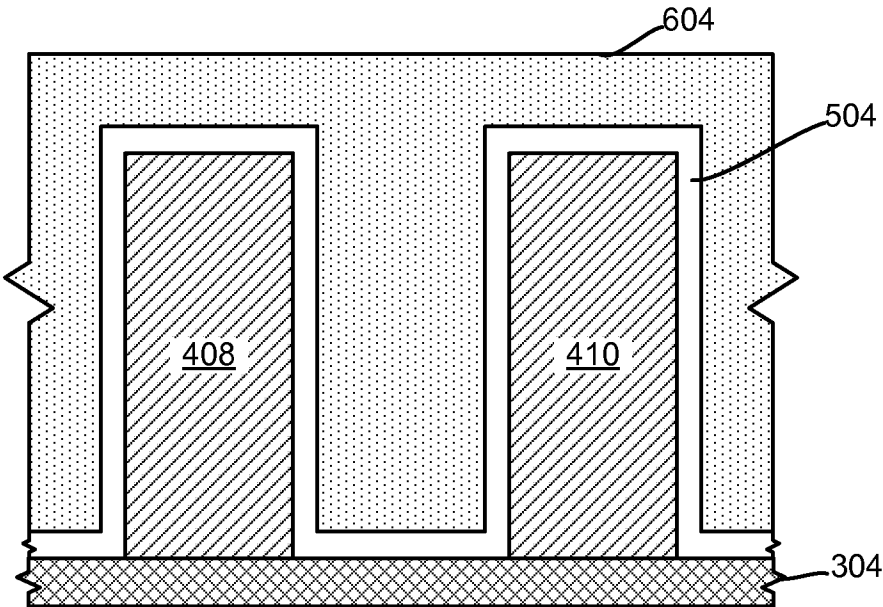


FIG. 6

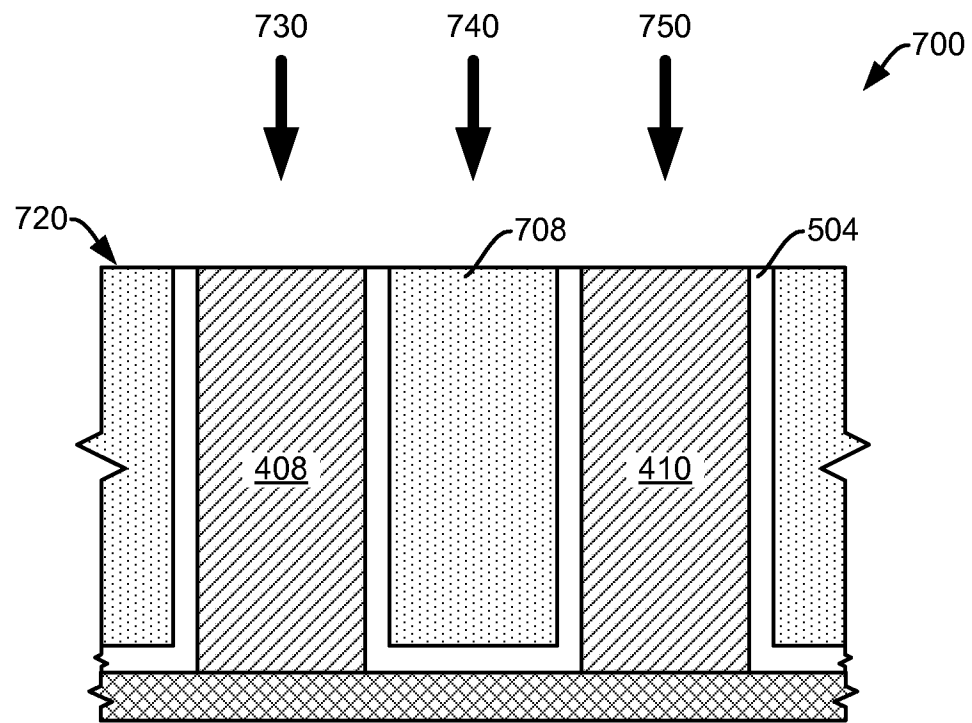


FIG. 7

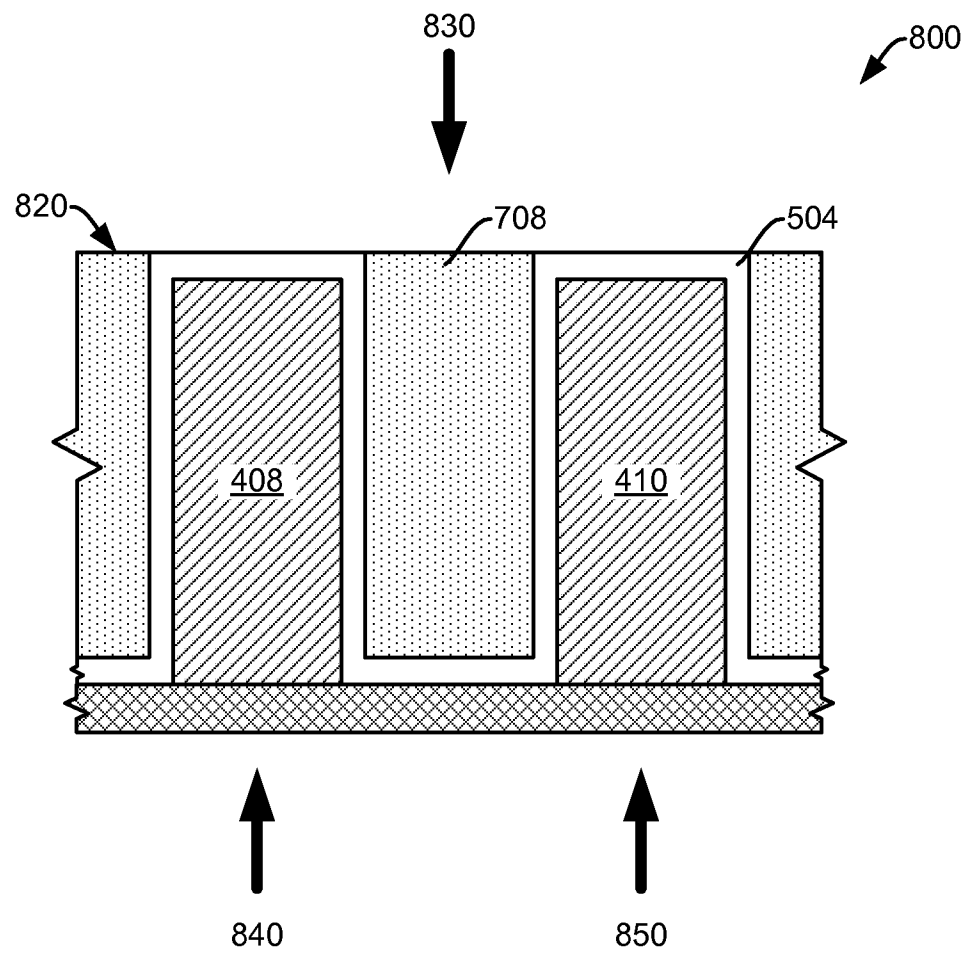


FIG. 8

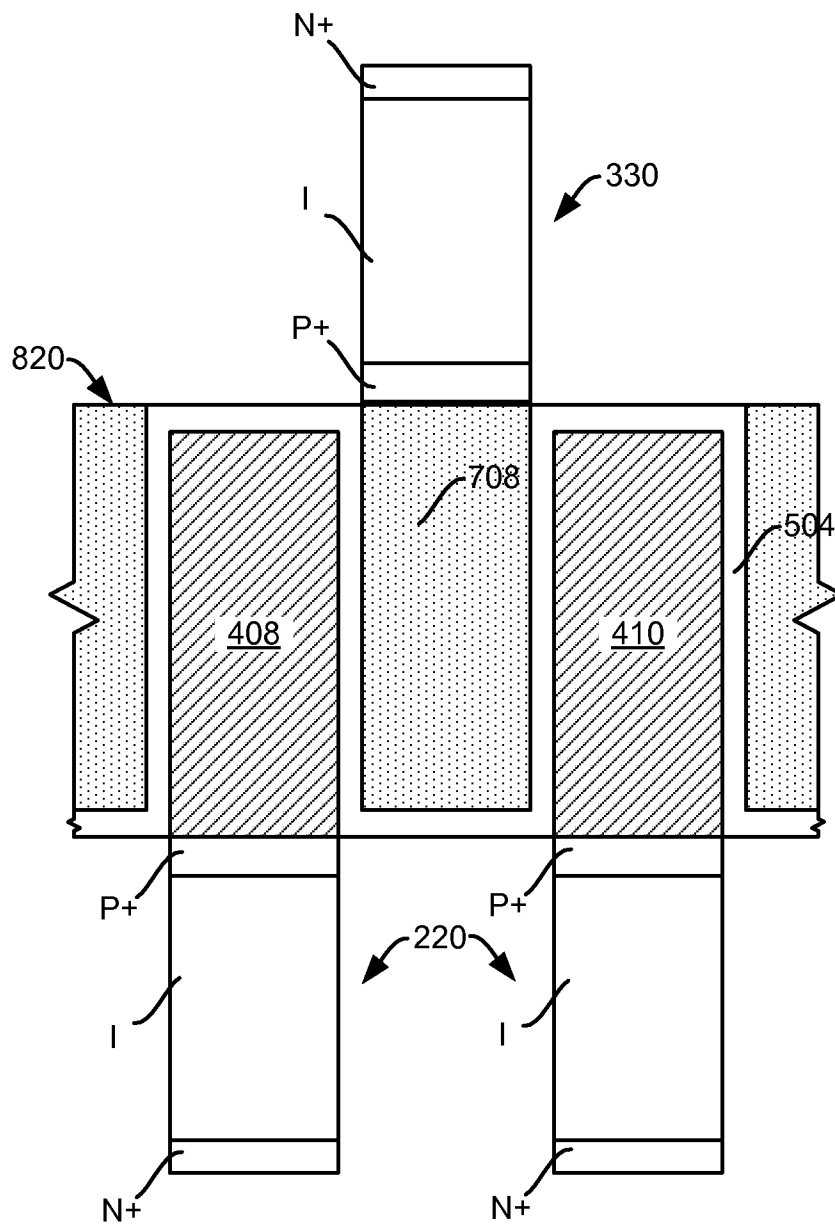


FIG. 9

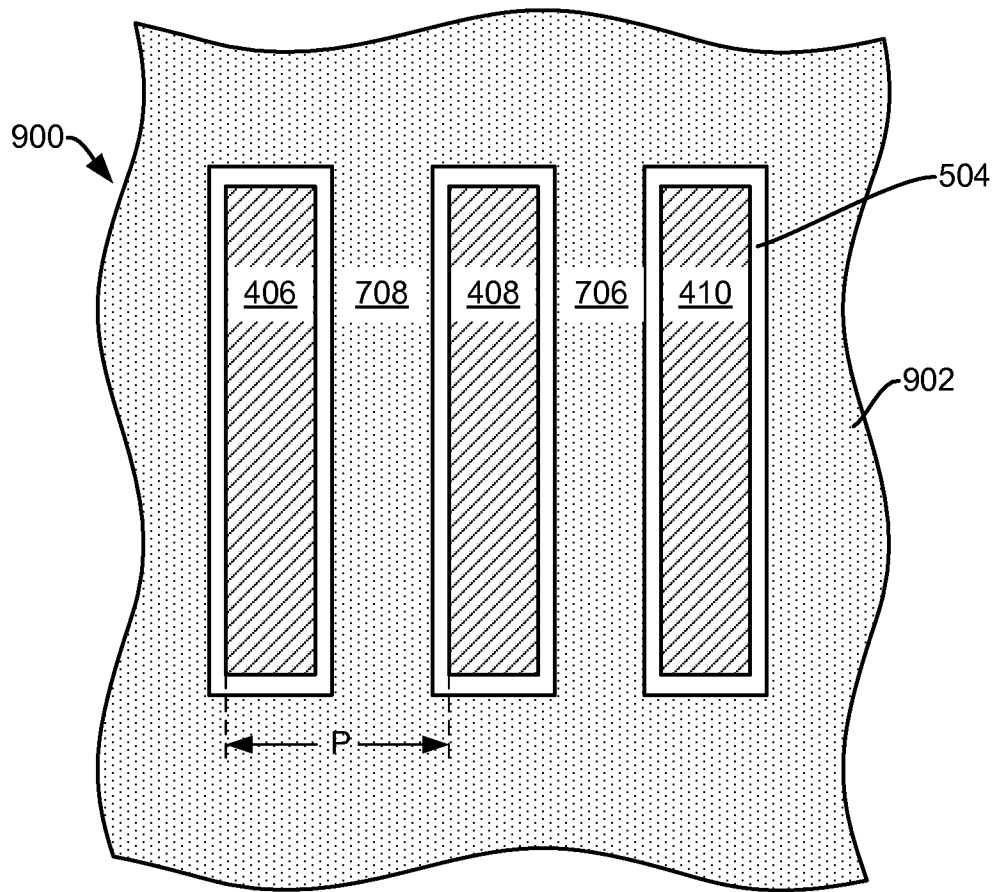


FIG. 10A

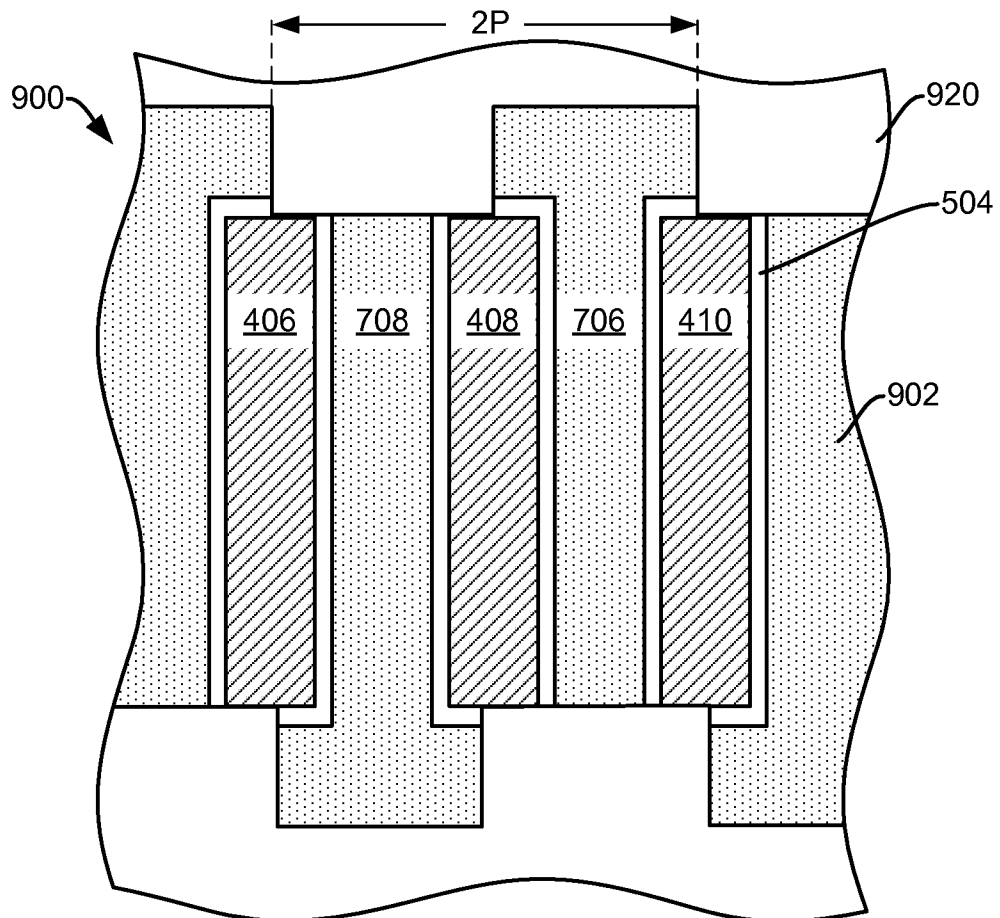


FIG. 10B

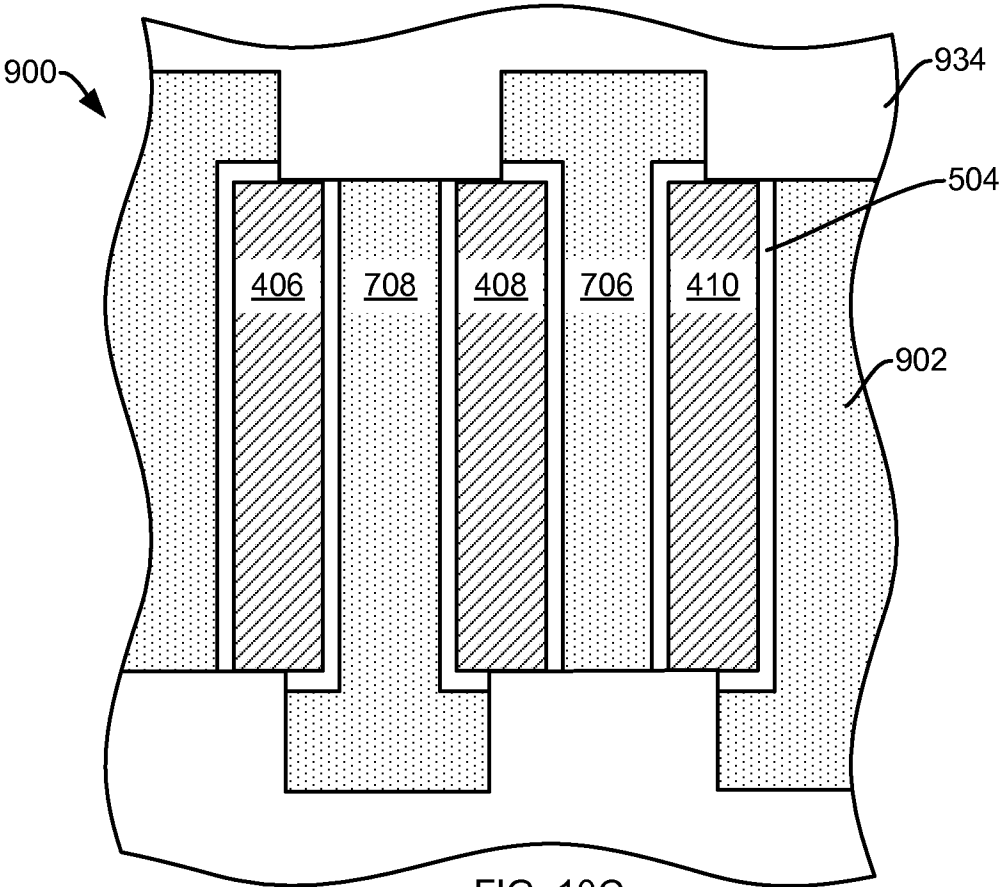


FIG. 10C

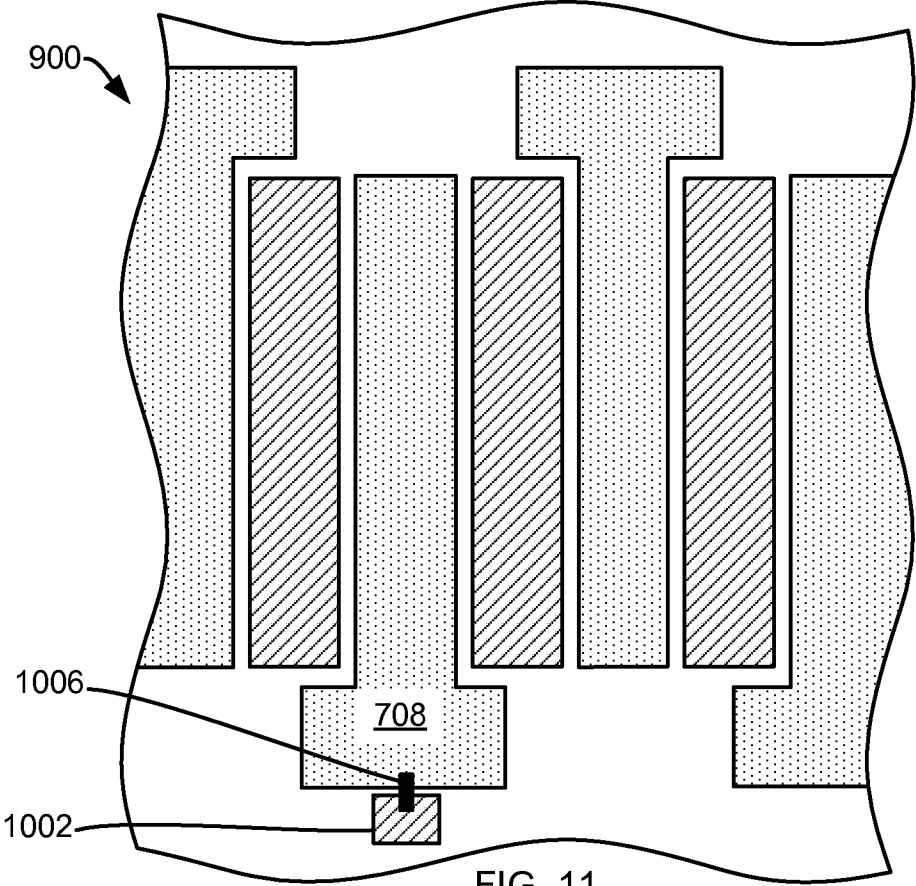


FIG. 11