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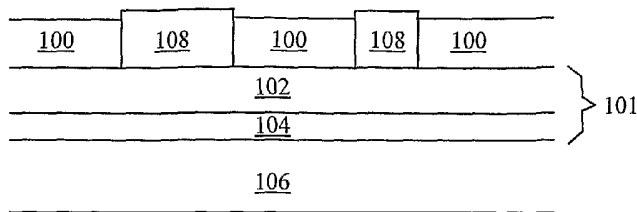
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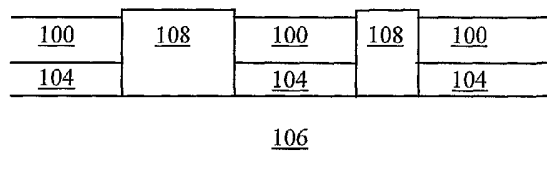
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[Continued on next page]

(54) Title: CONDUCTIVE PATTERN, CIRCUIT BOARD AND THEIR PRODUCTION METHOD



A



B

(57) Abstract: A conductive pattern (100) is electrodeposited on a separating layer (101) in openings in a patterned photoresist (108). The conductive pattern (100) is removable from an auxiliary substrate (106) by means of the separating layer (101). The conductive pattern (100) may be used in producing a circuit board, and components may be embedded in the circuit board.

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## CONDUCTIVE PATTERN, CIRCUIT BOARD AND THEIR PRODUCTION METHOD

### FIELD

**[0001]** The invention relates to a conductive pattern, a circuit board and to a method of producing them for electronic circuits.

### 5 BACKGROUND

**[0002]** Circuit boards provided with either rigid or flexible copper laminate are employed in electronics. The copper film of a copper laminate can be formed using electrodeposition or rolling, and the copper laminate can be formed by attaching the copper film to a suitable insulating circuit board material.

**[0003]** Conventionally, a circuit board is produced in two steps: in the first step, a copper laminate is produced, and in the second step, conductors are patterned on the copper surface of the circuit board.

**[0004]** The actual production of the conductive pattern on the circuit board surface can be carried out as follows, for example. A copper film is coated with a photosensitive material, which is generally called a photoresist. The conductive pattern to be produced is exposed on the surface of the photoresist. After the exposure and development have been performed, a protective layer of the photoresist remains in the areas where conductors are to be formed, and the photoresist is removed from the other areas. Then the copper laminate patterned with the photoresist is immersed in a suitable copper etchant. In that case, the unprotected copper is etched, and only the conductive pattern protected with the photoresist remains on the circuit board surface. Finally, the used photoresist is also removed.

**[0005]** In the production of a circuit board, pattern plating is frequently also used as a sub-process, where the surface patterned with a resist is coated, i.e. pattern plated, electrolytically with copper.

**[0006]** Electronic components and flip chips are usually assembled onto the circuit board surface and attached thereto electrically by a solder or adhesive joint.

**[0007]** As the packaging density has increased, components are more and more frequently embedded inside circuit boards. Several prior art methods are known for embedding ceramic or polymeric thick-film resistors, deposited or "pattern-etched" thin-film resistors, or semiconductor chips inside a circuit board.

[0008] Pattern transfer methods are also known where a conductive pattern is first deposited or etched on the surface of a temporary auxiliary substrate, from which the conductive pattern is transferred onto the final circuit board material.

5 [0009] The prior art methods involve several disadvantages. If circuit board conductors are produced by etching, the copper film patterned with the resist limits the accuracy of the resulting conductive pattern, known as "lateral under etching", because etching also proceeds in the horizontal direction when wet etching is used. For this reason, the cross section of the etched conductor will be a trapezoid. This shape restricts resolution and hinders the use  
10 of high frequencies, for instance.

[0010] If conductive patterns are formed on the circuit board surface by pattern plating, the conductive pattern will vary in height. This results from deposition geometry: the current density varies in different parts of the pattern.

15 [0011] In transfer methods, electrolytic metallization of through holes and vias is often very difficult, if not impossible altogether, because there is no uniform metal film on the circuit board surface that could be used for supplying electric current to metallize a through-hole. Furthermore, many transfer methods do not allow the use of a copper film as an auxiliary substrate. Problems are also posed by the recyclability, environment friendliness and health  
20 hazards of the materials used. An advantage of copper electrodeposition over chemical (electroless) deposition is its quickness and good quality of metals.

#### BRIEF DESCRIPTION

25 [0012] An object of the invention is to provide an improved production method and an improved circuit board. This is achieved by a method of producing a conduction pattern. The method comprises forming a separating layer on an auxiliary substrate, where at least the surface is conductive, forming a patterned resist layer on the separating layer, electrodepositing a patterned resist layer on the separating layer, electrodepositing a conductive pattern on the separating layer in openings in the patterns of the resist layer, at  
30 least the auxiliary substrate being removable from the layer structure formed.

[0013] The invention also relates to a method of producing a conductive pattern. The method comprises forming a patterned resist layer on an auxiliary substrate, where at least the surface is conductive, forming a separating  
35 layer on the auxiliary substrate in openings in the patterns of the resist

layer, electrodepositing a conductive pattern on the separating layer in the openings in the patterns of the resist layer, at least the auxiliary substrate being removable from the layer structure formed.

**[0014]** The invention also relates to a method of producing a circuit board. The method employs at least one auxiliary substrate with a conductive surface, the method comprising forming at least one separating layer on each auxiliary substrate, forming a patterned resist layer on each separating layer, electrodepositing a conductive pattern on each separating layer in openings in the patterns of the resist layer, embedding and attaching the at least one conductive pattern to electricity insulating material, and removing at least the auxiliary substrate from the rest of the layer structure.

**[0015]** The invention also relates to a method of producing a circuit board. The method employs at least one auxiliary substrate with a conductive surface, the method comprising forming a patterned resist layer on each auxiliary substrate, forming at least one separating layer on each auxiliary substrate in openings in the patterns of the resist layer, electrodepositing a conductive pattern on each separating layer in the openings in the patterns of the resist layer, embedding and attaching the at least one conductive pattern to electricity insulating material, and removing at least the auxiliary substrate from the rest of the layer structure.

**[0016]** The invention also relates to a circuit board. The circuit board has a layered structure and the circuit board has been formed using in the production at least one auxiliary substrate with a conductive surface, on which at least one separating layer has been formed, and the circuit board comprises at least one conductive pattern produced by forming a patterned resist layer on each separating layer, by electrodepositing a conductive pattern on each separating layer in openings in the patterns of the resist layer, and the circuit board has been formed by embedding and attaching the at least one conductive pattern to electricity insulating material and by removing at least the auxiliary substrate from the rest of the layer structure.

**[0017]** The invention also relates to a circuit board. The circuit board has a layered structure and the circuit board has been formed using in the production at least one auxiliary substrate with a conductive surface, and the conductive pattern has been produced by forming a patterned resist layer on each auxiliary substrate, by forming at least one separating layer in openings in the patterns of the resist layer, by electrodepositing a conductive pattern on each

separating layer in the openings in the patterns of the resist layer, and the circuit board has been formed by embedding and attaching the at least one conductive pattern to electricity insulating material and by removing at least each auxiliary substrate from the rest of the layer structure.

5           **[0018]** The invention also relates to a conductive pattern. The conductive pattern has been formed by using in the production at least one auxiliary substrate with a conductive surface, on which at least one separating layer has been formed, and each circuit board comprises at least one conductive pattern produced by forming and patterning a resist layer on the separating  
10 layer, by electrodepositing a conductive pattern on the separating layer in openings in the patterns of the resist layer, each auxiliary substrate being removable from the layer structure formed.

**[0019]** The invention also relates to a conductive pattern. The conductive pattern has been formed by using in the production at least one auxiliary  
15 substrate with a conductive surface, on which a patterned resist layer has been formed, and the conductive pattern has been produced by forming a separating layer on each auxiliary substrate in openings in the patterns of the resist layer, by electrodepositing growing a conductive pattern on the separating layer in the openings in the patterns of the resist layer, each auxiliary sub-  
20 strate being removable from the layer structure formed.

**[0020]** Preferred embodiments of the invention are described in the dependent claims.

**[0021]** The method and system according to the invention provide several advantages. The conductor cross section is rectangular and no lateral under etching occurs. Consequently, conductors and spaces between  
25 conductors can be provided with a high dimensional accuracy. There are fewer different production process steps than in etching methods and the production costs are low. Copper or copper-coated plastic can be used as the auxiliary substrate and intermediate layer, both copper and plastic being easily recyclable materials. The production process requires less corroding materials and  
30 materials that are poisonous and hazardous to the environment and humans, which reduces the need for post-processing of these materials and the costs resulting from post-processing.

## LIST OF FIGURES

[0022] The invention will now be described in greater detail by means of the presented embodiments, with reference to the accompanying drawings, in which

5 Figure 1A illustrates a layer structure comprising a temporary auxiliary substrate, a separating layer and a conductive pattern,

Figure 1B illustrates another kind of layer structure comprising a temporary auxiliary substrate, a separating layer and a conductive pattern,

Figure 2A illustrates a pre-form for a one-sided circuit board,

10 Figure 2B illustrates a one-sided circuit board,

Figure 2C illustrates attachment of circuit board material to a conductive pattern as a continuous process,

Figure 3 illustrates a two-sided circuit board provided with through-holes,

15 Figure 4 illustrates an "any layer microvia" circuit board,

Figures 5A and 5B illustrate a two-sided 2.5D circuit board, where the upper side and the lower side have been connected to each other electrically by a fold in the circuit board,

Figure 6 illustrates an L-shaped 2.5D circuit board,

20 Figure 7A illustrates production of a 3D circuit board between the jaws of a hot press,

Figure 7B illustrates production of a 3D circuit board in a mould,

Figure 7C illustrates a 3D circuit board,

25 Figures 8A to 8C illustrate embedding of a deposited/printed component in a circuit board,

Figures 9A to 9E illustrate embedding of a component in a circuit board,

Figures 10A to 10E illustrate embedding of a component in a circuit board,

30 Figure 11 illustrates production of a conductive pattern as a continuous process,

Figure 12 illustrates a production method of a conductive pattern as a flowchart,

35 Figure 13 illustrates a production method of a conductive pattern as a flowchart,

Figure 14 illustrates a production method of a circuit board as a flow chart, and

Figure 15 illustrates a production method of a circuit board as a flow chart.

## 5 DESCRIPTION OF EMBODIMENTS

**[0023]** Production of a conductive pattern will be examined first. Figure 1A illustrates a conductive pattern 100 on an intermediate layer 102. In the solution described, the conductive pattern 100 can be deposited on a separating layer 101 included in the layer structure. The separating layer 101  
10 may comprise both an intermediate layer 102 and a release layer 104, but the separating layer 101 may also be a mere release layer 104. The layer structure further comprises an auxiliary substrate 106. Before depositing the conductive pattern 100, the separating layer 101 is coated with a patterned resist 108. In that case, either the intermediate layer 102 or the release layer 104 is coated  
15 with a resist. The conductive pattern is electrodeposited in openings in the resist 108. The conductive pattern 100 together with the optional intermediate layer 102 can be removed from the auxiliary substrate 106 by means of the release layer 104.

**[0024]** Figure 1B illustrates an alternative way of producing a conductive pattern. In this solution, a patterned resist layer 108 is formed on the auxiliary substrate 106, where at least the surface is conductive. The release layer 104 is formed on the auxiliary substrate 106 in openings in the patterns of the resist layer 108. The conductive pattern 100 is electrodeposited on the release layer 104 in the openings in the patterns of the resist layer 108. Thus  
20 less release layer material is required. Also in this solution, at least the auxiliary substrate 106 is removable from the layer structure formed. Both in the case of Figure 1A and in the case of Figure 1B, the intermediate layer 102 (between layers 100 and 104) can be used to level out any non-homogeneities in the auxiliary substrate.  
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**[0025]** The temporary auxiliary substrate 106 may be totally conductive or only its surface. Even though the intermediate layer 102 is not necessarily needed in the solution described, the intermediate layer 102 may be employed to level out any non-homogeneity in the auxiliary substrate, to function as a current transmission layer in the metallization of vias and/or to facilitate  
30 the removal of the auxiliary substrate 106 and/or any bonded components. The  
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intermediate layer 102 can be omitted, for example, in a case where the adhesion of the circuit board material to be attached to the auxiliary substrate or to the auxiliary substrate 106 coated with a release layer 104 is so small that the circuit board material and the auxiliary substrate 106 can be reliably removed from each other.

5 [0026] The auxiliary substrate 106 may be made of metal, such as stainless steel, titan, nickel, aluminium or copper or of their combination in the form of a rigid plate, a three-dimensional shape, or a film-like or rollable ribbon. A metal-coated plastic board or film, such as a copper-coated plastic film in the form of a rollable ribbon, may also be used as the auxiliary substrate 106 since the auxiliary substrate needs to be conductive. PET (polyethylene terephthalate), for example, may be used as the plastic film. In practice, the thickness of the auxiliary substrate 106 may range from less than 15  $\mu\text{m}$  to several millimetres. The lower limit is restricted by the mechanical processability of the auxiliary substrate 106 and the upper limit by processability and cost factors. The auxiliary substrate may be used several times or it may be disposable. A disposable auxiliary substrate 106 may be made of copper ribbon or copper-coated plastic film, both of which are easily recyclable materials.

10 [0027] The release layer 104 between the auxiliary substrate 106 and the intermediate layer 102 or between the auxiliary substrate 106 and the conductive pattern 100 may be made of metals or other organic substances without being limited to these. The metal in the release layer 104 may be nickel and/or chrome, for example, with which the auxiliary substrate 106 is coated electrolytically. The thickness of a metal release layer 104 is typically 1 to 100 nm. If a very thin release layer 104 is used, release cannot be performed reliably. The use of a very thick release layer 104, on the other hand, is not reasonable in the economic sense or in view of recycling.

15 [0028] An organic release layer 104 may be made of carboxybenzotriazole, for instance. The substance of the release layer may be dissolved into water or solvent, where the auxiliary substrate 106 is kept for a certain time. A typical thickness of the organic release layer 104 is approximately 1 to 100 nm.

20 [0029] An intermediate layer 102 may be electrodeposited on the release layer 104. The intermediate layer 102 may be made of copper, for example, having a typical thickness of 0.5 to 7  $\mu\text{m}$ . The thinner the intermediate layer 102 used, the easier its removal usually is.

[0030] The separating layer 101 is coated with a patterned resist 108. In the patterning, it is feasible to use a patterned photoresist, for example. The patterning of a resist 108 is known per se. The patterned resist 108 can also be layered onto an underlying layer by printing. The surface of the intermediate layer 102 or auxiliary substrate 106 can be roughened to improve adhesion to the resist 108. Conductive patterns 100 with a desired thickness, typically 3 to 50  $\mu\text{m}$ , are deposited on the separating layer 101 in the openings in the resist 108. Also thinner or thicker conductors can be deposited.

[0031] After deposition, the conductors 100 can be roughened by known techniques to provide a better adhesion to the insulating circuit board material. The conductors need not be deposited from one material but they may consist of several different metal layers. For example, gold can be deposited as the lowest layer, on top of which nickel and copper layers are deposited. In a completed circuit board having this kind of layer structure, components may be contacted to the gold layer, which is often necessary with respect to contacting.

[0032] It may not be necessary to remove the resist 108, but the resist can be left in its place, and thus it will be part of the final circuit board.

[0033] Figure 2A illustrates a one-sided circuit board pre-form, which may be produced by attaching electricity insulating circuit board material 200 to the layer structure. The layer structure comprises as superimposed layers a temporary auxiliary substrate 106, a separating layer 101 and a conductive pattern 100, which is optionally treated with adhesive. The layer structure may also include a resist 108, but this is not necessary. The electricity insulating material 200 may be, for example, hardening epoxy, thermoplastic plastic or disposable plastic. Typical circuit board epoxy is curdled and hardened by increasing the temperature to a suitable temperature at a certain speed. Thermoplastic plastic softens when it is heated and hardens when cooled. The circuit board material 200 may be nearly any electricity insulating material that can be provided with a sufficiently fluid form for embedding conductive patterns in it. Furthermore, the circuit board material 200 has to re-harden after this. Inside the circuit board material 200, it is feasible to use structures and additives that stiffen the circuit board, affect the thermal properties and/or electric properties, such as mats or fibres made of glass fibre or Teflon, or ceramic powder, or their combinations.

**[0034]** After the layer structure, which comprises a temporary auxiliary substrate 106, a release layer 104, an optional intermediate layer 102 and a conductive pattern 100 (and possibly also a resist 108), has been attached to the circuit board material 200, the auxiliary substrate 106 is removed from the separating layer 101. When the release layer 104 has been properly produced, mechanical removal is easy to carry out without removing the optional intermediate layer 102 and the conductive pattern 100 from the circuit board material 200. In a preferred embodiment, adhesion should be within a range of approximately 0.001 to 0.2 N/mm, depending on the case and materials.

**[0035]** The optional intermediate layer 102 and any remains of the release layer 104 attached thereto can be removed by etching, for example. The result will be a one-sided circuit board 202 similar to the one illustrated in Figure 2B, where conductive patterns 100 have been pressed inside the circuit board and thus its surface is in one level.

**[0036]** Figure 2C illustrates attachment of circuit board material to a conductive pattern as a continuous process. Circuit board ribbon 222 is fed from a circuit board roll 220 into a laminator 224, into which conductive pattern ribbons 230, 232 are also fed from two conductive pattern rolls 226, 228, the ribbons comprising an auxiliary substrate, a separating layer and a conductive pattern. The laminator 224, which may comprise two rolls 234, 236, for example, presses the conductive pattern ribbons 230, 232 onto different sides of the circuit board ribbon 222 by means of increased temperature, for example, if the circuit board ribbon 222 is made of thermoplastic material. Finally, the two-sided circuit board pre-form 238 can be rolled up into a roll 240.

**[0037]** A two-sided circuit board may be produced in the same manner as the one-sided circuit board. As shown in Figure 3, a layer structure is attached to both sides of insulating circuit board material 200 so that the conductive pattern 100 faces the insulating circuit board material 200. Conductive patterns 100 on both sides of the board can be connected to each other through through-holes or microvias 300. Vias can be formed by laser drilling and using circuit board processes known per se to metallize a via and optionally fill it. In the metallization of a via, an intermediate layer may be employed in the transfer of electricity.

**[0038]** Figure 4 illustrates a multi-layer circuit board. Multi-layer circuit boards may be produced by connecting two or more one-sided or two-sided circuit boards produced by the process according to the presented solu-

tion or by piling circuit boards one on top of another or by combining both of these methods. As shown in Figure 4, it is also feasible to produce "any layer microvia" circuit boards where the micro through-hole 300 may go through the circuit board material 400 to 404 in any layer and micro through-holes may be superimposed.

5 [0039] Figures 5A and 5B illustrate a two-sided circuit board which may be produced by folding a layer structure comprising a temporary auxiliary substrate 106, a separating layer 101 and a conductive pattern 100 (optionally with resists 108) to cover both sides of the insulating circuit board material 200. 10 The conductive pattern 100 may be adhesion treated. The upper and lower sides of the circuit board are contacted to each other by a fold 500. The fold may be on one or several sides of the circuit board 200.

[0040] In addition to the fact that the conductive pattern and circuit board may be produced as a planar two-dimensional structure (2D conductive pattern), the presented solution enables production of two-and-half-dimensional or three-dimensional conductive patterns (2.5D or 3D conductive patterns). Thus a 2.5D conductive pattern may be formed on a 2D circuit board, as illustrated in Figures 5A and 5B. Here the 2.5D shape refers to a shape achieved by folding a planar pattern.

20 [0041] Structures having the 2.5 shape are easy to produce by providing the circuit board 200 with an L-shaped cross section, for example, as illustrated in Figure 6. In Figure 6, the conductive pattern 100 is on the inner surface of the circuit board 200, but it may naturally also be arranged on the outer surface or alternatively on both surfaces, which are optionally connected 25 by a fold extending across the circuit board edge or by through-holes.

[0042] A circuit board with a three-dimensional shape may be produced as follows, for example. The layer structure may be provided with the 3D shape using pressure and heat or other known shaping methods, such as hot pressing, pressure shaping or high speed shaping. These shaping methods are material-dependent. The conductive patterns may be adhesion treated to improve adhesion to the electricity insulating material where the conductive pattern is embedded.

30 [0043] Figures 7A to 7C illustrate solutions where the layer structure 716 has been folded into a spherical calotte. After the conductive pattern on the upper surface of the auxiliary substrate has been provided with the 3D shape in accordance with Figure 7A, the layer structure 716 can be placed in a 35

hot press together with the insulating material 200 to be attached thereto. The jaws 702, 704 of the hot press have been provided with the same 3D shape. The insulating material 200 is attached to the conductive pattern on the auxiliary substrate by pressing them between the jaws 702, 704 of the hot press.

5 The circuit board material functioning as the insulating material may also be provided with the 3D shape before hot pressing.

**[0044]** Figure 7B illustrates a layer structure 716 folded into the shape of a spherical calotte in the casting space 712 of an injection moulding die. The layer structure 716 provided with the 3D shape forms part of the die.

10 Injection moulding can be performed through a casting conduit 714. The conductive pattern on the layer structure attaches onto one or both surfaces of the injection moulded product. In the case of Figures 7A and 7B, pre-forming of the 3D shape is not always necessary, but forming may be carried out during pressing or casting. Figure 7C illustrates a cross section of a final 3D circuit board 710 with the shape of a spherical calotte.

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**[0045]** Now we will examine embedding of components in a circuit board. Components may be embedded in a circuit board together with conductive patterns by attaching components onto the conductive pattern or by forming components onto the intermediate layer before the conductive pattern is produced or after the conductive pattern has been produced. In the following, different ways of forming a component and a conductive pattern and of embedding them in a circuit board will be described in greater detail.

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**[0046]** Figures 8A to 8C illustrate examples of solutions where components are formed onto the conductive pattern (or under the conductive pattern).

25

**[0047]** Figure 8A illustrates a solution where at least one component 800, such as a resistor, may be electrodeposited on the conductive pattern 100 and the intermediate layer 102 in the openings in the resist pattern 108 (broken line). Alternatively, the component may be pressed onto the conductive pattern 100 and separating layer 101 by a screen printing method, for example, in which case no resist pattern is needed.

30

**[0048]** Figure 8B illustrates a production method where a component 800, such as a resistor, is first printed onto the separating layer 101 by a screen printing, for example. Thereafter, a conductive pattern 100 is formed on the component 800 and the separating layer 101 in the openings in the resist pattern. Alternatively, the component can be first formed by electrodepositing it

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on the separating layer 101 in the openings in the resist pattern (broken line), after which the resist pattern can be removed. Thereafter, the conductive pattern 100 may be electrodeposited on the component 800 and the separating layer 101 in the openings in the resist pattern 108.

5           **[0049]** Figure 8C illustrates a final circuit board 850 where the component 800 has been embedded. The component can be printed onto the conductive pattern 100 in the separating layer 101 or the component may be electrodeposited on the conductive pattern 100 and the separating layer 101 in the openings in the resist pattern. After insulating material 200 has been attached,  
10 the auxiliary substrate is removed and the intermediate layer etched.

**[0050]** Also leaded or bumped components and semiconductor chips attached to a conductive pattern are embeddable. A connection may be made conductive using conductive adhesive or a solder joint in attachment. The component may be, for example, a leaded surface mounting component, a  
15 leaded or a bumped module or a flip chip. Depending on the material, it may be necessary to provide the circuit board material with a cavity or an opening at the component before attaching the circuit board material. The component may also be protected with plastic encapsulation before attachment of the circuit board material.

20           **[0051]** Figure 9A illustrates a bumped component 900 whose bumps 902 are attached to the conductive pattern 100 functioning as the uppermost layer in the layer structure comprising the auxiliary substrate 106 and the separating layer 101 using an adhesive or a solder joint 904. Thereafter, the lower side of the component may be filled with an "underfill agent" 906, as  
25 shown in Figure 9B. This provides the final circuit board with an even surface. The component together with the conductive pattern 100 and any underfill agent 906 is attached to the circuit board material 200 as in Figure 9C.

**[0052]** Alternatively, the component 900 area in the circuit board material 200 may be provided with an opening 908, which may be filled with  
30 another material 910, as illustrated in Figure 9D. The opening may be filled, for example, with plastic which has been hardened chemically, by heat or ultraviolet. An advantage of this arrangement is that any stress to which the component may be subjected during the attachment of the conductive pattern to the circuit board material can be avoided. Furthermore, the filling material may be  
35 a material which stabilizes tensions caused by differences in the temperature expansion coefficient as the temperature between the component and the cir-

cuit board material varies. Finally, the auxiliary substrate is removed and any intermediate layer is etched, and thus a circuit board is obtained, as illustrated in Figure 9E.

5 [0053] Attachment of the component 900 may be carried out by electrodepositing copper on the conductive pattern 100 over the component 900 leg or bonding area, as illustrated in Figures 10A to 10E, where the layer 114 may comprise either a release layer 104 or an intermediate layer 102. The layer 114 may also comprise both a release layer 104 and an intermediate layer 102 or sections of them. A component or a semiconductor chip 900 according to Figure 10 A is attached by adhesive 910 to the conductive pattern 100, which is provided with openings 912 at the bonding areas of the component or the semiconductor chip 900. The adhesive may be conductive. Alternatively, it is feasible to use a component or a semiconductor chip provided with bumps or legs 950. Thereafter, in accordance with Figure 10B, the lower side of the component 900 may be filled with an "underfill agent" 906, which provides the final circuit board with an even surface. The same substance may be used both as the adhesive 910 and as the underfill agent 906, in which case the adhesion of the semiconductor chip and the underfill process can be performed in one and the same process step.

20 [0054] At the component 900, the circuit board material 200 may be provided with an opening, which may be filled with another material in the same way as described above in connection with Figure 9D. In accordance with Figure 10C, the component 900 may be attached to the circuit board material 200 together with the conductive pattern 100 and any underfill agent 906. 25 The auxiliary substrate is removed and openings 920 are formed in the layer 114 by laser machining, for example, at the bonding areas, bumps or legs 950 of the component. Remaining adhesive can also be removed by laser machining. Then an electric contact is formed between the component 900 leg 950 and the conductive pattern 100 using, for example, chemical or electrolytic coppering or their combination. In accordance with Figure 10D, the intermediate layer 102 may, before contacting, be covered with a patterned resist 922 to avoid depositing copper 924 on the whole sample area. A completed circuit board 1000, which may be a printed circuit board, with embedded components is obtained when any resist is removed and the layer 114 etched, as illustrated 35 in Figure 10E.

[0055] The component/components and/or semiconductor chips may naturally be embedded in a single-layer circuit board or in different layers of a multi-layer circuit board.

[0056] The component/components and/or semiconductor chips  
5 may naturally also be embedded in 2.5D and 3D structures.

[0057] Figure 11 illustrates a "from a roll to a roll" process where a layer structure including a conductive pattern can be produced as a continuous process. In this solution, auxiliary substrate ribbon is fed from a roll 1100 to another roll 1102. A release layer 104 is formed on a conductive auxiliary substrate 106 by means 1104 for producing a release layer. The conductive auxiliary substrate may be made of copper or provided with a copper surface. An intermediate layer 102 is formed on the release layer 104 by means 1106 for producing an intermediate layer. Resist spreading means 1108 are used for forming a patterned resist layer 108 on the intermediate layer 102. A conductive pattern 100 is electrodeposited on the intermediate layer 102 in openings in the resist layer 108 by means 1110 for producing a conductive pattern.  
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[0058] Figure 12 is a flow chart illustrating a method of producing a conductive pattern. In step 1200, a separating layer 101 is formed on an auxiliary substrate 106, where at least the surface is conductive. In step 1202, a patterned resist layer 108 is formed on the separating layer 101. In step 1204, a conductive pattern 100 is electrodeposited on the separating layer 101 in openings in the patterns of the resist layer 108.  
20

[0059] Figure 13 is also a flow chart illustrating a method of producing a conductive pattern. In step 1300, a patterned resist layer 108 is formed on an auxiliary substrate 106, where at least the surface is conductive. In step 1302, a separating layer 101 is formed on the auxiliary substrate 106 in openings in the patterns of the resist layer 108. In step 1304, a conductive pattern 100 is electrodeposited on the separating layer 101 in the openings in the pattern of the resist layer 108. Both in the case according to Figure 12 and in the case according to Figure 13, at least the auxiliary substrate 106 is removable from the layer structure thus formed.  
25  
30

[0060] Figure 14 illustrates a production method of a circuit board. The method employs at least one auxiliary substrate 106 with a conductive surface. In step 1400, at least one separating layer 101 is formed on each auxiliary substrate 106. In step 1402, a patterned resist layer 108 is formed on each separating layer 101. In step 1404, a conductive pattern 100 is electro-  
35

deposited on each separating layer 101 in openings in the patterns of the resist layer 108. In step 1406, the at least one conductive pattern is embedded and attached to electricity insulating material 200. In step 1408, the auxiliary substrate 106 is mechanically removed from the rest of the layer structure.

5           **[0061]** Figure 15 also illustrates a production method of a circuit board. The method employs at least one auxiliary substrate 106 with a conductive surface. In step 1500, a patterned resist layer 108 is formed on each auxiliary substrate 106. In step 1502, at least one separating layer 101 is formed on each auxiliary substrate 106 in openings in the patterns of the resist layer 108.  
10 In step 1504, a conductive pattern 100 is electrodeposited on each separating layer 101 in the openings in the patterns of the resist layer 108. In step 1506, the at least one conductive pattern 100 is embedded and attached to electricity insulating material 200. In step 1508, the auxiliary substrate 106 is mechanically removed from the rest of the layer structure.

15           **[0062]** A general advantage of the solution described is that there are no adverse local variations in height in the surface of a completed circuit board. A further advantage of the solution described is that both rigid and flexible circuit boards can be produced.

**[0063]** In the following, two examples illustrating the solution described will be examined. For example, a copper film with a thickness of 100  
20  $\mu\text{m}$  is coated in an electrolytic bath with a release layer having a thickness of 20 nm using the Atotech Trichrome plus electrolysis bath. Thereafter, the sample is rinsed and an intermediate layer of copper is deposited on it using the Atotech Cupracid BL-CT bath with a current density of  $1.5 \text{ A/dm}^2$ . The average  
25 thickness of the deposited layer may be  $3.5 \mu\text{m}$ . Thereafter, the surface of the deposited thin copper layer may be microetched and coated with a negative dry film resist with a thickness of  $38 \mu\text{m}$ , which is patterned with the desired pattern. A conductive pattern may be deposited in the openings in the resist pattern using the Atotech Cuparic Acid BL-CT bath with a current density of  $1.5$   
30  $\text{A/dm}^2$ . The average thickness of the conductive pattern may be  $25 \mu\text{m}$ . The upper surface of the conductive pattern may be roughened in an acid microetch and the resist removed. The conductive pattern thus produced can be pressed together with Hitachi GEA 67 b-state epoxy in a vacuum press at a pressure of 15 bar by increasing the temperature  $6^\circ\text{C/min}$  up to  $190^\circ\text{C}$ , which  
35 final temperature may be maintained for one hour. After the sample has cooled down, the copper film used as a temporary deposition substrate can be re-

moved from the sample surface by pulling. It can also be visually noted that the chrome film, which is seen as a layer darker than the copper layer, is removed with the temporary deposition substrate. Thereafter, the thin copper intermediate layer on the sample surface can be etched off. The final result will be a one-sided circuit board whose surface is in one plane and where the conductors are embedded in the circuit board material.

**[0064]** In the second example, a copper film with a thickness of 100  $\mu\text{m}$  is coated in an electrolytic bath with a release layer having a thickness of 20 nm using the Atotech Trichrome plus electrolysis bath. Thereafter, the sample is rinsed and an intermediate layer of copper is deposited on it using the Atotech Cupracid BL-CT bath with a current density of 1.5 A/dm<sup>2</sup>. The average thickness of the deposited layer may be 1  $\mu\text{m}$ . Thereafter, an AZ4562 resist may be spread on the thin copper layer and patterned with the desired pattern. A conductive pattern may be deposited in the openings in the resist pattern using the Atotech Cuparic Acid BL-CT bath with a current density of 1.5 A/dm<sup>2</sup>. This provides a conductive pattern with an average thickness of 9  $\mu\text{m}$ . The upper surface of the conductive pattern may be roughened in an acid micro-etch and the resist removed. The conductive pattern thus produced can be pressed together with Hitachi GEA 67 b-state epoxy in a vacuum press at a pressure of 15 bar by increasing the temperature 6°C/min up to 190°C, which final temperature may be maintained for one hour. After the sample has cooled down, the copper film used as a temporary deposition substrate can be removed from the sample surface by pulling. It can also be visually noted that the chrome film, which is seen as a layer darker than the copper layer, is removed with the temporary deposition substrate. Thereafter, the thin copper intermediate layer on the sample surface can be etched. The final result will be a one-sided circuit board whose surface is in one plane and where the conductors are embedded in the circuit board material. Even narrow conductors and conductor spaces (for example 6  $\mu\text{m}$ ) can be formed reliably.

**[0065]** Material combinations other than the ones used in the examples described may also be employed.

**[0066]** Even though the invention was described with reference to examples according to the accompanying drawings, it is clear that the invention is not limited thereto but it may be modified in various ways within the scope of the appended claims.

## CLAIMS

1. A method of producing a conductive pattern, **characterized** by forming (1200) a separating layer (101) on an auxiliary substrate (106), where at least the surface is conductive, forming (1202) a patterned resist layer (108) on the separating layer (101), electrodepositing a conductive pattern (100) on the separating layer (101) in openings in the patterns of the resist layer (108), at least the auxiliary substrate (106) being mechanically removable from the layer structure formed.
2. A method according to claim 1, **characterized** by forming the separating layer (101) by forming a release layer (104) on the auxiliary substrate (106) and by forming an intermediate layer (102) on the release layer (104).
3. A method according to claim 1, **characterized** by forming the separating layer (101) by forming a release layer (104) on the auxiliary substrate (106).
4. A method according to claim 1, **characterized** by forming a temporary auxiliary substrate (106) where at least the surface is made of copper.
5. A method according to claim 1, **characterized** in that the conductive pattern (100) comprises a plurality of layers made of different metals.
6. A method according to claim 1, **characterized** in that the auxiliary substrate (106) is made of flexible copper ribbon.
7. A method according to claim 1, **characterized** by forming the release layer (104) of metal having a thickness less than 1  $\mu\text{m}$ .
8. A method according to claim 1, **characterized** by forming the release layer (104) of electrolytically coated chrome or nickel.
9. A method according to claim 1, **characterized** by forming the release layer (104) of organic material.
10. A method according to claim 1, **characterized** by electrodepositing the intermediate layer (102) of copper.

11. A method according to claim 1, **characterized** by forming the conductive pattern (100) as a continuous process by a "from a roll to a roll" method.

12. A method according to claim 1, **characterized** by using a photoresist as the resist (108).

13. A method according to claim 1, **characterized** by pressing the resist (108) in the patterned form on the separating layer (101).

14. A method according to claim 1, **characterized** by roughening the intermediate layer (102) chemically before spreading the resist (108) to improve adhesion.

15. A method according to claim 1, **characterized** by roughening the surface of the conductive pattern (100) to increase adhesion for attachment to the circuit board material (200).

16. A method according to claim 1, **characterized** by forming the conductive pattern so that it has more than 2 dimensions.

17. A method of producing a conductive pattern, **characterized** by

forming (1300) a patterned resist layer (108) on an auxiliary substrate (106), where at least the surface is conductive,

forming (1302) a separating layer (101) on the auxiliary substrate in openings in the patterns of the resist layer (108),

electrodepositing (1304) a conductive pattern (100) on the separating layer (101) in the openings in the patterns of the resist layer (108), at least the auxiliary substrate (106) being mechanically removable from the layer structure formed.

18. A method of producing a circuit board, **characterized** by the method employing at least one auxiliary substrate (106) with a conductive surface,

forming (1400) at least one separating layer (101) on each auxiliary substrate (106),

forming (1402) a patterned resist layer (108) on each separating layer (101),

electrodepositing (1404) a conductive pattern (100) on each separating layer (101) in openings in the patterns of the resist layer (108),

embedding and attaching (1406) the at least one conductive pattern (100) to electricity insulating material (200), and

removing (1406) at least the auxiliary substrate (106) from the rest of the layer structure mechanically.

19. A method according to claim 18, **characterized** by forming the separating layer (101) by forming a release layer (104) on the auxiliary substrate (106) and by forming an intermediate layer (102) on the release layer (104).

20. A method according to claim 18, **characterized** by forming the separating layer (101) by forming a release layer (104) on the auxiliary substrate (106).

21. A method according to claim 18, **characterized** by forming a multi-layer auxiliary substrate where conductive patterns (100) are at least in two layers and connecting different conductive patterns electrically to each other.

22. A method according to claim 18, **characterized** by removing the resist layer (108) before embedding and attaching the conductive pattern (100) to the electricity insulating material (200).

23. A method according to claim 18, **characterized** by forming a multi-layer circuit board by folding a layer structure comprising a temporary auxiliary substrate (106), a separating layer (101) and a conductive pattern (100) to cover at least part of the both sides of the insulating material (200).

24. A method according to claim 18, **characterized** by connecting at least two conductive patterns (100) in different layers electrically to each other by electrodepositing metal.

25. A method according to claim 18, **characterized** by forming at least one component (800, 900) which is to be connected to the conductive pattern and embedded in the circuit board material (200) by electrodepositing each component (800) at an opening in the resist (108) in the intermediate layer (102).

26. A method according to claim 18, **characterized** by forming at least one component (800) at a desired point in the intermediate layer (102) by pressing and embedding the component in the circuit board material (200).

27. A method according to claim 18, **characterized** by forming the conductive pattern so that it has more than 2 dimensions.

28. A method according to claim 18, **characterized** by attaching at least one component (900) to the conductive pattern (100) and embedding the component in the circuit board.

29. A method according to claim 28, **characterized** by connecting the at least one component to the conductive pattern (100) by conductive adhesive or by soldering.

30. A method according to claim 28, **characterized** by using a  
5 flip chip as the component (900).

31. A method according to claim 28, **characterized** by using a bumped component as the component (900).

32. A method according to claim 18, **characterized** by electrically contacting at least one component (900) to the conductive pattern (100)  
10 by means of electrolytic metallization and embedding the component in the circuit board.

33. A method according to claim 28, 29, 30, 31 or 32, **characterized** by using more than one material in the same layer as the circuit board material by leaving a hole in the first connecting board material (200) at at least  
15 one embedded component (900) and filling the hole with another material (908).

34. A method of producing a circuit board, **characterized** by the method employing at least one auxiliary substrate (106) with a conductive surface,  
20

forming (1500) a patterned resist layer (108) on each auxiliary substrate (106),

forming (1502) at least one separating layer (101) on each auxiliary substrate (106) in openings in the pattern of the resist layer (108),

25 electrodepositing (1504) a conductive pattern (100) on each separating layer (101) in the openings in the patterns of the resist layer (108),

embedding and attaching (1506) the at least one conductive pattern (100) to electricity insulating material, and

removing (1508) at least the auxiliary substrate from the rest of the layer structure mechanically.

30 35. A circuit board, **characterized** in that the circuit board has a layered structure and the circuit board has been formed using in the production at least one auxiliary substrate (106) with a conductive surface, on which at least one separating layer (101) has been formed, and the circuit board comprises at least one conductive pattern (100) produced by

35 forming a patterned resist layer (108) on each separating layer (101),

electrodepositing a conductive pattern (100) on each separating layer (101) in openings in the patterns of the resist layer (108), and the circuit board has been formed by embedding and attaching the at least one conductive pattern (100) to electricity insulating material, and removing at least the auxiliary substrate (106) from the rest of the layer structure mechanically.

36. A circuit board according to claim 35, **characterized** in that the conductive pattern (100) comprises a plurality of layers made of different metals.

37. A circuit board according to claim 35, **characterized** in that the resist layer (108) has been removed before embedding and attaching the conductive pattern (100) to the electricity insulating material (200).

38. A circuit board according to claim 35, **characterized** in that at least one component (800, 900) has been formed in the conductive pattern and electrically contacted to it and the component is embedded in the electricity insulating material (200) of the circuit board.

39. A circuit board, **characterized** in that the circuit board has a layered structure and the circuit board has been formed using in the production at least one auxiliary substrate (106) with a conductive surface, and the conductive pattern is produced by

forming a patterned resist layer (108) on each auxiliary substrate (106),

forming at least one separating layer (101) on each auxiliary substrate (106) in openings in the patterns of the resist layer (108),

electrodepositing a conductive pattern (108) on each separating layer (101) in the openings in the patterns of the resist layer (108), and

the circuit board has been formed by embedding and attaching the at least one conductive pattern (100) to electricity insulating material (200), and

removing at least each auxiliary substrate (106) from the rest of the layer structure mechanically.

40. A conductive pattern, **characterized** in that the conductive pattern has been formed by using in the production at least one auxiliary substrate (106) with a conductive surface, on which at least one separating layer

(101) has been formed, and each circuit board (106) comprises at least one conductive pattern (100) produced by

forming and patterning a resist layer (108) on the separating layer (101),

5 electrodepositing a conductive pattern (100) on the separating layer (101) in openings in the patterns of the resist layer (108), each auxiliary substrate being mechanically removable from the layer structure formed.

41. A conductive pattern, **characterized** in that the conductive pattern has been formed using in the production at least one auxiliary substrate (106) with a conductive surface, on which a patterned resist layer (108) has been formed, and the conductive pattern has been produced by

10 forming a separating layer (101) on each auxiliary substrate (106) in openings in the patterns of the resist layer (108),

15 electrodepositing a conductive pattern (100) on the separating layer (104) in the openings in the patterns of the resist layer (108), each auxiliary substrate (106) being mechanically removable from the layer structure formed.

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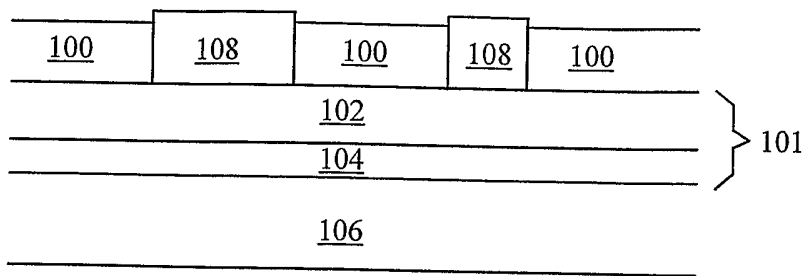


FIG. 1A

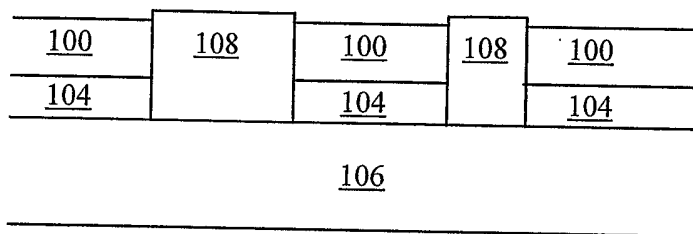


FIG. 1B

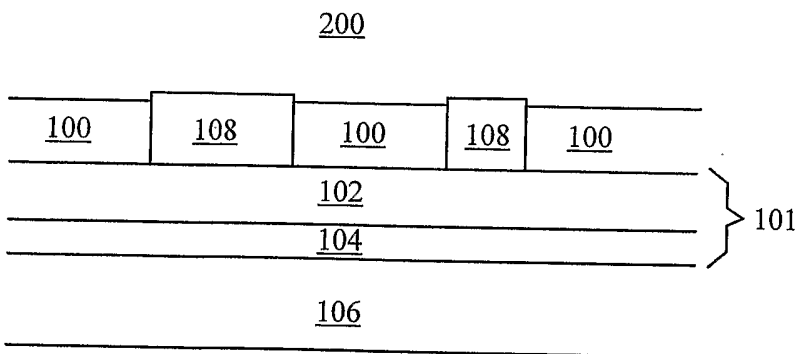


FIG. 2A

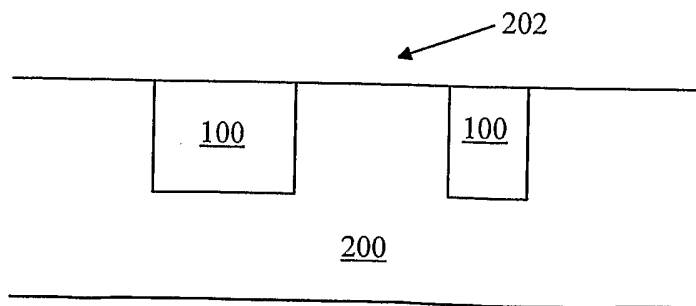


FIG. 2B

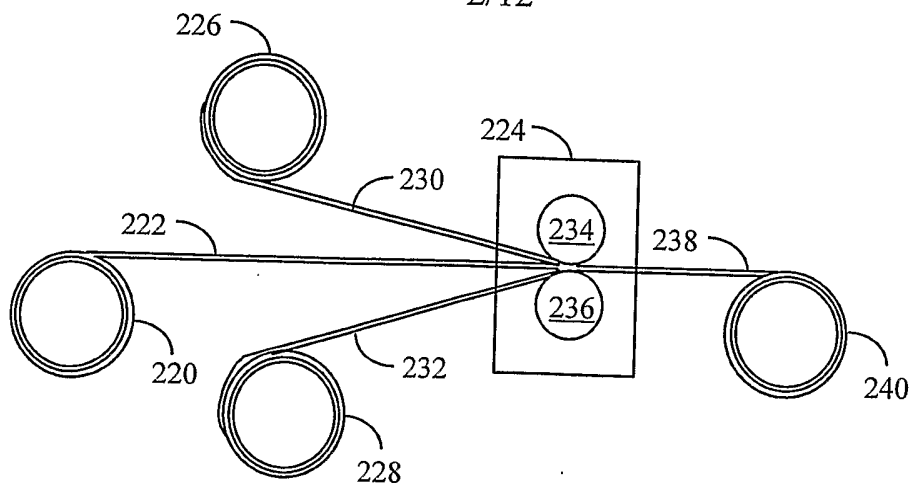


FIG. 2C

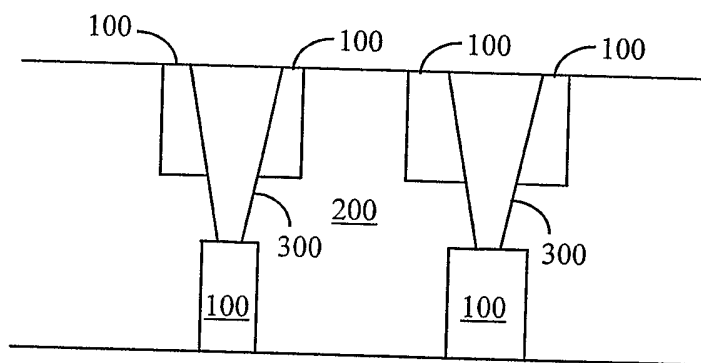


FIG. 3

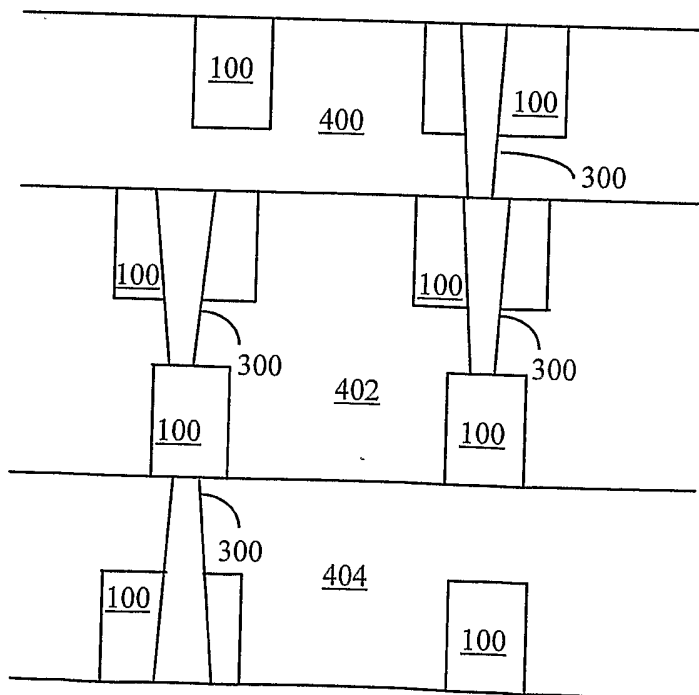


FIG. 4

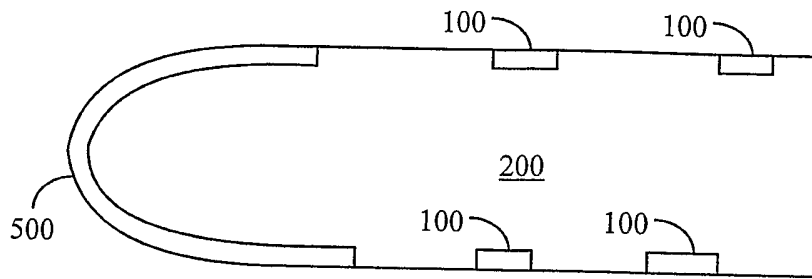


FIG. 5A

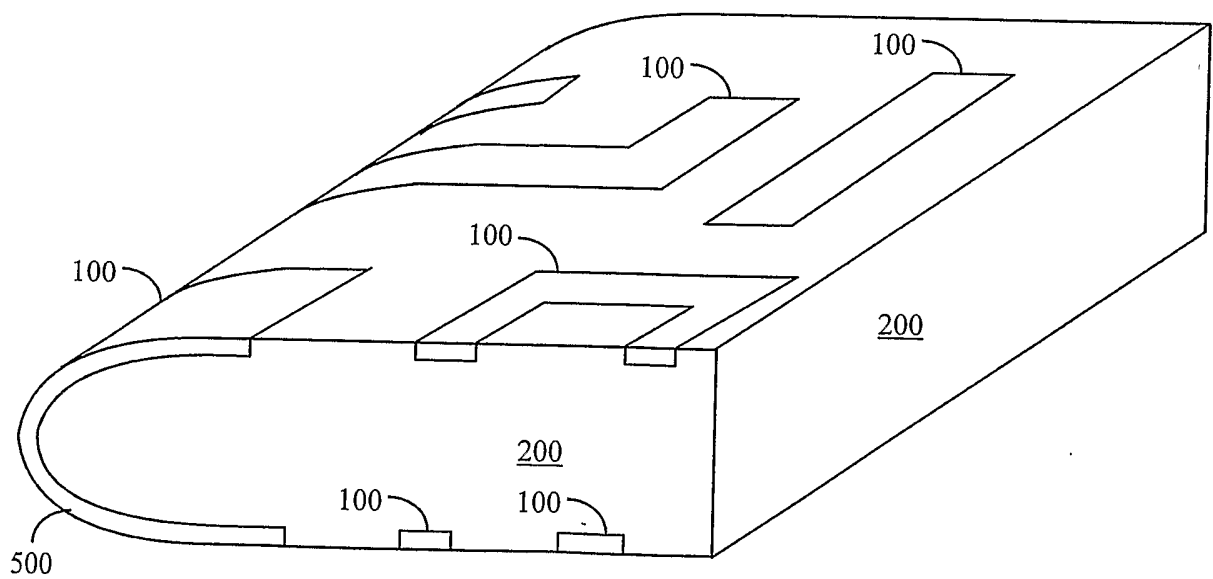


FIG. 5B

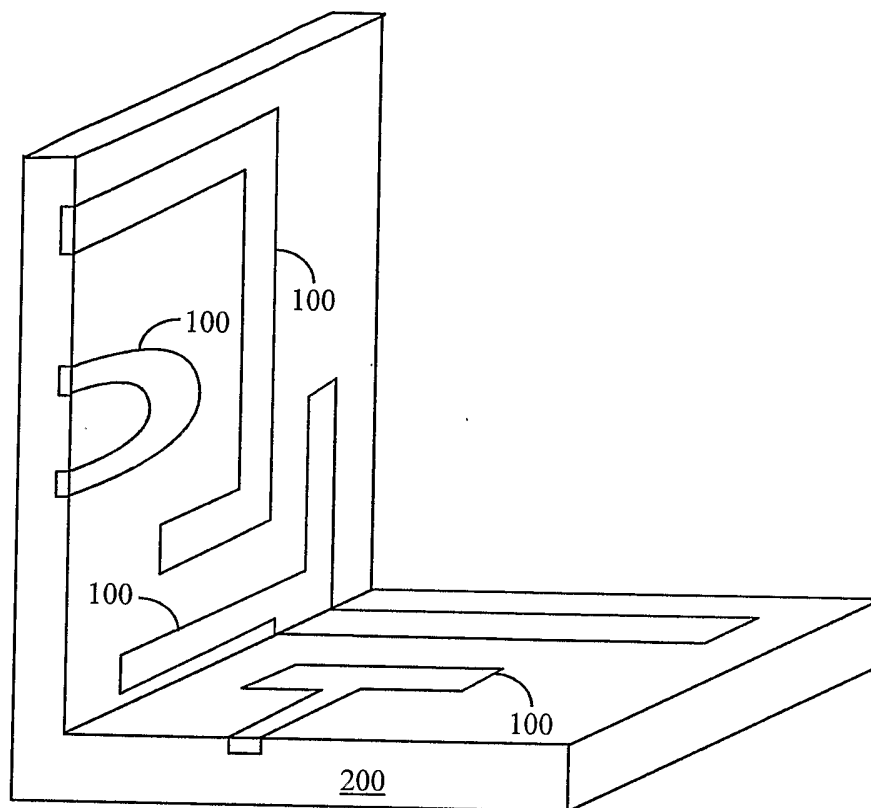


FIG. 6

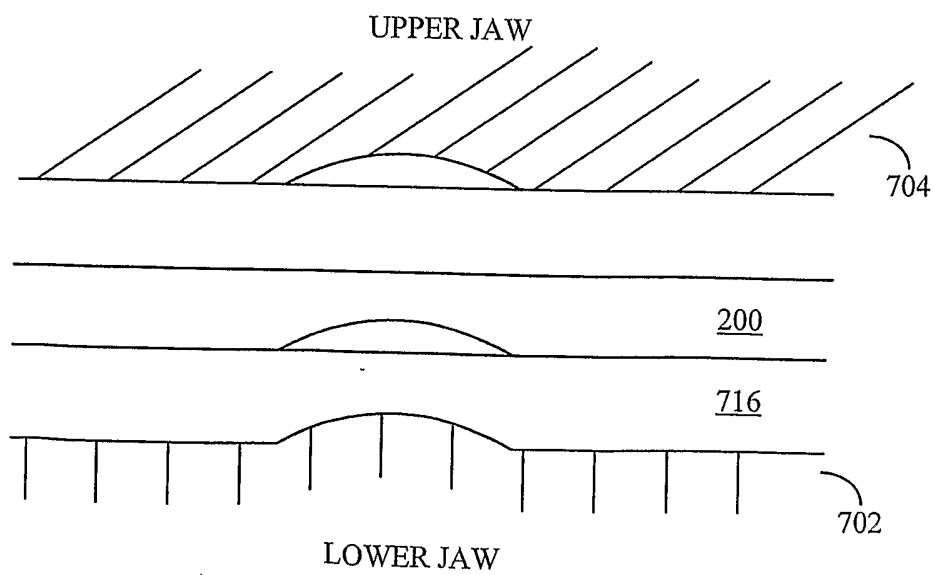


FIG. 7A

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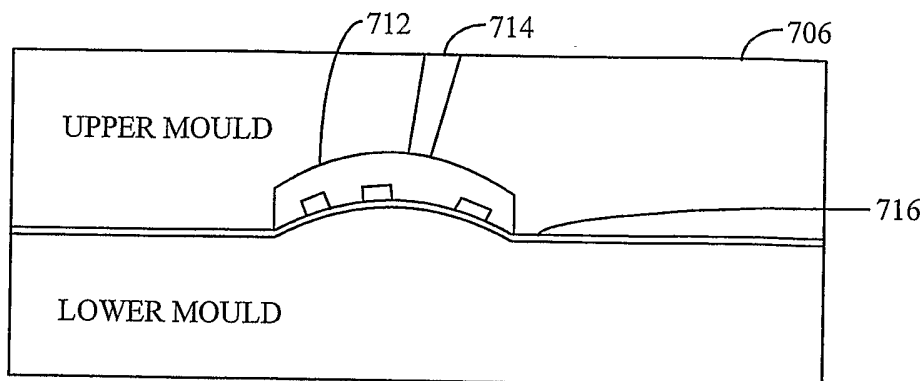


FIG. 7B

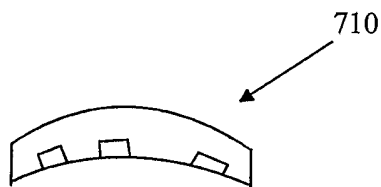


FIG. 7C

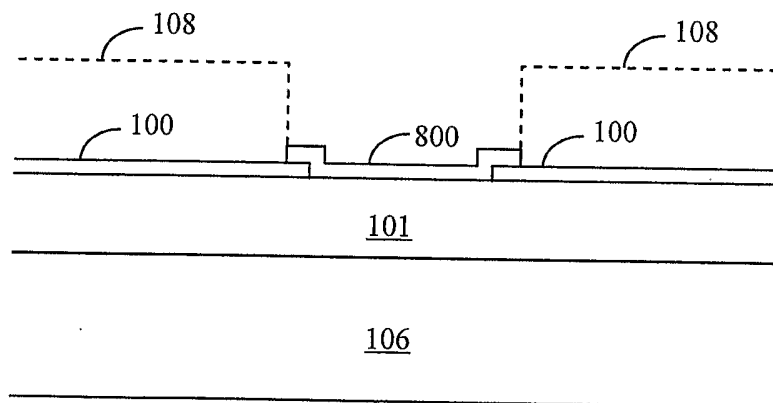


FIG. 8A

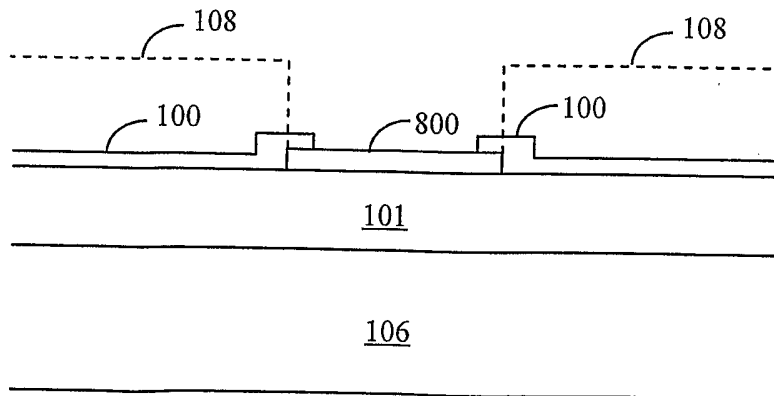


FIG. 8B

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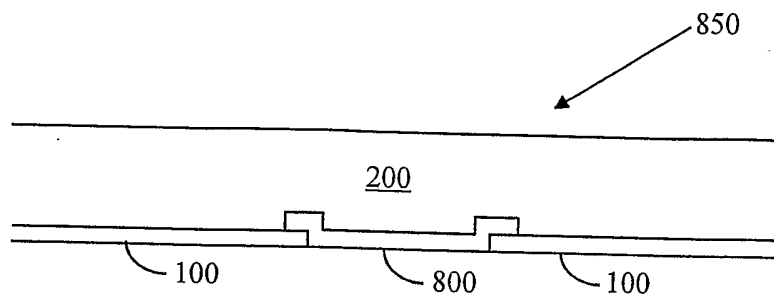


FIG. 8C

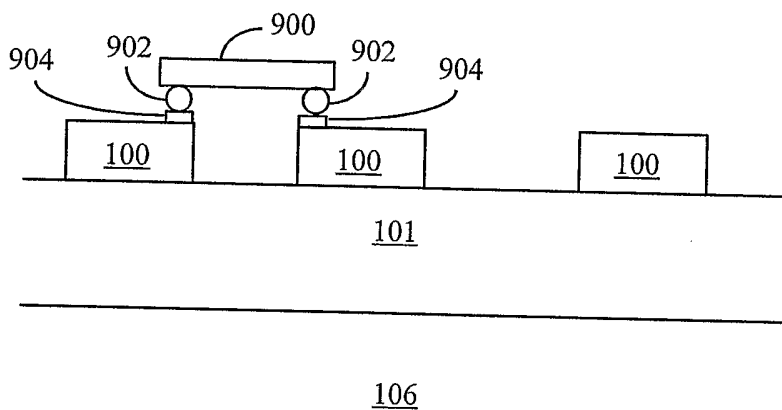


FIG. 9A

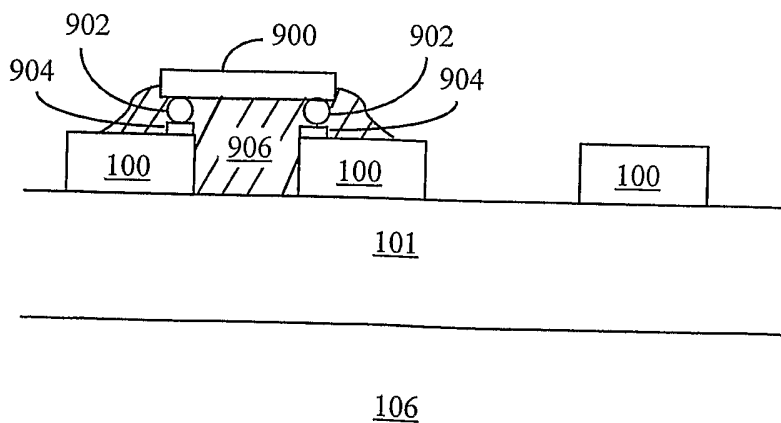


FIG. 9B

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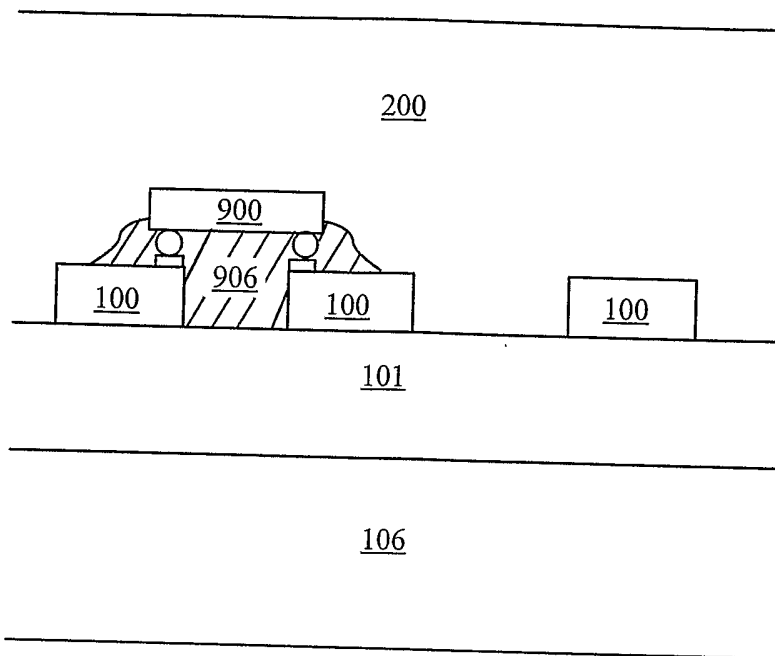


FIG. 9C

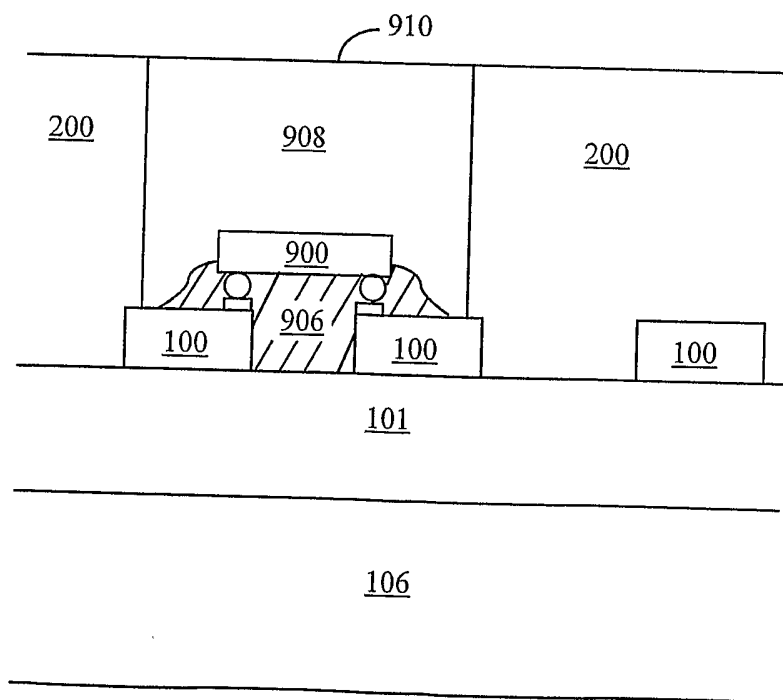


FIG. 9D

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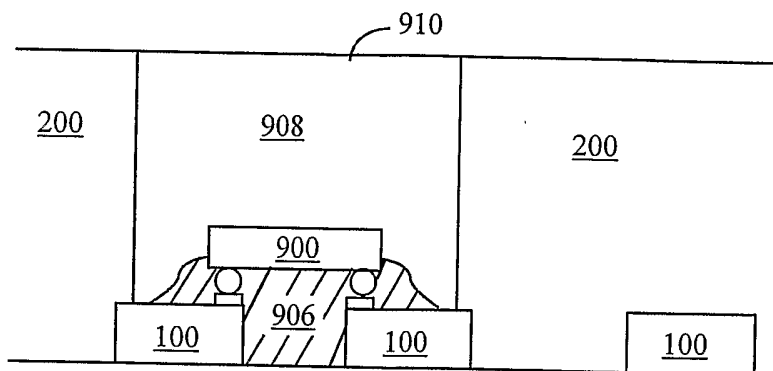


FIG. 9E

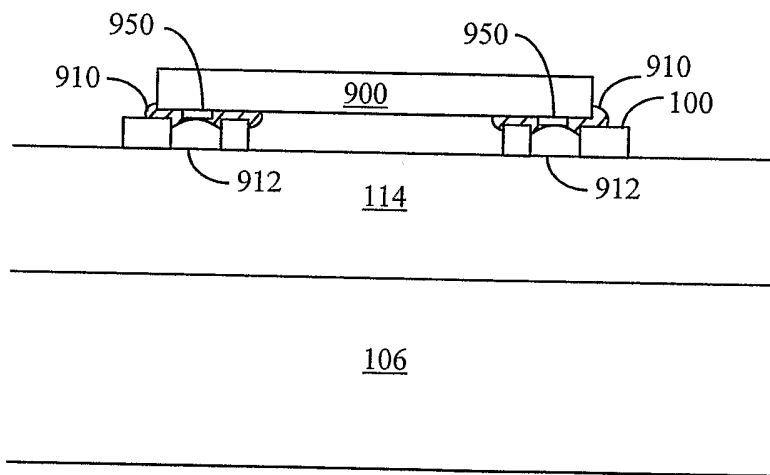


FIG. 10A

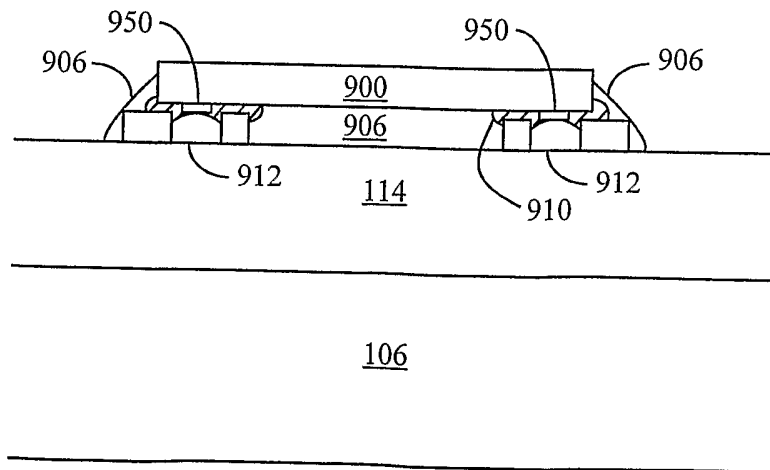


FIG. 10B

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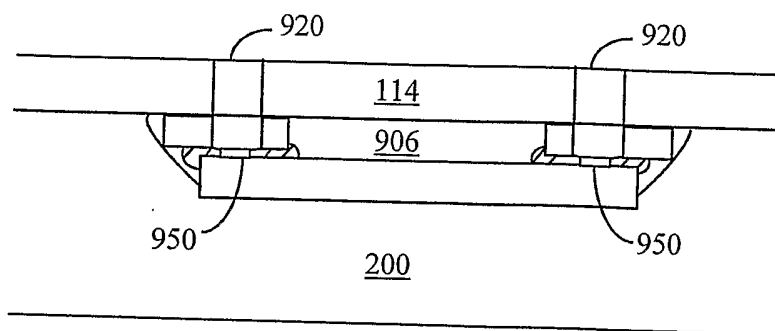


FIG. 10C

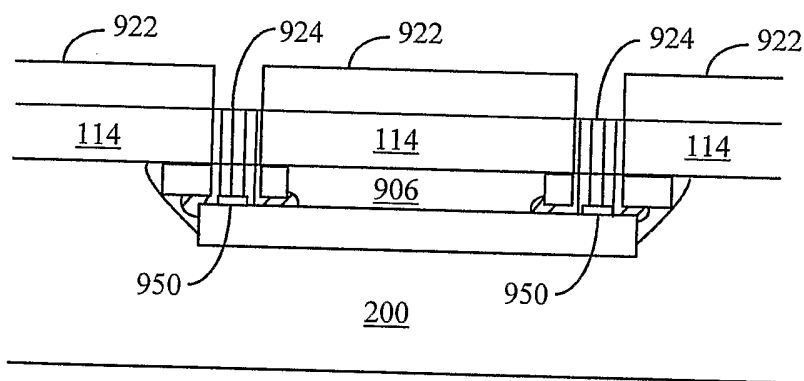


FIG. 10D

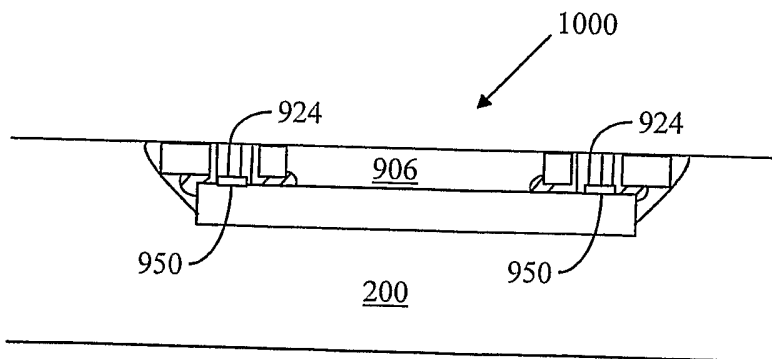


FIG. 10E

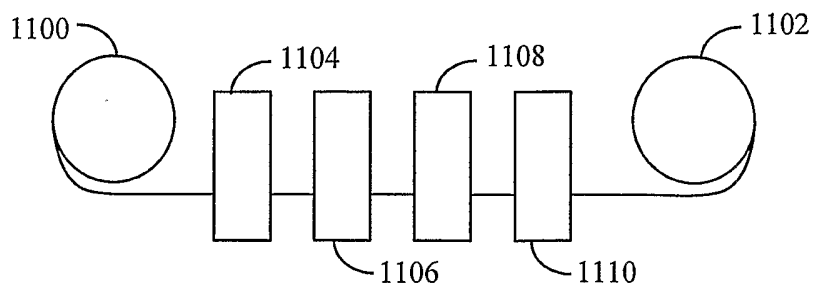


FIG. 11

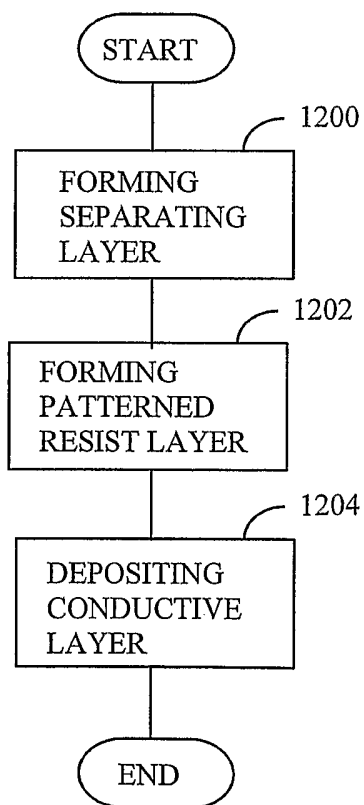


FIG. 12

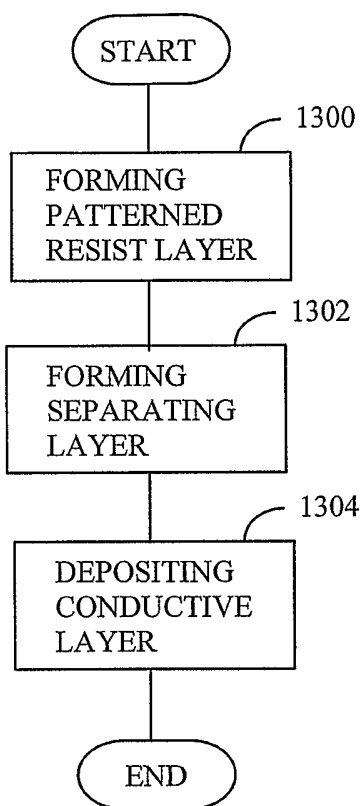


FIG. 13

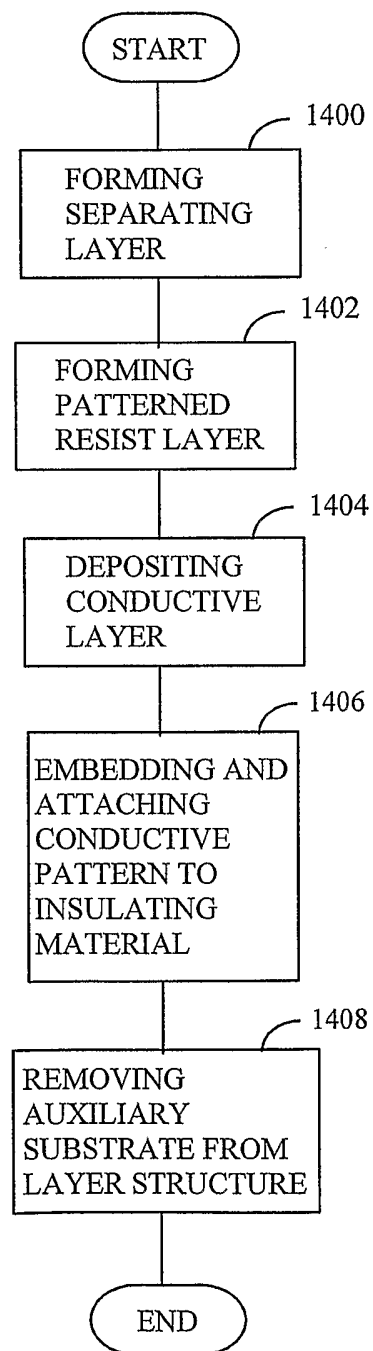


FIG. 14

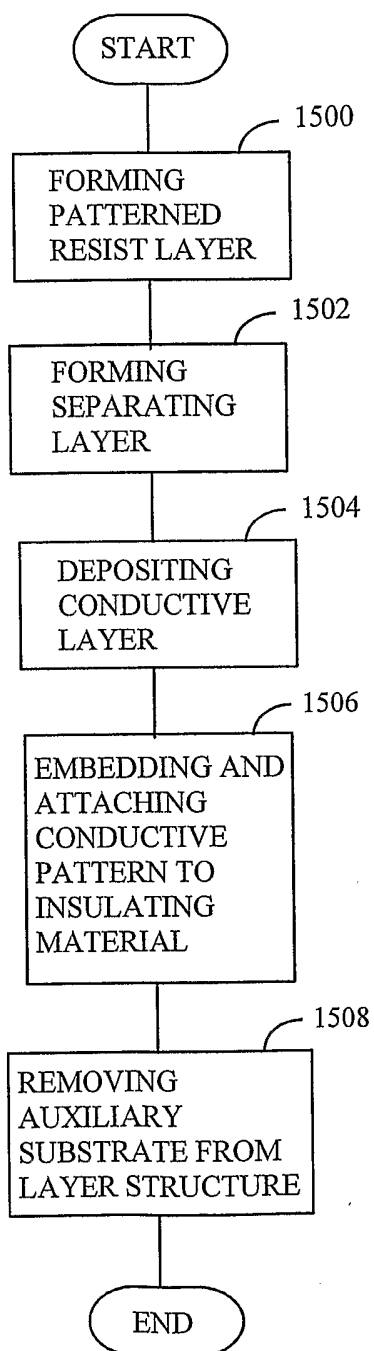


FIG. 15

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI2005/050466

A. CLASSIFICATION OF SUBJECT MATTER See extra sheet According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC8 : H05K  Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched FI, SE, NO, DK  Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0078969 A1 (KANZAWA et al.) 29 April 2004 (29.04.2004)	1, 3, 4, 8, 12, 18, 20, 21, 22, 23, 28, 29, 30, 31, 32, 35, 37, 40
Y	paragraphs [0022], [0065] -[0068], [0075]-[0077], [0079]-[0085], [0091]	34, 39
X	US 4606787 A (PELLIGRINO) 19 August 1986 (19.08.1986)	1, 3, 10, 12, 18, 20, 21, 22, 24, 35, 37, 40
Y	column 4 lines 61-68, column 5 line 37 - column 6 line 60, column 7 lines 26-29, column 8 lines 27-47	7, 25, 26, 34, 38, 39
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input checked="" type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed		"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search 15 March 2006 (15.03.2006)		Date of mailing of the international search report 21 March 2006 (21.03.2006)
Name and mailing address of the ISA/FI National Board of Patents and Registration of Finland P.O. Box 1160, FI-00101 HELSINKI, Finland Facsimile No. +358 9 6939 5328		Authorized officer Tapani Salonen Telephone No. +358 9 6939 500

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI2005/050466

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 792920 A (PHILIPS ELECTRICAL IND LTD) 09 April 1958 (09.04.1958)	1, 3, 5, 10, 12, 13, 18, 20, 22, 35, 36, 37, 40
Y	page 1 lines 84-87, page 2 lines 11-16, 48-92 and 102-109	6, 7, 11, 16, 25, 26, 27, 34, 38, 39
X	US 4790902 A (WADA et al.) 13 December 1988 (13.12.1988)	1, 3, 4, 8, 10, 12, 13, 15, 18, 20, 22, 35, 37, 40
Y	column 6 line 48 - column 7 line 16, column 8 lines 7-15, column 9 lines 15-31, column 10 lines 19-35 and 48-61, column 11 lines 30-44, column 12 lines 25-29	6, 7, 11, 16, 25, 26, 27, 34, 38, 39
X	JP 9064514 A (MATSUSHITA ELECTRIC WORKS LTD) 07 March 1997 (07.03.1997)	1, 2, 9, 10, 12, 18, 19, 22, 35, 37, 40
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