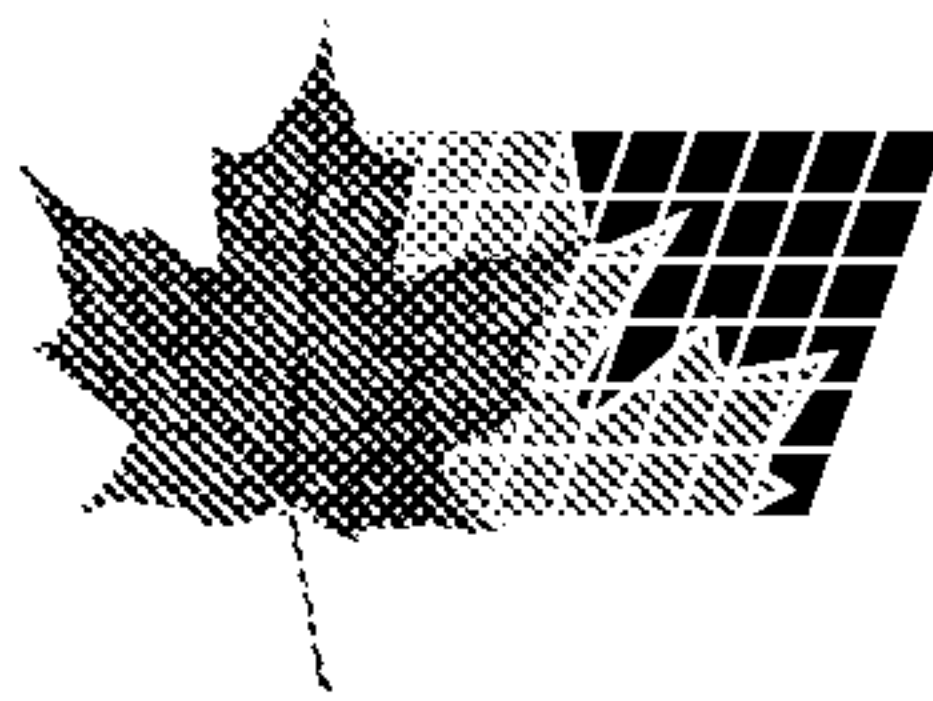




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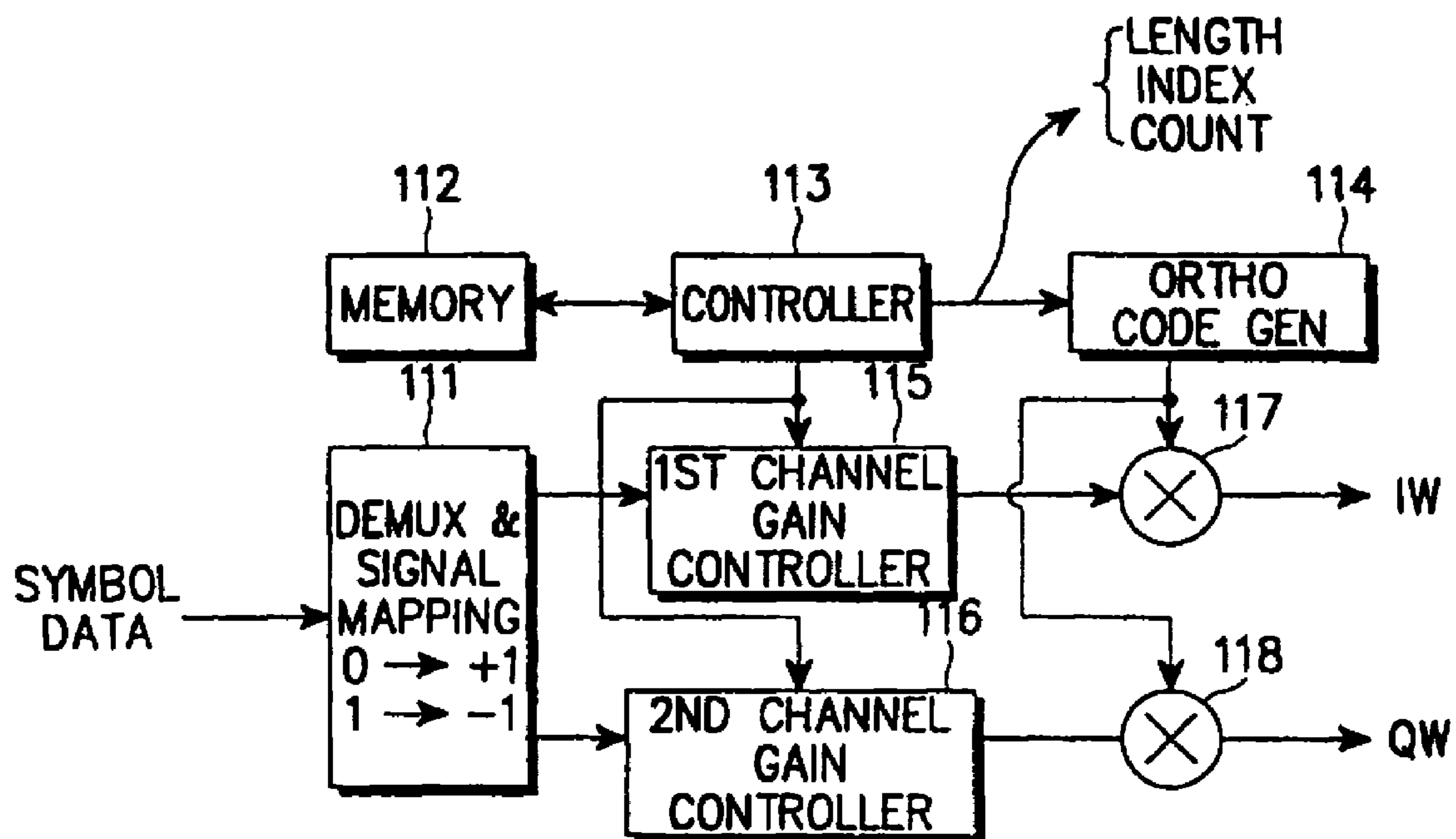
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(30) 1998/08/28 (1998/35118) KR

(54) **DISPOSITIF ET PROCEDE DE GENERATION DE CODES
ORTHOGONAUX DANS UN SYSTEME DE
COMMUNICATION MOBILE**

(54) **DEVICE AND METHOD FOR GENERATING ORTHOGONAL
CODES IN MOBILE COMMUNICATION SYSTEM**



(57) L'invention concerne un dispositif et un procédé de génération de codes orthogonaux de différentes longueurs en fonction de vitesses de modulation. On calcule une longueur de code orthogonal correspondant à une vitesse de modulation variable pour déterminer un nombre de bits effectif. On génère de façon séquentielle une valeur de compte d'élément jusqu'à une valeur maximale, cette valeur pouvant être comptée grâce au nombre de bits effectifs. On génère un code orthogonal par une opération logique d'un indice de code orthogonal qui est converti en nombre binaire du nombre de bits effectif et des valeurs de compte d'élément générées de façon séquentielle.

(57) A device and method for generating orthogonal codes differing in length according to symbol rates. An orthogonal code length corresponding to a variable symbol rate is calculated to determine an effective bit number. A chip count value is sequentially generated up to a maximum value, which can be counted by the effective bit number. An orthogonal code is generated by a logic operation of an orthogonal code index which is converted into the binary number of the effective bit number and the sequentially generated chip count values.

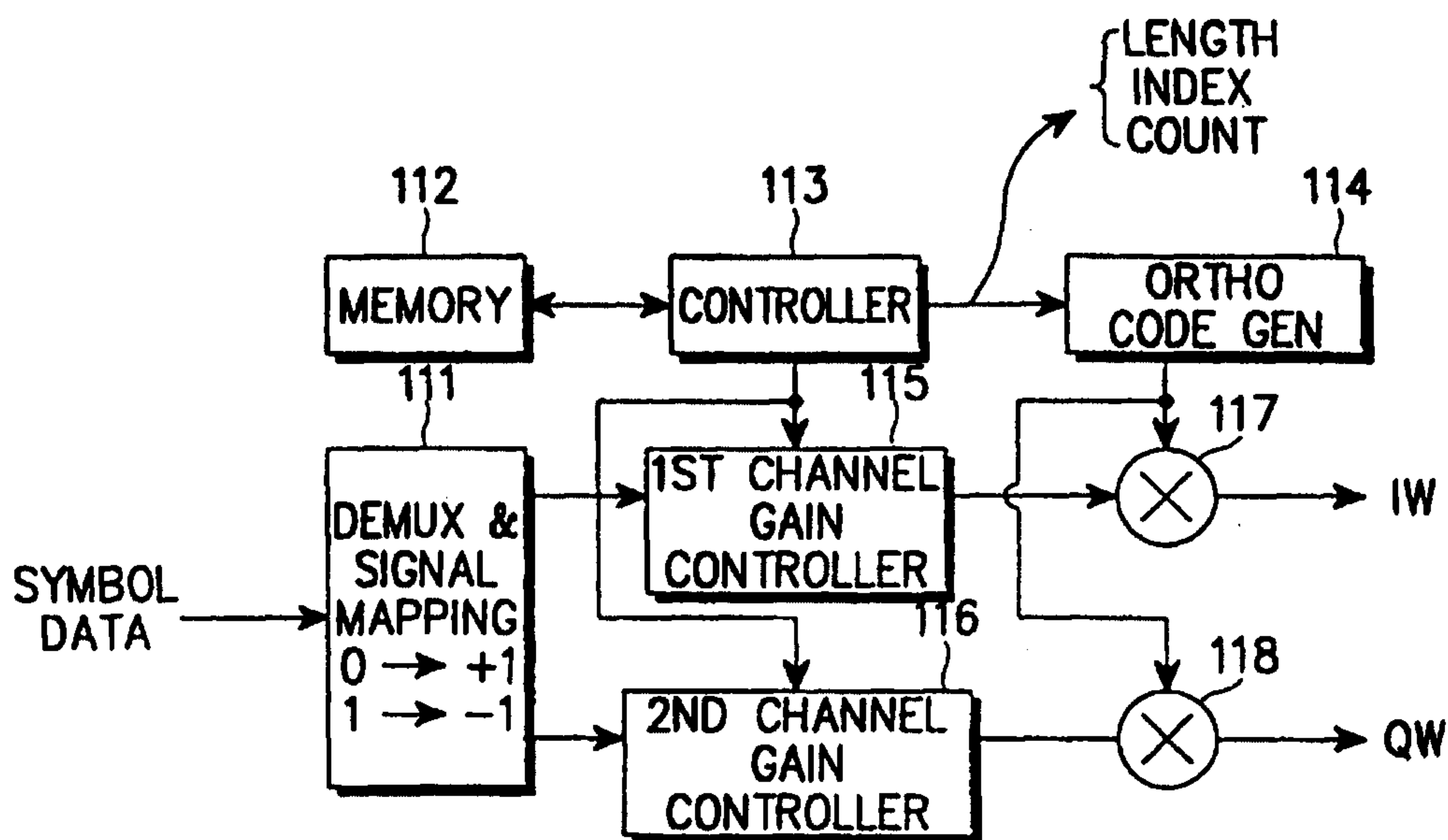


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(54) Title: DEVICE AND METHOD FOR GENERATING ORTHOGONAL CODES IN MOBILE COMMUNICATION SYSTEM



(57) Abstract

A device and method for generating orthogonal codes differing in length according to symbol rates. An orthogonal code length corresponding to a variable symbol rate is calculated to determine an effective bit number. A chip count value is sequentially generated up to a maximum value, which can be counted by the effective bit number. An orthogonal code is generated by a logic operation of an orthogonal code index which is converted into the binary number of the effective bit number and the sequentially generated chip count values.

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DEVICE AND METHOD FOR GENERATING ORTHOGONAL CODES IN MOBILE COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to a device and method for generating orthogonal codes in a mobile communication system, and in particular, to a device and method for generating orthogonal codes differing in length according to various symbol rates.

2. Description of the Related Art

10 Typically, orthogonal codes are used for spreading channels and for distinguishing between channels as identifiers. In a conventional transmitter using an IS-95 CDMA system, a Walsh code (which is one form of the orthogonal code) having a 64-chip length has been used to maintain orthogonality between
15 channels and to spread bands. By using the 64-chip Walsh code, a band spreading rate of 1.2288 Mcps is obtained, since the symbol rates of coded data for various channels which are provided from a modulator of the transmitter to a spreader are uniformly maintained at 19.2 Kbps. For this, a 64×64 Walsh code table has been used.

20 However, in a CDMA-2000 (Code Division Multiple Access-2000) mobile communication system applied to an IMT-2000 system, for example, symbol rates of data provided to a spreader in the process of modulating forward channels differ according to channel types, and thus Walsh codes having lengths
25 which vary with the channels are needed.

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To generate Walsh codes having different lengths in a conventional way, Walsh code tables are provided which correspond to the different lengths. This requires multiple varying memories, while still making it difficult to flexibly use
5 Walsh codes having different lengths according to various symbol rates.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a device and
10 method for generating orthogonal codes differing in length according to various symbol rates in a mobile communication system.

It is another object of the present invention to provide a device and method for generating orthogonal codes by an orthogonal code index and a chip
15 count in a mobile communication system.

In accordance with one aspect of the present invention, a device for generating orthogonal codes in a mobile communication system includes a memory having registers for respectively storing an effective bit number, an
20 orthogonal code index and a chip count value, and an orthogonal code generating circuit for sequentially generating the chip count value up to a maximum value which can be counted by the effective bit number, and generating an orthogonal code by logic operation of the orthogonal code index and the sequentially generated chip count values.

25

In accordance with another object of the present invention, a method for generating orthogonal codes in a mobile communication system includes the steps

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of: calculating an orthogonal code length corresponding to a variable symbol rate; determining an effective bit number by the calculated orthogonal code length; sequentially generating a chip count value up to a maximum value which can be counted by the effective bit number; converting an orthogonal code index into a binary number of the effective bit number; and performing a logic operation of the orthogonal code index converted into the binary number and the sequentially generated chip count values to generate an orthogonal code.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

FIG. 1 is a block diagram illustrating a modulator of a mobile communication system according to an embodiment of the present invention;

FIG. 2 is a diagram illustrating an orthogonal code generating process expressed by an equation according to an embodiment of the present invention; and

FIG. 3 is a circuit diagram illustrating the orthogonal code generator illustrated in FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described hereinbelow with reference to the accompanying drawings. In the following

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description, well-known functions or constructions are not described in detail as not to obscure the invention in unnecessary detail.

FIG. 1 illustrates a modulator of a mobile communication system according to an embodiment of the present invention. The description of the modulator will be focused on parts relating to orthogonal spreading.

Referring to FIG. 1, a demultiplexer (DEMUX) & signal mapping circuit 111 demultiplexes input symbol data (or coded data) to separately output an I-channel (or first channel) signal and a Q-channel (or second channel) signal. The DEMUX & signal mapping circuit 111 also converts a level of the symbol data, for instance, "0" into "+1" and "1" into "-1". First and second channel gain controllers 115 and 116 control gains of the first and second channel signals output from the DEMUX & signal mapping circuit 111, respectively, by a gain control signal provided by a controller 113. A memory 112 stores data for various programs and data temporarily generated in the course of executing the programs. The memory 112 includes a register having information about orthogonal code lengths varying with symbol rates of channels, a register having orthogonal code indexes assigned to the channels, and a register having chip counts, which are obtained by counting one symbol to be orthogonally spread by a corresponding chip clock. The information about the orthogonal code lengths, which is described below, can be defined as a meaning to restrict an actually effective bit number of the orthogonal code index and chip count. The controller 113 controls the overall operation of the modulator. More particularly, the controller 113 reads parameters relating to generating the orthogonal code from the memory 112 and provides the parameters to an orthogonal code generator 114 of each channel generator. The orthogonal code generator 114 generates a corresponding

- 5 -

orthogonal code according to the orthogonal code length information (i.e., the effective bit number), orthogonal code index and chip count provided from the controller 113. First and second multipliers 117 and 118 multiply the first and second channel signals output from the first and second channel gain controllers 115 and 116 by the orthogonal code to generate orthogonally modulated first and second channel signals IW and QW, respectively.

In achieving a device for generating the orthogonal code according to the present invention, the memory 112, controller 113, and orthogonal code generator 114 may be indispensable constituents. To refer to both the controller 113 and orthogonal code generator 114, the term "orthogonal code generating circuit" will be used.

In the orthogonal spreading operation of the modulator above, the coded data (or symbol data) is separated by the DEMUX & signal mapping circuit 111 into the first and second channel signals. The separated signals are gain-controlled by the first and second channel gain controllers 115 and 116, as instructed by the controller 113. The gain-controlled first and second channel signals are respectively provided to the first and second multipliers 117 and 118. The controller 113 receives the orthogonal code length corresponding to a symbol rate of the coded data, the chip count and the orthogonal code index to be assigned to the channel. Those parameters are obtained by accessing the registers contained in the memory 112 and provided to the orthogonal code generator 114 of a corresponding channel generator. The orthogonal code generator 114 then generates a corresponding orthogonal code through a program stored in its internal DSP (Digital Signal Processor) or through an ASIC (Application Specific Integrated Circuit). The generated orthogonal code is provided to the multipliers 117 and 118. The multipliers 117 and 118 respectively multiply the gain-

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controlled first and second channel signals output from the first and second channel gain controllers 115 and 116 by the orthogonal code, to generate the orthogonally modulated first and second channel signals IW and QW corresponding to the I and Q channels, respectively.

5

The process of generating the orthogonal code will now be described in more detail. The orthogonal code generating process is executed by the orthogonal code generating circuit, which consists of the controller 113 and the orthogonal code generator 114. It should be noted that the orthogonal code length information is used interchangeably as the effective bit number.

10

The orthogonal code generating process is broadly divided into two steps; a first step of generating information needed to generate the orthogonal code, and a second step of generating the orthogonal code based on the generated information. The information needed is the orthogonal code index assigned to each channel, the chip count obtained by counting one symbol period by a chip clock, and the orthogonal code length.

15

The first step of generating the information based on the orthogonal code index, chip count and orthogonal code length will now be described.

20

In the CDMA-2000 system, a symbol rate of data provided to a spreader in the process of modulating forward channels differs according to channel types, unlike the conventional IS-95 CDMA system. To uniformly adjust a band spreading rate, orthogonal code lengths become different according to the different symbol rates. For instance, the orthogonal code lengths may have 8, 16, 32, 64, 128, 256, 512, and 1024 chips. If the band spreading rate is 3.6864 Mcps,

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and the symbol rates of data provided to the spreader are 14.4 Kbps, 28.8 Kbps, 57.6 Kbps and 115.2 Kbps, the orthogonal code lengths become 256 chips, 128 chips, 64 chips and 32 chips to produce the band spreading rate of 3.6864 Mcps. That is,

5

$$14.4 \text{ Kbps} \times 256 \text{ chips} = 3.6864 \text{ Mcps}$$

$$28.8 \text{ Kbps} \times 128 \text{ chips} = 3.6864 \text{ Mcps}$$

$$57.6 \text{ Kbps} \times 64 \text{ chips} = 3.6864 \text{ Mcps}$$

$$115.2 \text{ Kbps} \times 32 \text{ chips} = 3.6864 \text{ Mcps}$$

10

Thus, the orthogonal codes having different lengths according to the various symbol rates of data provided to the spreader are generated to obtain a uniform band spreading rate. To this goal, a processor for controlling the modulator provides information relating to the orthogonal code length to the modulator. As an example, the orthogonal code lengths varying according to the symbol rates can be expressed by 2 raised to the power of a prescribed number. For instance, $4 = 2^2$, $8 = 2^3$, $16 = 2^4$, ..., and $1024 = 2^{10}$.

15

As noted above, the base corresponding to each orthogonal code length is 2 and only the exponent differs. Therefore, the orthogonal code length information determined by the symbol rate uses the exponent. The processor provides the exponent to the modulator as orthogonal code length information I.

20

The range of an orthogonal code index n assigned to each channel and a chip count t , which is obtained by counting one symbol period using a chip clock, can flexibly be enlarged or reduced by the various orthogonal code lengths 4, 8, 16, 64, 128, ...

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More particularly, the orthogonal code index n and the chip count t are each determined within the same range of $0 \leq n, t \leq 2^I - 1$. The orthogonal code index indicates a value expressing one of the integers within the above range as a binary number of I bits. The chip count sequentially designates an integer within the above range by a binary number of I bits. Assuming that the orthogonal code length information I is 4, the orthogonal code index becomes a binary number expressing one of integers 0 to 15 as 4 bits. As the chip count, binary number values of 4 bits, that is, 0000 through 1111 are sequentially provided to designate integers ranging from 0 to 15. Although the above example restricts the bit number of the orthogonal code index and chip count to I bits, the bit number need not be restricted. Namely, it is possible to assign the bit number of the orthogonal code index and chip count up to the maximum bit number. Then all bits except actually effective bits among the assigned bit number are set to "0". The maximum bit number is determined on the basis of the longest Walsh code used in a mobile communication system. The actually effective bits represent the bit number of the orthogonal code index and chip count. For instance, if the longest Walsh code which is usable in the mobile communication system is 128 ($=2^7$) chips, the maximum bit number is 7 bits.

Consequently, if the symbol rate is designated, the orthogonal code length is determined by the designated symbol rate, and the range of the chip count and the orthogonal code index are determined by the orthogonal code length. Once the range of the chip count is determined, the chip count is sequentially increased within the determined range. The orthogonal code length, the orthogonal code index, and the increased chip count are provided as information for generating the orthogonal code. If the orthogonal code generator 114 has a function which can estimate the orthogonal code length by the orthogonal code index, the controller

- 9 -

113 need not provide the orthogonal code length information.

In the second step, the orthogonal code is generated by using the orthogonal code length information, the orthogonal code index assigned to each channel, and the chip count which are provided from the processor. That is, an algorithm is supplied with the orthogonal code length information in addition to the orthogonal code index and chip count so that the orthogonal codes of differing length can be generated.

The processor for controlling the modulator determines the orthogonal code length information based on the symbol rate and provides this information to the orthogonal code generator 114, thereby generating the orthogonal code having a variable length according to the symbol rate. The orthogonal code of a necessary length is generated by restricting the number of digits of the orthogonal code index n and chip count t expressed as a binary number through the orthogonal code length information. This can be represented by Equation 1:

[Equation 1]

$$W(I,n,t)=(n_{I-1} \times t_{I-1}) \dots (n_4 \times t_4) \oplus (n_3 \times t_3) \oplus (n_2 \times t_2) \oplus (n_1 \times t_1) \oplus (n_0 \times t_0)$$

where I is orthogonal code length information (i.e., 2, 3, 4,...), n is an orthogonal code index assigned to each channel, and t is a chip count obtained by counting one symbol period by a chip clock.

If the orthogonal code length information, the orthogonal code index and the chip count are designated by Equation 1, a corresponding one-chip orthogonal code is generated. As can be appreciated from Equation 1, an effective calculation

- 10 -

range is determined by the orthogonal code length information I. Meanwhile, the orthogonal code of one bit is obtained by logic operation of bits constituting the chip count and bits constituting the orthogonal code index within the effective calculation range. That is, the chip count and the orthogonal code index are
 5 ANDed in the unit of bits and the ANDed results are XORed.

The effective calculation range determined according to the orthogonal code length information I is illustrated in FIG. 2. If the orthogonal code length information I is 3 (=011), the range of the chip count t is 0 to 7, and the
 10 orthogonal code index n is 3 (i.e., $n_2, n_1, n_0 = 0, 1, 1$), a one-chip orthogonal code is generated using the range corresponding to a reference numeral 214 shown in FIG. 2. That is:

$$W(3,3,t) = (n_2 \times t_2) \oplus (n_1 \times t_1) \oplus (n_0 \times t_0)$$

15 where $n = (011)$ and $0 \leq t \leq 7$.

Therefore,

for $t = 0(000)$, $W(3,3,0) = (0 \times 0) \oplus (1 \times 0) \oplus (1 \times 0) = 0$;

for $t = 1(001)$, $W(3,3,1) = (0 \times 0) \oplus (1 \times 0) \oplus (1 \times 1) = 1$;

20 for $t = 2(010)$, $W(3,3,2) = (0 \times 0) \oplus (1 \times 1) \oplus (1 \times 0) = 1$;

for $t = 3(011)$, $W(3,3,3) = (0 \times 0) \oplus (1 \times 1) \oplus (1 \times 1) = 0$;

for $t = 4(100)$, $W(3,3,4) = (0 \times 1) \oplus (1 \times 0) \oplus (1 \times 0) = 0$;

for $t = 5(101)$, $W(3,3,5) = (0 \times 1) \oplus (1 \times 0) \oplus (1 \times 1) = 1$;

for $t = 6(110)$, $W(3,3,6) = (0 \times 1) \oplus (1 \times 1) \oplus (1 \times 0) = 1$; and

25 for $t = 7(111)$, $W(3,3,7) = (0 \times 1) \oplus (1 \times 1) \oplus (1 \times 1) = 0$.

Finally, an orthogonal code (0 1 1 0 0 1 1 0) is generated. The orthogonal

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code generating process based on Equation 1 can be expressed by Equation 2, which is written in C language:

[Equation 2]

```

5      Walsh(int length, int index, int count)
      {
          int i, wc = 0;
          for (i = 0; i < length; i++)
              wc = wc ^ (((index >> i) & 0x01) & ((count >> i) & 0x01))
10         return(wc);
      }

```

where i is a temporary count parameter; wc is a parameter in which a final value is to be stored; length is a parameter having an orthogonal code length information value determined according to the symbol rate; index is an orthogonal code index assigned to a channel; and count is a chip count obtained by counting one symbol period by a chip clock.

The range of the chip count differs according to the orthogonal code length as listed below in Table 1:

[Table 1]

Length	Count range	Orthogonal Code Length
2	0 – 3	4
3	0 – 7	8
4	0 – 15	16
5	0 – 31	32

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The orthogonal code generating process may be achieved by a program as shown in Equation 2 on a DSP or by algorithm such as HDL (Hardware Development Language) on an ASIC.

5

An example for achieving the orthogonal code generator on the ASIC is illustrated in FIG. 3. Referring to FIG. 3, the orthogonal code generator includes an AND gate circuit 310 consisting of a plurality of AND gates 310_0,...,310_M-1 and an XOR gate 320. The number of AND gates constituting the AND gate circuit 310 is the same as the maximum bit number determined on the basis of the longest orthogonal code. If the orthogonal code lengths are 4, 8, 16, 32, 64 and 128 chips, the number of the AND gates is determined on the basis of 128 ($= 2^7$) chips. In this case, the number of the AND gates will be 7, which corresponds to the bit number, the orthogonal code index, and chip count. When the orthogonal code having a length shorter than the longest orthogonal code length is generated, all bits other than the actually effective bits are considered to be "0". In other words, bits except the actually effective bits are considered masked to "0".

10

15

The AND gates 310_0,...,310_M-1 each perform an AND operation of a corresponding bit of the orthogonal code index and a corresponding bit of the chip count. The XOR gate 320 performs an XOR operation of the outputs of the AND gate circuit 310 to generate one bit constituting the orthogonal code. A reference symbol Walsh_Index is a register for storing the orthogonal code index to be calculated; Chip_count is a register for storing the current chip count; Walsh_code is a currently calculated orthogonal code value; and M is a value expressing the longest orthogonal code length as 2 to the power of a prescribed number (for instance, if the longest orthogonal code length is 128 chips, M is 7).

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The operation of the orthogonal code generator of FIG. 3 will now be described by way of example, on the assumption that the orthogonal code length information I is 3(011), the chip count t is 0-7, and the orthogonal code index n is 3($n_2, n_1, n_0 = 0, 1, 1$). It is also assumed that the longest orthogonal code length is 128 chips, that is, M is 7. Therefore, the number of the AND gates actually required by the orthogonal code information I (= 3) is restricted to 3.

As the orthogonal code index, the actual information 011 is continuously provided together with 4 bits masked to "0". As the chip count, 4 bits masked to "0" and 3 least significant bits varying from 000 to 111 are provided. The output of the AND gate circuit 310 according to the orthogonal code index and the chip count is listed in below in Table 2.

[Table 2]

Orthogonal Code Index (n)							Chip Count (n)							Output (q) of AND Gate						
n_6	n_5	n_4	n_3	n_2	n_1	n_0	t_6	t_5	t_4	t_3	t_2	t_1	t_0	q_6	q_5	q_4	q_3	q_2	q_1	q_0
0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							0	0	0	0	0	0	1	0	0	0	0	0	0	1
							0	0	0	0	0	1	0	0	0	0	0	0	1	0
							0	0	0	0	0	1	1	0	0	0	0	0	1	1
							0	0	0	0	1	0	0	0	0	0	0	0	0	0
							0	0	0	0	1	0	1	0	0	0	0	0	0	1
							0	0	0	0	1	1	0	0	0	0	0	0	1	0
							0	0	0	0	1	1	1	0	0	0	0	0	1	1

The outputs q_0 to q_6 of the AND gates 310_0,...,310_M-1 are provided to the XOR gate 320. The XOR gate 320 generates the orthogonal code "01100110" by XOR operation of the outputs q_0 to q_6 .

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In the preferred embodiment of the present invention, the controller 113 has determined the information for generating the orthogonal code, including the chip count, and provided the information to the orthogonal code generator 114. However, the controller 113 may provide only the orthogonal code length and orthogonal code index, and the orthogonal code generator 114 generates the chip count. In this case, the orthogonal code generator should include a counter to generate the chip count based on the orthogonal code length.

As described above, since the orthogonal codes having different lengths according to the symbol rates can be generated, the present invention may usefully be applied to a CDMA-2000 mobile communication system in which symbol rates vary according to channel types. Furthermore, since there is no need to make various types of orthogonal code tables corresponding to the different orthogonal code lengths, multiple varying memories are not required and the hardware configuration can be realized by a common structure which is applicable to various symbol rates.

While the invention has been shown and described with reference to certain preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

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CLAIMS:

1. A device for generating orthogonal codes in a mobile communication system, comprising:

a memory having registers for respectively storing an effective bit number, an orthogonal code index and a chip count value; and

an orthogonal code generating circuit for sequentially generating said chip count value up to a maximum value which can be counted by said effective bit number, and generating an orthogonal code by logic operation of said orthogonal code index and said sequentially generated chip count values.

2. The device as claimed in claim 1, wherein said effective bit number designates a bit number of an exponent when an orthogonal code length corresponding to a variable symbol rate is expressed as 2 raised to the power of a prescribed number.

3. The device as claimed in claim 1, wherein said orthogonal code generating circuit receives said effective bit number, orthogonal code index and chip count value and generates an orthogonal code according to the equation:

$$W(I,n,t)=(n_{I-1}\times t_{I-1})\dots(n_4\times t_4)\oplus(n_3\times t_3)\oplus(n_2\times t_2)\oplus(n_1\times t_1)\oplus(n_0\times t_0)$$

where I is an effective bit number, n ($=n_{I-1},\dots,n_4,n_3,n_2,n_1,n_0$) is an orthogonal code index, and t ($=t_{I-1},\dots,t_4,t_3,t_2,t_1,t_0$) is a chip count value.

4. The device as claimed in claim 2, wherein said orthogonal code generating circuit includes:

a controller for determining said effective bit number, sequentially

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generating said chip count value up to a maximum value which can be counted by said effective bit number, and converting said orthogonal code index into a binary number of said effective bit number; and

an orthogonal code generator for generating an orthogonal code by logic
5 operation of said orthogonal code index converted into the binary number and the sequentially generated chip count values.

5. The device as claimed in claim 4, wherein said orthogonal code generator includes:

10 AND gates for ANDing bits of said orthogonal code index converted into the binary number and bits of said sequentially generated chip count values; and
an XOR gate for XORing outputs of said AND gates to generate an orthogonal code in a chip unit.

15 6. A method for generating orthogonal codes in a mobile communication system, comprising the steps of:

calculating an orthogonal code length corresponding to a variable symbol rate;

20 determining an effective bit number based on the calculated orthogonal code length;

sequentially generating a chip count value up to a maximum value which can be counted by said effective bit number;

converting an orthogonal code index into a binary number of said effective bit number; and

25 performing a logic operation on said orthogonal code index converted into the binary number and said sequentially generated chip count values in order to generate an orthogonal code.

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7. The method as claimed in claim 6, wherein said effective bit number designates an exponent when said orthogonal code length is expressed as 2 raised to the power of a prescribed number.

5

8. The method as claimed in claim 6, wherein said logic operation includes the steps of:

ANDing bits of said orthogonal code index converted into the binary number and bits of said sequentially generated chip count values; and

10

XORing the ANDed results.

9. A method for generating orthogonal codes in a mobile communication system, comprising the steps of:

15

calculating an orthogonal code length corresponding to a variable symbol rate to determine an effective bit number; and

receiving said effective bit number, an orthogonal code index and a chip count value and generating an orthogonal code in accordance with the following equation:

20

$$W(I,n,t)=(n_{I-1}\times t_{I-1})\dots(n_4\times t_4)\oplus(n_3\times t_3)\oplus(n_2\times t_2)\oplus(n_1\times t_1)\oplus(n_0\times t_0)$$

where I is an effective bit number, n ($=n_{I-1},\dots,n_4,n_3,n_2,n_1,n_0$) is an orthogonal code index, and t ($=t_{I-1},\dots,t_4,t_3,t_2,t_1,t_0$) is a chip count value.

25

10. The method as claimed in claim 9, wherein said effective bit number designates an exponent when said orthogonal code length is expressed as 2 raised to the power of a prescribed number.

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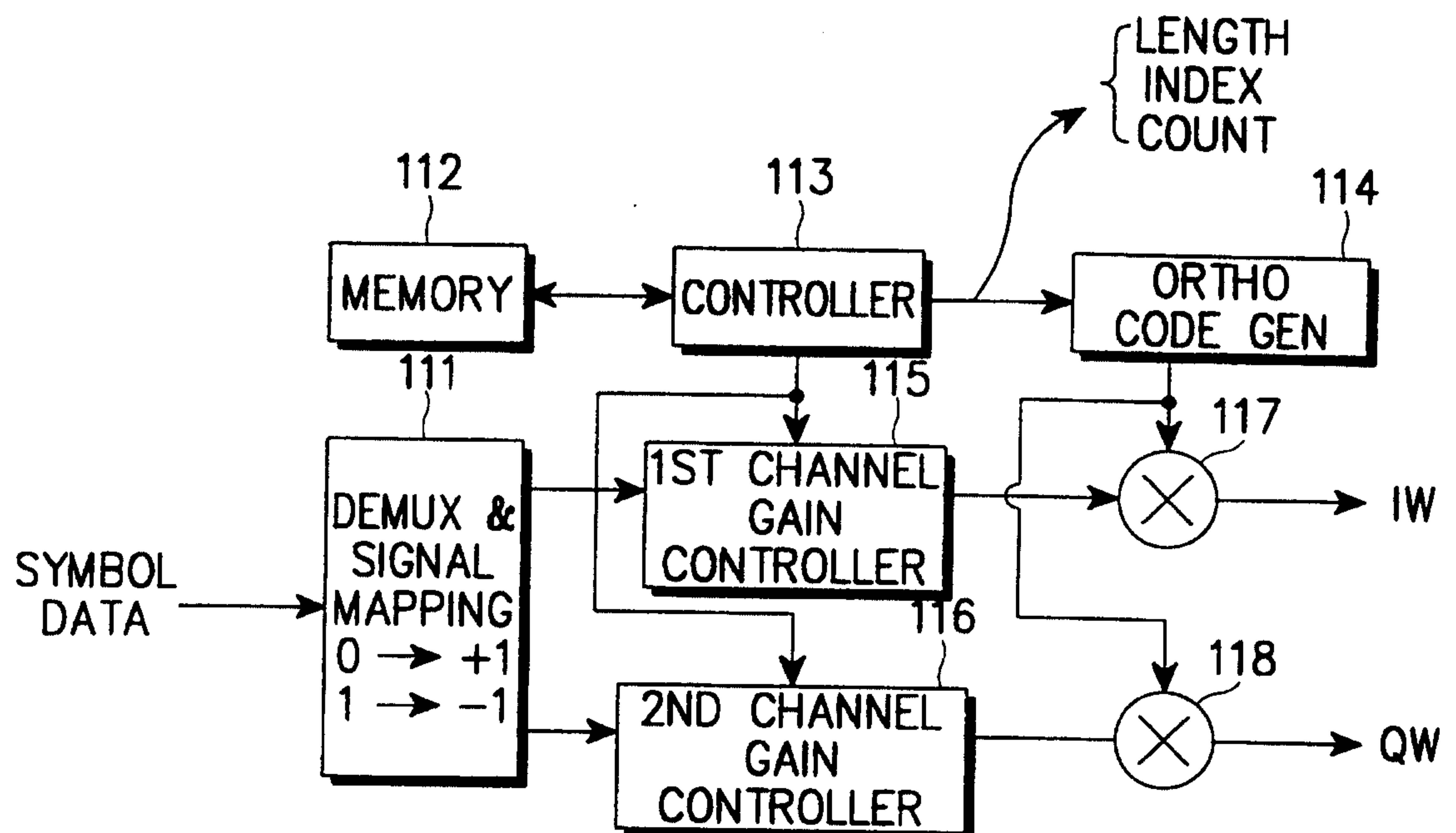
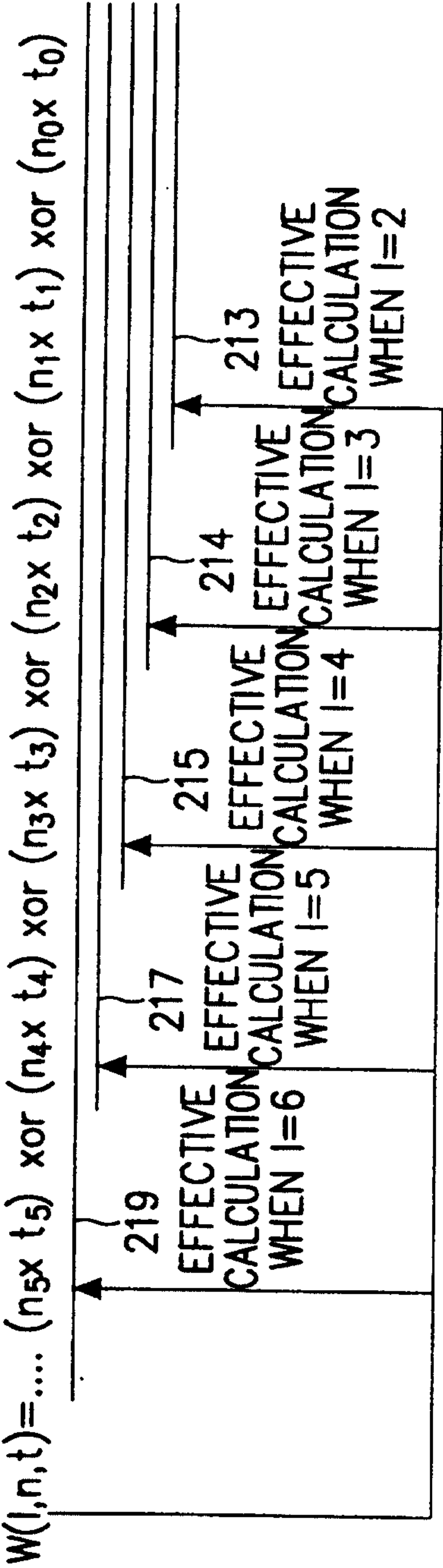


FIG. 1

FIG. 2



3/3

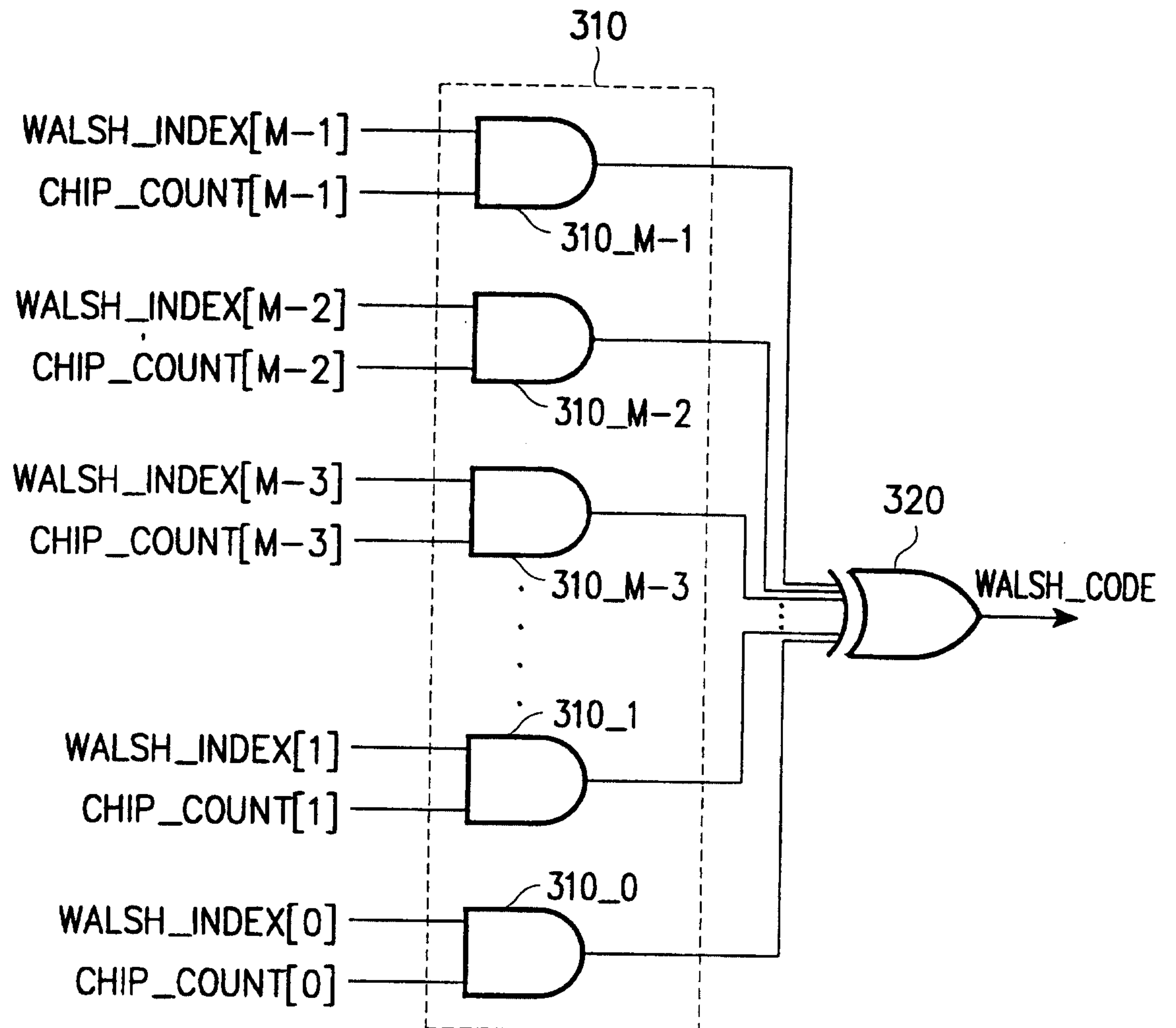


FIG. 3