

[54] ACOUSTIC CONTROL RECEIVER

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[51] Int. Cl. H04g 9/00

[58] Field of Search 340/164 R, 171 A, 340/171 R

[56] References Cited
UNITED STATES PATENTS

3,138,778	6/1964	Dulin	340/164 A X
3,335,406	8/1967	Clark	340/164 R
3,581,208	5/1971	Buehrle	340/171 PF X
3,588,826	6/1971	Vaccaro	340/171 PF X
3,618,020	11/1971	Parker	340/171 A X
3,638,174	1/1972	Haase	340/171 A X

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[57] ABSTRACT

An acoustical control receiver is disclosed for receiving and responding to a transmitted coded acoustic signal having a plurality of space tones at one acoustic frequency with a data tone of a different acoustic frequency between successive space tones to provide control of an utilization device. The receiver includes an input circuit that receives the transmitted coded signal and responds to the space tones to turn on detecting and decoding means connected to the input means to detect and decode the data tones and provide a control signal for controlling the utilization device when a proper sequence of space tones is received and a proper sequence of data tones is decoded.

8 Claims, 8 Drawing Figures

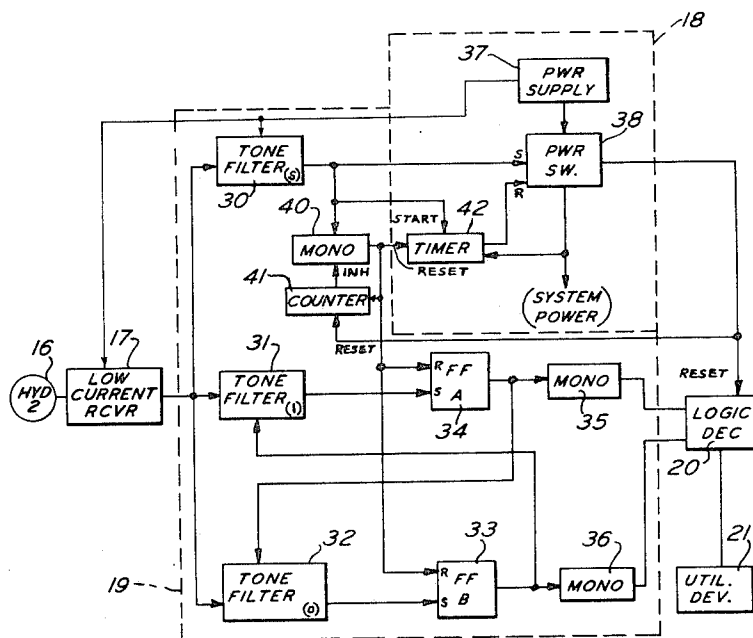


FIG. 1

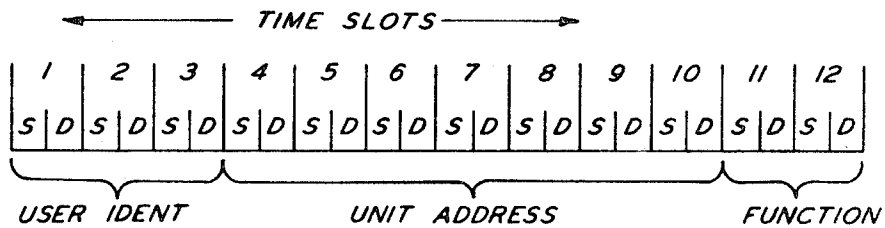
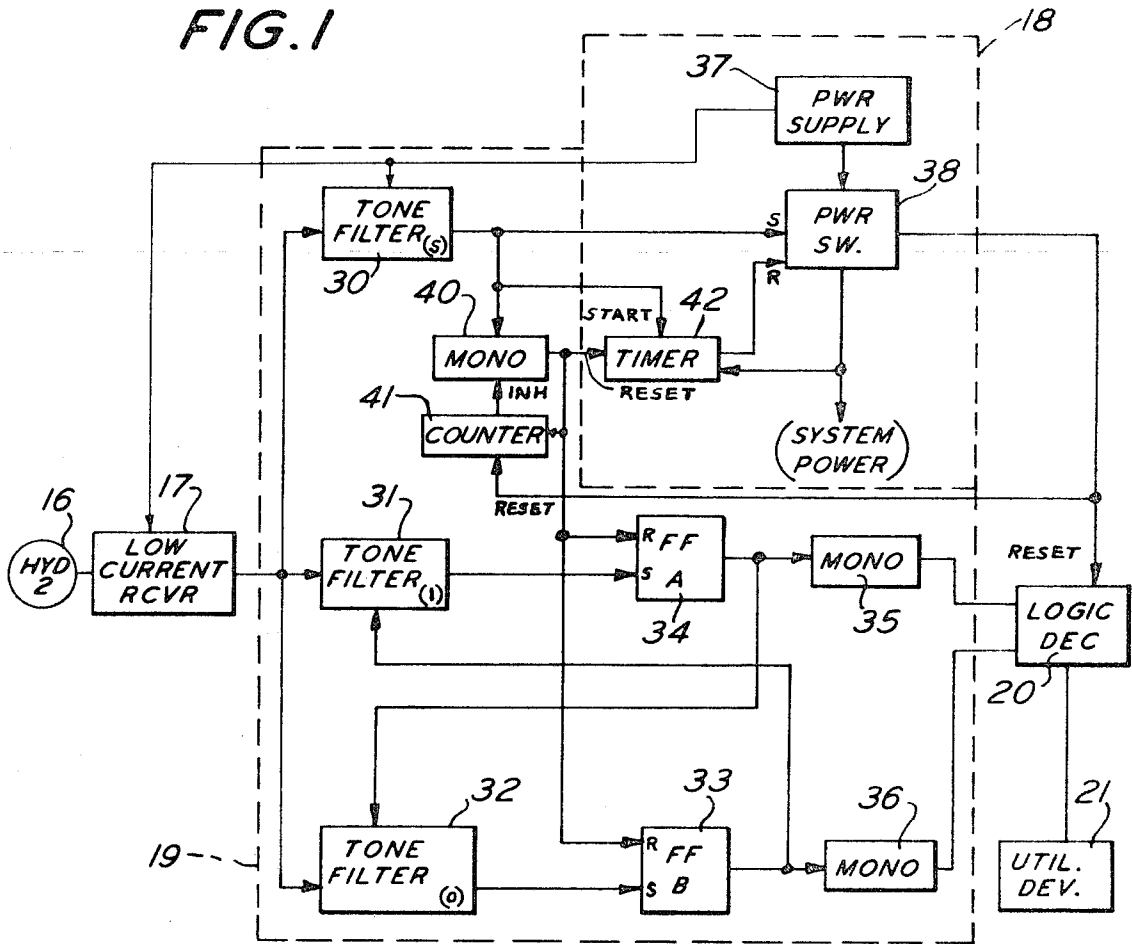


FIG. 2

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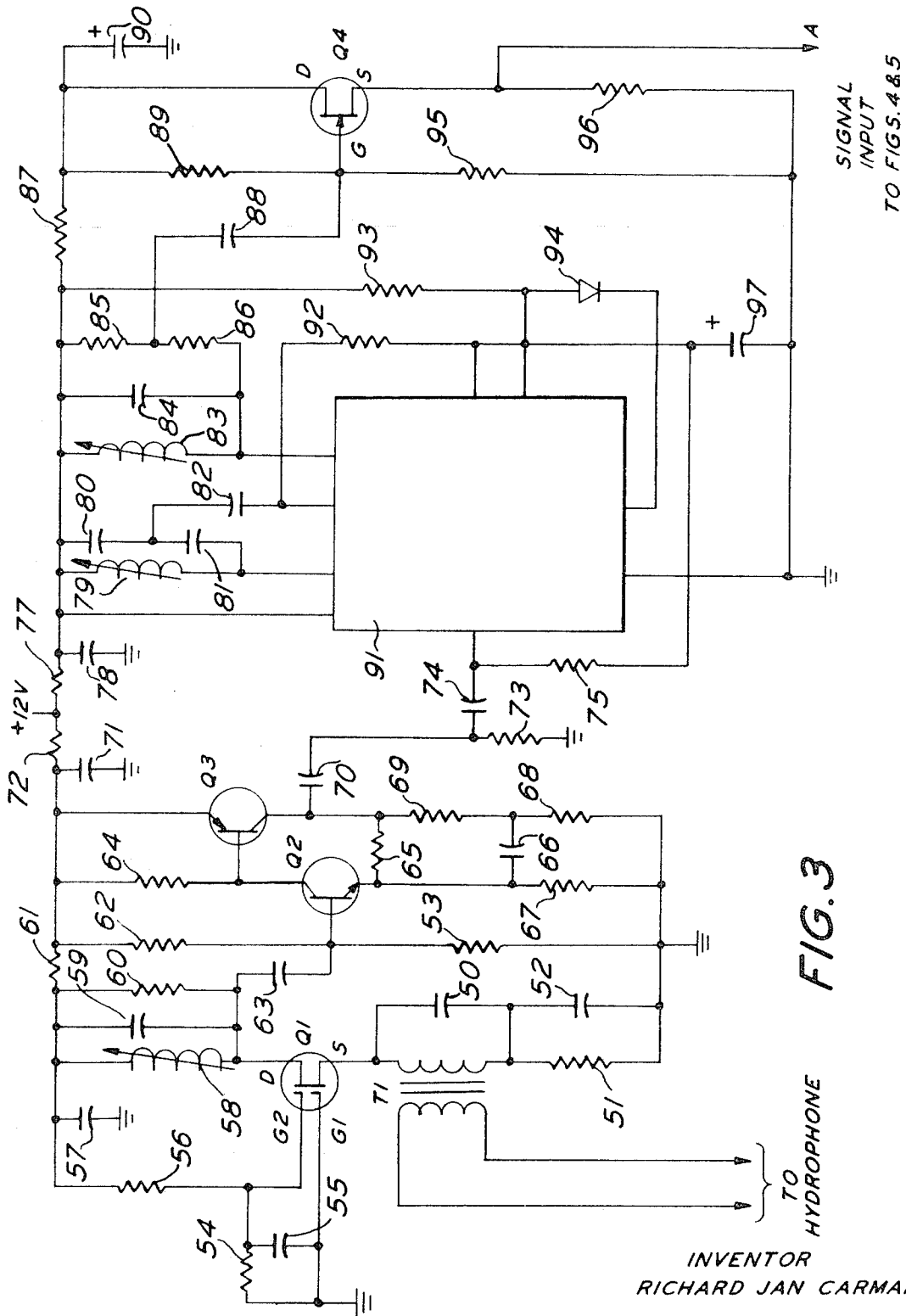


FIG. 3

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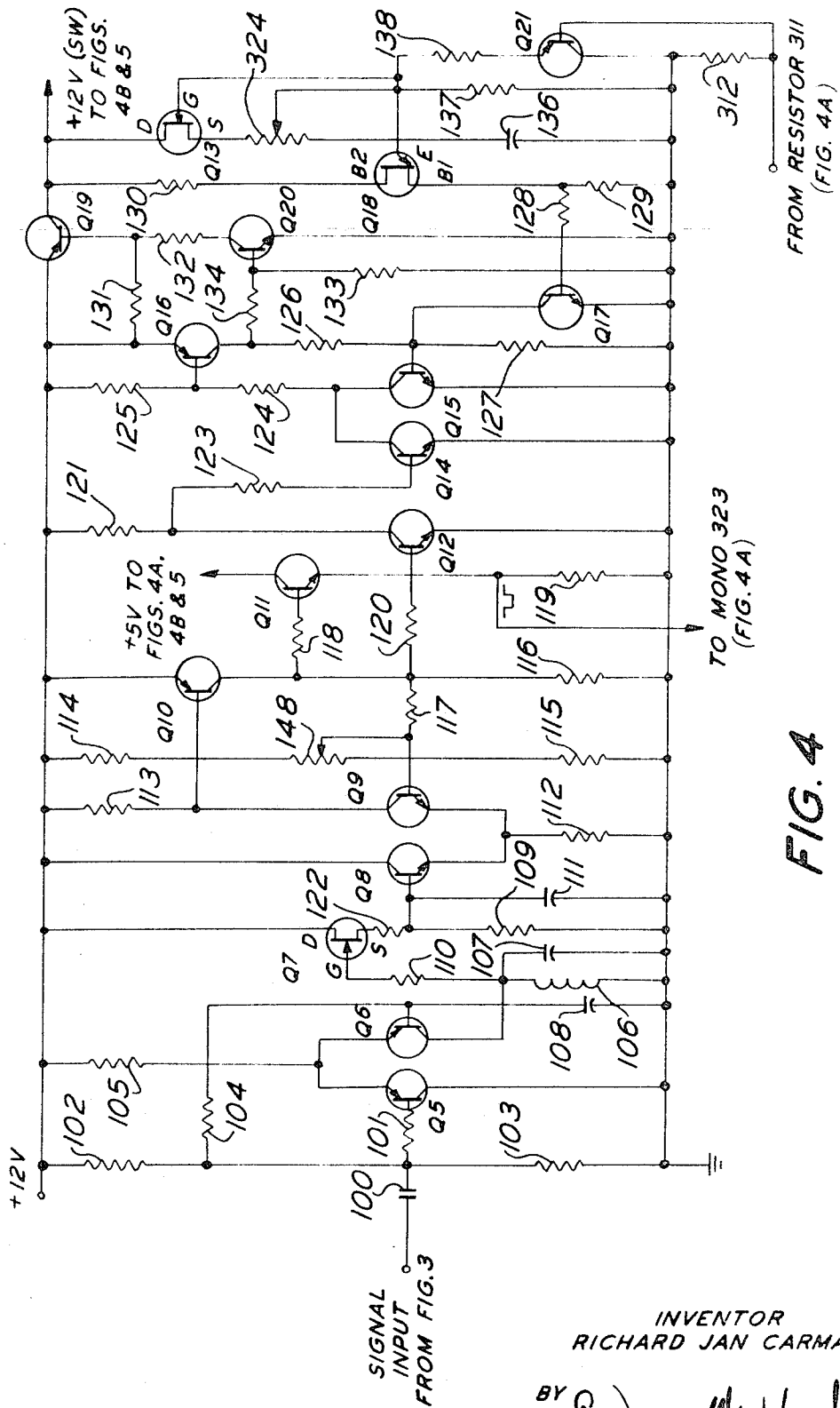
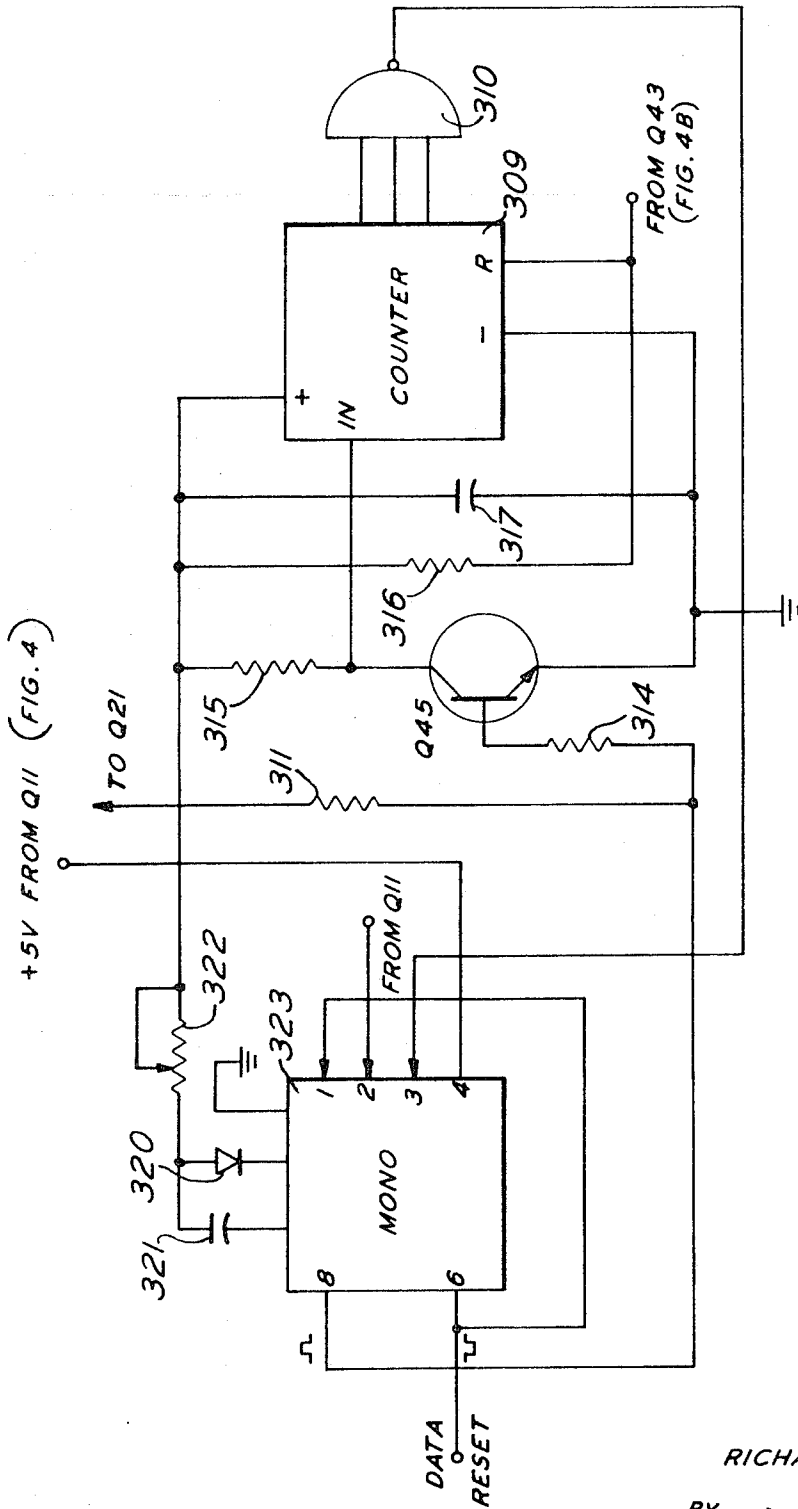


FIG. 4

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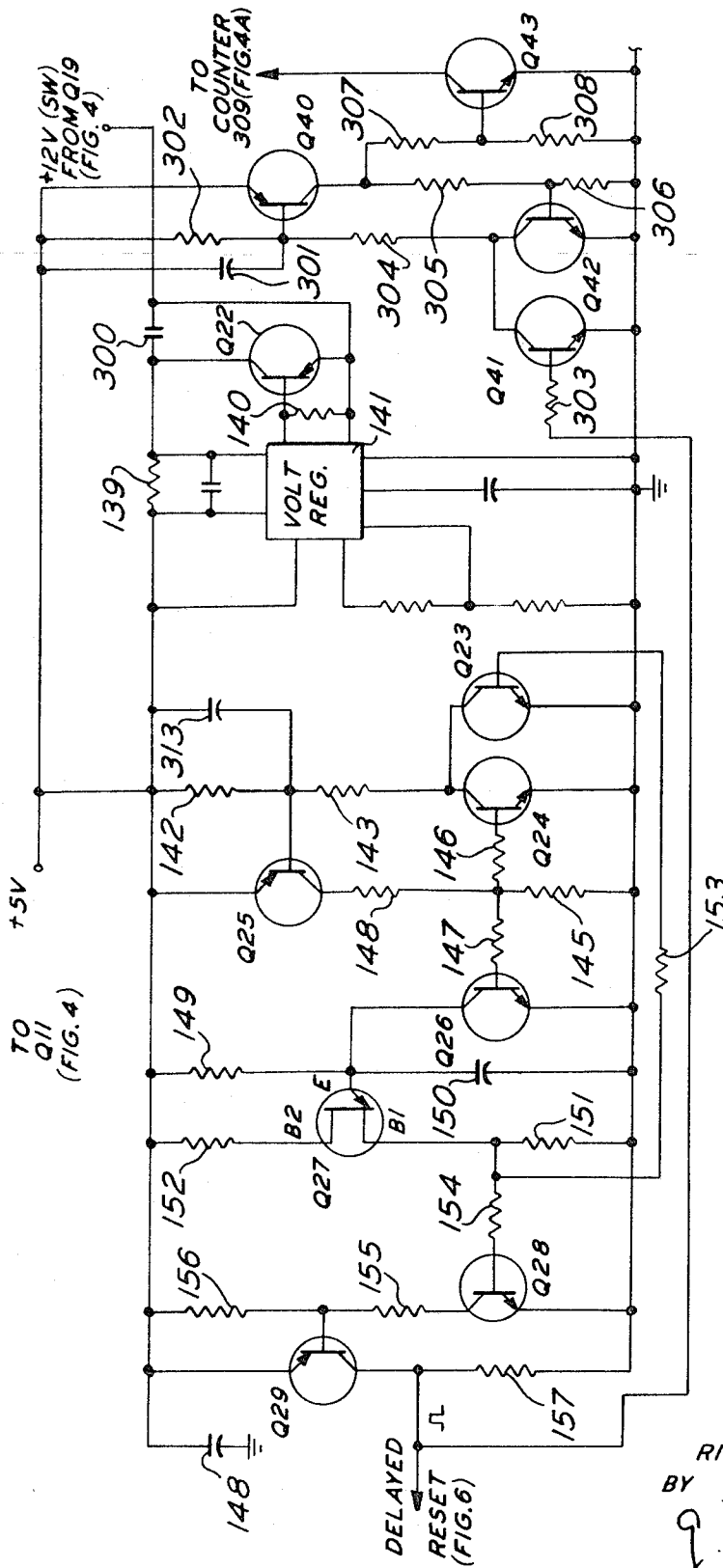


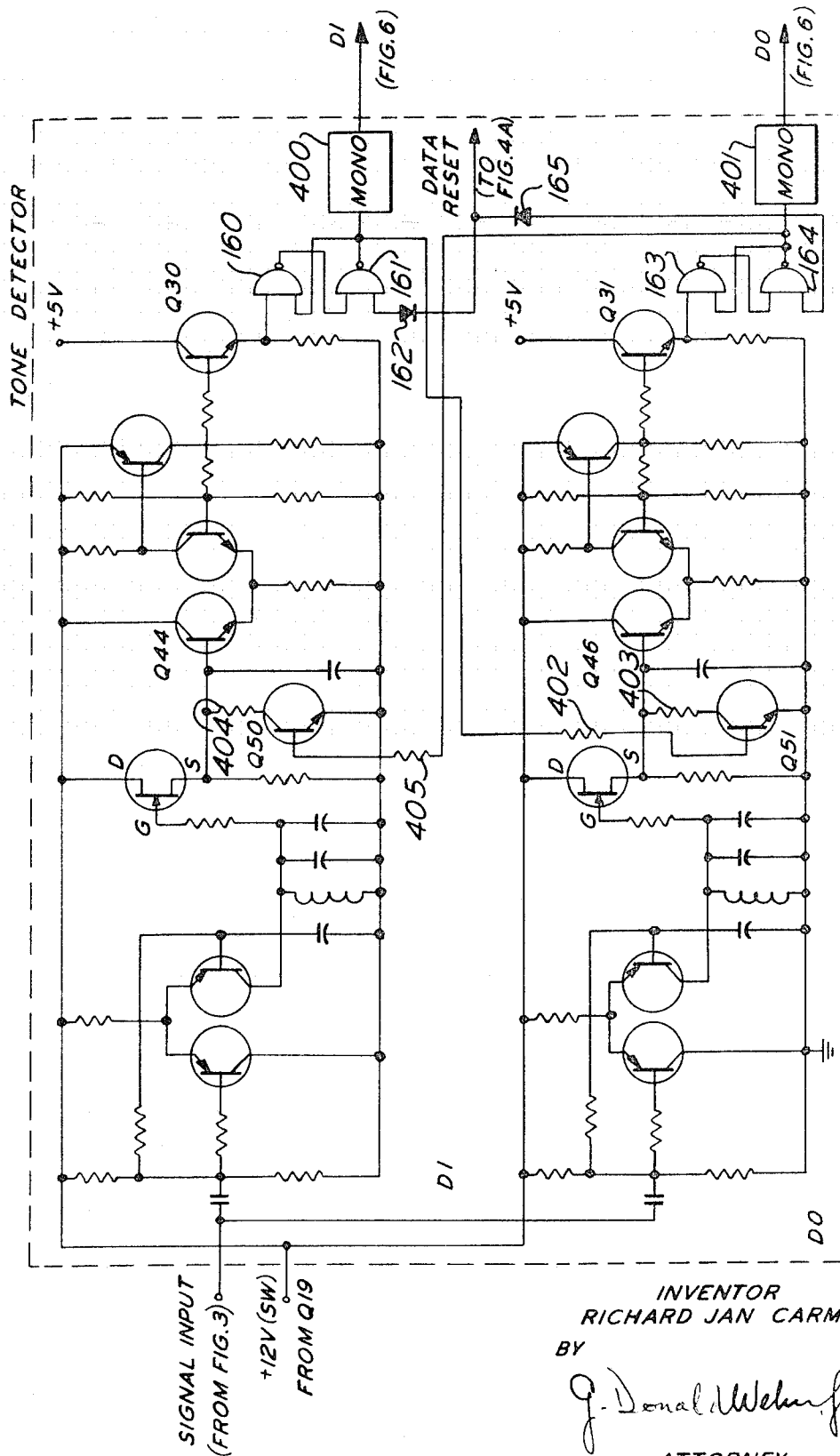
FIG. 4B

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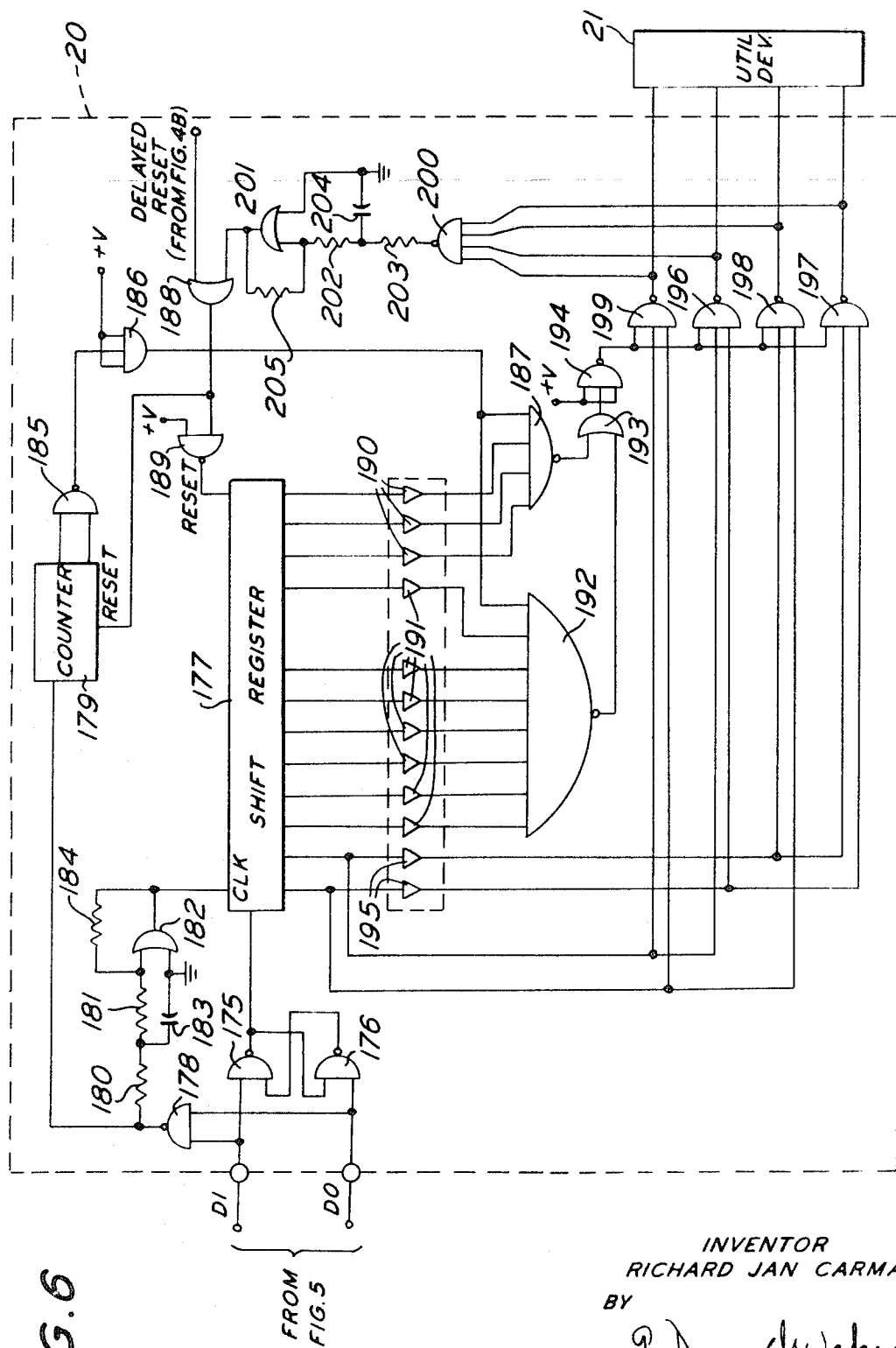


FIG. 6

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ACOUSTIC CONTROL RECEIVER

BACKGROUND

In the offshore petroleum industry, the current and apparent future trend is toward operations in deeper water. This fact occurs inasmuch as most of the relatively shallow waters have been or are now being fully exploited. In deeper water, many producers are investigating the desirability of issuing acoustically controlled subsea systems whereby the subsea equipment can be controlled by an acoustic interface from a surface unit. As has been experienced, subsea acoustic conditions are unusual and difficult. Many random noises and signals are present. Moreover, many of the signals which are deliberately produced are subject to reflection and other distortions. Furthermore, since one or more producers may be operating in adjacent fields, it is mandatory that coding of the control signals be utilized to identify the particular user and to identify the particular equipment of a specific user as well as to define the function which is to be performed by the subsea equipment.

Several techniques along this line are known in the art. Such background techniques are described in U.S. Pat. No. 3,405,387, entitled ACOUSTICAL UNDERWATER CONTROL APPARATUS by P. C. Koomey et al. and assigned to the instant assignee. In addition, the copending application entitled ACOUSTIC CONTROL SYSTEM by R. J. Carman, bearing Ser. No. 245,582, filed on Apr. 19, 1972 as a continuation of Patent application Ser. No. 28,761, filed May 19, 1970, now abandoned, and assigned to the instant assignee describes another acoustic system for subsea control. The latter named application describes a system which is designed to use a receiver such as described herein.

SUMMARY OF THE INVENTION

The receiver system described herein is, nominally, a passive circuit whereby low standby power drain is experienced. However, upon application of a suitable signal, the system is selectively energized by connecting a power supply thereto. The system is energized for accurately controlled time periods to prevent erroneous operations thereof. Thus, by operating in accordance with and as a function of the coded control signals, unauthorized operation of the system is avoided.

In essence, the system includes a first signal detector which operates in response to one portion of the coded signal. This detector, effectively, energizes the remainder of the circuit by connecting the power supply to the circuit. A timing network is arranged to disconnect the power supply (and de-energize the circuit) in the absence of additional signals at the first signal detector.

Other signal detectors operate on other portions of the coded signal to supply appropriate signals to a logic decoder. The logic decoder operates on these signals to produce output signals to a utilization device. The output signals are, of course, representative of the coded signals detected by the signal detectors.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram representation of the instant invention.

FIG. 2 is a schematic representation of the coded signal utilized by the instant invention.

FIGS. 3 through 6 are detailed schematic representations of portions of the circuitry in the instant invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to FIG. 1, there is shown a block diagram of the receiver circuit. In FIG. 1, components which are similar to components shown and described in other Figures bear similar reference numerals.

Input transducer or hydrophone 16 is connected to an input of low current receiver 17. The output of low current receiver 17 is supplied to tone detector 19 shown in dashed outline. More particularly, the output of low current receiver 17 is connected to the inputs of three separate tone filters 30, 31 and 32. Tone filter 30 is a specially designed circuit which is utilized to detect a "space" tone. A space tone is defined as a signal tone which is utilized between data tones as shown in FIG. 2. The space tone may be considered to be an identifying tone which signifies that useful data follows thereafter. As will be seen, a space tone operates as an enabling signal for the receiver signal circuit. Thus, the space tone effects synchronization as well as improving reliability.

Tone filter 31 is a specially designed circuit which detects a suitable "data" tone (see FIG. 2). This data tone is representative of a prescribed signal, for example, a binary 1. Tone filter 32 is another specially designed circuit which detects a data tone which is representative of a different signal such as a binary 0. The output of tone filter 31 is connected to the set input of set-reset flip-flop 34. Flip-flop 34 is designated as FF A. The output of tone filter 32 is connected to the set input of set-reset flip-flop 33 which is designated as FF B.

The output of tone filter 30 is connected to the set input of power switch 38. Power switch 38, along with a suitable power supply 37 and timer 42, is included in power switching circuit 18 shown in dashed outline. The power output of power switch 38 is connected to the circuit components in the system and selectively supplies power thereto. For example, one power output of power switch 38 is connected to logic decoder 20 and supplies a +5 volt (switched) signal thereto. Another power output of power switch 38 is connected to the circuit components of tone decoder 19 and provides a +12 volt (switched) signal thereto especially including timer 42. This power input also triggers timer 42 into operation. A control output of power switch 38 is connected to the automatic reset terminal of logic decoder 20 to automatically reset the circuitry therein to a suitable initial condition shortly after power switch 38 is rendered operative. Thus, it is assured that the decoder circuits are all in the proper initial state and switching noise abated when power is supplied thereto.

The output of tone filter 30 is also connected to an input of monostable 40. The output of monostable circuit 40 is connected to the reset input of timer 42. The output of monostable 40 is further connected to the reset inputs of flip-flops 33 and 34. In addition, the output of monostable 40 is connected to an input of counter 41. The output of counter 41 is connected to the inhibit input of monostable 40.

The output of flip-flop 34 is connected to an input of monostable multivibrator (mono) 35 and to an inhibit input of tone filter 32. The output of flip-flop 33 is connected to the input of monostable multivibrator

(mono) 36 and to an inhibit input of tone filter 31. The cross-connected inhibit inputs cause the respective tone filters to be rendered nonconductive when the associated flip-flop is engaged. This cross-connection serves to reduce multipath signal problems. The outputs of monostable circuits 35 and 36 are connected to inputs of logic decoder 20. It should be understood, that the outputs of monostable circuits 35 and 36 can be gated together within the functional block designated as tone decoder 19 or within the functional block designated as logic decoder 20 thereby supplying a serial input to logic decoder 20. For purposes of this illustration, the appropriate gating network is defined to be included within logic decoder 20 (see FIG. 3). Likewise, in this embodiment, logic decoder 20 is defined to operate in the serial to parallel converter mode whereby parallel output signals are supplied to utilization device 21.

Referring now to FIGS. 1 and 2 concurrently, the operation of the receiver system shown in FIG. 1 is described. Typically, a command code (see FIG. 2) consists of a set of three distinct frequency shift keyed (FSK) TONES. Two of the tones are called data tones and correspond to a binary logic 1 and a binary logic 0, respectively. The third tone is called a space tone and is used to provide several characteristics such as receiver synchronization, receiver power supply switching, false alarm rejection, code security and to reduce response to multipath effects. The coding sequence consists of a plurality of time slots where the number of time slots is a function of number of operations or commands to be utilized, the number of the code is utilized as identification, for example to identify the operator or owner of the subsea equipment.

In the embodiment described herein, a code sequence having 12 time slots is utilized. Each time slot includes a space tone followed by a data tone as illustrated in FIG. 2 and each space and data tone may, for example, be of 100ms duration. Three of the time slots are used for company identification, seven for unit address and two for command functions. Obviously, as more command functions are required or desired, the code sequence could increase or the unit address or company identification must decrease. Moreover, with the binary format, an exponential relationship for the number of time slots exists. For example, in the code format described supra, eight different companies or groups could use up to 128 subsea units each and provide for four separate functions at each unit. Without changing the code format substantially, a realignment of the time slots would permit four companies to supply four commands to 256 subsea units. Similarly, three companies would address 64 units and provide eight command functions. The specific number of time slots and the application thereof to the system is determined by the requirements of the individual user. The specific number of time slots and the allotment thereof does not form a portion of this invention, per se.

However, the concept of utilizing a space tone prior to the application of a data tone is instrumental in permitting the utilization and operation of the instant invention. The utilization of the space tone for receiver synchronization, power supply switching and the like, as noted supra, permits a system such as herein described to be operative with a minimum number of parts and minimal energy requirement. Typically, the operator at the surface unit will manipulate switches

and the like on a suitable command console (not shown). Manipulation of the switches will cause suitable coded signals to be produced for transmission to the underwater receiver. For a detailed description of the transmitter circuit an the operation thereof, reference is made to the co-pending application of R. J. Carman, entitled ACOUSTICAL CONTROL TRANSMITTER (OSI-ZJ-19), filed on Aug. 5, 1970, bearing Ser. No. 61,339 and assigned to the instant assignee.

The signal from the surface unit is transmitted to hydrophone 16 and applied to low current receiver 17. As noted, receiver 17 includes a band-pass amplifier and amplifies the signal received from hydrophone 16 to a level sufficient to drive the tone filters. An AGC or limiter amplifier circuit provides a constant signal level to the tone filters, independent of the signal level at hydrophone 16. The signal produced by receiver 17 is supplied to each of the tone filters 30, 31 and 32 simultaneously. However, only tone filter 30 has power supplied thereto continuously. Consequently, tone filters 31 and 32 are not immediately operative when a signal is supplied by receiver 17. Provided the signal supplied is of the proper frequency, tone filter 30 will be rendered operative to produce a suitable output signal. The proper frequency which renders tone filter 30 operative is, of course, the frequency previously defined as the space tone. Thus, it is mandatory that a space tone be received to initiate operation of the receiver circuit.

When the proper space tone signal is received, tone filter 30 produces an output signal (s) which is supplied to power switch 38. Power switch 38 includes a set-reset (RS) flip-flop the set input terminal of which receives the set signal (s) from tone filter 30. With the application of set signal (s), the RS flip-flop of power switch 38 is switched whereby power supply 37 supplies power to the remainder of the receiver system as suggested supra. For example, +12 volt and +5 volt power signals are supplied to the system.

In addition, tone filter 30 supplies a signal to monostable 40 which operates as a single-pulser. That is, when monostable 40 is triggered, it produces an output of constant width and amplitude. For example, the pulse may be of about 100 millisecond duration (i.e., the duration of a space tone). Thus, for each space tone detected by tone filter 30, one and only one output signal is produced by monostable 40. This signal is supplied to the reset (or inhibit) terminal of flip-flops 33 and 34 to prevent operation thereof. Consequently, multipath signals produced in the water and subsequently received by hydrophone 16 cannot inadvertently cause operation of the receiver circuit.

Furthermore, the output signal produced by tone filter 30 is supplied to timer 42. Timer 42 exhibits a time constant which is equal to at least one but less than one and one-half times the duration of a space tone, i.e., 100ms to 150ms with the example to be given. Operation of timer 42 is enabled by application of power thereto by power switch 38, as a result of the application of a space tone to tone filter 30. However, as noted, timer 42 cannot begin a timing cycle until the inhibit signal supplied by monostable 40 is terminated. With the termination of the signal from monostable 40, timer 42 begins a timing cycle. If a space tone signal is not detected within a time period between one and one and one-half times the duration of a space tone (or between one-half and the duration of a time slot) after

termination of the monostable signal, timer 42 produces a signal which resets the RS flip-flop in power switch 38 thereby removing power from the remainder of the circuit. Thus, if the space tone signal is the last in a sequence (or if one is missed in normal transmission) the receiver is "shut down" and extraneous or inaccurate signals are not operated upon. However, if another space tone is received (and the appropriate signal produced by tone filter 30) during the timing cycle of timer 42, monostable 40 emits another reset signal whereby timer 42 is reset and a new timing cycle begins after the reset signal is terminated power switch 38 continues to supply power to the system.

Counter 41 also has the input thereof connected to the output of monostable 40 whereby each output signal produced by monostable 40 is counted by counter 41. At a predetermined count (representative of an information code word), an inhibit signal is supplied to monostable 40. The inhibit signal prevents monostable 40 from operating upon input signals from tone filter 30. If monostable 40 cannot operate upon input signals, timer 42 will "time out" and reset power switch 38 thereby deactivating the receiver system.

Furthermore, whenever the system is deactivated due to timer 42 completing a timing cycle, the various circuits are deactivated. These circuits are designed to revert to an initial condition; therefore, the counter circuit and the like must begin a completely new cycle of operation. With this condition, the utilization device cannot receive inaccurate information. Thus, monostable 40 receives signals from tone filter 30 and produces a single output signal having a duration of approximately one-half slot duration (i.e., 1 space tone duration). Timer 42 has a duration somewhat in excess of a single space tone. Counter 41 has a count capability of a predetermined number which is dictated by the code format. Therefore, counter 41 controls when monostable 40 can and cannot operate on signals from tone filter 30. Monostable 40 controls when timer 42 is reset to the initial condition and timer 42 controls when power switch 38 connects power supply 37 to the remainder of the circuit.

With the application of the +12 volt signal to tone filters 31 and 32 (via switch 38) these circuits are enabled. However, the circuits are not rendered operative to receive and operate on the data signals supplied by receiver 17 until the pulse from monostable 40 terminates. That is, the signal from monostable 40 is applied to the reset terminal of flip-flops 33 and 34 to assure that the flip-flops are inoperative until a data signal (D0 or D1) is applied. Depending upon the frequency of the signal supplied thereto, a suitable output signal is supplied by one of filters 31 and 32. This signal is supplied to the set input of the appropriate one of flip-flop 33 or flip-flop 34 to cause the flip-flop to switch states after termination of the monostable 40 signal. The change in state of the flip-flop will produce a change in the output signal which is supplied to one of the monostable circuits 35 and 36, respectively. The monostable circuit which receives the signal is designed to produce a single signal in response to the first detectable input signal supplied thereto. This single, constant width signal is supplied to logic decoder 20. As noted supra, by means of suitable gating logic, a binary 1, or binary 0 (depending upon the data tone supplied) is stored in a suitable position in logic decoder circuit 20. This information is serially stored.

Moreover, as suggested supra, an output signal is supplied from flip-flop 34 to inhibit operation of tone filter 32. Likewise an output signal from flip-flop 33 is supplied to inhibit tone filter 31. This arrangement prevents a binary 1 data tone from being detected concurrently with a binary 0 data tone. By eliminating this difficulty, multipath or reverberation signals are overcome.

Thus, a signal is supplied to logic decoder 20 which is representative of a signal received at hydrophone 16. The data signals are not supplied to logic decoder 20 until the application of a space tone at low current receiver circuit 17. In addition to providing synchronization of the receiver circuit, the controlled activation of operational power switch 38 reduces the drain on the power supply. That is, unless reset by a subsequent space tone, the circuit remains inactive.

In continuous operation, for example, when a suitable code word is being received, the space tone will operate the power switch and the flip-flops as noted supra. The data tones will be received by the appropriate tone filters and supplied to logic decoder 20. In addition, upon detection of a data tone by one of the tone filters, the associated flip-flop assumes the set condition and will not detect additional signals from the tone filter until reset. Furthermore, the cross-coupled flip-flops inhibit the counterpart tone filters. Thus, spurious noise or random signals in the environment cannot supply erroneous signals which would trigger the other tone filter to produce an erroneous condition.

Referring now to FIG. 3, there is shown a detailed schematic drawing of low current receiver 17. Low current receiver 17 comprises a preamplifier circuit portion and a limiter circuit portion. The preamplifier circuit portion includes transformer T1 which has the primary winding thereof connected to the hydrophone or transducer. The primary winding is inductively coupled to the secondary winding of transformer T1. One terminal of the secondary winding of transformer T1 is connected via the parallel combination of resistor 51 and capacitor 52 to ground. Capacitor 50 is connected in parallel with the secondary winding of transformer T1. The second terminal of the secondary winding of transformer T1 is connected to the source electrode of field effect transistor Q1. Gate electrode G1 of transistor Q1 is connected directly to ground. A second gate electrode G2 of transistor Q1 is connected to ground via resistor 54. Bypass capacitor 55 is connected between gate G2 and ground. Gate G2 of transistor Q1 is further connected to ground via resistor 56 and filter capacitor 57. The common junction between resistor 56 and capacitor 57 is connected to the +12 volt source via the decoupling networks comprising resistor 61 and capacitor 57 as well as resistor 72 and capacitor 71. The decoupling networks effectively remove any noise at the +12 volt source from the preamplifier circuit. The common junction of resistor 56 and capacitor 57 is further connected to one terminal of variable inductor 58 which is further connected at the other end thereof to the drain electrode D of a field effect transistor Q1. Resistor 60 and capacitor 59 are connected in parallel with inductor 58 to form a suitable R, L, C network which is broadly tuned to the space tone frequency.

The drain electrode of FET Q1 is connected via coupling capacitor 63 to the base of NPN transistor Q2. The base of transistor Q2 is also connected to the common junction of resistors 53 and 62 which form a volt-

age divider network connected between ground and the common junction between resistors 61 and 72 of the decoupling networks. This same common junction is connected via resistor 64 to the collector of transistor Q2 and directly to the emitter of PNP transistor Q3. The base of transistor Q3 is also connected to the collector of transistor Q2. The emitter of transistor Q2 is connected to ground via resistor 67. In addition, the emitter of transistor Q2 is connected via coupling capacitor 66, to the common junction of resistors 68 and 69. Resistors 68 and 69 are connected between ground and the collector of transistor Q3. Resistor 65 is connected between the emitter of transistor Q2 and the collector of transistor Q3. With this negative feedback gain adjusting circuit arrangement, low D.C. gain is provided by the arrangement of resistors 65 and 67. Likewise, resistors 68 and 69, along with capacitor 60 provide high A.C. gain. The output of the preamplifier network is obtained at the collector of transistor Q3. Specifically, the collector of transistor Q3 is coupled via capacitor 70 to load resistor 73 which is referenced to ground.

The preamplifier output detected across resistor 73 is A.C. coupled to amplifier 91 via capacitor 74. The details of the amplifier circuit are not critical to the circuit application and are, therefore, not described in detail. However, in this embodiment, amplifier circuit 91 is known integrated circuit having a pair of amplifier stages. The +12 volt source is connected to one terminal of amplifier 91 via the decoupling network comprising resistor 77 and capacitor 78. This decoupling network prevents noise at the +12 volt source from being transmitted to the limited circuit. In addition to the common junction of amplifier 91 via tuned circuit comprising inductor 79 and series connected capacitors 80 and 81.

The series connected capacitors are connected in parallel with inductor 79. The common junction of capacitors 80 and 81 is connected via coupling capacitor 82 to a terminal of the second stage of amplifier 91. In addition, the last mentioned terminal of amplifier 91 is connected, via resistor 92, to a bias terminal of amplifier 91.

A second tuned circuit comprising inductor 83 and capacitor 84 connected in parallel therewith is connected between the common junction associated with resistor 77 and an output terminal of a second stage of amplifier 91. The series connected resistors 85 and 86 are connected in parallel with capacitor 84 to affect the Q of the tuned circuit. The common junction of resistors 85 and 86 is connected via coupling capacitors 88 to the gate electrode of FET Q4. The gate electrode of FET Q4 is further connected to the common junction of resistors 89 and 95 which form a bias network. The bias network is connected between ground and a positive voltage terminal. The positive voltage terminal is connected to the +12 volt source via the decoupling network comprising resistor 87 and capacitor 90.

The common junction between resistors 77 and 87 is further connected to another input terminal of amplifier 91 via resistor 93. The last mentioned terminal is connected to another terminal of amplifier 91 via diode 94. Resistor 93 and diode 94 provide a bias network for amplifier 91. A series connected network comprising resistor 75 and capacitor 97 is connected between one input terminal of amplifier 91 and ground. The common junction between resistor 75 and capacitor 97 is

also connected to the amplifier input associated with the anode of diode 94. The source electrode of transistor Q4 is connected to ground via resistor 96 while the drain electrode is connected to the +12 volt source via resistors 87 and 77. The output of the limiter circuit is connected to the source electrode of transistor Q4.

In operation, the preamplifier and limiter operate upon the signal supplied by the hydrophone unit. For example, the hydrophone supplies an alternating signal to the primary winding of the transformer T1. This signal is coupled to the secondary winding of the transformer. The signal detected at the secondary winding of transformer T1 is applied to the source electrode of FET Q1. In the circuit configuration shown, transistor Q1 provides high gain with low drain current. The tuned circuit comprising conductor 58 and capacitor 59 is a relatively broad band filter which accepts all signal frequencies applied to the receiver. For example, the frequencies applied vary between 14.5 KHz to 15.5 KHz. Resistor 61 and capacitor 57 operate as a decoupler which isolates the circuit portions on either side of the resistor and prevents spurious signals from being applied to the tuned circuit.

The output of the tuned circuit is supplied to the base of transistor Q2 which transistor is biased by resistors 62 and 53. The output of transistor Q2 is supplied to the base of transistor Q3. Transistors Q2 and Q3 operate as amplifier circuits. The connection of resistors 65 and 67 cause the amplifier to have low DC gain. In addition, resistors 68 and 69 along with capacitor 66 produce a somewhat higher AC gain. This arrangement permits relatively high stability and reliability regardless of temperature changes in the system and the like. The circuit comprising resistor 72 and capacitor 71 essentially decouples the +12 volt source from the remainder of the preamplifier circuit. Thus, spurious noise or other random signals are prevented from being applied to the preamplifier circuit.

The output of the tuned circuit is supplied to the base of transistor Q2 which transistor is biased by resistors 62 and 53. The output of transistor Q2 is supplied to the base of transistor Q3. Transistors Q2 and Q3 operate as amplifier circuits. The connection of resistors 65 and 67 cause the amplifier to have low DC gain. In addition, resistors 68 and 69 along with capacitor 66 produce a somewhat higher AC gain. This arrangement permits relatively high stability and reliability regardless of temperature changes in the system and the like. The circuit comprising resistor 72 and capacitor 71 essentially decouples the +12 volt source from the remainder of the preamplifier circuit. Thus, spurious noise or other random signals are prevented from being applied to the preamplifier circuit.

The output signal from transistor Q3 (i.e. the output signal from the preamplifier) is coupled via capacitor 70 and detected across load resistor 73. This input signal is AC coupled by capacitor 74 to the input of amplifier 91. In this embodiment amplifier 91 is a Signetics type NE511B two-stage amplifier limiter. The tuned circuits are broadly tuned for the frequencies of the system and connected to the different stages of the amplifier. The amplifier amplifies the input signal where necessary or limits the signal so that a relatively constant output is provided thereby at output terminal A. Terminal A is connected in similar terminals in FIGS. 4 and 5. The network comprising resistors 75, 92, 93

and diode 94 is a bias network which is associated with amplifier 91.

The junction between resistors 85 and 86 are as coupled to transistor Q4 via capacitor 88. Transistor Q4 provides relatively high power gain with high input impedance and low output impedance. Again, resistor 96 operates as a bias resistor for transistor Q4.

In essence, the preamplifier and limiter circuits shown in FIG. 3 function to provide a large amplification factor and yet a limiting function. Thus, if a very small signal is supplied by the hydrophone, sufficient amplification is provided whereby the smallest receivable signal can be amplified to a utilizable level. However, since the input signal may be a much larger amplifier, the limiter function assures that an output signal of only a prescribed amplitude will be produced. Thus, a broad range of input signals is acceptable so that satisfactory and useful operation of the circuit can be maintained without fear of overdriving the following circuitry.

Referring concurrently now to FIGS. 4, 4A and 4B, there is shown the sequence control circuit which includes space tone detector 50 and power switching circuit 18. Coupling capacitor 100 (FIG. 4) is connected to transfer the output signal from low current receiver 17 (FIG. 3), to the space tone detector circuit. Coupling capacitor 100 is connected to the base of transistor Q5 via resistor 101. A voltage divider network comprising resistors 102 and 103 is connected between the +12 volt source and ground to provide a bias signal for transistor Q5. The common junction between resistors 102 and 103 is also connected to the common junction of resistor 101 and capacitor 100. Furthermore, the common junction of resistors 102 and 103 is connected via resistor 104 to the base of transistor Q6. The emitter electrodes of transistors Q5 and Q6 are connected together and to the +12 volt source via resistor 105. The collector of transistor Q5 is connected directly to ground while the collector of transistor Q6 is connected to ground via the tank circuit comprising inductor 106 and capacitor 107. The base of transistor Q6 is connected to ground via filter capacitor 108.

Field effect transistor Q7 has the drain electrode thereof connected to the +12 volt source while the source electrode is connected to ground via series connected resistors 109 and 122. The gate electrode of FET Q7 is connected via resistor 110 to the tank circuit including inductor 106. The base of transistor Q8 is connected to the common junction of resistors 109 and 122. Also, the base of transistor Q8 is connected to ground via filter capacitor 111. The collector electrode of transistor Q8 is connected directly to the +12 volt source. The emitter electrode of transistor Q8 is connected to the emitter electrode of transistor Q9, and, via resistor 112 to ground. The collector of transistor Q9 is connected to the +12 volt source via resistor 113. The base of transistor Q9 is connected to the adjustable tap of variable resistor 148 which is connected between resistors 114 and 115. The series connected resistors 114, 115 and 148 form a voltage divider network connected between the +12 volt source and ground.

The base of transistor Q10 is connected to the collector of transistor Q9. The emitter of transistor Q10 is connected to the positive potential source while the collector thereof is connected to ground via resistor 116. In addition, resistor 117 connects to collector of transistor Q10 to the center tap of variable resistor 148.

The base of emitter follower transistor Q11 is connected to the collector of transistor Q10 via resistor 118. The collector of transistor Q11 is connected to the +5 volt power supply. The emitter of transistor Q11 is connected to ground via resistor 119. In addition, transistor Q11 provides a data reset output control signal as described hereinafter. This control signal is produced at the emitter of transistor Q11 and is supplied to monostable 323 (FIG. 4A) which is equivalent to monostable 40 (FIG. 1).

The collector of transistor Q10 is connected via resistor 120 to the base of transistor Q12 which is the input transistor of power switching circuit 58. (see FIG. 1). The emitter of transistor Q12 is connected to ground while the collector thereof is connected to the +12 volt source via load resistor 121. In addition, the collector of transistor Q12 is connected to the base of transistor Q14 via resistor 123. The collectors of transistor Q14 and transistor Q15 are connected together and to the +12 volt source via series connected resistors 124 and 125. The emitters of transistors Q14 and Q15 are connected to ground. The base of transistor Q16 is connected to the common junction of resistors 124 and 125. The emitter of transistor Q16 is connected directly to the +12 volt source while the collector thereof is connected via series connected resistors 126 and 127 to ground. The common junction of resistors 126 and 127 is connected to the base of transistors Q15 and to the collector of transistor Q17. The emitter of transistor Q17 is connected directly to ground while the base thereof is connected via coupling resistor 128 to the base B1 of unijunction transistor Q18 and to ground via resistor 129. Base B2 of transistor Q18 is connected to the collector of switching transistor Q19 via resistor 130. The collector of transistor Q19 is the output terminal of this circuit and is connected to the other tone filters as described hereinafter. The emitter of transistor Q19 is connected directly to the +12 volt source. The base of transistor Q19 is connected to the +12 volt source via resistor 131. In addition, the base of transistor Q19 is connected to the collector of transistor Q20 via resistor 132. The emitter of transistor Q20 is connected directly to ground. The base of transistor Q20 is connected to ground via resistor 133 and to the collector of transistor Q16 via resistor 134.

Field effect transistor Q13 has the drain electrode thereof connected to the collector of transistor Q19 to receive the switched output voltage. The source electrode of FET Q13 is connected to ground via the series network including variable resistor 324 and capacitor 136. The common junction of this series network is further connected to the emitter of transistor Q18 and the gate electrode of FET Q13. Resistor 137 is connected in parallel with capacitor 136. Transistor Q21 has the emitter thereof connected to ground while the collector is connected, via resistor 138, to the common junction at the emitter electrode of transistor Q18. The base of transistor Q21 is connected to ground via bias resistor 312 and, as well, to receive control signals as described hereinafter.

Sequencing of the system is controlled by counter 323 and associated circuitry shown in FIG. 4A. Suitable supply voltages are provided via variable resistor 322 and, thence, via capacitor 321 and diode 320. Also, one terminal of monostable 323 is connected to ground potential. Input signals are supplied at terminals 1, 2, 3 and 4. The signal supplied at terminal 3 func-

tions to inhibit monostable 323 from operating on additional input signals. This inhibit signal is generated by gate 310 described hereinafter. Input terminal 4 is connected to the positive voltage source represented by the collector of transistor Q11 so that a binary 1 is continuously supplied. Input terminal 2 is connected to receive a signal from the emitter of transistor Q11 (FIG. 4). Input terminal 1 and output terminal 6 are connected to a data reset terminal which is connected to logic decoder 20. Output terminal 8 is connected to supply a signal to the input of the sequencer circuit and to the base of transistor Q21 via resistor 311.

Transistor Q45, the input of the sequencer circuit, has the base thereof connected via resistor 314 to output terminal 8 of monostable 323. The emitter of transistor Q45 is grounded while the collector thereof is connected to the positive source via resistor 315. The collector of transistor Q45 is further connected to an input of counter 309. Suitable relatively positive and negative sources are connected to counter 309. The output terminals of counter 309 are connected to the input terminals of gate 310. The output of gate 310 is connected to the inhibit input of counter 323 as noted supra. In addition, reset terminal 12 of counter 309 is connected to transistor Q43 of FIG. 4B.

A +12 volt (switched) signal is supplied to the timer circuit from the collector electrode of transistor Q19. Also, the +12 volt and +5 volt signals are selectively supplied to the circuit of FIG. 4B, depending upon the operating condition of transistors Q11 and Q19. The +12 volt switched signal is supplied directly to the emitter of transistor Q22 and to the collector of transistor Q22 via bypass capacitor 300. The +5 volt signal is received from the collector of transistor Q22 via resistor 139. The base of transistor Q22 is connected via resistor 140 to the +12 volt signal. The base of transistor Q22 is further connected to one terminal of voltage regulator 141 while the emitter of transistor Q22 is connected to another input thereof. Voltage regulator 141 is a typical integrated circuit component which operates on signals supplied thereto to produce regulated voltages. This circuit is, essentially, connected between the +12 volt signal and ground to receive appropriate power signals. The specific arrangement is not a critical portion of the invention per se and is not described in detail.

The +5 volt signal is also supplied to the collector electrodes of transistors Q24 and Q23 via series connected resistors 142 and 143. The emitter electrodes of transistors Q24 and Q23 are connected to ground. The base of transistor Q25 is connected to the common junction between resistors 142 and 143. This junction is also connected to the +5 volt source. The collector of transistor Q25 is connected to ground via the series combination of resistors 148 and 145. The common junction of this voltage divider network is connected to the base of transistor Q24 via resistor 146 and to the base of transistor Q26 via resistor 147. The emitter of transistor Q26 is connected directly to ground while the collector thereof is connected to the emitter of unijunction transistor Q27. The emitter of unijunction transistor Q27 is further connected to ground via capacitor 150 and to the +5 volt source via resistor 149. Base B1 of transistor Q27 is connected to ground via resistor 151 while base B2 of transistor Q27 is connected to the +5 volt source via resistor 152. Base

B1 of transistor Q27 is also connected to the base of transistor Q23 via coupling resistor 153.

Base B1 of transistor Q27 is further connected, via resistor 154, to the base of transistor Q28 which has the emitter thereof connected directly to ground. The collector of transistor Q28 is connected via resistors 155 and 156 to the +5 volt source. In addition, the base of transistor Q29 is connected to the common junction of resistors 155 and 156. The emitter of transistor Q29 is connected directly to the +5 volt source while the collector thereof is connected to ground via resistor 157. The collector of transistor Q29 is further connected to the output terminal where the delayed RESET signal is provided and supplied.

In operation, the sequence control circuit (FIGS. 4, 4A and 4B) receives an input signal from the low current receiver. The signal is supplied across coupling capacitor 100 and to the bases of transistors Q5 and Q6 via resistors 101 and 104, respectively. Transistors Q5 and Q6 are biased to similar operating conditions. However, since the base of transistor Q6 is coupled to ground via capacitor 108, substantially all of the AC portion of the signal supplied thereto is deleted. The signal supplied to the emitter-coupled amplifier comprising transistors Q5 and Q6 is amplified and supplied to the tuned filter circuit comprising inductor 106 and capacitor 107. This filter is tuned to the space tone frequency. Consequently, only when the space tone frequency is applied thereto, is a signal supplied to the gate electrode (G) of field effect transistor Q7. When FET Q7 receives a signal, a current path to the base of transistor Q8 is established via FET Q7 and resistor 122. The low pass filter comprising resistor 109 and capacitor 111 permits only a low frequency, substantially DC, signal to be supplied to the base of transistor Q8. Transistors Q8 and Q9 represent a threshold detector. When the signal supplied to the base of transistor Q8 exceeds the potential applied to the base of transistor Q9, transistor Q8 is rendered conductive and transistor Q9 is rendered nonconductive. When transistor Q9 is rendered nonconductive, transistor Q10 is also turned off. As will be seen, transistor Q10 is turned off so long as a space tone signal is supplied to the circuit to maintain transistor Q8 in the nonconductive condition. The output signal supplied at the collector of transistor Q10 switches from a high level to a low level when transistor Q10 is rendered nonconductive. Thus, a low level output signal from transistor Q10 represents the application of a space tone at the input terminal. When a low level signal is produced at the collector of transistor Q10, transistor Q12 is rendered nonconductive by this relatively negative signal at its base electrode. When transistor Q12 is nonconductive, transistor Q14 is rendered conductive whereby transistor Q16 is rendered conductive. When transistor Q16 is rendered conductive, transistor Q15 is rendered conductive as well. The interaction of the transistor operation is readily apparent and not explained in detail. It will be noted that transistors Q15 and Q16 represent a set-reset flipflop which is now locked in the on or conductive condition. Furthermore, when transistor Q16 is rendered conductive, a current path is provided (via resistor 134) whereby transistor Q20 is rendered conductive. When transistor Q20 is rendered conductive a suitable current path is provided whereby transistor Q19 is also rendered conductive. Transistor Q19 is a switching transistor connected in series with the 12 volt line.

Thus, when transistor Q19 is conductive, the +12 volt signal is supplied at the collector thereof. When the +12 volt signal is supplied across transistor Q19, field effect transistor Q13 operates as a substantially constant current source. The constant current is supplied to capacitor 136. When capacitor 136 charges to the threshold potential of unijunction transistor Q18, this transistor conducts from the emitter electrode (E) to the base electrode (B1) and causes transistor Q17 to be conductive. When transistor Q17 is conductive, transistor Q15 is reset to the nonconductive condition. When transistor Q15 is reset, the current path related to transistor Q16 is interrupted and transistor Q16 is rendered nonconductive. Thus, the timer circuit comprising FET Q13, unijunction transistor Q18 and capacitor 136 operates to reset the flipflop comprising resistors Q15 and Q16 after a time delay determined by the RC time constant related to capacitor 136.

Obviously, when the flipflop comprising resistors Q15 and Q16 is tuned off, transistor Q19 will also become nonconductive. When transistor Q19 is nonconductive, the +12 volt signal is not supplied at the collector thereof. Thus, the remainder of the receiver network is effectively turned off.

Typically, the time period for operation of the timer network is between 1 and 1½ typical space tone durations. Thus, a space tone will trigger and initiate operation of the monostable and enable the power switch. When the monostable signal terminates, the timer begins its timing cycle. Subsequent space tones will restart the monostable which inhibits the timer and permits essentially continuous operation insofar as the +12 volt signal is concerned. However, in the event that a space tone is not received at the input and the monostable does not inhibit operation, the timer will cause the flipflop and transistor Q19 to be rendered nonconductive prior to the application of a data tone which would normally follow, in time sequence, after the space tone was not received.

In order to reset the timer network, additional circuitry is utilized. Thus, it is seen that the emitter of transistor Q11 is connected to one input of monostable circuit 323 (FIG. 4A). Another input of monostable 323 is connected through a feedback loop to one of the outputs of the monostable. This connection renders the monostable non-retriggerable. A further input of the monostable 323 is connected to the power source, for example, +5 volts. Another input of monostable 323 is connected to receive the inhibit signal which will be described hereinafter. Suitable power and energy sources are connected to appropriate terminals of monostable 323 via resistor 322 and then via diode 320 and capacitor 321. The signal from transistor Q11 operates to cause monostable 323 to produce a single, constant width, output signal in response to a space tone signal. Thus, if noise or spurious space tone signals are detected by the space tone circuitry during operation thereof, the additional signals to monostable 323 will have no effect thereupon.

The output terminals of monostable 323 produce complementary output signals. One output of monostable 323 is connected via resistor 311 to the base of transistor Q21. This output signal is positive going and is operative to render transistor Q21 conductive. When transistor Q21 is rendered conductive, capacitor 136 is essentially short circuited. Thus, the charge stored thereon is removed and capacitor 136 must be re-

charged. In essence, the timer network is reset at this point. Of course, transistor Q21 is maintained in the conductive condition only so long as the positive pulse is supplied by the operation of monostable 323. As soon as this single pulse is terminated, transistor Q21 becomes nonconductive and the timer circuit begins to operate again.

The positive going signal supplied by monostable 323 is also connected to the base of transistor Q45 to render this transistor conductive. When transistor Q45 is conductive, the potential at the collector thereof is a negative going signal. This negative going signal is supplied to counter 309 which operates to count only negative going pulses and produces binary outputs. The outputs of counter 309 are connected to gate 310 which normally produces a high level output signal until the inputs thereto are all binary ones. All binary ones at the input of gate 310 are indicative of a predetermined count at counter 309. When the output signal from gate 310 switches from the high level to the low level (i.e., representative of the predetermined count at counter 309), a relatively negative signal is supplied to the inhibit input (terminal 3) of monostable 323 thereby inhibiting operation thereof. That is, further space tone signals applied at terminal 2 of monostable 323 will not produce any operation by the monostable. Since monostable 323 can no longer receive space tones, it cannot produce a positive going pulse at the output thereof. Since this pulse cannot be produced, the timer network cannot be reset and the time signal produced thereby will be applied to the flipflop (transistors Q15 and Q16) and to transistor Q19. When transistor Q19 is switched to the nonconductive condition, the +12 volt signal supplied to the remainder of the circuit is terminated.

The +12 volt output signal produced by the entire switching portion of the sequence control circuit is supplied to an amplifier circuit including voltage regulator 141. This circuit operates to produce a +5 volt signal which is supplied to other portions of the system.

The +5 volt signal is applied to transistor Q25 via capacitor 313 whereby transistor Q25 is rendered nonconductive. When transistor Q25 is rendered nonconductive, the current path therethrough is interrupted and transistors Q24 and Q26 are also rendered nonconductive. When transistor Q26 is nonconductive capacitor 150 begins to charge until the threshold level for unijunction transistor Q27 is achieved. When the threshold level is reached, transistor Q27 conducts from emitter E to base B1 and supplies a positive signal to the bases of transistors Q28 and Q23 such that each of these transistors is rendered conductive. When transistor Q28 is conductive, a signal is supplied to the base of transistor Q29 whereby this transistor is also rendered conductive. When transistor Q29 is conductive the output signal detected at the collector thereof (i.e., across resistor 157) is a positive going signal. This signal is supplied to the decoding network as described hereinafter.

When transistor Q23 is rendered conductive by the application of the signal from transistor Q27, a relatively negative signal is supplied to the base of transistor Q25 via resistor 143 whereby this transistor is turned on. When transistor Q25 is conductive, the current paths relative to the bases of transistors Q24 and Q26 is changed and each of these transistors is now rendered conductive. Transistor Q24 latches transistor

Q25 in the conductive condition. Transistor Q26 is connected in parallel with capacitor 150. When transistor Q26 is operative, capacitor 150 is short circuited and transistor Q27 is rendered nonconductive. Since transistors Q24 and Q25 operate as a set-reset flipflop, the circuit now remains in this condition.

The output signal detected at the collector of transistor Q29 is also supplied via resistor 303 to the base of transistor Q41. This positive going signal renders transistors Q41 conductive to create a current path whereby transistor Q40 is rendered conductive. When transistor Q40 is conductive, a conduction path is provided (resistors 305, 306) whereby transistor Q42 is also rendered conductive. It will be seen that transistors Q40 and Q42 represent a set-reset flipflop and are substantially latched in this condition. When transistor Q40 is conductive, transistor Q43 is also rendered conductive whereby a relatively negative signal is supplied to the reset terminal of counter 309 to reset this circuit for subsequent counting.

Since the initial application of the +5 volt signal would be such as to render transistors Q40 and Q42 nonconductive, and since transistor Q41 is initially nonconductive, appropriate signals are supplied whereby transistor Q43 is initially nonconductive. Consequently, a relatively positive signal is supplied to the reset terminal of counter 309 via resistor 316. However, with the application of the positive going signal to the base of transistor Q41 via resistor 303, each of transistors Q40, Q42 and Q43 are rendered conductive as described. Thus, a relatively negative signal is supplied to the reset terminal of 309. With the termination of the positive signal applied via resistor 303 to base of transistor Q41, transistors Q40, Q42, and Q43 remain in the conductive condition. That is, transistors Q40 and Q42 represent a set-reset flipflop and are latched in the conductive condition. Consequently, a negative signal is supplied to reset terminal 309 until the counter circuit again completes its operation (i.e., reaches the predetermined count) and a new +5 volt signal is supplied to the circuit.

Referring now to FIG. 5, there is shown a schematic diagram of the tone detectors which operate on the data tones. Since the data tone detectors are essentially the same as the space tone detector, a detailed description thereof is deemed unnecessary. However, minor differences in circuit configuration are noted at the FET connections and the second differential amplifier network as described hereinafter.

The low current receiver signal which is supplied to the space tone detector input terminal is also supplied to the data tone detector input terminals. The respective data tone detector circuits operate upon this signal and produce output signals at the emitters of transistors Q30 and Q31, respectively. The emitter of transistor Q30 is connected to one input of nand gate 160 which, together with nand gate 161 comprises a flipflop. Thus, the output of nand gate 160 is connected to one input of gate 161. The output of gate 161 is returned to a second input of gate 160. The second input of gate 161 is connected via diode 162 to the data reset terminal of the space tone detector.

The output of gate 161 is connected via resistor 402 to the base of NPN transistor Q51. Transistor Q51 is connected between ground and the base of transistor Q44 in the D0 data tone network. Transistor Q51, when conductive in response to a signal from gate 161,

effectively clamps the D0 network and inhibits operation thereof when the D1 network is functioning.

The output circuitry (including gates 163 and 164) connected to the emitter of transistor Q31 (the D0 network) is similar in configuration to the circuitry described relative to the D1 network connected to transistor Q30. Gates 163 and 164 comprise a flipflop. One input of gate 163 is connected to the emitter of transistor Q31. One input of gate 164 is connected, via diode 165, to the data reset terminal of the space tone detector. The other inputs of each of gates 163 and 164 are connected to the output of the other of these gates. Furthermore, the output of gate 164 is connected to the base of NPN transistor Q50 via resistor 405. Transistor Q50 selectively clamps the D1 network and inhibits operation thereof when the D0 network is functioning. The cross-coupling between the D1 and D0 networks provides an additional measure of circuit operation protection.

The output of gates 161 and 164 are also connected to inputs of monostable circuits 400 and 401, respectively. The outputs D0 and D1 of the monostables are connected to inputs of the logic decoder circuit described hereinafter. Monostable circuits 400 and 401 produce uniform signals which trigger the logic circuit once and only once, for a prescribed time duration, after the appropriate data decoder network has been activated by an input signal.

Referring now to FIG. 6, there is shown the detailed circuitry of logic decoder 20. The inputs to logic decoder circuit 20 are supplied, as described supra, by the data tone detector circuits of FIG. 5. In addition, a delayed reset signal is supplied by the power switching circuit of FIG. 4B. The D1 data tone signal is supplied to one input of gate 175 which, together with gate 176, provides a flipflop circuit. Thus, the output of gate 175 is connected to one input of gate 176. The other input of gate 176 is provided by the D0 data tone input. The output of gate 176 is supplied to the second input of gate 175. The output of gate 175 is also connected to the input of shift register 177.

The D1 and D0 inputs are further supplied to the inputs of gate 178. The output of gate 178 is connected via series connected resistors 180 and 181 to one input of OR gate 182. Capacitor 183 connects the common junction of resistors 180 and 181 to a second input of gate 182 and also to ground potential. The output of gate 182 is connected to the first input thereof via feedback resistor 184. The output of gate 182 is further connected to the clock input of shift register 177. The output of gate 178 is also supplied directly to the input of counter circuit 179 which is shown in block diagram and is of any suitable design.

The output of counter 179 is supplied to the two terminals of nand gate 185. The output of gate 185 is connected to one input of gate 186. The other inputs of gate 186 are connected to a +V source whereby gate 186 is enabled. Thus, the input signal supplied by gate 185 acts as a toggle or switching signal and determines the output signal level of gate 186. The output of gate 186 is connected to one input of nand gate 187 described hereinafter.

The delayed reset signal from the circuit of FIG. 4B is supplied to one input of OR gate 188. The output of gate 188 is connected to a reset input of counter 179. The output of gate 188 is also connected to one input of nand gate 189. The other input of gate 189 is con-

nected to the +V source whereby the signal supplied by gate 188 operates as a toggle signal. The output of gate 189 is connected to an input of shift register 177 to supply a reset signal thereto.

A plurality of parallel output terminals of shift register 177 are connected to inputs of inverter gates 190. The outputs of gates 190 are supplies to inputs of gate 187 in addition to the input supplied by gate 186. An additional plurality of output signals supplied by shift register 177 is connected to inverter gates 191 which are connected to the inputs of gate 192. The output of gate 192 is supplied to one input of gate 193. The other input of gate 193 is supplied by the output of gate 187. The output of gate 193 is connected to an input of gate 194. The other inputs of gate 194 are connected to the +V source whereby gate 194 operates as an inverter relative to the signals supplied by gate 193.

Another plurality of output signals of shift register 177 are connected to inverter gates 195. The outputs of these gates are supplied to inputs of gate 197. In addition, the output of one of gates 195 is supplied to the input of gate 198 while the output of the other gate 195 is supplied to an input of gate 196. Moreover, the inputs of gates 195 are connected directly to two inputs of gate 199 and to one of the inputs of gates 196 and 198, respectively. Thus, gate 199 has two inputs thereof connected to receive the signals supplied by the last plurality of terminals on shift register 177 while gate 197 receives the complement of these signals. Gates 196 and 198 each receive one of the aforesaid signals directly and one signal after being inverted by gates 195. In addition, each of gates 196, 197, 198 and 199 has one input thereof connected to the output of gate 194 to thereby be concurrently enabled or disabled.

The outputs of gates 196, 197, 198 and 199 are connected directly to utilization device 21. The output signals produced by these gates are representative of the signal conditions in shift register 177. The signal conditions in shift register 177 are representative of the data tone information which has been received from a surface transmitter. Thus, the utilization device is controlled in accordance with this information.

In addition, the outputs of gates 196-199 are connected to inputs of nand gate 200. The output of gate 200 is connected to an input of OR gate 201 via series connected resistors 202 and 203. The common junction between resistors 202 and 203 is connected via capacitor 204 to ground. The second input of gate 201 is also connected to ground. Feedback resistor 205 is connected between the output of gate 201 and the first mentioned input thereof. The output of gate 201 is further connected to a second input of OR gate 188 to supply a reset signal thereto. Thus, gate 188 supplies reset signals to shift register 189 and counter 179 in response to operation within the decoder network, per se, or in response to the delay reset signal (from FIG. 4B).

In operation, the input signals D0 or D1 are supplied to the respective inputs of gates 175, 176 and 178. The flipflop, comprising gates 175 and 176, is set to the appropriate condition and a signal is supplied thereby to shift register 177. Simultaneously, the signal produced by gate 178 is supplied to the pulse delay circuit comprising resistors 180, 181, 184, capacitor 183 and OR gate 182. The length of the delay period is determined by the time constant of resistor 180 and capacitor 183. At the expiration of the delay period, a signal is sup-

plied (via gate 182) to the CLK (clock) input of shift register 177. When the CLK input signal is supplied, shift register 177 is enabled and the input signal (from gate 175) is entered into the shift register. The delay circuit is utilized to permit the input data signal to have achieved a steady-state condition and, thereby, prevent erroneous information from being stored in the shift register. Thus, the circuit becomes self-clocking in response to an input signal.

In addition, the signals generated by gate 178 (in response to an input signal D0 or D1) are supplied to counter 179. When the appropriate count has been achieved, gate 185 effectively decodes this signal, and causes gate 186 to supply an enabling signal to gates 187 and 192. When the enabling signal is supplied thereto, gates 187 and 192 effectively decode the signals supplied thereto by shift register 177. The signals from gates 187 and 192 are gated (and decoded) by gates 193 and 194 (which include level shifting and the like). If the input information is correct, gate 194 will supply an enabling signal to gates 196-199, inclusive. These gates then produce output signals which are a function of the input signals supplied thereto. The input signals are representative of the function to be performed by utilization device 21.

Of course, it should be understood that the gating arrangement from the output of shift register 177 through to the output gates (e.g., gates 196-199), is a function of the code arrangement for the system. In other words, if the code format (see FIG. 2) is changed, the aforesaid gating arrangement may have to be changed as well. However, this technique is known in the art and easily implemented.

Also, the output signals from gates 196-199 are supplied to gate 200. Thus, gate 200 will produce an output signal only when the enabling signal from gate 194 enables gates 196-199. The output signal from gate 200 is delayed by the pulse delay circuit including resistors 202, 203, and 205, capacitor 204 and OR gate 201. Again the delay period is determined by the time constant defined by resistor 203 and capacitor 204. At the expiration of the delay period, gate 201 produces a reset signal which is supplied to counter 179 and to shift register 177 (via gate 189). This reset signal (like the delayed reset signal from FIG. 4B) causes counter 179 and shift register 177 to be reset to a zero (or initial) condition. The delay in the output signal is included to delay the reset signal so that it has sufficient duration to ensure the operation of the succeeding circuitry. Thus, the decoder circuit must begin a new cycle. This requirement is especially desirable in the case of a reset signal produced by a missing space tone signal whereby an erroneous operation cannot be implemented.

Thus, there has been shown and described a proposed embodiment of a secure signalling system. While the input signals may be generated by acoustic means, other types of input devices are also contemplated. Also, the code format and the attendant coding arrangements are illustrative only. Changes in these areas are fully expected to be made as a function of the specific application of the system. These and other modifications which fall within the purview of the invention are intended to be included therein.

Having thus described a preferred embodiment of the invention, what is claimed is:

1. An acoustical receiver for receipt of a coded acoustical control signal having a plurality of distinctive space tones arranged at predetermined intervals with a distinctive data tone between successive space tones, a combination of a predetermined number of said data tones and space tones providing such a coded acoustic signal to be decoded at said receiver, said receiver providing for control of an utilization device upon receipt of a properly coded acoustic control signal, comprising, in combination: input means for receiving said coded acoustical control signal; detecting means connected to said input means and responding to receipt of said coded acoustical control signal to provide first output signals in response to received space tones and second output signals in response to received data tones; decoding means connected to said detecting means for decoding said second output signals; and switch means connected to said detecting means and said decoding means and operable in response to each of said first output signals to enable decoding of said second output signals for a time period at least as great as the time interval between successive space tones in said coded acoustical control signal, but substantially less than the duration of said acoustic coded signal whereby upon failure of receipt of at least one of said space tones said receiver means will be inhibited from acting upon further received data tones.

2. The receiver of claim 1 wherein said switch means includes a switching circuit adapted to assume a first condition in response to said first output signals to permit such detection and decoding and a second condition in response to a reset signal to inhibit such detection and decoding; and a timing circuit connected to said switching circuit and operable in response to said first output signal to begin a timing cycle of duration at least as great as said time interval between successive space tones, and responsive to the end of said timing cycle to provide said reset signal.

3. The receiver of claim 2 wherein said detecting means includes inhibit means connected to said timing circuit and responsive to said first output signal to in-

hibit the beginning of the timing cycle of said timing circuit during receipt of a space tone.

4. The receiver of claim 3 wherein said detecting means further includes counter means connected to said inhibit means for counting each of the received space tones and generating a signal to stop the operation of said inhibit means when a predetermined number of space tones in a sequence are counted.

5. The receiver of claim 1 wherein said detecting means includes a space tone circuit for providing said first output signals, and at least one data tone circuit for providing said second output signals, said data tone circuits connected to said switch means and operable to provide said second output signal upon receipt of a data tone in response to receipt of said first output signal by said switch means.

6. The receiver of claim 5 wherein said coded acoustical control signal includes two data tones each at a distinctive acoustical frequency, and said detecting means includes two data tone circuits, each being responsive to one of said distinctive data tones to provide said second output signals, and further including means connected to each of said data tone filters to inhibit the operation of one of said data tone circuits when the other data tone circuit is detecting its respective distinctive data tone.

7. The receiver of claim 5 wherein said input means, said space tone circuit and said switch means are continuously connected during operation of said receiver to a source of electrical power, and wherein said switch means connects said data tone circuit and said detecting means to said source of power when, during operation of said receiver, said first output signal is generated by said space tone circuit.

8. The receiver of claim 1 wherein said detecting means further includes counter means for counting each of the received space tones and generating a signal to stop the operation of said decoding means when a predetermined number of space tones in a sequence are counted.

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