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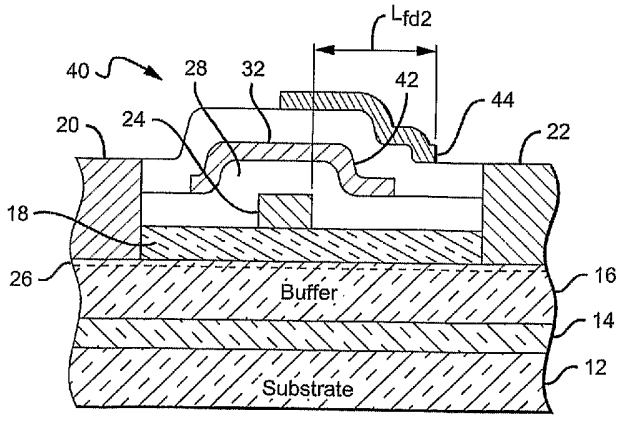

(57) Abstract: A transistor comprising an active region having a channel layer, with source and drain electrodes formed in contact with the active region and a gate formed between the source and drain electrodes and in contact with the active region. A spacer layer is on at least part of the surface of the plurality of active region between the gate and the drain electrode and between the gate and the source electrode. A field plate is on the spacer layer and extends on the spacer and over the active region toward the drain electrode. The field plate also extends on the spacer layer over the active region and toward the source electrode. At least one conductive path electrically connects the field plate to the source electrode or the gate.

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WIDE BANDGAP TRANSISTORS WITH GATE-SOURCE FIELD PLATES

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to transistors and particularly to transistors utilizing field plates to improve performance.

Description of the Related Art

Improvements in the manufacturing of AlGaN/GaN semiconductor materials have helped advance the development of AlGaN/GaN transistors, such as high electron mobility transistors (HEMTs) for high frequency, high temperature and high power applications. AlGaN/GaN has large bandgaps, high peak and saturation electron velocity values [B. Gelmont, K. Kim and M. Shur, *Monte Carlo Simulation of Electron Transport in Gallium Nitride,* J.Appl.Phys. 74, (1993), pp. 1818-1821]. AlGaN/GaN HEMTs can also have 2DEG sheet densities in excess of $10^{13}cm^{-2}$ and relatively high electron mobility (up to 2019 cm^2/Vs) [R. Gaska, et al., *Electron Transport in AlGaN-GaN Heterostructures Grown on 6H-SiC Substrates,* Appl.Phys.Lett. 72, (1998), pp. 707-709]. These characteristics allow AlGaN/GaN HEMTs to provide very high voltage and high power operation at RF, microwave and millimeter wave frequencies.

AlGaN/GaN HEMTs have been grown on sapphire substrates and have shown a power density of 4.6 W/mm and a total power of 7.6 W [Y.F. Wu et al., *GaN-Based FETs for Microwave Power Amplification,* IEICE Trans. Electron. E-82-C, (1999). pp. 1895-1905]. More recently, AlGaN/GaN HEMTs grown on SiC have shown a power density of 9.8 W/mm at 8 GHz [Y.F. Wu, et al., *Very-High Power Density AlGaN/GaN HEMTs*, IEEE Trans.Electron.Dev. 48, (2001), pp. 586-590] and a total output power of 22.9 W at 9 GHz [M. Micovic, et al., *AlGaN/GaN Heterojunction Field Effect Transistors Grown by Nitrogen Plasma Assisted Molecular Beam Epitaxy,* IEEE Trans.Electron.Dev.48, (2001), pp. 591-596].

U.S. Patent number 5,192,987 to Khan et al. discloses GaN/AlGaN based HEMTs grown on a buffer and a substrate. Other AlGaN/GaN HEMTs and field effect transistors (FETs) have been described by Gaska et al., *High-Temperature Performance of AlGaN/GaN HFET's on SiC Substrates*, IEEE Electron Device Letters, 18, (1997), pp. 492-494; and Wu et al.. *High Al-content AlGaN/GaN HEMTs With Very High Performance*, IEDM-1999 Digest, pp. 925-927, Washington DC, Dec. 1999. Some of these devices have shown a gain-bandwidth product (f_T) as high as 100 gigahertz (Lu et al., *AlGaN/GaN HEMTs on SiC With Over 100 GHz ft and Low Microwave Noise*, IEEE Transactions on Electron Devices, Vol. 48, No. 3, March 2001, pp. 581-585) and high power densities up to 10 W/mm at X-band (Wu et al., *Bias-dependent Performance of High-Power AlGaN/GaN HEMTs*, IEDM-2001, Washington DC, Dec. 2-6, 2001) and Wu et al.,*High Al-Content AlGaN/GaN MODFETs for Ultrahigh Performance,* IEEE Electron Device Letters 19, (1998), pp. 50-53).

Electron trapping and the resulting difference between DC and RF characteristics have been a limiting factor in the performance of these devices. Silicon nitride (SiN) passivation has been successfully employed to alleviate this trapping problem resulting in high performance devices with power densities over 10W/mm at 10 Ghz. For example, U.S. Patent No. 6,586,781, which is incorporated herein by reference in its entirety, discloses methods and structures for reducing the trapping effect in GaN-based transistors. However, due to the high electric fields existing in these structures, charge trapping is still an issue.

Field plates have been used to enhance the performance of GaN-based HEMTs at microwave frequencies [See S Kamalkar and U.K. Mishra, *Very High Voltage AlGaN/GaN High Electron Mobility Transistors Using a Field Plate Deposited on a Stepped Insulator,* Solid State Electronics 45, (2001), pp. 1645-1662]. These approaches, however, have involved a field plate connected to the gate of the transistor with the field plate on top of the drain side of the channel. This results in reducing the electric field on the gate-to-drain side of the transistor thereby increasing breakdown voltage and reducing the high-field trapping effect. Transistors, however, with gate-drain field plates only have shown relatively poor reliability performance, particularly at class C (or higher class) operation where the electric field on the source side of the gate becomes significant.

SUMMARY OF THE INVENTION

The present invention provides transistors that operate with reduced electric field on the source side of the gate. One embodiment of a transistor according to the

present invention comprises an active region having a channel layer. Source and drain electrodes are in contact with the active region and a gate is between the source and drain electrodes and in contact with the active region. A spacer layer is on at least part of the surface of said active region between the gate and the drain electrode and between the gate and the source electrode. A field plate is on the spacer layer and extends on the spacer and over the active region toward the drain electrode. The field plate also extends on the spacer layer over the active region and toward the source electrode. At least one conductive path electrically connects the field plate to the source electrode or the gate.

One embodiment of a high electron mobility transistor (HEMT) according to the present invention comprises a buffer layer and barrier layer arranged successively on a substrate, with a two dimensional electron gas (2DEG) channel layer at the heterointerface between the buffer layer and said barrier layer. A source and a drain electrode are included both making contact with the 2DEG, and a gate is included on the barrier layer between the source and drain electrodes. A spacer layer is on at least part of the surface of the barrier layer between the gate and the drain electrode and between the gate and the source electrode. A field plate is on the spacer layer, extending on the spacer over the barrier layer toward the drain electrode and extending on the spacer layer over the barrier layer toward the source electrode. At least one conductive path electrically connects the field plate to the source electrode or the gate.

One embodiment of a metal semiconductor field effect transistor (MESFET) according to the present invention comprises a buffer layer on a substrate and a channel layer on the buffer layer, with the buffer layer sandwiched between the channel layer and substrate. A source electrode is in electrical contact with the channel layer and a drain electrode is also in electrical contact with the channel layer. A gate is included also in electrical contact with the channel layer between the source and drain electrodes. A spacer layer is on at least part of the surface of the channel layer between the gate and the drain electrode and between the gate and the source electrode. A field plate is on the spacer layer, extending on the spacer over the channel layer toward the drain electrode and extending on the spacer layer over the channel layer toward the source electrode. At least one conductive path electrically connects the field plate to the source electrode or the gate.

These and other further features and advantages of the invention would be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of one embodiment of a HEMT according to the present invention;

FIG. 2 is a sectional view of the HEMT shown in FIG. 1;

FIG. 3 is a sectional view of another embodiment of a HEMT according to the present invention;

FIG. 4 is a sectional view of another embodiment of a HEMT according to the present invention;

FIG. 5 is a sectional view of another embodiment of a HEMT according to the present invention having multiple field plates;

FIG. 6 is a sectional view of another embodiment of a HEMT according to the present invention having multiple field plates;

FIG. 7 is a sectional view of another embodiment of a HEMT according to the present invention having multiple field plates;

FIG. 8 is a sectional view of another embodiment of a HEMT according to the present invention;

FIG. 9 is a sectional view of one embodiment of a MESFET according to the present invention;

FIG. 10 is a sectional view of another embodiment of a MESFET according to the present invention; and

FIG. 11 is a table comparing the operating characteristics of a HEMT according to the present invention compared to a HEMT with no field gate-source field plate.

DETAILED DESCRIPTION OF THE INVENTION

The gate-source field plate arrangements according to the present invention can be used with many different transistor structures, such as transistor structures made of wide bandgap materials. Transistors generally include an active region having a plurality of semiconductor layers, one of which is a channel layer. Metal source and drain electrodes formed in contact with the active region, and a gate formed on the active region between the source and drain electrodes for modulating electric fields within the active region. A first spacer layer is formed above the active region, over at least a portion of the surface of the active region between the gate and

the drain. The first spacer layer can comprise a dielectric layer or a combination of multiple dielectric layers, and in certain embodiments other materials such as epitaxially grown layers. In one embodiment the first spacer layer covers the gate and the topmost surface of the active region between the gate and the drain electrode, and between the gate and the source electrode. In other embodiments as described below the spacer layer can cover less of the surface of the active region. In still other embodiments the spacer layer covers only the topmost surface of the active region between the gate and the source and drain, and not the gate.

A conductive first field plate is formed on the first spacer layer with the first spacer layer providing isolation between the field plate the active region below. The first field plate extends a distance L_{fd} on the spacer layer from the edge of the gate toward the drain electrode, and extends a distance L_{fs} on the spacer layer toward the source electrode. The first field plate can be electrically connected to either the source electrode or the gate. Additional spacer layer field and field plate pairs can also be included in different embodiments according to the invention.

This field plate arrangement can reduce the peak electric field in the device on both the source and drain side of the gate, resulting in increased breakdown voltage and reduced trapping. The reduction of the electric field can also yield other benefits such as reduced leakage currents and enhanced reliability. The field plates on both the source and drain sides of the gate are arranged such that the electric field on the source side of the gate is reduced, which enhances performance and robustness for applications that require

more negatively biased gate conditions. This includes class-C and other higher classes (e.g. E, F) of operations. By having the field plate on the drain side as well, the transistor also experiences reduced peak electric field on the drain side.

One type of transistor that can utilize the gate-source plate arrangement according to the present invention is a high electron mobility transistor (HEMT), which typically includes a buffer layer and a barrier layer on the buffer layer. A two dimensional electron gas (2DEG) channel layer is induced at the heterointerface between the buffer layer and the barrier layer. A gate electrode is formed on the barrier layer between source and drain electrodes. The HEMT also includes the multiple spacer layer and field plate arrangement described above.

Another type of transistor that can utilize the gate-source field plate arrangement according to the present invention is a field effect transistor and particularly a metal semiconductor field effect transistor (MESFET), which typically includes a buffer layer and a channel layer on the buffer layer. A gate is formed on the channel layer between source and drain electrodes and the MESFET also includes the multiple spacer layer and field plate arrangement described above.

It will be understood that when an element or layer is referred to as being "on", "connected to", "coupled to" or "in contact with" another element or layer, it can be directly on, connected or coupled to, or in contact with the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to" , "directly coupled to" or "directly in contact with" another element or layer, there are no

intervening elements or layers present. Likewise, when a first element or layer is referred to as being "in electrical contact with" or "electrically coupled to" a second element or layer, there is an electrical path that permits current flow between the first element or layer and the second element or layer. The electrical path may include capacitors, coupled inductors, and/or other elements that permit current flow even without direct contact between conductive elements.

FIGs. 1 and 2 show one embodiment of a HEMT 10 according to the present invention that is preferably Group-III nitride based, although other material systems can also be used. Group III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in the Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and tertiary compounds such as AlGaN and AlInGaN.

The HEMT 10 comprises a substrate 12 which can be made from silicon carbide, sapphire, spinet, ZnO, silicon, gallium nitride, aluminum nitride, or any other material or combinations of materials capable of supporting growth of a Group-III nitride material. A nucleation layer 14 can be formed on the substrate 12 to reduce the lattice mismatch between the substrate 12 and the next layer in the HEMT 10. The nucleation layer 14 should be approximately 1000 angstroms (Å) thick, although other thicknesses can be used. The nucleation layer 14 can comprise many different materials, with a suitable material being $Al_zGa_{1-z}N$ ($0<=z<=1$), and can be formed on the substrate 12 using known semiconductor growth techniques such as Metal Organic Chemical Vapor

Deposition (MOCVD), Hydride Vapor Phase Epitaxy (HVPE), or Molecular Beam Epitaxy (MBE).

Substrate 12 can be made of many different materials with a suitable substrate being a 4H polytype of silicon carbide, although other silicon carbide polytypes can also be used including 3C, 6H and 15R polytypes. Silicon carbide has a much closer crystal lattice match to Group III nitrides than sapphire and results in Group III nitride films of higher quality. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is not limited by the thermal dissipation of the substrate (as may be the case with some devices formed on sapphire). Also, the availability of silicon carbide substrates provides the capacity for device isolation and reduced parasitic capacitance that make commercial devices possible. SiC substrates are available from Cree, Inc., of Durham, North Carolina and methods for producing them are set forth in the scientific literature as well as in a U.S. Patents, Nos. Re. 34,861; 4,946,547; and 5,200,022.

The formation of a nucleation layer 14 can depend on the material used for the substrate 12. For example, methods of forming a nucleation layer 14 on various substrates are taught in U.S. Patents 5,290,393 and 5,686,738, each of which are incorporated by reference as if fully set forth herein. Methods of forming nucleation layers on silicon carbide substrates are disclosed in U.S. Patents 5,393,993, 5,523,589, and 5,739,554 each of which is incorporated herein by reference as if fully set forth herein.

The HEMT 10 further comprises a high resistivity buffer layer 16 formed on the nucleation layer 14. The

buffer layer 16 can comprise doped or undoped layers of Group III-nitride materials with a preferred buffer layer 16 made of a Group III-nitride material such as $Al_xGa_yIn_{(1-x-y)}N$ ($0<=x<=1$, $0<=y<=1$, $x+y<=1$). Other materials can also be used for the buffer layer 16 such as GaN that is approximately 2μm thick, with part of the buffer layer doped with Fe.

A barrier layer 18 is formed on the buffer layer 16 with the buffer layer 16 being sandwiched between the barrier layer 18 and the nucleation layer 14. Like the buffer layer 16, the barrier layer 18 can comprise doped or undoped layers of Group III-nitride materials. The barrier layer can be made of one or multiple layers of $Al_xGa_{1-x}N$, where x ranges from 0-1, and x can be a function of depth such that the barrier layer 18 can be a graded layer. A 2DEG channel layer 26 is induced at the heterointerface between the buffer layer 16 and the barrier layer 18, with the buffer layer 16, 2DEG channel layer 26 and barrier layer 18 generally forming the HEMTs active region.

Exemplary HEMT structures are illustrated in U.S. Patent Nos. 6,316,793, 6,586,781, 6,548,333 and U.S. Published Patent Application Nos. 2002/0167023 and 2003/00020092 each of which is incorporated by reference as though fully set forth herein. Other nitride based HEMT structures are illustrated in U.S. Patents 5,192,987 and 5,296,395 each of which is incorporated herein by reference as if fully set forth herein. The buffer and barrier layers 16, 18 can be made using the same methods used to grow the nucleation layer 14. Electric isolation between the devices is accomplished through mesa etch or ion implementation outside the active HEMT.

Metal source and drain electrodes 20, 22 are formed in contact with the barrier layer 18, and a gate 24 is formed on the barrier layer 18 between the source and drain electrodes 20, 22. Electric current can flow between the source and drain electrodes 20, 22 through the 2DEG channel layer 26 between the buffer layer 16 and the barrier layer 18 when the gate 24 is biased at the appropriate level. The formation of source and drain electrodes 20, 22 is described in detail in the patents and publications referenced above.

The source and drain electrodes 20, 22 can be made of different materials including but not limited to alloys of titanium, aluminum, gold or nickel. The gate 24 can also be made of different materials including but not limited to gold, nickel, platinum, titanium, chromium, alloys of titanium and tungsten, or platinum silicide. The gate 24 can have many different lengths (L_g), with a suitable gate length ranging from 0.1 to 2.0 microns (μm), although other gate lengths can also be used. In one embodiment according to the present invention a preferred gate length (L_g) is approximately 0.5 microns.

A first non-conducting spacer layer 28 is formed over the gate 24 and at least part of the surface of the barrier layer 18 between the gate 24 and the source and drain electrodes 20, 22. As shown in FIG. 2, the spacer layer 28 covers all of the barrier layer 18 between the gate 24 and source and drain electrodes 22, 24. The spacer layer 28 can comprise a dielectric layer, or a combination of multiple dielectric layers. Different dielectric materials can be used such as a SiN, SiO2, Si, Ge, MgOx, MgNx, ZnO, SiNx, SiOx, alloys or layer sequences thereof. The spacer layer can be many different thicknesses, with a suitable range of thicknesses being

approximately 0.03 to 0.5 microns. As best shown in FIG. 1, the gate 24 is contacted at a gate contact 30.

A first field plate 32 is formed on the spacer layer 28 over the gate 24, with the first field plate extending on the spacer layer 28 a distance L_{fd} toward the drain electrode 22 and extending a distance L_{fs} toward the source electrode 20. The spacer layer 28 is arranged to provide isolation between the first field plate 32 and the barrier layer 18 and gate 24, so the spacer layer 28 need only cover the gate 18 and barrier layer 18 below the first field plate 32. For ease of manufacturing, however, the spacer layer typically covers the entire barrier layer 18. L_{fd} can be different distances with a suitable range of distances being from 0.1 to 5 microns. Similarly, L_{fs} can be different distances with a suitable range of distances being 0.1 to 2 microns. In other embodiments, the field plates may not be continuous, but can have holes or interruptions as desired.

The field plate 32 can comprise many different conductive materials with a suitable material being a metal deposited using standard metallization methods. In one embodiment according to the present invention the field plate 30 comprises the same metal as the feature that it is electrically connected to as described below.

The first field plate 32 can be electrically connected to either the source electrode 20 or the gate 24. FIG. 1 shows one embodiment according to the present invention wherein the first field plate 32 is connected to the source electrode 20, with two alternative connection structures being shown. First conductive buses 34 can be formed on the spacer layer 26 to extend between the first field plate 32 and the source electrode 20. Different numbers of buses 34 can be used although the

more buses 32 that are used, the greater the unwanted capacitance that can be introduced by the buses. The buses 34 should have a sufficient number so that current effectively spreads between the source electrode 20 and the first field plate 32, while covering as little of the HEMTs active region as possible. A suitable number of buses 34 can be three as shown in FIG. 1.

The first field plate 32 can also be electrically connected to the source electrode 20 through a first conductive path 36 that runs outside of the active region of the HEMT 10 and is connected to the source electrode 20. As shown in FIG. 1, the path 36 runs outside the active area of the HEMT at the edge opposite the gate contact 30. In alternative embodiments according to the present invention, the conductive path could run outside the active area of the HEMT 10 on the side of the gate contact 30, or the HEMT 10 could include two or more conductive paths running on one or both sides of the HEMT 10. In one embodiment, the conductive paths 34, 36 can be made of the same material as the source electrode 20 and in other embodiments they can be made of a different material and can be formed at a different step in the fabrication process after formation of the source electrode 20.

The first field plate 32 can also be electrically connected to the gate 24 by many different methods, with two suitable methods described herein. First, the field plate can be connected to the gate 24 by a second conductive path 38 that runs outside of the active region of the HEMT 10 between the first field plate 32 and gate 24. The conductive path 38 can connect to the gate contact 30 or a portion of the gate 24 outside of the HEMTs active region, such as the portion of the gate 24

opposite the gate contact 30. Alternatively, more than one conductive path can be used to connect the field plate 32 and gate 24.

An alternative connection structure comprises conductive paths in the form of conductive vias (not shown), which can be formed running from the first field plate 32 to the gate 24, through the first spacer layer 28. The vias provide an electrical connection between the gate 24 and first field plate 32 and the vias can be formed by first forming holes in the first spacer layer 28, such as by etching, and then filling the holes with a conductive material either in a separate step or during formation of the first field plate 32. The vias can be arranged periodically down the first field plate 32 to provide for effective current spreading from the gate 24 to the field plate 32.

FIG. 3 shows the HEMT 40 that is the same as the HEMT 10 of FIGs. 1 and 2, but also includes a second non-conducting spacer layer 42 that is formed over at least a portion of the first field plate 32, with a preferred second spacer layer 42 as shown covering the first field plate and the exposed surface of the first spacer layer 28. The second spacer layer 42 can be formed of the same material or layers of material as the first spacer layer 28 and can have a total thickness in the range of 0.05 to 2 microns.

A second field plate 44 can then be deposited on the second spacer layer 42. Different second field plates according to the present invention can provide different coverage, with the second field plate 44 as shown overlapping the gate 24. Other second field plates according to the present invention can have a space between the edge of the gate 24 and the starting edge of

the second field plate. Another portion of the second field plate 44 extends from the edge of gate 24 toward the drain contact 22 a distance L_{fd2}, which can be in the range of 0.2 to 5 microns. In those embodiments where the second spacer layer 42 covers less than all of the first field plate 32 and spacer layer 28, the second spacer layer 42 must cover enough of the first field plate 32 to provide electrical isolation between the first and second field plates 32, 44.

The second field plate 44 can be connected to the source electrode 20 or the gate 24 and many different connecting structures can be used. Second conductive buses can be formed on the second spacer layer 42 to extend between the second field plate 44 and the source electrode 20. Different numbers of buses can be used so that current effectively spreads from the source electrode 20 into the second field plate 44, while not covering too much of the active region such that unwanted capacitance is introduced. The first field plate 32 can also be electrically connected to the source electrode 20 through a third conductive path that runs outside of the active region of the HEMTs 40 and is connected to the source electrode 20.

After deposition of the second field plate 44 and its connection to the source electrode 20, the active structure can be covered by a dielectric passivation layer (not shown), such as silicon nitride. Methods of forming the dielectric passivation layer are described in detail in the patents and publications referenced above. The HEMT 10 in FIGs. 1 and 2 and the HEMTs and MESFETs described below can also be covered by a dielectric passivation layer after formation of the spacer layer(s) and field plates(s).

FIG. 4 shows another embodiment of a HEMT 60 according to the present invention having many features that are similar to those in HEMT 10, and for those similar features the same reference numbers are used. HEMT 60 comprises a substrate 12, nucleation layer 14, buffer layer 16, barrier layer 18, source electrode 20, drain electrode 22, gate 24 and 2DEG 26 channel layer. Like above, the gate 24 has a width L_g ranging from 0.1 to 5 microns.

The HEMT 60, however, comprises a spacer layer 62 that does not cover the gate 24, but instead covers the barrier layer 18 between the gate 24 and the source and drain contacts 20, 22. In other embodiments, the spacer layer can cover less than the entire surface of the barrier layer 18, as described above. The coverage should be enough to provide electric isolation between the first field plate 64 and the barrier layer 18. The first field plate 64 is formed integral to the gate 24 and extends on the spacer layer 62 a distance L_{fd} in the range of 0.2 to 5 microns toward the drain contact 22, and a distance L_{fs} in the range of 0.1 to 2 microns toward the source contact 20. For the HEMT 60 the first field plate is electrically connected to the gate 24 by its integral formation with the gate 24. The field plate 62 can be fully integral with the gate or can have breaks of holes in its integral connection on either the source or drain side of the contact, or both, as long as enough conductive paths are available to effectively spread current between the gate 24 and field plate 64.

In HEMT 60 the first spacer layer 62 can be formed before device metallization and in those instances the spacer layer can comprise an epitaxial material such as a Group III nitride material having different Group III

elements such as alloys of Al, Ga, or In, with a suitable spacer layer material being $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$). After epitaxial growth of the barrier layer 18, the first spacer layer 62 can be grown using the same epitaxial growth method. The first spacer layer 62 is then etched to provide an opening for the gate 24, source electrode 20 and drain electrode 22. During metallization the gate 24 is formed in electrical contact with the barrier layer 18 and the first field plate 64 is formed integral to the gate and extending on the spacer layer 62. The source and drain electrodes 20, 22 can be formed during this same metallization step.

In other embodiments the gate 24 can be first metalized on the active region and the spacer layer can be formed of a dielectric material on the active region between the gate 24 and source and drain contacts 20, 22. The field plate 64 can then be formed integral to the gate 24. By having the field plate 64 extend toward both the source electrode 20 and the gate electrode 22, the HEMT 60 experiences the same operating benefits as the HEMT 10 in FIGs. 1 and 2.

FIG. 5 shows another embodiment of a HEMT 70 that is similar to the HEMT 60 shown in FIG. 4 and has a substrate 12, nucleation layer 14, buffer layer 16, barrier layer 18, source electrode 20, drain electrode 22, gate 24, 2DEG channel layer 26, first spacer layer 62 and first field plate 64. The HEMT 70, however, also has a second dielectric spacer layer 72 and a second field plate 74, with the second spacer layer covering enough of the first field plate 64 to provide electric isolation between the first and second field plates 64, 74. As shown, the spacer layer covers the first field plate 64 and the exposed surfaces of the first spacer layer 62.

The second field plate 74 can be electrically connected to the source contact 20 or the gate using different methods, including the conductive paths described above that run outside the HEMT's active region.

The HEMTs 40 and 70 (as well as the HEMTs and MESFETs described below) can also comprise additional spacer layer and field plate pairs over the second field plate 72 and second spacer layer 74. FIG. 5 shows an additional pair on the HEMT 70 comprising a third spacer layer 76 (in phantom) and a third field plate 78 (in phantom), with the spacer layer 76 covering enough of the second field plate 74 to provide electric isolation between the second and third field plates 74, 76. The third field plate 78 (and any subsequent field plates) can also be electrically coupled to the source electrode or gate, by the methods described above.

In a preferred embodiment, the top field plate is connected to the source electrode while the intermediate field plates below can be connected to the source electrode or the gate. For example, a transistor according to the present invention can have three field plates, with the top one connected to the source electrode and the ones below connected to either the source electrode or the gate.

This multiple field plate arrangement can further reduce the peak electric field in the device, resulting in increased breakdown voltage and reduced trapping. This can improve gain and stability that can be negatively impacted by gate connected field plates. When arranged according to the present invention, the shielding effect of a source-connected field plate can reduce C_{gd}, which enhances input-output isolation.

FIG. 6 shows another embodiment of a HEMT 80 according to the present invention that is similar to the HEMT 10 in FIGs. 1 and 2, and FIG. 7 shows another embodiment of a HEMT 90 according to the present invention that is similar to the HEMT 70 in FIG. 5. HEMTs 80 and 90 each have a substrate 12, nucleation layer 14, buffer layer 16, barrier layer 18, source electrode 20, drain electrode 22 and 2DEG channel layer 26. The HEMT 80 has a gate 82, a first dielectric spacer layer 84 and first field plate 86, but unlike the gate 24 in FIGs. 1 and 2, the gate 80 is recessed in the barrier layer 18. The first spacer layer 84 covers the gate 82 and barrier layer sufficiently to provide electric isolation between the gate 82 and the field plate 86, and the field plate extends on the spacer layer 84 on one side of the gate toward the drain electrode 20 and on the other side toward the source electrode 22, both in the ranges of distances described above. Additional spacer layer and field plate pairs can be included and electrically connected as described above, with the HEMT 80 having a second pair 88 (shown in phantom).

The HEMT 90 has a gate 92, spacer layer 94 and integral field plate 96, with the gate 92 recessed in the barrier layer 18. The spacer layer 94 can be made of the same materials as the spacer layer 84 shown in FIG. 5 and described above, and could cover enough of the barrier layer 18 to provide electrical isolation between the field plate 96 and the barrier layer. In other embodiments the bottom surface of the gate can be partially recessed or different portions of the gate can be recessed to different depths in the barrier layer 18. Additional spacer layer and field plate pairs can be included and electrically connected as described above,

with the HEMT 90 having a second pair 98 (shown in phantom).

FIG 8 shows another embodiment of a HEMT 100 according to the present invention that is similar to the HEMT 10 shown in FIGs. 1 and 2 and has a substrate 12, nucleation layer 14, buffer layer 16, barrier layer 18, source electrode 20, drain electrode 22, gate 24, 2DEG 26 and first spacer layer 28. However, instead of having a single first field plate, it has a first field plate that is separated into a source field plate 102 and a drain field plate 104. The source field plate 102 overlaps the source side of the gate 24 and extends a distance L_{fs} on the spacer layer 28 toward the source electrode 20, with L_{fs} being in the range of distances described above. The drain field plate 104 overlaps the gate 24 and extends a distance L_{fd} on the spacer layer 28 toward the drain contact 22, with L_{fd} being in the range of distances described above. The source and drain field plates 102, 104 can each be connected to the source contact 20 or the gate 24 (using the methods described above), or one can be connected to the source contact 20 and the other connected to the gate 24.

In different embodiments, the source and drain field plates 102, 104 do not need to overlap the gate 24, and one or both can have a gap between the edge of the gate and the edge of the field plate. Overlapping of the gate can introduce additional capacitance that can negatively impact performance. For source and drain field plates to effectively reduce the electric field, a gap between the edge of the gate and the field plates must be relatively small, which can present some difficulties during fabrication. By having the field plates 102, 104 overlap the gate 24, the HEMT can be fabricated without having to

meet the tolerances of this small gap. In determining whether to use an overlapping field plate or non-overlapping field plate, the ease of manufacturing is balanced with the reduced capacitance.

The structures of the present invention can also be used in other types of transistors made of different material systems. FIG. 9 shows one embodiment of a MESFET 110 according to the present invention that is silicon carbide based. MESFET 110 comprises a silicon carbide substrate 112 on which a silicon carbide buffer 114 and a silicon carbide channel layer 116 are formed with the buffer 114 sandwiched between the channel layer 116 and substrate 112. The buffer 114 and channel layer 116 generally form the MESFET's active region. Source and drain electrodes 118, 120 are formed in contact with the channel layer 116 and a gate 122 is formed on the channel layer 116 between the source and drain electrodes 118, 120. In the preferred embodiment, the gate 122 is recessed in the channel layer 116, although it can also be on the channel layer 116 without recess as long as adequate electrical contact is made between the two. The gate 122 can also be partially recessed, with only part of its bottom surface recessed in the channel layer 116.

A non-conducting (dielectric) spacer layer 124 is formed over the gate 122 and the surface of the channel layer 116 between the gate 122 and the source and drain electrodes 118, 120. Similar to the spacer layer 28 described above and shown in FIGs. 1 and 2, the spacer layer 124 can comprise a layer of non-conducting material such as a dielectric, or a number of different layers of non-conducting materials such as different dielectrics.

A first field plate 126 is formed on the spacer layer 124 between and over the gate 122 and extends a

distance L_{fs} on the spacer layer 124 toward the source electrode 118, and a distance L_{fd} toward the drain electrode 120, both in the range of distances described above. The field plate 126 can also be connected to either the source electrode 118 or the gate 122 using the same connecting structures as described above. The first field plate can also comprise more than one field plate, such as the two piece drain field plate and source field plate arrangement described above.

A second non-conducting spacer layer 128 (in phantom) can be formed over the first field plate 126 and first spacer layer 124 and is similar to second spacer layer 40 described above and shown in FIG. 3. Similarly, a second field plate 130 (in phantom) is provided on the second spacer layer 128, and is similar to the second field plate 42 described above and shown in FIG. 3, and is similarly connected.

FIG. 10 shows another embodiment of a silicon carbide MESFET 140 according to the present invention that has similar features of the MESFET 110 in FIG. 9, including a substrate 112, buffer 114, channel layer 116, source electrode 118, drain electrode 120. A recessed gate 142 is formed on the channel layer 116 between the source and drain electrodes 118, 120, although it can also be on the channel layer 116. MESFET 140 also comprises a spacer layer 144 that does not overlap the gate 142, but covers at least part of the surface of the channel layer 116 between the gate 142 and the source and drain electrodes 118, 120. Field plate 146 is formed integral with the gate 142 and extends a distance L_{fs} on the spacer layer 144 toward the source electrode 118, and a distance L_{fd} toward the drain electrode 120, both in the range of distances described above. The spacer layer 144

can be a dielectric material and in those instances where the spacer layer 144 is formed before device metallization, the spacer layer can comprise an epitaxial material as described above.

FIG. 11 shows a table 130 comparing the operating characteristics of GaN based HEMT (Device A) with no gate-source field plate compared to the operating characteristics of a GaN based HEMT (Device B) with a gate-source field plate having a length of 0.2 microns. The measurements of Device A and B were taken in reference to power degradation at 200C class-C operation for 10 hours with Vg = -7V at 4 gigahertz (GHz) driven to 1 decibel (dB) compression. The measurements show breakdown in Device A, while Device B does not experience breakdown under the same conditions.

It is understood that the field plate arrangement can be applied to other transistors beyond HEMTs and MESFETs, with one example being a Metal Oxide Semiconductor Heterostructure Field Effect Transistor (MOSHFET). In MOSHFETS, the spacer layer can be formed between the gate and the MOSHFETs active region. The spacer layer can be partially removed from under the gate so that the gate is on a then spacer (insulator) layer while the field plate is on a thicker spacer (insulator) layer. The gate would still be "in contact" with the active region through the insulator layer, with the MOSHFET arrangement designed to reduce gate leakage.

The embodiments above provide wide bandgap transistors with improved power at microwave and millimeter wave frequencies. The transistors exhibit simultaneous high gain, high power, and more stable operation due to higher input-output isolation. The

structure could be extended to larger dimensions for high voltage applications at lower frequencies.

Although the present invention has been described in considerable detail with reference to certain preferred configurations thereof, other versions are possible. The field plate arrangement can be used in many different devices. The field plates can also have many different shapes and can be connected to the source contact in many different ways. For example, the field plate can extend from over the HEMT's active area such that the connection is continuous between the field plate and source contact, instead of through buses or conductive paths. This arrangement can, however, introduce prohibitive capacitance into the structure. Accordingly, the spirit and scope of the invention should not be limited to the preferred versions of the invention described above.

WE CLAIM:

1. A transistor, comprising:

an active region having a channel layer;

source and drain electrodes in contact with said active region;

a gate between said source and drain electrodes and in contact with said active region;

a spacer layer on at least part of the surface of said active region between said gate and said drain electrode and between said gate and said source electrode;

a field plate on said spacer layer and extending on said spacer and over said active region toward said drain electrode, and extending on said spacer layer over said active region and toward said source electrode; and

at least one conductive path electrically connecting said field plate to said source electrode or said gate.

2. The transistor of claim 1, wherein said field plate extends on said spacer layer a distance L_{fd} from the edge of said gate toward said drain electrode.

3. The transistor of claim 1, wherein said field plate extends on said spacer layer a distance L_{fs} from the edge of said gate toward said source electrode.

4. The transistor of claim 1, wherein said spacer layer covers said gate and said field plate overlaps said gate and extends on said spacer toward said drain electrode and extends on said spacer layer toward said source electrode.

5. The transistor of claim 1, wherein said at least one conductive path runs between said field plate and source electrode, each said path running outside of said active region and providing said field plate electrical connection with said source electrode.

6. The transistor of claim 1, wherein said at least one conductive path runs between said field plate and source electrode over said spacer layer.

7. The transistor of claim 1, wherein said at least one conductive path runs between said field plate and gate, each said path running outside of said active region and providing said field plate electrical connection with said gate.

8. The transistor of claim 1, wherein said at least one conductive path comprises conductive vias running between said field plate and said gate through said spacer layer.

9. The transistor of claim 1, wherein said spacer layer covers at least part of the surface of said active region from said gate to said drain electrode, and from said gate to said source electrode, said field plate formed integral to said gate and extending on said spacer layer toward said source electrode and said drain electrode.

10. The transistor of claim 1, wherein said plurality of active region is formed on a substrate.

11. The transistor of claim 1, wherein said plurality of active region is formed of Group-III nitride based semiconductor materials.

12. The transistor of claim 1, wherein said spacer layer comprises a dielectric material, or multiple layers of dielectric material.

13. The transistor of claim 1, wherein said gate is at least partially recessed in said active region.

14. The transistor of claim 1, wherein said field plate reduces the peak operating electric field in said HEMT on the drain side of said gate and the source side of said gate.

15. The transistor of claim 14, wherein said reduction in peak operating electric field increases the breakdown voltage of said transistor.

16. The transistor of claim 14, wherein said reduction in peak operating electric field reduces trapping in said HEMT.

17. The transistor of claim 14, wherein said reduction in peak operating electric field reduces leakage currents in said transistor.

18. The transistor of claim 1, comprising a high electron mobility transistor (HEMT).

19. The transistor of claim 1, comprising a field effect transistor.

20. The transistor of claim 1, further comprising one or more spacer layers and field plate pairs, each spacer

layer in said pairs providing electric separation between its field plate and the field plate below, each field plate in said pairs electrically connected to said source electrode or said gate.

21. The transistor of claim 1, wherein said field plate comprises separate source and drain field plates said source field plate extending on said spacer layer toward said source electrode and said drain field plate extending on said spacer layer toward said drain electrode, said source and drain field plates electrically connected to said source electrode or said gate.

22. The transistor of claim 1, wherein said field plate comprises separate source and drain field plates said source field plate extending on said spacer layer toward said source electrode and said drain field plate extending on said spacer layer toward said drain electrode, said source field plate electrically connected to one of said source electrode and said gate, said drain field plate connected to the other of said source electrode and said gate.

23. A high electron mobility transistor (HEMT), comprising:

a buffer layer and barrier layer arranged successively on a substrate;

a two dimensional electron gas (2DEG) channel layer at the heterointerface between said buffer layer and said barrier layer;

a source and a drain electrode both making contact with said 2DEG;

a gate on said barrier layer between said source and drain electrodes;

a spacer layer on at least part of the surface of said barrier layer between said gate and said drain electrode and between said gate and said source electrode;

a field plate on said spacer layer and extending on said spacer over said barrier layer and toward said drain electrode, and extending on said spacer layer over said barrier layer and toward said source electrode; and

at least one conductive path electrically connecting said field plate to said source electrode or said gate.

24. A metal semiconductor field effect transistor (MESFET), comprising:

a buffer layer on a substrate;

a channel layer on said buffer layer with said buffer layer sandwiched between said channel layer and substrate;

a source electrode in electrical contact with said channel layer;

a drain electrode also in electrical contact with said channel layer;

a gate in electrical contact with said channel layer between said source and drain electrodes;

a spacer layer on at least part of the surface of said channel layer between said gate and said drain electrode and between said gate and said source electrode;

a field plate on said spacer layer and extending on said spacer over said channel layer and toward said drain electrode, and extending on said spacer layer over said channel layer and toward said source electrode; and

at least one conductive path electrically connecting said field plate to said source electrode or said gate.

FIG. 1

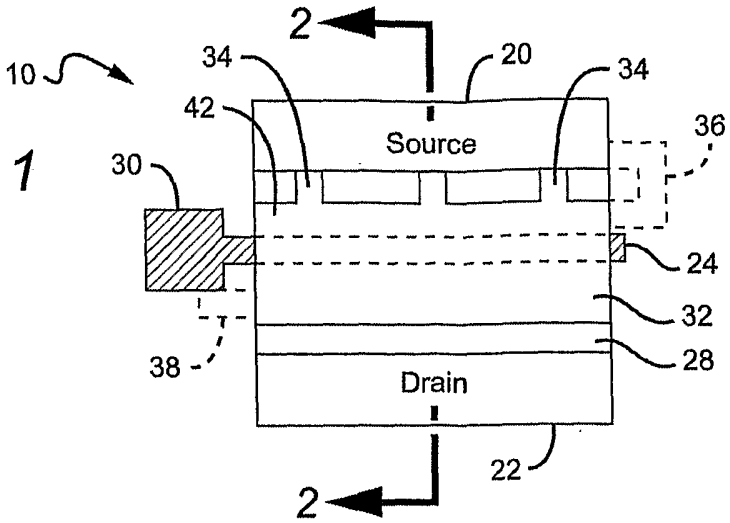


FIG. 2

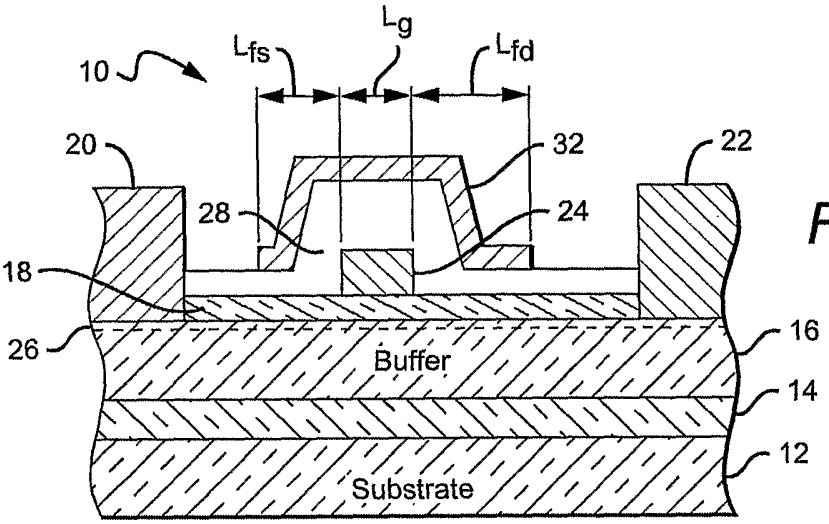
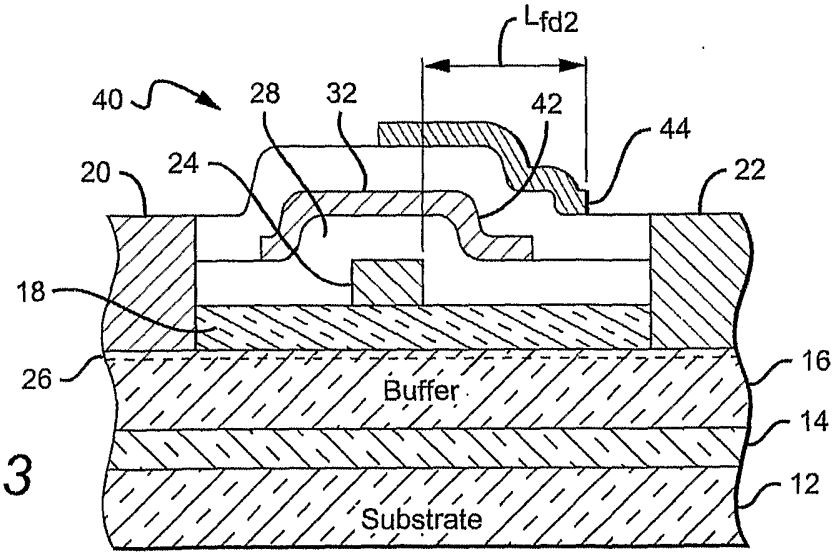


FIG. 3



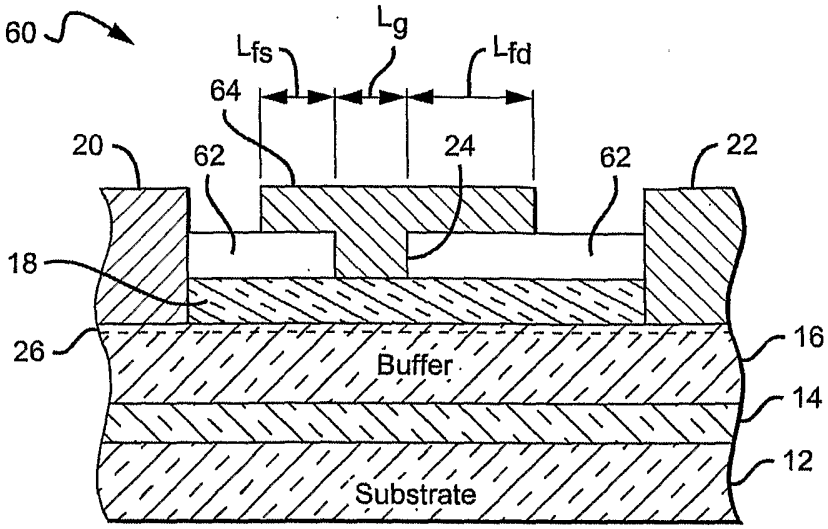

60
L_{fs}
L_g
L_{fd}
64
20
62
24
62
22
18
26
Buffer
16
14
12
Substrate

FIG. 4

FIG. 5

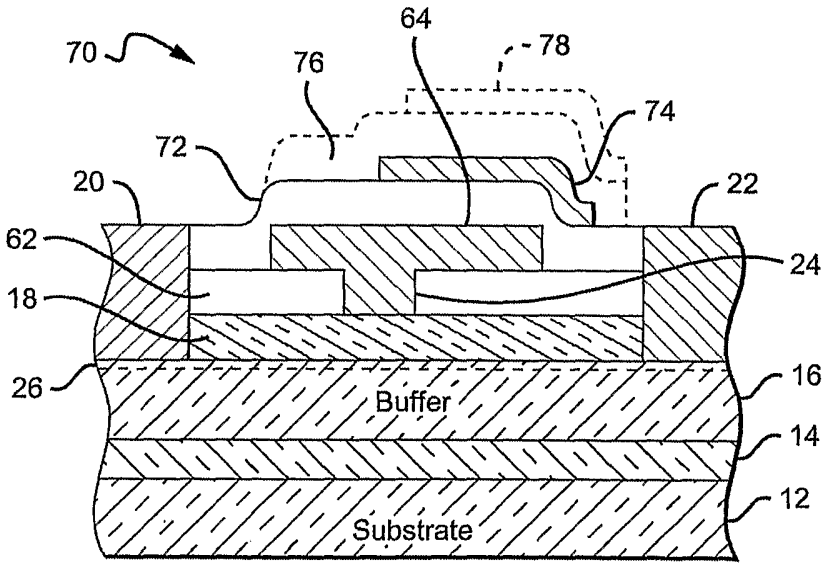

70
64
78
76
74
72
20
22
62
24
18
26
Buffer
16
14
12
Substrate

FIG. 6

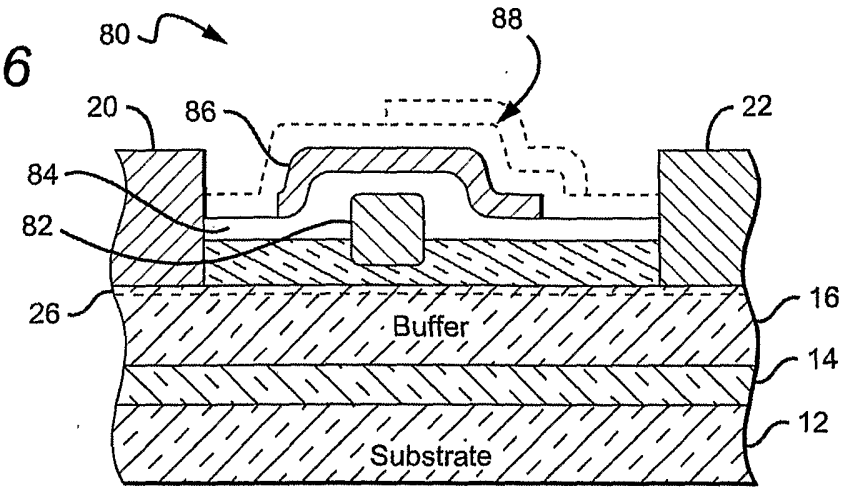


FIG. 7

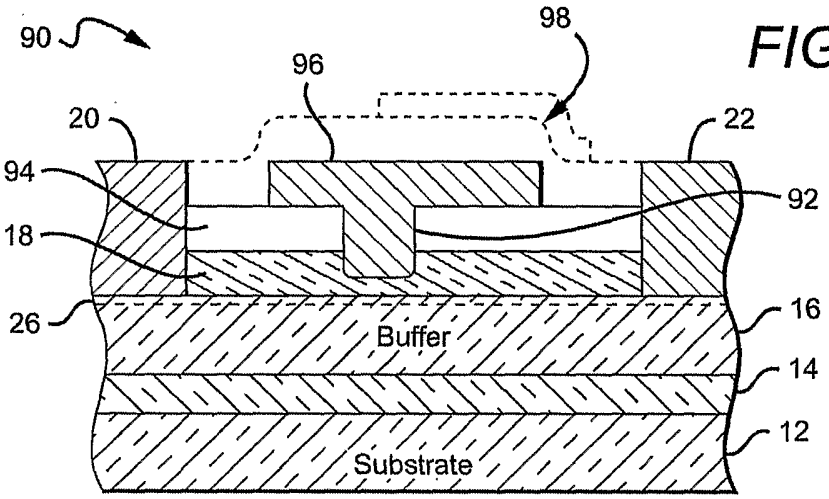


FIG. 8

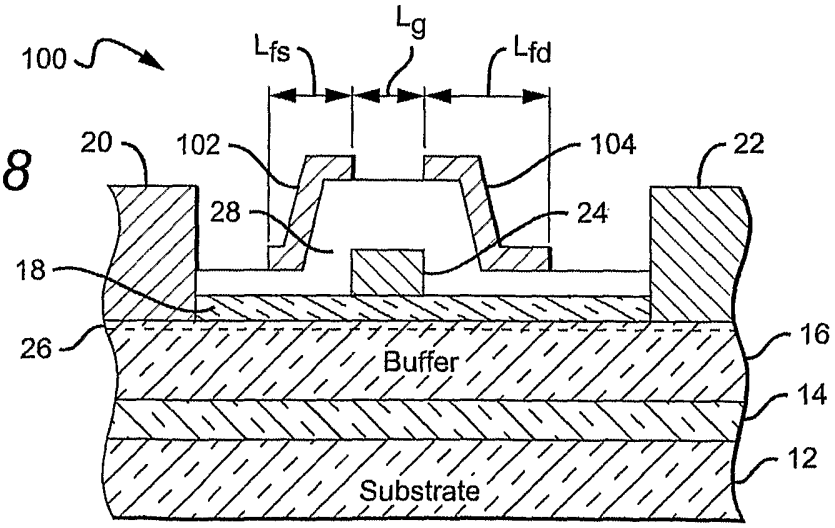
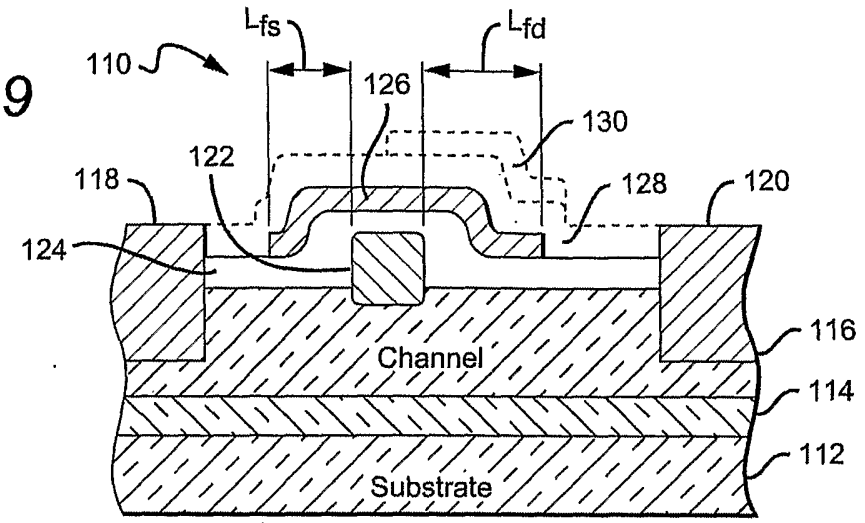


FIG. 9



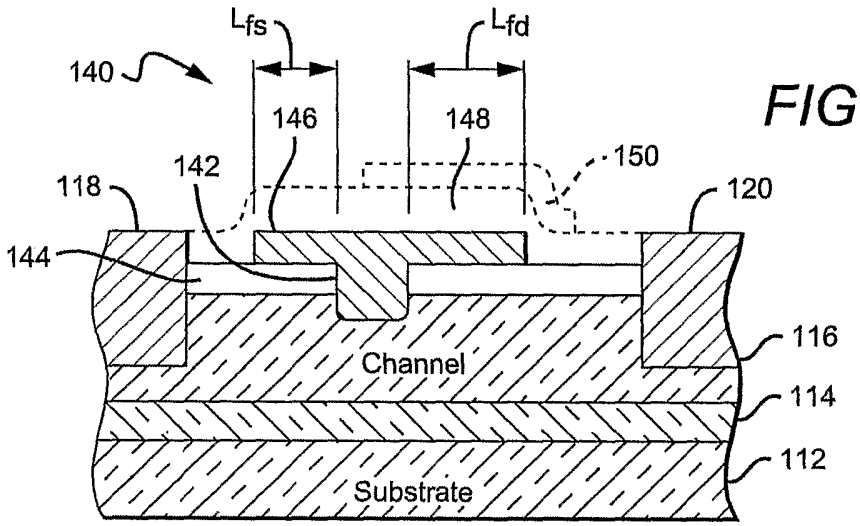


FIG. 10

130

FIG. 11

	I_d, max: before/after (mA/mm)	Pinch-off V_t: before/after (V)	I_g at -25V: before/after (mA/mm)	Output power: before/after (dBm)
Device A: no gate-source FP	1061 / Broke down	-3.62 / Broke down	0.148 / Broke down	30.36 / Broke down
Device B: with gate- source FP of 0.2 μm long	1056 / 1043	-3.55 / -3.41	0.114 / 0.370	30.50 / 30.40

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/001058

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/778 H01L29/812 H01L29/06
ADD. H01L29/24 H01L29/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	paragraphs [0031], [0043], [0049] - [0054]; claims 1,5,8; figures 5,7,10	7,20-22
Y	figure 11	20
X	SAITO W ET AL: "DESIGN AND DEMONSTRATION OF HIGH BREAKDOWN VOLTAGE GAN HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) USING FIELD PLATE STRUCTURE FOR POWER ELECTRONICS APPLICATIONS" JAPANESE JOURNAL OF APPLIED PHYSICS, JAPAN SOCIETY OF APPLIED PHYSICS, TOKYO, JP, vol. 43, no. 4B, April 2004 (2004-04), pages 2239-2242, XP001227744 ISSN: 0021-4922 the whole document	1-6,10, 12, 14-19,23

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 August 2006	23/08/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Dauw, X

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Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/001058

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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2

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/001058

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