



- (51) International Patent Classification:
H04L 7/02 (2006.01) *A61B 5/00* (2006.01)
- (21) International Application Number:
PCT/IB2012/055877
- (22) International Filing Date:
25 October 2012 (25.10.2012)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
61/552,627 28 October 2011 (28.10.2011) US
- (71) Applicant: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; High Tech Campus 5, NL-5656 AE Eindhoven (NL).
- (72) Inventors: **VAN RENS, Antonia, Cornelia**; c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL). **JOYE, Neil, Francis**; c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL). **MARCELIS, Bout**; c/o High Tech Campus Building 44, NL-5656 AE Eindhoven (NL).
- (74) Agents: **VAN VELZEN, Maaike, M.** et al.; High Tech Campus 44, NL-5600 AE Eindhoven (NL).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,

HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))

(54) Title: DATA COMMUNICATION WITH INTERVENTIONAL INSTRUMENTS

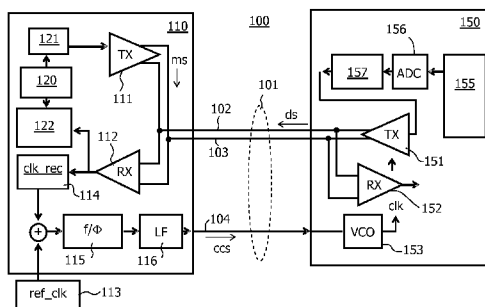


Fig. 3

(57) Abstract: The invention relates to a data communication system (100) and a method that can particularly be applied for communicating data from a medical instrument like a catheter or a guide-wire via a high-speedlink (101). The system (100) comprises (in-vivo) a slave component (150) with a controllable slave clock (153) and a transmitter (151) for transmitting a data signal (ds) that is clocked by the slave clock signal (clk). Moreover, it comprises (ex-vivo) a master component (110) with a clock controller (114,115,116) that receives a master clock signal (ref_clk) and the data signal (ds) and that generates a clock control signal (ccs) for adjusting the slave clock (153) to the master clock (113). The slave clock (153) may thus be realized with low space and energy requirements, e.g. by a voltage controlled oscillator (VCO). Moreover, the link (101) via which the data signal (ds) and the clock control signal (ccs) are exchanged may be realized by just two signal wires.



Data communication with interventional instruments

FIELD OF THE INVENTION

The invention relates to a data communication system and a method for communicating a data signal. Moreover, it relates to components of the data communication system, to a medical instrument, particularly a catheter or a guide-wire, and to a medical system.

BACKGROUND OF THE INVENTION

Instruments used in medical interventions like minimal invasive surgery are increasingly equipped with one or more sensors that transmit data from inside the body. A cardiovascular catheter has for example been described that comprises a pressure sensor, wherein an external clock signal is provided to this sensor to allow for a digital data communication (Jin Ji et al., "An Ultraminature CMOS Pressure sensor for a multiplexed cardiovascular catheter", IEEE transactions on electron devices, Vol. 39, No. 10, Oct 1992).

SUMMARY OF THE INVENTION

It is an object of the present invention to provide means that allow for a high-speed data communication, particularly a communication between an interventional instrument and external equipment, wherein the components inside the instrument shall preferably have low space and/or energy demands.

This object is achieved by a data communication system according to claim 1, a method according to claim 2, a slave component according to claim 11, a master component according to claim 12, a medical instrument according to claim 13, and a medical system according to claim 14. Preferred embodiments are disclosed in the dependent claims.

A data communication system according to the present invention serves for the communication or transfer of data from one communication partner to another. It comprises the following components:

a) A first component, called "slave component" (or briefly "slave") in the following to indicate that it is the subject of a higher level control of the communication system. The slave component shall comprise the following subcomponents:

a1) A clock for generating a clock signal, wherein these elements will in the following be called "slave clock" and "slave clock signal" for purposes of reference. The slave clock shall be controllable, which means that a characteristic parameter of the slave clock signal (typically its frequency) can be adjusted within given limits.

5 a2) A transmitter for transmitting a data signal that is clocked by the slave clock signal. This means that the data signal will "embed" at least a part of the slave clock signal and have a direct relation thereto (such that the clock signal can at least partially be retrieved from the data signal). This is preferably achieved with a digital data signal, in which the sequence of data bits may for example be synchronized with the slave clock signal.

10 Analog data signals are however possible, too, for example by use of amplitude modulation or multilevel signaling.

The data that are encoded in this data signal are assumed to be provided by another (logical) component than the slave component, for example by one or more sensors (which are functionally not a part of the communication system, though they may e.g. be realized on the same ASIC device).

b) A second component, called "master component" in the following, which comprises the following subcomponents:

b1) A receiver for receiving the above mentioned data signal.

20 b2) A clock for generating a clock signal, wherein these elements will in the following be called "master clock" and "master clock signal" for purposes of reference.

b3) A clock controller that receives the aforementioned master clock signal and the received data signal and that generates a "clock control signal" by which the slave clock can be adjusted to the master clock. This adjustment means that at least one characteristic parameter of the slave clock signal is altered to optimally match a given target parameter provided by the master clock signal. As a typical example, the frequency of the slave clock signal may be adjusted to the frequency of the master clock signal.

25 c) A link or communication channel via which the above mentioned data signal and the clock control signal can be exchanged between the slave component and the master component. Via this link, the transmitter of the slave component is hence coupled to the receiver of the master component, and the clock controller of the master component is coupled to the slave clock of the slave component.

30 According to a second aspect, the invention relates to a method for transmitting a data signal via a link from a slave component to a master component, said method comprising the following steps:

a) Clocking the data signal with a slave clock signal that is generated by a slave clock in the slave component.

b) Receiving said data signal in the master component.

5 c) Recovering at least partially the slave clock signal from the data signal.

c) Comparing the recovered slave clock signal with a master clock signal that is generated by a master clock in the master component, and generating a clock control signal that is associated to the result of this comparison.

10 d) Adjusting, based on the clock control signal, the slave clock in the slave component to the master clock.

The data communication system and the method are different realizations of the same inventive concept. Explanations and definitions provided for one of these realizations are therefore valid for the other realization, too.

15 In high-speed data communication (typically taking place with 100 Mbps or higher), there is a need to have accurate knowledge about the actual clock frequency. This can be done by using accurate clocks (e.g. crystal clocks on two sides), or there is a need to be able to track the non-accurate clock frequency. An important advantage of the proposed data communication system and method is that the data arrives at a frequency that is "prescribed" by the master (e.g. an important system clock frequency), without the need to
20 have an accurate clock at the slave side (the side which is restricted in space and power). Accordingly, the slave clock can be realized with small components having a low power consumption.

In the following, various preferred embodiments of the invention will be described that relate to the data communication system and the method described above.

25 According to a first preferred embodiment, the slave clock comprises or completely consists of a voltage controlled oscillator (VCO) or current controlled oscillator (CCO). A VCO and a CCO are components known to persons skilled in the art that allow for an adjustment of their output frequency by an external control voltage or current, respectively.

30 In general, the link between the slave component and the master component may be any kind of communication channel that can carry the data signal and the clock control signal. If the data signal and/or the clock control signal are for example realized by wireless (RF) signals or optical signals, the link may simply be a medium in which these

signals can propagate. If the data signal and the clock control signal are realized by different modalities, the link will comprise carriers for both of them.

In a preferred embodiment, the link comprises (at least) two signal wires via which electrical signals can be changed between the slave component and the master component. In this case the data signal and/or the clock control signal can for example be represented by voltages or currents applied to said signal wires. Most preferably, the link consists of just two signal wires that can carry the data signal and/or the clock control signal. Realizing the link by just two signal wires minimizes the space requirements while simultaneously guaranteeing a reliable connection.

The master component may optionally comprise a transmitter for transmitting a (preferably digital) signal via the link, said signal being called "master signal" in the following. Additional data and/or control commands (besides the clock control signal) can be communicated from the master component to the slave component by this master signal, wherein this communication advantageously uses the available link.

The slave component preferably comprises a receiver for receiving an "additional signal" (besides the clock control signal) via the link. This additional signal may particularly be the master signal of the aforementioned embodiment that is generated by the master component.

According to a preferred embodiment of the invention, the data signal, the clock control signal, the master signal, and/or the additional signal is represented by the difference in a voltage and/or a current between two signal wires of the link (for example as the difference $(V1-V2)$ if $V1$ and $V2$ are the voltages on said two signal wires). The sign (polarity) of this difference may then for example represent the "0" and "1" bits of the respective signal.

According to another embodiment, the data signal is represented by the variation of a load that is coupled in the slave component to two signal wires of the link. This load variation can then be sensed by a receiver in the master component.

The clock control signal, the additional signal, and/or the master signal is preferably represented by a common mode voltage and/or current on two signal wires of the link (for example as the value $(V1+V2)/2$ if $V1$, $V2$ are the voltages on said two signal wires). This representation can favorably be combined with the above mentioned embodiment in which the data signal is represented by the difference between a voltage and/or a current because it allows that the same two signal wires are used for the communication of the data signal and the clock control signal (and/or master signal,

additional signal). The representation of these signals could (theoretically) also be reverse (i.e. the data signal could be common mode and the clock control signal differential). Representation of the data signal as a difference is however preferred because this typically requires a higher transmission rate.

5 According to another embodiment of the invention, the master signal (or the "additional signal") overrides the data signal. For example, if both the data signal and the master signal are represented as a difference between currents or voltages on two signal wires of the link, the difference imposed by the master signal may be so large that its sign (polarity) is not changed by the simultaneous data signal. Accordingly, information encoded in said
10 sign (polarity) of the master signal can be retrieved irrespective of the data signal.

 The master component and the slave component are two compatible parts of the data communication system that are specifically designed with respect to each other. An essential part of the invention is realized in each of these components, which are commercial commodities of their own. Accordingly, the invention also relates to a slave component as an
15 element of its own, said slave component comprising:

- A controllable slave clock for generating a slave clock signal, wherein said clock can be adjusted by a clock control signal.
- A transmitter for transmitting a data signal that is clocked by the slave clock signal.

20 Similarly, the invention relates to a master component as an element of its own, said master component comprising:

- A receiver for receiving a data signal from the aforementioned slave component.
- A master clock for generating a master clock signal.
- 25 - A clock controller that receives the master clock signal and the data signal and that generates a clock control signal which can adjust the slave clock of the aforementioned slave component to the master clock.

 The invention further relates to a medical instrument, particularly an interventional instrument like a catheter or a guide-wire, said instrument comprising a slave
30 component of the kind described above. An advantage of this medical instrument is that it can be miniaturized due to the low space requirements of the slave component while it allows at the same time for a high-speed data transmission to external equipment.

 Finally, the invention relates to a medical system that comprises the aforementioned instrument and external equipment with a master component, wherein the

slave component of the instrument and said master component are compatible (i.e. form a data communication system according to the invention) and are coupled via a link, for example a cable.

5 BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 illustrates a data communication with reference clocks in both the slave
10 and the master;

Fig. 2 illustrates a data communication in which a clock signal of a master clock is transmitted to a slave;

Fig. 3 illustrates schematically a communication system according to the present invention;

Fig. 4 schematically illustrates a particular embodiment of the data
15 communication system in which data signals are represented by current differences;

Fig. 5 schematically illustrates a particular embodiment of the data communication system in which data signals are represented by load variations;

Fig. 6 shows exemplary courses of the voltage and current on the link of the
20 data communication system of Figure 5.

Like reference numbers or numbers differing by integer multiples of 100 refer in the Figures to identical or similar components.

DETAILED DESCRIPTION OF EMBODIMENTS

25 Diagnosis and treatment in minimally invasive healthcare procedures may be improved by integrating imaging and sensing devices at the tip of interventional instruments - such as catheters and guide-wires. However, the very limited size of these instruments poses an important challenge in integrating the required functionality. Micro-machining (MEMS) sensors can be integrated with ASIC technology and enable advanced imaging and/or sensing
30 functionality in a very small area. The related trend is that an increasing amount of data needs to be transferred from the tip of the instrument to the external equipment.

Communication between the devices at the tip of an instrument (in-vivo) and the external equipment (ex-vivo) requires a link that is capable of transferring data in an effective way. In this context "effective" refers to: causing little in-vivo power dissipation,

requiring simple and small in-vivo functionality, and requiring a low number of signal wires to connect the in-vivo and the ex-vivo functionality.

A low wire-count is important due to the limited space available to route the wires. The lumen of a guide-wire typically is 250 μm while the diameter of a catheter is 1-5 mm (with a trend towards smaller catheters). This also restricts the available area for in-vivo functionality. The in-vivo power dissipation is important because of safety regulations on heating human tissue.

Realization of a robust (bi-directional) high speed serial link between two cable ends typically requires:

- One or two transmitter(s) that send data at a defined speed.
- One or two receivers(s) that receive data at the intended speed.
- Two signal wires that allow transferring high speed signals in a differential way.
- One or two reference clock devices.

Figure 1 shows schematically a data communication with two clock devices, one device (ref_clk_1) being located at the master site and one device (ref_clk_2) being located at the slave site. Typically, there are strict requirements on clock jitter and clock frequency matching in this case.

Figure 2 shows schematically a data communication in which there is only one reference clock (ref_clk_1) at the master site. As this clock is not located near the (active) transmitter of the slave, extra circuitry (e.g. receiver circuitry and PLL) and extra wire(s) are needed to transfer the clock signal from the master to the slave site of the link.

In case of catheter or guide-wire applications, most of the high-speed dataflow is from the devices at the tip (slave, "in-vivo") to external equipment (master, "ex-vivo").

Transmitting high-speed (HS) data from slave to master at the required speed typically requires an accurate reference clock (e.g. a crystal oscillator) at the slave or transport of an accurate clock signal via one or two wires towards the slave. Due to the limited area available, it is not attractive to implement a crystal in-vivo in order to generate a reference clock signal (Figure 1). For the same reason, the transport of an accurate clock signal (Figure 2) is not attractive due to the need of additional wire(s), hardware and power dissipation.

The present invention proposes a solution that is capable of sending data from slave to master at a defined speed without the need of such accurate clock reference at the slave. The solution requires only two signal wires and the functional partitioning is such that

most functionality and power dissipation is "ex-vivo". Full control of the link remains "ex-vivo".

Figure 3 shows a block diagram of a data communication system 100 according to an embodiment of the present invention. The system 100 comprises three main components, namely:

- A "slave component" 150 on the "in-vivo" side that delivers most data, but contains simple data link functionality and consumes little power.
- A "master component" 110 on the "ex-vivo" side that has full control over the link, contains more complex functionality, and consumes more power.
- A link 101 connecting them, for example a cable or other type of inter-connect.

The slave component 150 may for example be integrated into a smart guide-wire or a catheter that is equipped with sensors, actuators and/or imaging devices at the tip, which are schematically represented by a box 155. The gathered (analogue) signals will be converted into digital data e.g. by means of a sigma-delta ADC 156. The data is encoded in an encoder 157 and sent by a transmitter 151 as a "data signal" ds over the link 101 to the ex-vivo world.

The cable 101 preferably comprises two signal wires 102 and 103 (a third connection 104 is only shown to illustrate the separate signal flow). As will be explained in more detail below, these signal wires 102 and 103 transfer the high-speed data signal ds (via differential signaling), a VCO clock control signal ccs (via common-mode signaling), and additional control and/or low-speed data (via differential or common-mode signaling). Besides the two signal wires (or "functional wires"), the cable 101 may in practice additionally comprise extra connections (not shown) for power supply (VDD, GND), yielding a total of four wires (in case of a full electrical link). If a battery would be supplied to the slave component 150, it might be possible to limit the total number of wires to two.

The in-vivo slave component 150 contains a "slave clock", here realized by a voltage controlled oscillator (VCO) 153 that delivers a "slave clock signal" clk to the local high-speed transmitter 151 and receiver 152. The speed depends on the application but the effective data rate could be hundreds of Mbit/s. The high-speed transmitter 151 can be an active transmitter (Figure 4) or a load modulating device (Figure 5). As the latter one will give less in-vivo dissipation, it might be preferred. The in-vivo receiver 152 must be capable of determining the polarity of the differential input signal. The speed of the receiver depends on the application, but will be moderate in most cases.

The ex-vivo master component 110 comprises a high-speed receiver 112 for receiving the data signal ds sent by the in-vivo slave component 150. Moreover, the master component 110 is the master of the communication. It controls the slave data rate and the mode of operation of both master and slave. To be able to control the HS-data rate, the master component 110 comprises a "clock controller" with the following components:

- means 114 to do clock recovery,
- a frequency- and/or phase-detector 115 to compare the frequency of the recovered slave clock signal and the reference clock frequency of a master clock signal ref_clk provided by a master clock 113,
- a loop-filter 116.

The master component 110 also contains means 122 to do data recovery and data decoding. Data recovery is possible by means of oversampling techniques or by means of an (extra) PLL that locks on the incoming data.

Furthermore, the master component 110 contains a control unit 120 that is capable of sending low speed data (storage 121) or control bits as a "master signal" ms via a transmitter 111 to the slave 150. Said transmitter 111 may also provide energy (a fixed current) to the in-vivo transmitter 151 in case of a passive in-vivo HS-transmitter.

The VCO 153 may be realized in an ASIC at the tip of the corresponding instrument (e.g. guide-wire or catheter). This non-accurate clock source generates a clock signal clk , using only a low amount of power and requiring a limited amount of space. As described above, this signal clocks the local transmitter 151 and receiver 152. The in-vivo transmitter 151 sends encoded HS-data as a data signal ds across the link 101, wherein the encoding is such that the clock frequency can be retrieved from this transmitted signal. The ex-vivo master component 110 receives the data signal ds , performs the clock recovery, after which the clock frequency is compared with a reference clock frequency ref_clk . By means of a negative feedback loop, the frequency of the VCO is regulated to fit the reference clock frequency.

Furthermore, it is possible to combine the HS-data ds and the VCO clock control signal ccs (and optionally also a master signal ms provided by the in-vivo transmitter 111) across the same two signal wires 102 and 103: HS-data ds can be driven differentially, using a small signal swing. The VCO clock control voltage ccs is transferred via the common-mode (CM) voltage level of the signal wires. This approach will be explained in more detail below with reference to Figures 4 and 5.

Figure 4 shows a block diagram of a communication system 200 with a master component 210 and a slave component 250 that are generally designed as shown in Figure 3. Particular components of this system are shown in more detail to illustrate a possible implementation of a two signal wire interface (as explained above, there are typically extra wires for power supply that will not be considered in the following).

Due to the typical length of the cable wiring of the link 201 (± 2 m) and the typical speed of the data-link ($\gg 10$ MHz), the cable behaves as a transmission line. Therefore, the characteristic impedance (Z_0) of the cable is important and matched termination resistors R1, R2, R3, R4 on termination and/or transmission side need to be placed to minimize undesirable reflections.

During high-speed transmission, the in-vivo high speed transmitter 251 transmits gathered data (D1). The HS-signal ds uses differential signaling to minimize electromagnetic radiation (EMI) and susceptibility (EMS). The shown implementation of the transmitter 251 runs at a fixed bias current (I1a and I1b), which minimizes disturbance of the local supply voltage. A data bit D1 = "1" may for example be encoded by connecting a first current source I1a to a first signal wire 202 and a second current source I1b to the other signal wire 203, while a data bit D1 = "0" is encoded by connecting the first current source I1a to the second signal wire 203 and the second current source I1b to the first signal wire 202. During high-speed transmission mode, the ex-vivo low-speed transmitter 211 maybe turned off.

The loop filter 216 in the master component 210 is a part of the negative feedback loop that will regulate the frequency of the VCO 253 in the slave 250 to the required value. In the shown implementation, the loop-filter output delivers a regulated current I2, which is translated (by a resistor R5) into a common mode (CM) voltage in the close vicinity of the VCO 253.

The ex-vivo master component 210 is capable of overruling the HS-data-stream ds by activating its transmitter 211 and driving low-speed (or medium speed) data D2 or control data as a "master signal" ms across the link 201. By choosing the ex-vivo bias currents (I3a and I3b) larger than the in-vivo currents (I1a and I1b), the in-vivo receiver (not shown) can detect the ex-vivo data signal ms by sensing the polarity of the differential signal. During low speed data-transmit mode of the master signal ms, the in-vivo HS-transmitter 251 preferably remains active. This allows the frequency control loop to remain active and to keep lock between the reference clock and the in-vivo clock.

Figure 5 shows a block diagram of a communication system 300 with a master component 310 and a slave component 350 that are generally designed as shown in Figure 3. Particular components of this system are shown in more detail to illustrate an alternative implementation of the high-speed transmitter.

5 In this version, the in-vivo HS-transmitter 351 has been implemented as a load modulating device. During HS-transmit of a data signal d_s , the ex-vivo LS-transmitter 311 delivers a fixed differential current. Resistors R1 and R2 in the master component 210 provide a matched termination at the ex-vivo side. The termination at the in-vivo site comprises the resistors R3 and R4, to which the resistors R6 and R7 can optionally be
10 coupled in parallel by the HS-transmitter 351. Thus the termination can be switched between a value larger than the characteristic impedance (e.g. $5 \cdot Z_0$) and a value lower than the characteristic impedance (e.g. $0.5 \cdot Z_0$). This switching, which represents the HS-data D1, will cause reflections (constituting the data signal d_s). As the reflections are the only HS-information happening on the link 301, they can be detected rather easily.

15 The ex-vivo transmitter 311 can send data D2 as a master signal m_s across the link 301 by toggling the polarity of the (fixed) current of the low-speed transmitter 351. The low-speed data m_s can be sensed by the in-vivo receiver (not shown) by sensing the polarity of the differential signal.

The data bit ("1" or "0") can be encoded in the master signal m_s in many ways, for example by varying the duration of the inverse polarity pulse. Figure 6 shows an example of such pulse width modulation, wherein the upper curve represents the current I flowing in a signal wire 302 of the link and the lower diagram shows the voltage between the signal wires 302 and 303 of the link. In this example, the HS-transmitter 351 sends a fixed clock (no data contents) at a clock rate of 200 Mbit/s. The low-speed data rate is a factor of 12 lower.
20 The long pulses can be distinguished from the short pulses by clocking the (polarity of the) voltage signal with the in-vivo clock 353. The duration of the inverse polarity pulses ($I = -5 \text{ mA}$) determines the value of the transmitted data bits. Accordingly, the shown low speed master signal is a (010101) sequence.

It should be noted that the HS-data encoding in the data signal d_s is an
30 important aspect of the proposed systems. The data encoding must allow clock recovery under all conditions. Clock recovery is required to be able to regulate the HS-data rate. Clock recovery is possible by counting the number of transitions in the HS-data signal (frequency detection) or by comparing the position of the HS-data transitions and the reference clock transitions (phase comparison) or by a mix of these two methods. At start-up, frequency

detection works best as it cannot cause false locks while phase detection can. The disadvantage of frequency detection is that it requires a fixed/known amount of transitions in the HS-data signal; this can be arranged in the encoding of the data or can be guaranteed by sending a fixed/known data pattern at the start of a data sequence.

5 Furthermore, HS-data encoding is important as the in-vivo clock signal may suffer from jitter due to electrical disturbances on the VCO control signal. By choosing a type of data encoding with a strong clock frequency component, the data recovery will suffer less from this jitter.

10 A basic data encoding could be the well known Manchester coding (i.e. "0" and "1" are expressed by a transition between low and high at the midpoint of a fixed period). The efficiency of the Manchester coding is rather low (many transitions, high bandwidth needed for data transfer). Furthermore, Manchester does not foresee a word-sync or frame-sync, this probably needs to be added on top the Manchester coding. 8bit-to-10bit encoding could therefore be an alternative (cf. US4486739).

15 In summary, an electrical high speed serial link was described that is capable of transferring data from devices at the tip of an interventional instrument (in-vivo) to the external equipment (ex-vivo) in a power efficient and area effective way. The ability to transfer the high-speed data from the tip at a defined speed is achieved without the need of an accurate in-vivo clock reference source. Only two signal wires are required, and the
20 functional partitioning is such that most of the functionality and power dissipation is ex-vivo. Full control of the link remains ex-vivo. All these aspects allow for large amounts of data being transferred in a highly miniaturized solution.

25 The system according to the invention avoids the need of an accurate reference clock signal at the slave side. Instead, a control signal is needed. An important aspect in this respect is that it is easier to transfer a low-frequency control signal (potentially via multiplexing) than a high speed clock signal (especially in a catheter or guide-wire). High speed signals are difficult to multiplex and often require multiple signal wires if done in the electrical domain (coax like cable or twisted pair etc). The same holds for receiving the signals; it is easier to receive a low-frequency control signal than a high speed clock signal.

30 Accordingly, the approach of the invention implies the use of one high-speed data signal and one low frequency control signal. In general, the high-speed data signal could be transferred via (two) electrical signal wires, via a single optical wire, or wirelessly. The control signal could be transferred in multiple ways, but due to the low-frequency contents of this signal it is not attractive to do it wirelessly or optically (assumed that the system will

contain electrical signals). If there are no electrical wires (e.g. for MRI compatibility reasons), of course also the control signal needs to be transferred optically or wirelessly.

The proposed solution is especially useful in communication links with minimally invasive instrumentation that require high-speed data transport, e.g. ultrasound
5 imaging from a catheter or guide-wire, such as intravascular ultrasound (IVUS), intra-cardiac echography (ICE), forward-looking IVUS/ICE, ultrasound-based ablation monitoring, but also all types of in-body sensors (flow, pressure, temperature) etc.

In-body sensors do not really require a high-speed link. Speeds of sensors are limited to e.g. 1 MHz. while all kind of imaging easily requires hundreds of Mb/s.

10 While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the

15 disclosure, and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS:

1. A data communication system (100-300), comprising:
 - a) a slave component (150-350) with
 - a1) a controllable slave clock (153-353) for generating a slave clock signal (clk),
 - 5 a2) and a transmitter (151-351) for transmitting a data signal (ds) that is clocked by the slave clock signal (clk);
 - b) a master component (110-310) with
 - b1) a receiver (112) for receiving said data signal (ds),
 - b2) a master clock (113) for generating a master clock signal (ref_clk),
 - 10 b3) and a clock controller (114, 115, 116-316) that receives the master clock signal (ref_clk) and the data signal (ds) and that generates a clock control signal (ccs) for adjusting the slave clock (153-353) to the master clock (113);
 - c) a link (101-301) via which the data signal (ds) and the clock control signal (ccs) can be exchanged.
- 15 2. A method for transmitting a data signal (ds) via a link (101-301) from a slave component (150-350) to a master component (110-310), said method comprising the following steps:
 - a) clocking the data signal (ds) with a slave clock signal (clk) that is generated
 - 20 by a slave clock (153-353) in the slave component (150-350);
 - b) receiving the data signal (ds) in the master component (110-310);
 - c) recovering at least partially the slave clock signal (clk) from the data signal (ds);
 - d) comparing the recovered slave clock signal (clk) with a master clock
 - 25 signal (ref_clk) generated by a master clock (113) in the master component (110-310), and generating an associated clock control signal (ccs);
 - e) adjusting the slave clock (153-353) by the clock control signal (ccs) to the master clock (113).

3. The system (100-300) according to claim 1, characterized in that the slave clock comprises a voltage or current controlled oscillator (153-353).

4. The system (100-300) according to claim 1, characterized in that the link (101-301) comprises or preferably consists of two signal wires (102-302, 103-303).

5. The system (100-300) according to claim 1, characterized in that the master component (110-310) comprises a transmitter (151-351) for transmitting a master signal (ms) via the link (101-301).

6. The system (100-300) according to claim 1, characterized in that the slave component (150-350) comprises a receiver (152) for receiving an additional signal (ms) from the link (101-301).

7. The system (100-300) according to claim 1, 5, or 6, characterized in that the data signal (ds), the clock control signal (ccs), the master signal (ms), and/or the additional signal is represented by a difference of a voltage and/or a current between two signal wires (102-302, 103-303) of the link (101-301).

8. The system (100, 300) according to claim 1, characterized in that the data signal (ds) is represented by the variation of a load (R3, R3, R6, R7) coupled in the slave component (150, 350) to two signal wires (102, 302, 103, 303) of the link.

9. The system (100-300) according to claim 1 or 5, characterized in that the data signal (ds), the clock control signal (ccs), and/or the master signal (ms) is represented by a common mode voltage and/or current on two signal wires (102-302, 103-303) of the link (101-301).

10. The system (100-300) according to claim 5, characterized in that the master signal (ms) overrides the data signal (ds).

11. A slave component (150-350) for a data communication system (100-300) according to claim 1, comprising a slave component (150-350) with:

a1) a controllable slave clock (153-353) for generating a slave clock

signal (clk),

a2) a transmitter (151-351) for transmitting a data signal (ds) that is clocked by the slave clock signal (clk).

5 12. A master component (110-310) of a data communication system (100-300) according to claim 1, comprising a master component (110-310) with:

b1) a receiver (112) for receiving a data signal (ds),

b2) a master clock (113) for generating a master clock signal (ref_clk),

b3) a clock controller (114, 115, 116-316) that receives the master clock
10 signal (ref_clk) and the data signal (ds) and that generates a clock control signal (ccs) for adjusting a controllable clock (153-353) to the master clock (113).

13. A medical instrument, particularly a catheter or a guide-wire, comprising a slave component (150-350) with:

15 a1) a controllable slave clock (153-353) for generating a slave clock signal (clk),

a2) a transmitter (151-351) for transmitting a data signal (ds) that is clocked by the slave clock signal (clk).

20 14. A medical system, comprising:

a) a medical instrument including a slave component (150-350) with

a1) a controllable slave clock (153-353) for generating a slave clock
signal (clk),

a2) and a transmitter (151-351) for transmitting a data signal (ds) that is
25 clocked by the slave clock signal (clk);

b) external equipment including a master component (110-310) with

b1) a receiver (112) for receiving said data signal (ds),

b2) a master clock (113) for generating a master clock signal (ref_clk),

b3) and a clock controller (114, 115, 116-316) that receives the master
30 clock signal (ref_clk) and the data signal (ds) and that generates a clock control signal (ccs) for adjusting the slave clock (153-353) to the master clock (113);

c) a link (101-301) via which the data signal (ds) and the clock control
signal (ccs) can be exchanged.

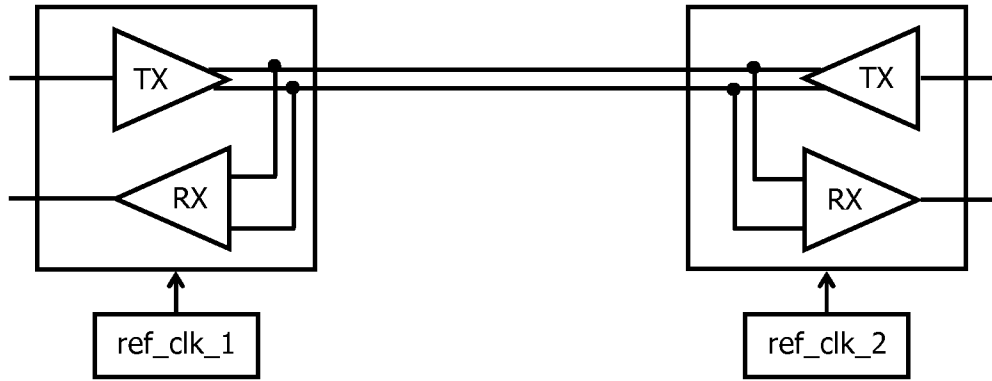


Fig. 1

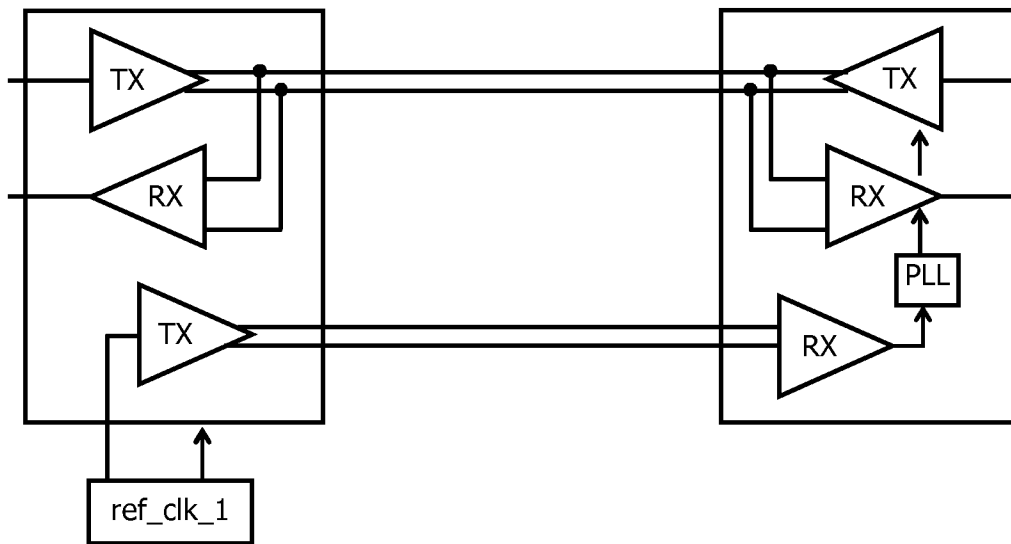


Fig. 2

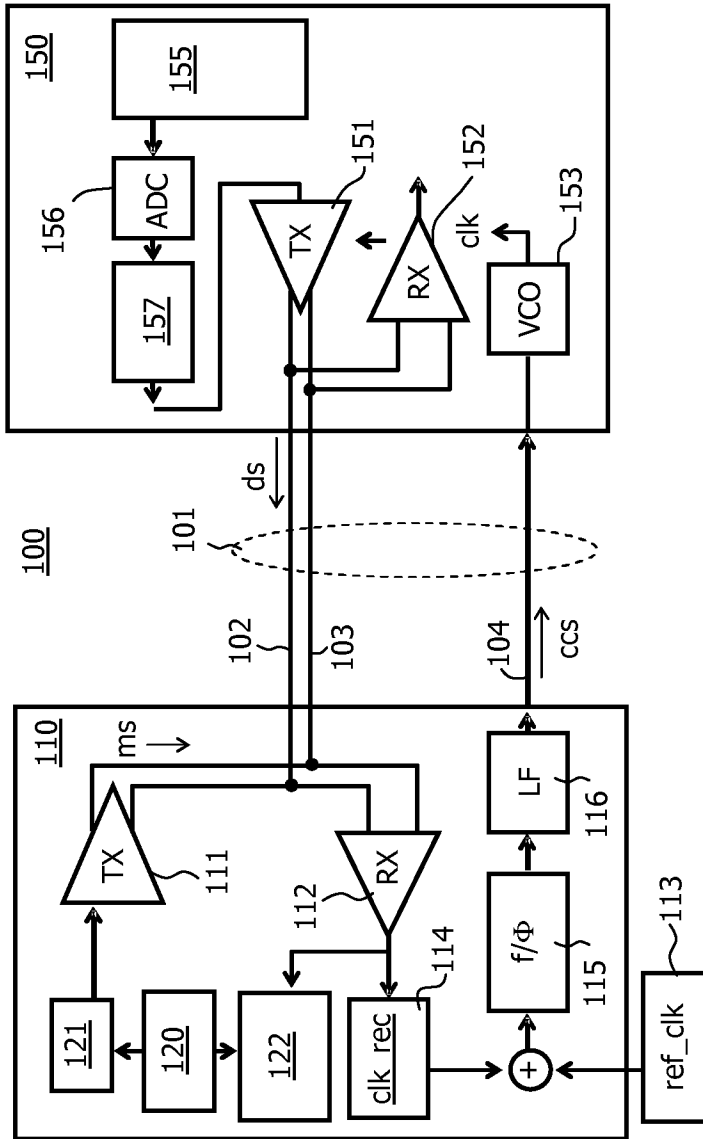


Fig. 3

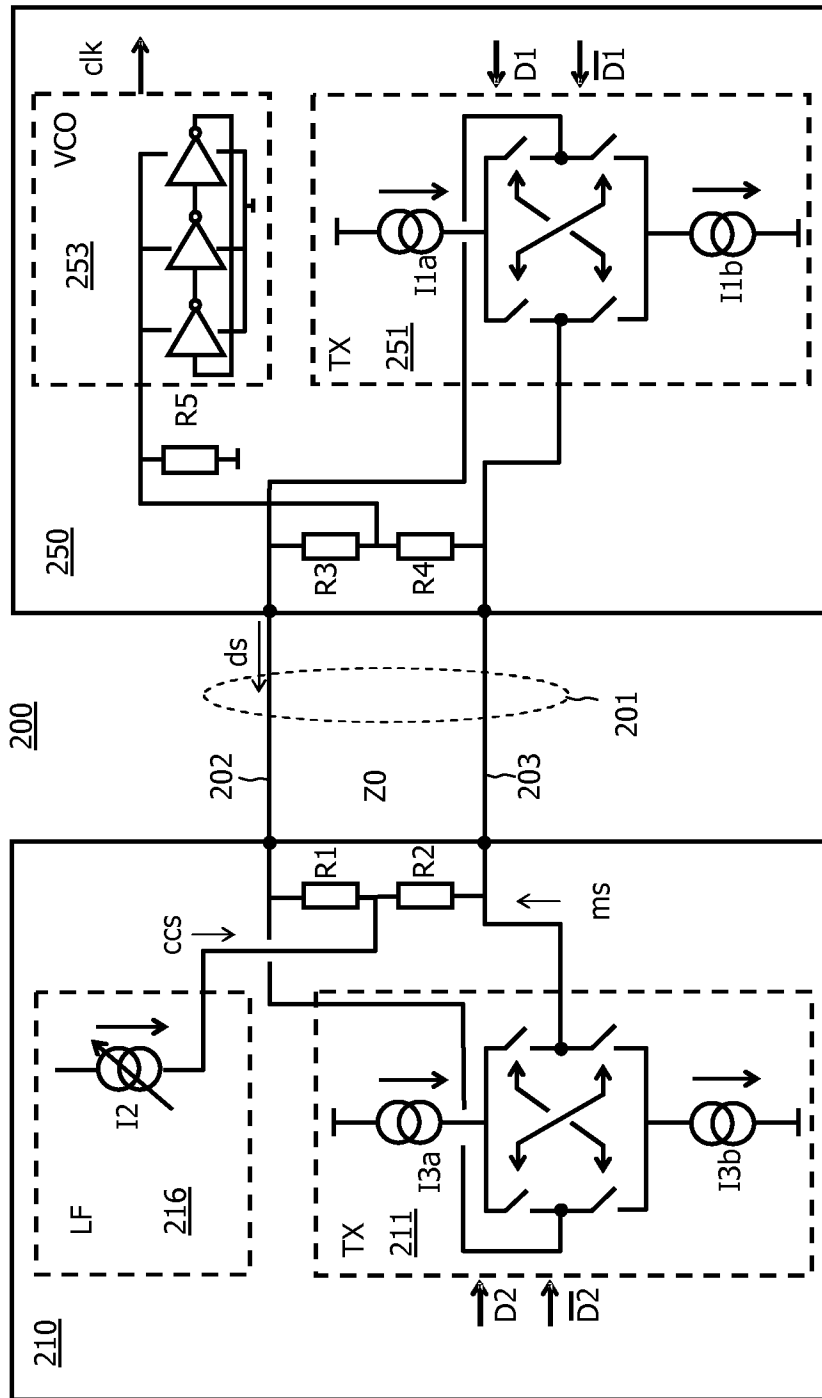


Fig. 4

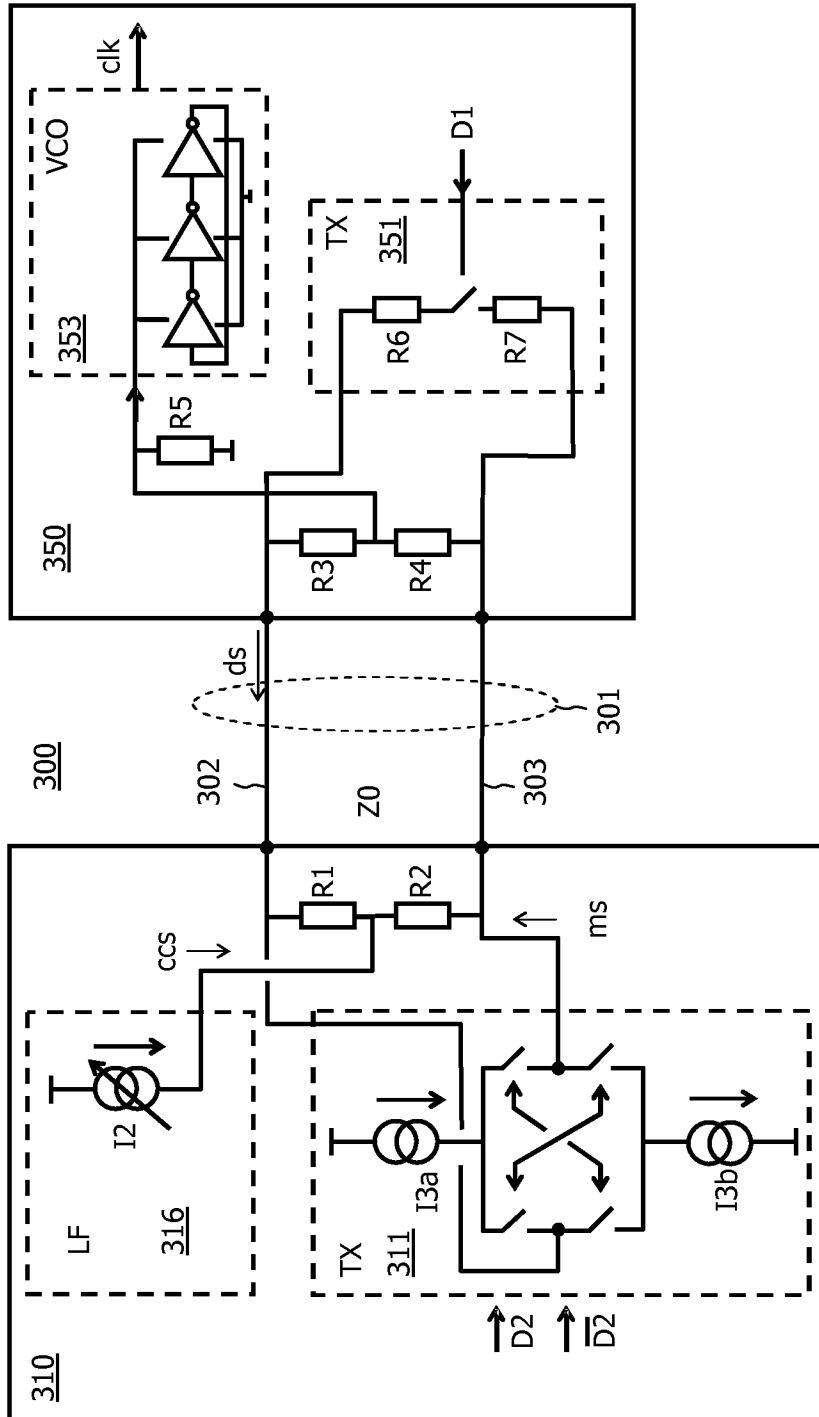


Fig. 5

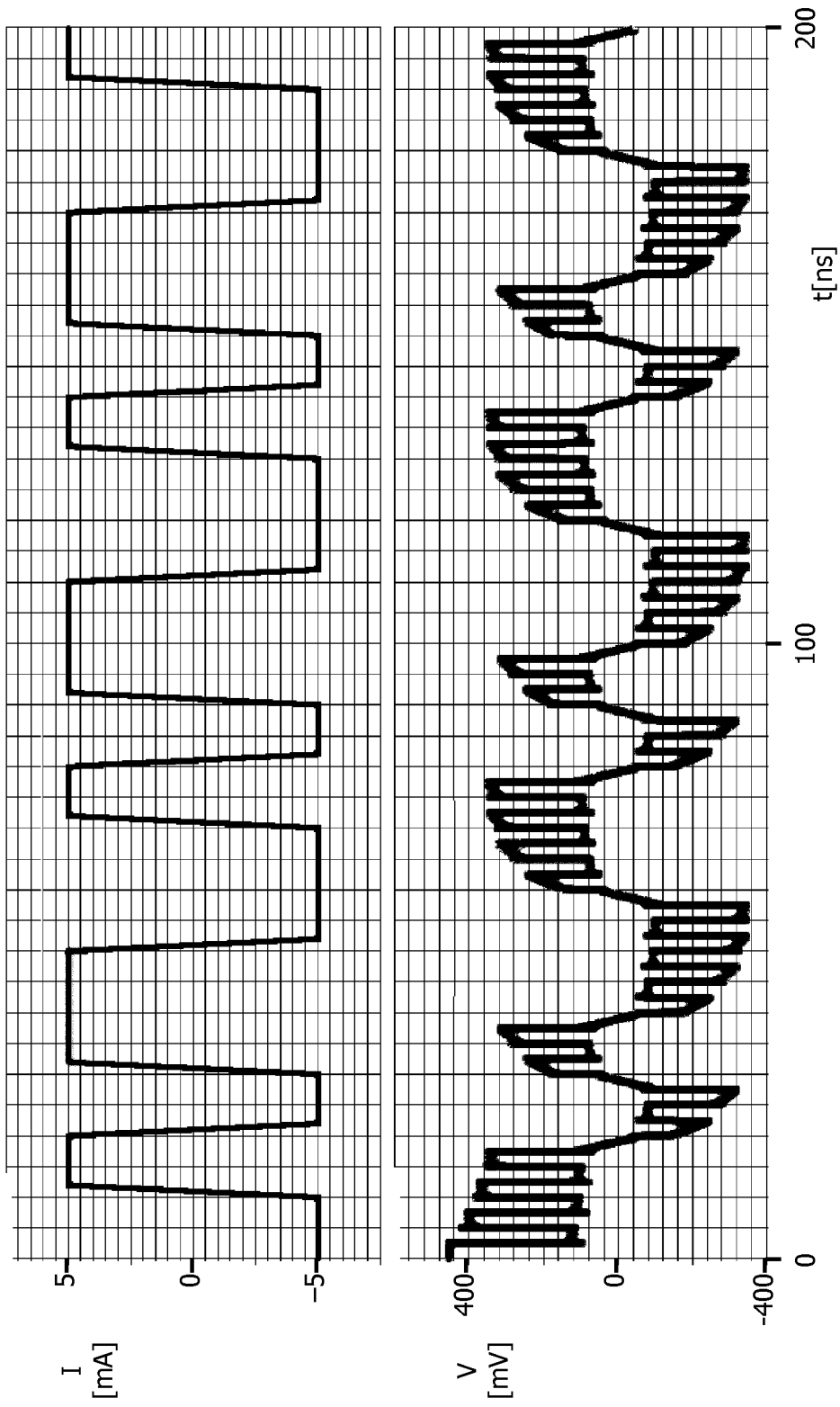


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/055877

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04L7/02 A61B5/00
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
H04L A61B G06F G01D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/015304 A1 (YIN JOHN [US] ET AL) 15 January 2009 (2009-01-15) paragraph [0001] - paragraph [0002] paragraph [0010] - paragraph [0012] paragraph [0034] paragraph [0038] figures 6-9	1-14
X	WO 2010/097111 A1 (ERICSSON TELEFON AB L M [SE]; HODGE ROBERT [GB]; RUFFINI STEFANO [IT]) 2 September 2010 (2010-09-02) page 3, line 1 - page 4, line 7 page 9, line 10 - line 22 page 12, line 8 - line 10 ----- -/--	1-14

Further documents are listed in the continuation of Box C.

See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 27 February 2013	Date of mailing of the international search report 06/03/2013
--	---

Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Marongiu, M
--	--

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/055877

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 2 158 841 A2 (BIOSENSE WEBSTER INC [US]) 3 March 2010 (2010-03-03) paragraph [0001] - paragraph [0002] paragraph [0016] - paragraph [0020] paragraph [0023] - paragraph [0025] figures 1,2 -----	1-14
A	EP 0 889 616 A1 (SIEMENS MEDICAL SYSTEMS INC [US] SIEMENS MEDICAL SOLUTIONS [US]) 7 January 1999 (1999-01-07) column 1, line 3 - line 21 column 7, line 9 - line 26 column 11, line 32 - line 38 figures 1,2 -----	1-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No PCT/IB2012/055877

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009015304	A1	15-01-2009	US 2009015304 A1 15-01-2009
			US 2011099408 A1 28-04-2011
			US 2011099410 A1 28-04-2011

WO 2010097111	A1	02-09-2010	EP 2401827 A1 04-01-2012
			JP 2012518924 A 16-08-2012
			US 2012027146 A1 02-02-2012
			WO 2010097111 A1 02-09-2010

EP 2158841	A2	03-03-2010	AU 2009212831 A1 18-03-2010
			CA 2675087 A1 28-02-2010
			CN 101675900 A 24-03-2010
			EP 2158841 A2 03-03-2010
			JP 2010051801 A 11-03-2010
			RU 2009132436 A 10-03-2011
			US 2010056871 A1 04-03-2010

EP 0889616	A1	07-01-1999	CA 2241706 A1 30-12-1998
			DE 69815212 D1 10-07-2003
			DE 69815212 T2 29-04-2004
			EP 0889616 A1 07-01-1999
			JP 11149349 A 02-06-1999
			US 5914991 A 22-06-1999
