Nov. 25, 1958 F. B. MAYNARD 2,862,127

BINARY TO DECIMAL CONVERTER TUBE

Filed May 17, 1954 3 Sheets-Sheet 1

Fig. 1.

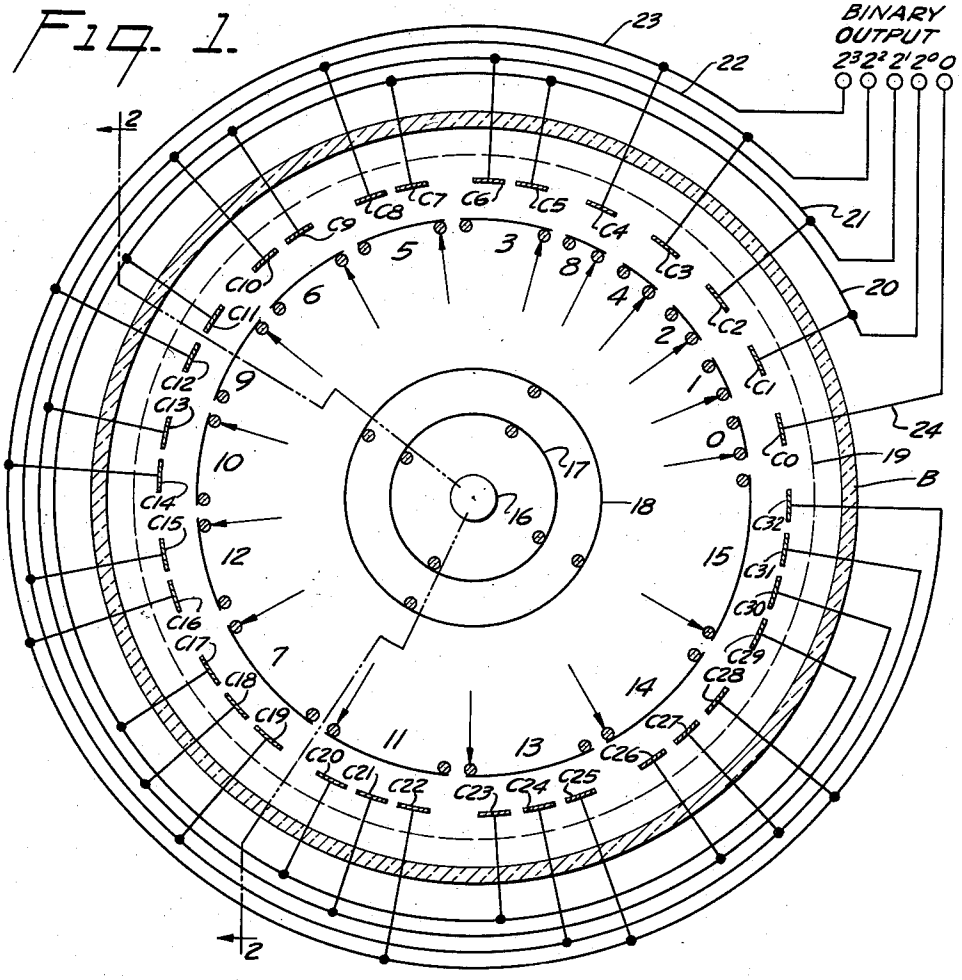
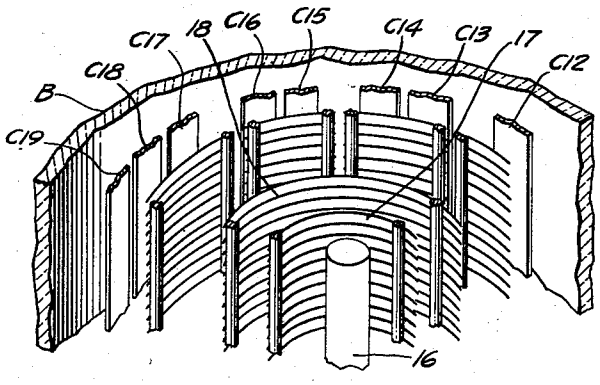


Fig. 2.



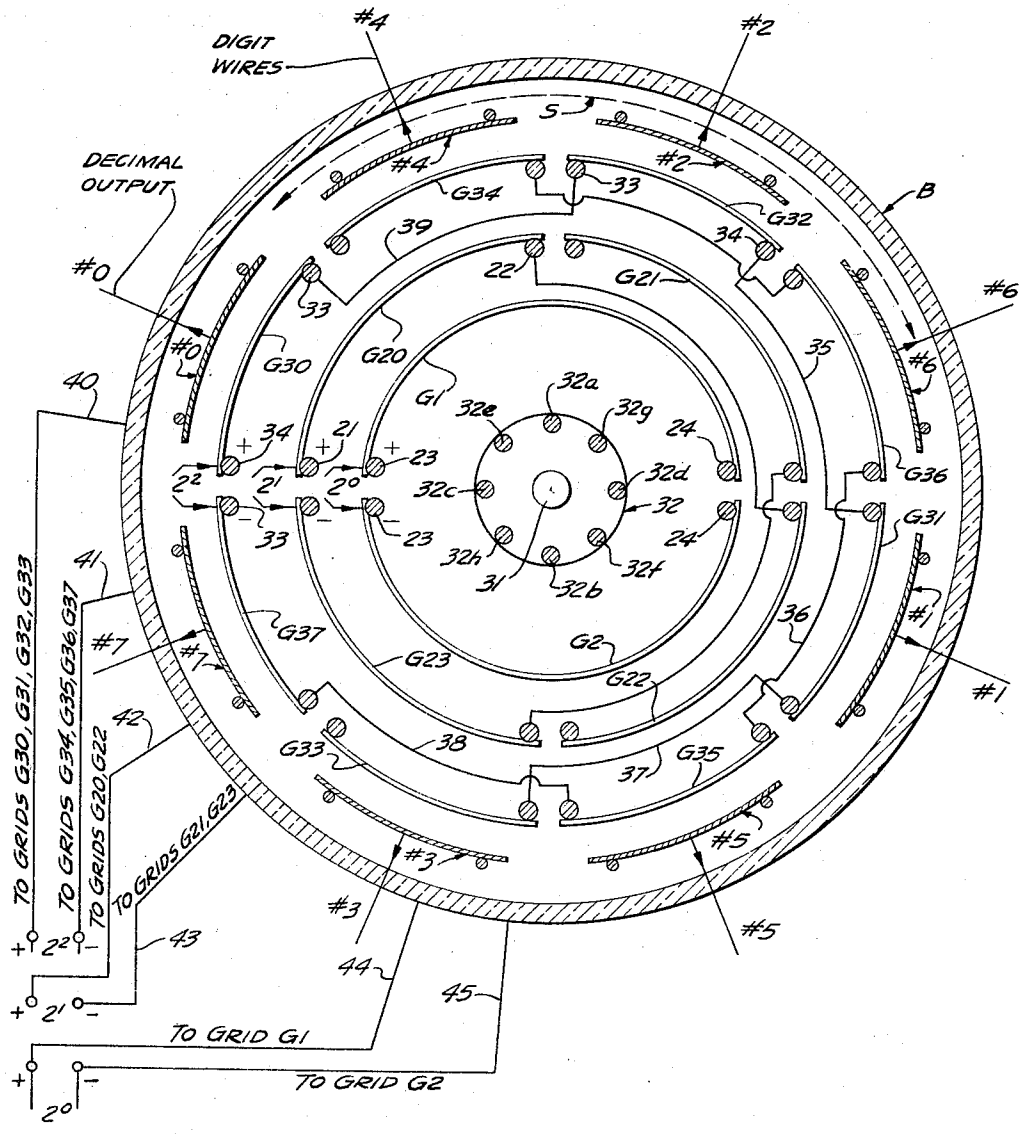
INVENTOR.
FRED B. MAYNARD
BY John J. Regan
ATTORNEY.

Nov. 25, 1958 F. B. MAYNARD 2,862,127

BINARY TO DECIMAL CONVERTER TUBE

Filed May 17, 1954 3 Sheets-Sheet 2

Fig. 3.



INVENTOR.
FRED B. MAYNARD
BY John J. Rogan
ATTORNEY.

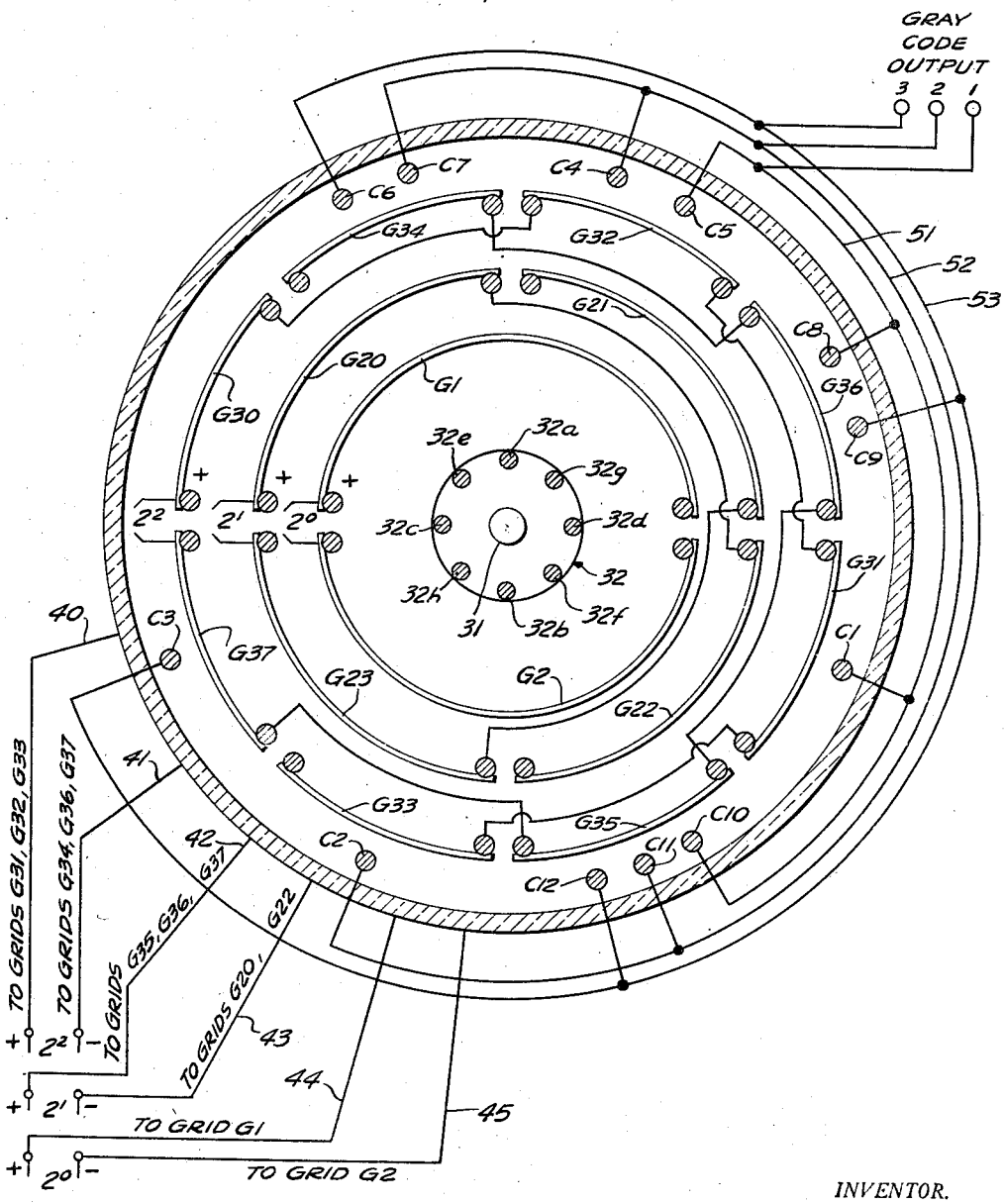
Nov. 25, 1958 F. B. MAYNARD 2,862,127

BINARY TO DECIMAL CONVERTER TUBE

Filed May 17, 1954

3 Sheets-Sheet 3

Fig. 4.



INVENTOR.
FRED B. MAYNARD
BY John J. Logan
ATTORNEY

United States Patent Office

2,862,127

Patented Nov. 25, 1958

2,862,127

BINARY TO DECIMAL CONVERTER TUBE

Fred B. Maynard, Cedar Grove, N. J., assignor to National Union Electric Corporation, Hatboro, Pa., a corporation of Delaware

Application May 17, 1954, Serial No. 430,300

3 Claims. (Cl. 313—73)

This invention relates to electron tubes and more especially to converter tubes for use in electronic computer systems and the like.

A principal object of the invention is to provide a simplified and easily manufactured electron tube for converting input voltages representing one class of digits, for example decimal digits, into output voltages representing another class of digits, for example those used in the well-known binary system.

A feature of the invention relates to a novel and symmetrical electrode arrangement for an electron tube whereby a decimal-digit input voltage can be directly translated into binary number output voltages, and vice versa.

Another feature relates to a novel and symmetrical electrode arrangement for an electron tube whereby signal voltages representing a number in the binary system are converted into a single voltage representing a number in the decimal system.

Another feature relates to an electron tube of the multi-channel gating type wherein a single central electron emitter is surrounded concentrically with a series of gating control grids each of which cooperates with one or a plurality of collectors or anodes. These anodes are interconnected in preselected combinations so that the application of any single voltage representing for example a decimal digit, results in the application simultaneously of on-off voltage conditions in permuted combinations in so-called binary computer wires.

A further feature relates to the novel organization, arrangement, and relative location and interconnection of parts which cooperate to provide an improved signal converter tube for converting numbers in one computing system to numbers in a different computing system.

Other features and advantages not particularly enumerated will be apparent after a consideration of the following detailed descriptions and the appended claims.

In the drawing which shows, by way of example, one preferred embodiment,

Fig. 1 is a schematic plan view of a tube and converting system according to the invention;

Fig. 2 is a perspective view of part of the tube of Fig. 1;

Fig. 3 is a schematic plan view of a modification of the tube and converting system according to the invention;

Fig. 4 is a schematic plan view of a further modification of the invention.

Referring to Figs. 1 and 2 there is shown a tube for the conversion of an input voltage representing for example a digit in the decimal system, to a permuted combination of voltages or lack of voltages on a plurality of so-called binary wires. Thus, for purposes of illustration, assuming a system employing sixteen decimal digits #0 to #15, these digits can be represented on five so-called binary wires according to the well-known arrangement illustrated as follows:

Decimal Digit	Binary Wires Energized				
	0	1	2	3	4
0					
1		x			
2			x		
3		x	x		
4				x	
5		x		x	
6			x	x	
7		x	x	x	
8					x
9		x			x
10			x		x
11		x	x		x
12				x	x
13		x		x	x
14			x	x	x
15		x	x	x	x

In the foregoing chart the letter "x" indicates that the corresponding binary wire has a voltage impressed thereon or is in the "on" condition, whereas the absence of the letter "x" indicates the corresponding binary wire is deenergized or in the "off" condition, thus enabling each wire to control any well-known binary or flip-flop type of control circuit. Referring to Figs. 1 and 2 of the drawing, the tube comprises an enclosing evacuated glass bulb B containing a central electron-emitting cathode **16** which may be of any well-known type such as is used conventionaly in so-called indirectly heated cathodes. It may comprise, for example, a tubular metal sleeve, the periphery of which is coated with any well-known thermionic electron-emissive material. The sleeve is arranged to be heated by any well-known internal heater element. Surrounding the cathode **16** concentrically are two accelerating grids **17**, **18**, which may be connected to suitable positive biasing potentials so as to accelerate the electrons from the cathode **16** to the required degree. Concentrically surrounding the cathode **16** and grids **17**, **18**, is a circumferential array of sixteen discrete gating control grids numbered **0** to **15**. These grids may be of any well-known open work or foraminous structure and are designed so that normally they are connected to a suitable negative potential so as to bias them to plate current cutoff. Each grid may comprise a pair of metal side rods across which extend the spaced final wire grid laterals as shown in Fig. 2.

Suitably mounted in radial alignment with each of the gating grids is one of a series of 33 electron collector electrodes designated C_0–C_{32}. If desired, a foraminous shield grid **19** can surround all the preceding electrodes and this shield grid can be connected to a suitable positive potential. Each of the gating grids is provided with a separate lead-in member designated respectively G_0 to G_{15} so that each grid may be separately energized by a suitable positive input signal representing the respective decimal digit. For example, if the input signal represents the decimal digit zero, only the gating grid #**0** will have a positive potential applied thereto so that the electrons from the cathode **16** will pass only through the grid #**0** to the corresponding electron electrode C_0, which thereupon assumes a steady negative potential. On the other hand, if for example the input decimal-digit signal is #**3**, there will be a positive voltage applied only to gating grid #**3** and the electrons from the cathode **16** will be gated only by that grid so as to reach only the collector electrodes C_5, C_6. In order that each collector electrode may receive the same amount of electron flow when its associated grid is gated on, these collectors should all have the same area and should all subtend the same angle with respect to the cathode.

Since the tube is designed to convert any one of **15** input decimal input digit signals into corresponding binary output signals, the gating grids will have either 1,

2, 3 or 4 collector electrodes in radial registry therewith. For example, gating grids **0**, **1**, **2**, **4**, **8**, have in radial registry therewith a corresponding single collector electrode C_1, C_2, C_3, C_4. Each of the gating control grids **3**, **5**, **6**, **9**, **10** and **12**, has in radial registry therewith a corresponding pair of collector electrodes, namely (C_5, C_6), (C_7, C_8), (C_9, C_{10}), (C_{11}, C_{12}), (C_{13}, C_{14}), (C_{15}, C_{16}). Each of the gating control grids **7**, **11**, **13** and **14**, has in radial registry therewith a set of three collector electrodes. Thus the set of collectors C_{17}, C_{18}, C_{19}, are in radial registry with grid #**7**. Collector electrodes C_{20}, C_{21}, C_{22}, are in radial registry with grid #**11**. Collector electrodes C_{23}, C_{24}, C_{25}, are in registry with grid #**13**. Collector electrodes C_{26}, C_{27}, C_{28}, are in registry with grid #**14**. The grid **15** has a series of four collector electrodes C_{29}, C_{30}, C_{31}, C_{32}, in radial registry therewith.

The #**0** grid and its collector electrode C_0 are connected to the #**0** wire of a set of five binary output wires. The collector electrodes C_1, C_5, C_7, C_{11}, C_{17}, C_{20}, C_{23}, C_{29}, are all connected together by a conductor **20** and thence to the #**1** wire of the binary output wires. Collector electrodes C_2, C_6, C_9, C_{13}, C_{18}, C_{21}, C_{26}, C_{29}, C_{30}, are connected together by a conductor **21** and thence to the #**2** wire of the five binary outputs. Collector electrodes C_3, C_8, C_{10}, C_{15}, C_{19}, C_{24}, C_{27}, C_{31}, are connected together by a conductor **22** and thence to the #**3** wire of the five binary outputs. Finally, collector electrodes C_4, C_{12}, C_{14}, C_{16}, C_{22}, C_{25}, C_{28} and C_{32}, are connected together by a wire **23** and thence to the #**4** wire of the five binary outputs.

From the foregoing it will be seen that by applying the appropriate signal representing a decimal-digit to the corresponding control grid it is possible to set up on the five binary output wires the corresponding "off" and "on" potential combinations as indicated hereinabove. It will be understood, of course, that each of the control grids #**0** to #**15** is provided with a separate lead-in member (not shown) which can be sealed through the base or header or any other convenient portion of the wall of tube **B**.

While in the embodiment of Figs. 1 and 2, the device is arranged to translate an input voltage representing a decimal digit into a combination of "off" and "on" conditions on binary code wires representing the corresponding binary member, it may be desirable to reverse the process. Fig. 3 shows a device for accomplishing this reverse conversion. In other words, the input signals may be those received for example from the five binary leads **20**, **21**, **22**, **23**, **24** (Fig. 1) which are to be converted into a single corresponding output voltage representing the corresponding decimal digit. A device for accomplishing this purpose is shown in schematic plan view in Fig. 3. Merely for simplicity in the drawing, the device is shown employing only three sets of binary input wires, namely 2^0, 2^1, 2^2, although obviously any greater or less number may be employed with corresponding increase in the number of electrodes.

Referring to Fig. 3, the device comprises the evacuated enclosing bulb or envelope B having the usual header through which are sealed in a vacuum-tight manner the various lead-in wires to the various electrodes. Suitably supported within the bulb B centrally thereof is the elongated tubular electron-emitting cathode **31** which may be similar to the cathode **16** of Fig. 1.

Suitably supported concentrically around the cathode **31** are a series of eight parallel metal rods **32** which extend parallel to the length of the cathode **31** and are equally spaced from each other therearound. These rods may be connected to a single lead-in (not shown) for connection to a suitable positive potential whereby the electrons from the cathode are accelerated to the required degree. Concentrically surrounding the cathode are a series of eight collector plates or anodes designated respectively #**0** to #**7**. Each of these electron collector electrodes has the same circumferential arcuate width so that each subtends the same angle with respect to the cathode. Also concentrically surrounding the cathode are a series of eight gating control grids designated respectively **G30** to **G37**. Each of these grids is mounted in front of a corresponding one of the collector electrodes as shown in the drawing. Each grid may comprise a pair of parallel supporting side rods **33**, **34**, across which extend the parallel fine wire grid laterals which constitute the grid. It will be understood, of course, that any well-known form of foraminous structure may be used for these grids. Preferably, the side rods **33** and **34** are arranged so that the effective arcuate width of each gating grid **G30**–**G37** is equal to the arcuate width of the corresponding collector electrode. The gating grids **G32**–**G37** are interconnected in alternate pairs by means of wires **35**, **36**, **37**, **38**, **39**. Thus, wire **35** connects grid **G32** directly to grid **G31**; wire **36** connects grid **G36** directly to grid **G35**; wire **37** connects grid **G31** to grid **33**; wire **38** connects grid **G35** to grid **G37**; and wire **39** connects grid **G30** to grid **G32**.

Also concentrically surrounding the cathode is another set of four gating control grids **G20**–**G23**. The grids of this second set are also provided with respective parallel side rod supports **21**, **22**, across which extend the fine wire grid laterals. The grids **G20**–**G23** are all of equal circumferential arcuate width, and each grid subtends at the cathode an angle equal to that subtended by the corresponding pair of the grids in the first set. For example, grid **G20** subtends the same effective angle at the cathode as both of the grids **G30** and **G34**. Likewise grid **G21** subtends at the cathode substantially the same angle as both grids **G22**, **G36**. Grid **G22** subtends the same angle as both grids **G31**, **G35**. Grid **G23** subtends the same angle as both grids **G33** and **G37**.

Similarly, concentrically surrounding the cathode **G31** is a third set of two gating control grids **G1**, **G2**, each supported on respective side rods **23**, **24**. The grids **G1** and **G2** are of equal circumferential arcuate width, and each subtends at the cathode an angle substantially the same as that subtended by a pair of gating grids. For example, grid **G1** subtends the same angle as both the grids **G20** and **G21** together. Grid **G2** subtends the same angle as both grids **G22** and **G23** together. If it were not for the fact that the gating grids are to be mechanically spaced, the grids **G1** and **G2** might be considered as being approximately 180 degrees in arcuate width. In any event the various gating grids are supported with their corresponding respective side rods in radial alignment so as to cause a minimum amount of electron shadow between successive grids. Likewise, preferably the accelerating grid side rods **32***a*, **32***b*, **32***c*, **32***d* are mounted diagonally opposite to each other and in alignment with the spaces between the ends of the corresponding gating grid pairs so as to cast the minimum electron shadow on the said gating control grids.

Each collector electrode is provided with a separate sealed-in conductor by means of which each collector can be connected to a separate utilization circuit, such for example as a computator circuit element which responds to successive voltages representing successive decimal digits.

The gating grids **G30**, **G31**, **G32**, **G33**, are connected to a single lead-in member **40**; gating grids **G34**, **G35**, **G36**, **G37**, are likewise connected to a single lead-in member **41**. Similarly, the gating grids **G20**, **G22** are connected to a single lead-in **42**; and gating grids **G21**, **G23**, are connected to a single lead-in **43**. In like manner, gating grid **G1** is connected to lead-in member **44**; and gating grid **G2** is connected to lead-in **45**. Therefore, by applying suitable "on" and "off" potential pulses to these various lead-ins in accordance with the above chart, a particular one of the collector electrodes alone is gated into circuit. In other words, for any given combination of pulse and no-pulse potentials applied to the pairs of

lead-ins, there is only one conductive path between the cathode **31** and the particular collector electrode representing the desired decimal digit.

When a gating "on" voltage pulse, for example a positive pulse, is applied to one-half the number of grids in one set of gating grids, an "off" voltage is also simultaneously applied to the remaining half of the number of grids in the same set. For example, if the incoming binary signal voltage is to represent the output decimal-digit #1, a positive or "on" voltage pulse is applied to lead-in **40** and a negative or "off" pulse is applied to lead-in **41**. At the same time a positive "on" pulse is applied to conductor **42**, and an "off" pulse is applied to conductor **43**; and a positive or "on" pulse is applied to lead-in **45**, and a negative or "off" pulse is applied to lead-in **44**. As a result, the electron stream from the cathode **31** will flow only through grids **G2**, **G22**, **G31**, and thence to collector **#1**, which represents an output for the #1 decimal digit. Thus, any collector electrode can be selectively charged by the electron stream in accordance with the binary number pulses applied in "on" and "off" pairs to the respective pairs of lead-ins **40—41**, **42—43**, **44—45**.

While in the embodiment of Fig. 3, the tube illustrates only eight, i. e., 2^n decimal output channels, where "n" is three, it will be understood that any number of channels may be provided by adding more concentric grid systems according to the disclosure, and the number of output collector channels increases as 2^n, while "n" is the number of successive rows of gating grids.

If desired, the tube of Fig. 3 can be modified in accordance with the teaching of the embodiment of Figs. 1 and 2. In other words, instead of using a single collector electrode in back of each of the gating grids **G30–G37**, one, two, or three such collector electrodes may be mounted in back of each of these grids. Such an embodiment is illustrated in Fig. 4. In the embodiment of Fig. 4, the parts which are identical with those of Fig. 3 bear the same designation numerals. The only difference is that associated with each of the said gating grids **G30–G37** are respective one, two, or three collector electrodes. For example, in radial alignment with gating grids **G31**, **G33** and **G37**, are respective single collector electrodes C_1, C_2, and C_3. In radial alignment with each of the collector electrodes **G32**, **G34**, **G36**, are corresponding pairs of collector electrodes C_4—C_5, C_6—C_7, C_8—C_9; while in radial alignment with the gating grid **G35** is a set of three collectors C_{10}, C_{11}, C_{12}. Collectors C_5, C_8, C_1, C_{10}, are connected together by a conductor **51** and thence to the corresponding coded output terminal, which for example may be the **#1** terminal of a well-known "Gray" coding system. Likewise, collectors C_7, C_4, C_{11}, C_2, are connected together by a conductor **52** and thence to the **#2** terminal of the "Gray" code wires. Similarly, collectors C_6, C_9, C_{12}, and C_3 are connected together by a conductor **53** and thence to the **#3** output terminal of the "Gray" code wires. The **#0** terminal of this "Gray" coded output is left blank. Therefore, by applying appropriate combinations of "on" and "off" binary pulses to the lead-ins **40—41**, **42—43**, **44—45**, as described above in connection with Fig. 3, the "Gray" output terminals will be correspondingly energized in accordance with the following chart:

Decimal Digits	Binary Code Conductors			Gray Code Conductors		
	3	2	1	3	2	1
0						
1			x			x
2		x			x	x
3		x	x		x	
4	x			x	x	
5	x		x	x	x	x
6	x	x		x		x
7	x	x	x	x		

In the foregoing chart the letter "x" indicates that the corresponding coded wire has a voltage impressed thereon or is in the "on" condition, whereas the absence of the letter "x" indicates the corresponding coded wire is de-energized or in the "off" condition.

From the foregoing, it will be seen that the embodiments of Figs. 1 and 4 can be combined in series so as to convert decimal input signals applied to the input terminals of Fig. 1 so as to convert them into corresponding binary outputs. These binary outputs in turn can be connected to the binary input terminals **40–45** of a tube according to Fig. 4 to produce at the output of the tube of Fig. 4 the desired combinations of Gray coded wires in accordance with the above chart.

Various changes and modifications may be made in the disclosed embodiments without departing from the spirit and scope of the invention.

What is claimed is:

1. An electron tube for converting input signals in the binary code into corresponding output signals in the decimal system, comprising an evacuated envelope, an electron emitting cathode, a series of 1 to "N" pairs of binary coded input terminals, a set of "n" output electron collector electrodes each connected to a corresponding one of said output terminals and where "n" is 2^N, a series of "N" radially successive sets of gating control grids with the grids of each set being in circumferential array around the cathode and with the grids of each set spaced substantially the same distance from the cathode but with succesive sets at respectively greater distances from the cathode, the first set of gating grids nearest the cathode comprising two grids each subtending an angle of approximately "A" degrees with respect to the cathode, the next set of gating grids comprising four grids each subtending an angle of approximately A/2 degrees with respect to the cathode, the final set of gating grids comprising 2^N grids each subtending an angle of approximately $A/2^N$ degrees with respect to the cathode, means connecting the two grids of the first set each individually to a corresponding one of a first pair of said input terminals, means connecting the alternate grids of the second set together and thence to corresponding terminals of the second pair of input terminals, means connecting the alternate grids of the final set together and thence to corresponding terminals of the final pair of said input terminals, and each of said output electrodes being in alignment with a corresponding one of the gating grids of the said final set.

2. An electron tube according to claim 1 in which the angle "A" subtended by the first grids is approximately 180°.

3. An electron tube for converting input signals in the binary code into corresponding output signals in the decimal system, comprising an evacuated envelope, an electron emitting cathode, a series of "N" pairs of binary coded input terminals, a set of "n" output electron collector electrodes each connected to a respective one of said output terminals, where "n" is 2^N, a series of "N" sets of gating grids with the grids of the first set being spaced each a substantially uniform distance from the cathode and with the grids of each succeeding set being substantially uniformly spaced from the grids of the next preceding set, the first gating grid set nearest the cathode comprising two grids each subtending an angle of "A" degrees with respect to the cathode, the second gating grid set comprising four grids each subtending an angle of approximately A/2 degrees with respect to the cathode, the final gating grid set comprising 2^N grids each subtending an angle of approximately $A/2^N$ degrees with respect to the cathode, means connecting the two grids of the first set each to a corresponding one of the first pair of binary input terminals, means connecting the alternate grids of the second set together and thence to corresponding ones of the second set of input terminals, means connecting the alternate grids of the final set together and

thence to corresponding ones of the final set of input terminals, and each of said output electrodes being in alignment respectively with one corresponding grid of the final set of grids.

References Cited in the file of this patent

UNITED STATES PATENTS

1,630,443	McCullough	May 31, 1927
2,217,774	Skellett	Oct. 15, 1940
2,396,211	Skellett	Mar. 5, 1946
2,424,289	Snyder	July 22, 1947
2,494,670	Rajchman	Jan. 27, 1950
2,519,172	Brown	Aug. 15, 1950
2,533,401	Schramm	Dec. 12, 1950
2,533,405	Skellett	Dec. 12, 1950
2,558,460	Rajchman	June 26, 1951
2,570,716	Rochester	Oct. 9, 1951
2,658,166	Depp	Nov. 3, 1953
2,766,376	Maynard	Oct. 9, 1956
2,784,312	Kates	Mar. 5, 1957

FOREIGN PATENTS

707,632	Great Britain	Apr. 21, 1954