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(54) **Title**: NANOWIRE LED PIXEL

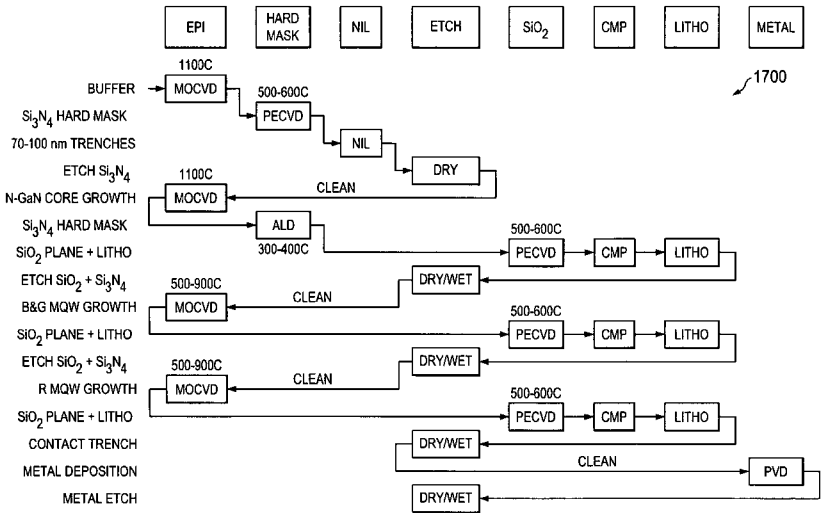

FIG. 17

(57) **Abstract**: Substrates, assemblies, and techniques for enabling a nanowire LED pixel are disclosed herein. For example, some embodiments include growing a buffer layer on a support substrate, growing an N-type GaN layer on the buffer layer, growing a core of N-type GaN rods from the N-type GaN layer, growing an active emitting region (AER) around a portion of the N-type GaN core nanorods to create a blue AER LED, growing a AER around a portion of the N-type GaN core nanorods to create a green AER LED, and growing a AER around a portion of the N-type GaN core nanorods to create a red AER LED. This allows for the fabrication of RGB pixels on wafers monolithically (i.e., on a single wafer). The RGB pixels may then be transferred all at once, from source wafers to TFT backplanes.

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NANOWIRE LED PIXEL

Technical Field

[0001] The present disclosure relates generally to the field of displays, and more particularly, to substrates, assemblies, and techniques to enable a nanowire LED pixel.

Background

[0002] To make active matrix micro LED display panels, micro LEDs that emit red, green and blue colors are first fabricated on separate wafers. The separate LEDs are then transferred from the wafers to backplanes to make red, green, and blue (RGB) pixels that make the active matrix micro LED display panel. Unfortunately, the process of transferring each separate LED can be time consuming and error prone.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGURE 1 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0005] FIGURE 2 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0006] FIGURE 3 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0007] FIGURE 4 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0008] FIGURE 5 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0009] FIGURE 6 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0010] FIGURE 7 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0011] FIGURE 8 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0012] FIGURE 9 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0013] FIGURE 10 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0014] FIGURE 11 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0015] FIGURE 12 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0016] FIGURE 13 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0017] FIGURE 14 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0018] FIGURE 15 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0019] FIGURE 16 is a simplified flowchart illustrating potential operations that may be associated with one embodiment of the present disclosure;

[0020] FIGURE 17 is a simplified process flow diagram illustrating potential operations that may be associated with one embodiment of the present disclosure;

[0021] FIGURE 18 is an interposer implementing one or more of the embodiments disclosed herein; and

[0022] FIGURE 19 is a computing device built in accordance with an embodiment disclosed herein.

[0023] The figures of the drawings are not necessarily drawn to scale, as their dimensions can be varied considerably without departing from the scope of the present disclosure.

Detailed Description

[0024] Described herein are systems and methods of fabricating RGB, RYGB, RRGGBB, etc. pixels on wafers monolithically (i.e., on a single wafer). The pixels may then be transferred all at once, from source wafers to TFT backplanes. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the embodiments disclosed herein may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the embodiments disclosed herein may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0025] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the embodiments disclosed herein, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0026] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one material layer or component with respect to other layers or

components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0027] Implementations of the embodiments disclosed herein may be formed or carried out on a substrate, such as a semiconductor substrate or a sapphire substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the embodiments disclosed herein.

[0028] In the following detailed description, reference is made to the accompanying drawings that form a part hereof wherein like numerals designate like parts throughout, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0029] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be

performed, and/or described operations may be omitted in additional embodiments. For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C).

[0030] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. As used herein, a "package" and an "IC package" are synonymous. As used herein, the terms "chip" and "die" may be used interchangeably.

[0031] For smartphone/tablet users who are dissatisfied with their device charging cycle or battery life, micro LED displays can offer an improvement of the charging cycle of a smartphone. To make active matrix micro LED display panels, GaN-based micro LEDs that emit red, green and blue colors are first fabricated on separate wafers (silicon or sapphire) then transferred from the wafers to thin film transistor (TFT) backplanes to make red, green, and blue (RGB) pixels that make the active matrix micro LED display panel. One drawback of this process is that the transfer process has to be executed three times for the three colors. This affects the throughput of the transfer process and increases the chance of missing transfers which affect the overall production yield. The production cost of micro LED displays is very sensitive to the transfer tact time of micro LEDs from source wafers to host glass TFT backplanes, especially for large size displays such as tables or notebooks.

[0032] Disclosed herein are substrates, assemblies, and techniques for enabling a nanowire LED pixel. In an embodiment, RGB pixels may be fabricated on wafers monolithically. The nanowire RGB pixels may then be transferred all at once, from source wafers to TFT backplanes. This process can improve the throughput by three times and the overall production yield of display panels. In an example, red, yellow, green, blue (RYGB) pixels may be fabricated on wafers monolithically. The nanowire RYGB pixels may then be transferred all at once, from source wafers to TFT backplanes. In yet other examples, red, red, green, green, blue, blue (RRGGBB) pixels (or some other combination) may be fabricated on wafers monolithically. The nanowire RRGGGB pixels (or other combination) may then be transferred all at once, from source wafers to TFT backplanes.

[0033] In one specific example, a process for making pixels on a wafer can start with a silicon, silicon carbide, or sapphire wafer. A buffer stack can be grown on the silicon or sapphire wafer. The buffer stack should allow good quality EPI growth without delamination of the GaN active layer from the substrate wafer. Next, an N-type GaN layer can be gown on the buffer layer. In an example, the N-type GaN layer may be about 1um in thickness. A hard mask (e.g., Si3N4) can be deposited on the N-type GaN layer using chemical vapor deposition (CVD)/plasma enhanced CVD (PECVD) or atomic layer deposition (ALD). Nanoimprint Lithography (NIL) can be used to pattern and open trenches down to the buffer layer. In an example, the trenches may be about 50 to about 300 nm wide. In another example, the trenches may be about 70 to about 150 nm wide. A core of N-type GaN rods may be grown using metal organic chemical vapor phase deposition (MOCVD). Next, a Si3N4 hardmask may be deposited using ALD or CVD. In an example, the hardmask may be about 5 to about 20 nms thick. Then SiO2 may be deposited using a low temperature PECVD process. Chemical mechanical polishing may be used to planarize the SiO2.

[0034] Micrometer scale lithography can be used to uncover (e.g., by etching SiO2 and Si3N4) areas where blue and green (or some other color) LEDs will be located. MOCVD may be used to grow an InGaN multi quantum well around the exposed N-type GaN core nanorods. The indium composition in InGaN is determined by the diameter of the core N-GaN nanorods. MOCVD may also be used to grow p-type GaN for the contacts in the blue and green LEDs. SiO2 can be deposited using CVD or PECVD and CMP may be used to planarize the SiO2.

[0035] Micro-scale lithography techniques may be used to uncover the area of the red (or some other color) LED. MOCVD may be used to grow an InGaN multi-quantum well around the N-GaN nanorods in the red LED region. MOCVD may be used to grow P-type GaN for contacting the red LED. SiO2 can be deposited using CVD or PECVD and CMP can be used to planarize. A micro-scale lithograph method may be used to pattern the contacts for red, green and blue LEDs. A metal contact can be deposited and lithography and etch may be used again to make separate contacts to red, green and blue LEDs.

[0036] Turning to FIGURE 1, FIGURE 1 illustrates one embodiment of a nanowire LED pixel 100. Nanowire LED pixel 100 can include a support substrate 102, a buffer stack 104, a

GaN active layer 106, a hard mask 108, a first active emitting region (AER) LED 110, a second AER LED 112, a third AER LED 114, a metal contact 116, and a SiO2 layer 122. FIGURE 1 is an illustrative example of three nanowire LEDs (e.g., RGB, YGB, etc.) grown monolithically on the same support substrate 102. More than three nanowire LEDs (e.g., RYGB, RRGGBB, etc.) may be grown monolithically and is certainly within the scope of the embodiments disclosed herein. Support substrate 102 may be any type of wafer such as sapphire, silicon wafer, silicon carbide wafer, etc. The term "active emitting region" or "AER" is to include an active emitting region such as an p-n junction, multi-quantum well (MQW), pin junction, etc.

[0037] Turning to FIGURE 2, FIGURE 2 illustrates one embodiment of one of the early stages of building a nanowire LED pixel 100. As illustrated in FIGURE 2, GaN active layer 106 can be deposited on support substrate 102. Buffer stack 104 can help facilitate the process of creating GaN active layer 106 on support substrate 102. In an example, buffer stack 104 may be about 3um in thickness. In another example, GaN active layer 106 may include n-GaN and be about 1um in thickness.

[0038] Turning to FIGURE 3, FIGURE 3 illustrates one embodiment of one of the early stages of building a nanowire LED pixel 100. As illustrated in FIGURE 3, hard mask 108 can be deposited or layered onto GaN active layer 106. In an example, hard mask 108 may be a Si3N4 mask or some other similar type hard mask. Hard mask 108 may be deposited using CVD/PECVD or ALD.

[0039] Turning to FIGURE 4, FIGURE 4 illustrates one embodiment of one of the early stages of building a nanowire LED pixel 100. As illustrated in FIGURE 4, trenches 132 may be created in hard mask 108. Trenches 132 may be created by nanoimprint lithography (NIL) or some other means or method of creating nanometer scale trenches or cavities in hard mask 108. Trenches 132 may be about 50 to about 150 nms wide.

[0040] Turning to FIGURE 5, FIGURE 5 illustrates one embodiment of one of the early stages of building a nanowire LED pixel 100. As illustrated in FIGURE 5, a core 118 is grown through each trench 132. Core 118 can be the core shell for first AER LED 110, second AER LED 112, and third AER LED 112. In an example, core 118 may be N-type GaN rods grown using MOCVD.

[0041] Turning to FIGURE 6, FIGURE 6 illustrates one embodiment of one of the early stages of building a nanowire LED pixel 100. As illustrated in FIGURE 6, a hard mask 120 can

be deposited on each core 118. Hard mask 120 may be a Si3N4 hard mask. In one example, hard mark 120 may be about 5 to about 20 nm thick. Hard mask 120 can be deposited using ALD or CVD.

[0042] Turning to FIGURE 7, FIGURE 7 illustrates one embodiment of one of the early stages of building a nanowire LED pixel 100. As illustrated in FIGURE 7, SiO2 layer 122 may be deposited over hard mask 120. In an example, SiO2 layer 122 can be deposited using a low temperature PECVC process. For example, the temperature may be below about 500 °C or between about 400 °C to about 600 °C. SiO2 layer 122 may undergo chemical mechanical polishing to planarize SiO2 layer 122.

[0043] Turning to FIGURE 8, FIGURE 8 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 8, SiO2 layer 122 and hard mask 120 may be etched from each core 118 that will comprise first AER LED 110 and second AER LED 112. In an example, micrometer scale lithography may be used to uncover each core 118 that will comprise first AER LED 110 and second AER LED 112.

[0044] Turning to FIGURE 9, FIGURE 9 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 9, selective AER growth 124 on a portion of exposed cores 118 may be used to create first AER LED 110 and selective AER growth 126 on a portion of exposed cores 118 may be used to create second AER LED 112. In an example, MOCVD may be used to grow InGaN AERs around exposed cores 118. The indium composition in InGaN is determined by the diameter of each exposed core 118. For example, with the increase in nanowire diameters from 147 to 270 nm, the emission peak wavelengths shift monotonically from 480 to 632 nm, (i.e., from blue to red color). Such a wide range of emission wavelength tuning is attributed to the increased indium composition with increasing wire diameter.

[0045] Turning to FIGURE 10, FIGURE 10 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 10, SiO2 layer 122 may be deposited over first AER LED 110 and second AER LED 112. In an example, SiO2 layer 122 can be deposited using a low temperature PECVC process. For example, the temperature may be below about 500 °C or between about 400 °C to about 600 °C. SiO2 layer 122 may undergo chemical mechanical polishing to planarize SiO2 layer 122.

[0046] Turning to FIGURE 11, FIGURE 11 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 11, a photoresist layer 128 may be created on a region of SiO2 layer 122 that is over first AER LED 110 and second AER LED 112. Photoresist layer 128 may be created using photolithography. Photoresist layer 128 can be configured to provide first AER LED 110 and second AER LED 112 with photoresist protection from etching that will be used to create a red AER LED.

[0047] Turning to FIGURE 12, FIGURE 12 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 12, SiO2 layer 122 and hard mask 120 may be etched from each core 118 that will comprise third AER LED 112. In an example, micrometer scale lithography may be used to uncover each core 118 that will comprise third AER LED 112.

[0048] Turning to FIGURE 13, FIGURE 13 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 13, selective AER growth 130 on a portion of exposed cores 118 may be used to create third AER LED 112. In an example, MOCVD may be used to grow InGaN AERs around exposed cores 118 to create third AER LED 112.

[0049] Turning to FIGURE 14, FIGURE 14 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 14, SiO2 layer 122 may be deposited over third AER LED 112. In an example, SiO2 layer 122 can be deposited using a low temperature PECVC process. For example, the temperature may be below about 500 °C or between about 400 °C to about 600 °C. SiO2 layer 122 may undergo chemical mechanical polishing to planarize SiO2 layer 122.

[0050] Turning to FIGURE 15, FIGURE 15 illustrates one embodiment of one of the stages of building a nanowire LED pixel 100. As illustrated in FIGURE 15, portions of SiO2 layer 122 that are above first AER LED 110, second AER LED 112, and third AER LED 112 are etched away. In an example, a micro-scale lithography method is used to pattern etch the areas of SiO2 layer 122 that are above first AER LED 110, second AER LED 112, and third AER LED 112. Metal contacts 116 (shown in FIGURE 1) can be deposited into the areas etched away to create contacts for first AER LED 110, second AER LED 112, and third AER LED 112.

[0051] Turning to FIGURE 16, FIGURE 16 is an example flowchart illustrating possible operations of a flow 1600 that may be associated with a nanowire LED pixel, in accordance

with an embodiment. In an embodiment, at 1602, a buffer layer is created on a substrate. At 1604, a gallium nitride layer is created on the buffer layer. At 1606, a mask layer is created on the gallium nitride layer. At 1608, openings are etched in the mask layer. At 1610, nanowires from the gallium nitride layer are grown through the openings in the mask layer. At 1612, a mask layer is created over the nanowires. At 1614, silicon dioxide is planarized over the nanowires. At 1616, the silicon dioxide undergoes chemical mechanical polishing. At 1618, silicon dioxide that covers the nanowires that will become a green LED is etched away. At 1620, a multiple quantum well (or AER) is grown over the exposed nano wires to create a green LED. At 1622, silicon dioxide is planarized over the green LED. At 1624, silicon dioxide that covers the nanowires that will become a blue LED is etched away. At 1626, a multiple quantum well (or AER) is grown over the exposed nanowires to create a blue LED. At 1628, silicon dioxide is planarized over the blue LED. At 1630, a photo resist layer is created over the green LED and the blue LED. At 1632 silicon dioxide that covers the nano wires that will become a red LED is etched away. At 1634, a multiple quantum well (or AER) is grown over the exposed nanowires to create a red LED. At 1636, silicon dioxide is planarized over the red LED. At 1638, the silicon dioxide undergoes chemical mechanical polishing. At 1640, contacts over the green LED blue LED and red LED are opened.

[0052] Turning to FIGURE 17, FIGURE 17 is an example process flow illustrating possible operations of a flow 1700 that may be associated with a nanowire LED pixel, in accordance with an embodiment. In an embodiment, a buffer layer may be deposited on a wafer using MOCVD at a temperature of about 1100 °C. Then a hard mask may be deposited using PECVD at temperatures of about 500 °C to 600°C. Trenches may be formed in the hard mask using NIL and the trenches may be about 50 to about 300 nm wide. The structure may be dried and etched. Using MOCVD, a N-GaN core may be grown. A hard mask can be deposited using ALD at about 300 °C to about 400°C. A layer of SiO2 can be deposited using PECVD at about 500 °C to about 600 °C and the layer of SiO2 can undergo chemical mechanical planarization and lithography. The SiO2 layer can be etched and cleaned. MOCVD at about 500 °C to about 900°C can be used to facilitate blue LED AER growth and green LED AER growth. SiO2 can be deposited using CVD or PECVD and CMP may be used to planarize the SiO2. The SiO2 layer can be etched and cleaned. MOCVD at about 500 °C to about 900°C can be used to facilitate red LED AER growth. SiO2 can again

be deposited using CVD or PECVD and CMP can be used to planarize the SiO2. A micro-scale lithograph method may be used to create contact trenches for the red, green and blue LEDs and a metal deposition can be used to create metal contacts for each LED. Lithography and etch may be used again to make separate contacts for the red, green and blue LEDs

[0053] This allows RGB pixels to be fabricated on wafers monolithically and the RGB pixels may then be transferred all at once, from source wafers to TFT backplanes and coupled to one or more transistors on a substrate. In an embodiment, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the embodiments disclosed herein, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the embodiments disclosed herein may also be carried out using nonplanar transistors.

[0054] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0055] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some

implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0056] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0057] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0058] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate

implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0059] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0060] One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0061] Turning to FIGURE 18, FIGURE 18 illustrates an interposer 1800 that can include or interact with one or more embodiments disclosed herein. The interposer 1800 is an intervening substrate used to bridge a first substrate 1802 to a second substrate 1804. The first substrate 1802 may be, for instance, an integrated circuit die. The second

substrate 1804 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1800 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1800 may couple an integrated circuit die to a ball grid array (BGA) 1806 that can subsequently be coupled to the second substrate 1804. In some embodiments, the first and second substrates 1802/1804 are attached to opposing sides of the interposer 1800. In other embodiments, the first and second substrates 1802/1804 are attached to the same side of the interposer 1800. And in further embodiments, three or more substrates are interconnected by way of the interposer 1800.

[0062] The interposer 1800 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0063] The interposer may include metal interconnects 1808 and vias 1810, including but not limited to through-silicon vias (TSVs) 1812. The interposer 1800 may further include embedded devices 1814, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1800. In accordance with various embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 1800.

[0064] Turning to FIGURE 19, FIGURE 19 illustrates a computing device 1900 in accordance with various embodiments. The computing device 1900 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 1900 include, but are not limited to, an integrated circuit die 1902 and at least one communications logic unit 1908. In some implementations the communications logic unit 1908 is fabricated within the integrated circuit die 1902 while in other implementations the

communications logic unit 1908 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 1902. The integrated circuit die 1902 may include a CPU 1904 as well as on-die memory 1906, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0065] Computing device 1900 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1910 (e.g., DRAM), non-volatile memory 1912 (e.g., ROM or flash memory), a graphics processing unit 1914 (GPU), a digital signal processor 1916, a crypto processor 1942 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 1920, an antenna 1922, a display or a touchscreen display 1924, a touchscreen controller 1926, a battery 1928 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 1928, a compass 1930, a motion coprocessor or sensors 1932 (that may include an accelerometer, a gyroscope, and a compass), a speaker 1934, a camera 1936, user input devices 1938 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1940 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0066] The communications logic unit 1908 enables wireless communications for the transfer of data to and from the computing device 1900. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 1908 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1900 may include a plurality of communications logic units 1908. For instance, a first

communications logic unit 1908 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 1908 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0067] The processor 1904 of the computing device 1900 can communicate with one or more devices that are formed in accordance with various embodiments. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0068] The communications logic unit 1908 may also include one or more devices, such as transistors or metal interconnects, that are in communication with various ones of the embodiments disclosed herein. In further embodiments, another component housed within the computing device 1200 may contain one or more devices, such as transistors or metal interconnects, that are formed in accordance with implementations of the embodiments disclosed herein.

[0069] In various embodiments, the computing device 1900 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1900 may be any other electronic device that processes data.

[0070] The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the scope of the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the embodiments disclosed herein are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

OTHER NOTES AND EXAMPLES

[0071] Example 1 is a nanowire pixel including a support substrate, an n-type gallium nitride (GaN) layer on the support substrate, where the GaN layer includes a plurality of N-type GaN core nanorods, a first active emitting region (AER) on a first portion of the plurality of N-type GaN core nanorods to create a first AER LED, a second AER on a second portion of the plurality of N-type GaN core nanorods to create a second AER LED, and a third AER on a third portion of the plurality of N-type GaN core nanorods to create a third AER LED.

[0072] In Example 2, the subject matter of Example 1 can optionally include a fourth AER on a fourth portion of the plurality of N-type GaN core nanorods to create a fourth AER LED.

[0073] In Example 3, the subject matter of any one of Examples 1-2 can optionally include where the N-type GaN core nanorods extend from an N-type GaN layer on a buffer layer.

[0074] In Example 4, the subject matter of any one of Examples 1-3 can optionally include where the plurality of N-type GaN core nanorods were grown using metal organic chemical vapor phase deposition (MOCVD).

[0075] In Example 5, the subject matter of any one of Examples 1-4 can optionally include where MOCVD is capable of forming an indium GaN multi quantum well around the N-type GaN core nanorods.

[0076] In Example 6, the subject matter of any one of Examples 1-5 can optionally include where the N-type GaN layer is about 1um thick.

[0077] In Example 7, a method can include growing a buffer layer on a support substrate, growing an N-type gallium nitride (GaN) layer on the buffer layer, growing a core of N-type GaN rods from the N-type GaN layer, growing an active emitting region (AER) around a portion of the N-type GaN core nanorods to create a blue AER LED, growing a AER around a portion of the N-type GaN core nanorods to create a green AER LED, and growing a AER around a portion of the N-type GaN core nanorods to create a red AER LED.

[0078] In Example 8, the subject matter of Example 7 can optionally include where the core of N-type GaN rods may be grown using metal organic chemical vapor phase deposition (MOCVD).

[0079] In Example 9, the subject matter of any one of Examples 7-8 can optionally include where MOCVD may be used to grow an indium GaN multi quantum well around the N-type GaN core nanorods.

[0080] In Example 10, the subject matter of any one of Examples 7-9 can optionally include where the N-type GaN layer is about 1um thick.

[0081] In Example 11, the subject matter of any one of Examples 7-10 can optionally include depositing a hard mask on the N-type GaN layer using chemical vapor deposition (CVD)/plasma enhanced CVD (PECVD) or atomic layer deposition (ALD), opening trenches through the hard mask and down to the buffer layer, and allowing the core of N-type GaN rods to grow through the trenches from the N-type GaN layer.

[0082] In Example 12, the subject matter of any one of Examples 7-11 can optionally include where the hard mask is Si3N4.

[0083] In Example 13, the subject matter of any one of Examples7-12 can optionally include where the support substrate is a silicon or sapphire wafer.

[0084] In Example 14, the subject matter of any one of Examples 8-13 can optionally include growing a AER around a portion of the N-type GaN core nanorods to create a yellow AER LED.

[0085] Example 15 is an apparatus including a micro LED display that includes red, green, and blue (RGB) nanowire pixels, where the RGB nanowire pixels are fabricated on a wafer monolithically and then transferred all at once to a thin film transistor (TFT) backplane.

[0086] Example 16 the subject matter of Example 15 can optionally include where the micro LED display includes active matrix micro LED display panels that include gallium nitride (GaN)-based Micro LEDs that emit RGB colors.

[0087] In Example 17, the subject matter of Example 15-16 can optionally include where the RGB nanowire pixels were fabricated on the wafers monolithically by growing a buffer layer on a support substrate, growing an N-type gallium nitride (GaN)-layer on the buffer layer, growing a core of N-type GaN rods from the N-type GaN layer, growing an active emitting region (AER) around a portion of the N-type GaN core nanorods to create a blue AER LED, growing a AER around a portion of the N-type GaN core nanorods to create a

green AER LED, and growing a AER around a portion of the N-type GaN core nanorods to create a red AER LED.

[0088] In Example 18, the subject matter of any one of the Examples 15-17 can optionally include where the N-type GaN layer is about 1um thick.

[0089] In Example 19, the subject matter of any one of the Examples 15-18 can optionally include where the core of N-type GaN rods may be grown using metal organic chemical vapor phase deposition (MOCVD)..

[0090] In Example 20, the subject matter of any one of the Examples 15-19 can optionally include where MOCVD may be used to grow an InGaN multi quantum well around the N-type GaN core nanorods.

[0091] Example 21 is a computing device including a processor mounted on a substrate, a communications logic unit within the processor, a memory within the processor, a graphics processing unit within the computing device, an antenna within the computing device, a display on the computing device, a battery within the computing device, a power amplifier within the processor, and a voltage regulator within the processor, where the display includes, red, green, and blue (RGB) nanowire pixels, where the RGB nanowire pixels are fabricated on a wafer monolithically and then transferred all at once to a thin film transistor (TFT) backplane.

[0092] In Example 22, the subject matter of Example 21 can optionally include where the micro LED display includes active matrix micro LED display panels that include gallium nitride (GaN)-based Micro LEDs that emit RGB colors.

[0093] In Example 23, the subject matter of any one of the Examples 21-22 can optionally include where the RGB nanowire pixels includes a support substrate, an n-type gallium nitride (GaN) layer on the support substrate, where the GaN layer includes a plurality of N-type GaN core nanorods, a blue active emitting region (AER) grown around a blue portion of the plurality of N-type GaN core nanorods to create a blue AER LED, a green AER grown around a green portion of the plurality of N-type GaN core nanorods to create a green AER LED, and a red AER grown around a red portion of the plurality of N-type GaN core nanorods to create a red AER LED.

[0094] In Example 24, the subject matter of any one of the Examples 21-22 can optionally include where the N-type GaN core nanorods were grown from an N-type GaN layer on a buffer layer.

[0095] In Example 25, the subject matter of any one of the Examples 21-24 can optionally include where the plurality of N-type GaN core nanorods were grown using metal organic chemical vapor phase deposition (MOCVD).

[0096] In Example 26, the subject matter of any one of the Examples 21-25 can optionally include where wherein the N-type GaN layer is about 1um thick.

[0097] Example 27 is a nanowire pixel including a support substrate, an n-type gallium nitride (GaN) layer on the support substrate, where the GaN layer includes a plurality of N-type GaN core nanorods, a first active emitting region (AER) grown around a first portion of the plurality of N-type GaN core nanorods to create a first AER LED, a second AER grown around a second portion of the plurality of N-type GaN core nanorods to create a second AER LED, and a third AER grown around a third portion of the plurality of N-type GaN core nanorods to create a third AER LED.

[0098] In Example 28, the subject matter of Example 27 can optionally include a fourth AER grown around a fourth portion of the plurality of N-type GaN core nanorods to create a fourth AER LED.

[0099] In Example 29, the subject matter of any one of Examples 27-28 can optionally include where the N-type GaN core nanorods were grown from an N-type GaN layer on a buffer layer.

[00100] In Example 30, the subject matter of any one of Examples 27-29 can optionally include where the plurality of N-type GaN core nanorods were grown using metal organic chemical vapor phase deposition (MOCVD).

[00101] In Example 31, the subject matter of any one of Examples 27-30 can optionally include where MOCVD may be used to grow an indium GaN multi quantum well around the N-type GaN core nanorods.

[00102] In Example 32, the subject matter of any one of Examples 27-31 can optionally include where the N-type GaN layer is about 1um thick.

Claims

1. A nanowire pixel comprising:

a support substrate;

an n-type gallium nitride (GaN) layer on the support substrate, wherein the GaN layer includes a plurality of N-type GaN core nanorods;

a first active emitting region (AER) on a first portion of the plurality of N-type GaN core nanorods to create a first AER LED;

a second AER on a second portion of the plurality of N-type GaN core nanorods to create a second AER LED; and

a third AER on a third portion of the plurality of N-type GaN core nanorods to create a third AER LED.

2. The nanowire pixel of Claim 1, further comprising:

a fourth AER on a fourth portion of the plurality of N-type GaN core nanorods to create a fourth AER LED.

3. The nanowire pixel of Claim 1, wherein the N-type GaN core nanorods extend from an N-type GaN layer on a buffer layer.

4. The nanowire pixel of any of Claims 1-3, wherein metal organic chemical vapor phase deposition (MOCVD) is capable of forming an indium GaN multi quantum well around the N-type GaN core nanorods.

5. The nanowire pixel of Claim 4, wherein the N-type GaN layer is about 1um thick.

6. A method comprising:

growing a buffer layer on a support substrate;

growing an N-type gallium nitride (GaN) layer on the buffer layer;

growing a core of N-type GaN rods from the N-type GaN layer;

growing an active emitting region (AER) around a portion of the N-type GaN core nanorods to create a blue AER LED;

growing a AER around a portion of the N-type GaN core nanorods to create a green AER LED; and

growing a AER around a portion of the N-type GaN core nanorods to create a red AER LED.

7. The method of Claim 6, wherein the core of N-type GaN rods may be grown using metal organic chemical vapor phase deposition (MOCVD).

8. The method of Claim 7, wherein MOCVD may be used to grow an indium GaN multi quantum well around the N-type GaN core nanorods.

9. The method of any of Claims 6-8, wherein the N-type GaN layer is about 1um thick.

10. The method of Claim 9, further comprising:

depositing a hard mask on the N-type GaN layer using chemical vapor deposition (CVD)/plasma enhanced CVD (PECVD) or atomic layer deposition (ALD);

opening trenches through the hard mask and down to the buffer layer; and

allowing the core of N-type GaN rods to grow through the trenches from the N-type GaN layer.

11. The method of Claim 10, wherein the hard mask is Si3N4.

12. The method of Claim 6, wherein the support substrate is a silicon or sapphire wafer.

13. The method of Claim 6, further comprising:

growing a AER around a portion of the N-type GaN core nanorods to create a yellow AER LED.

14. An apparatus comprising:

a micro LED display that includes red, green, and blue (RGB) nanowire pixels, wherein the RGB nanowire pixels are fabricated on a wafer monolithically and then transferred all at once to a thin film transistor (TFT) backplane.

15. The apparatus of Claim 14, wherein the micro LED display includes active matrix micro LED display panels that include gallium nitride (GaN)-based Micro LEDs that emit RGB colors.

16. The apparatus of any of Claims 14 and 15, wherein the RGB nanowire pixels were fabricated on the wafers monolithically by:

growing a buffer layer on a support substrate;

growing an N-type gallium nitride (GaN)-layer on the buffer layer;

growing a core of N-type GaN rods from the N-type GaN layer;

growing an active emitting region (AER) around a portion of the N-type GaN core nanorods to create a blue AER LED;

growing a AER around a portion of the N-type GaN core nanorods to create a green AER LED; and

growing a AER around a portion of the N-type GaN core nanorods to create a red AER LED.

17. The apparatus of Claim 16, wherein the N-type GaN layer is about 1um thick.

18. The apparatus of Claim 16, wherein the core of N-type GaN rods may be grown using metal organic chemical vapor phase deposition (MOCVD).

19. The apparatus of Claim 18, wherein MOCVD may be used to grow an InGaN multi quantum well around the N-type GaN core nanorods.

20. A computing device comprising:

a processor mounted on a substrate;

a communications logic unit within the processor;

a memory within the processor;

a graphics processing unit within the computing device;

an antenna within the computing device;

a display on the computing device;

a battery within the computing device;

a power amplifier within the processor; and

a voltage regulator within the processor;

wherein the display includes:

red, green, and blue (RGB) nanowire pixels, wherein the RGB nanowire pixels are fabricated on a wafer monolithically and then transferred all at once to a thin film transistor (TFT) backplane.

21. The computing device of Claim 20, wherein wherein the micro LED display includes active matrix micro LED display panels that include gallium nitride (GaN)-based Micro LEDs that emit RGB colors.

22. The computing device of Claim 20, wherein the RGB nanowire pixels includes:

a support substrate;

an n-type gallium nitride (GaN) layer on the support substrate, wherein the GaN layer includes a plurality of N-type GaN core nanorods;

a blue active emitting region (AER) grown around a blue portion of the plurality of N-type GaN core nanorods to create a blue AER LED;

a green AER grown around a green portion of the plurality of N-type GaN core nanorods to create a green AER LED; and

a red AER grown around a red portion of the plurality of N-type GaN core nanorods to create a red AER LED.

23. The computing device of Claim 22, wherein the N-type GaN core nanorods were grown from an N-type GaN layer on a buffer layer.

24. The computing device of Claim 22, wherein the plurality of N-type GaN core nanorods were grown using metal organic chemical vapor phase deposition (MOCVD).

25. The computing device of Claim 21, wherein the N-type GaN layer is about 1um thick.

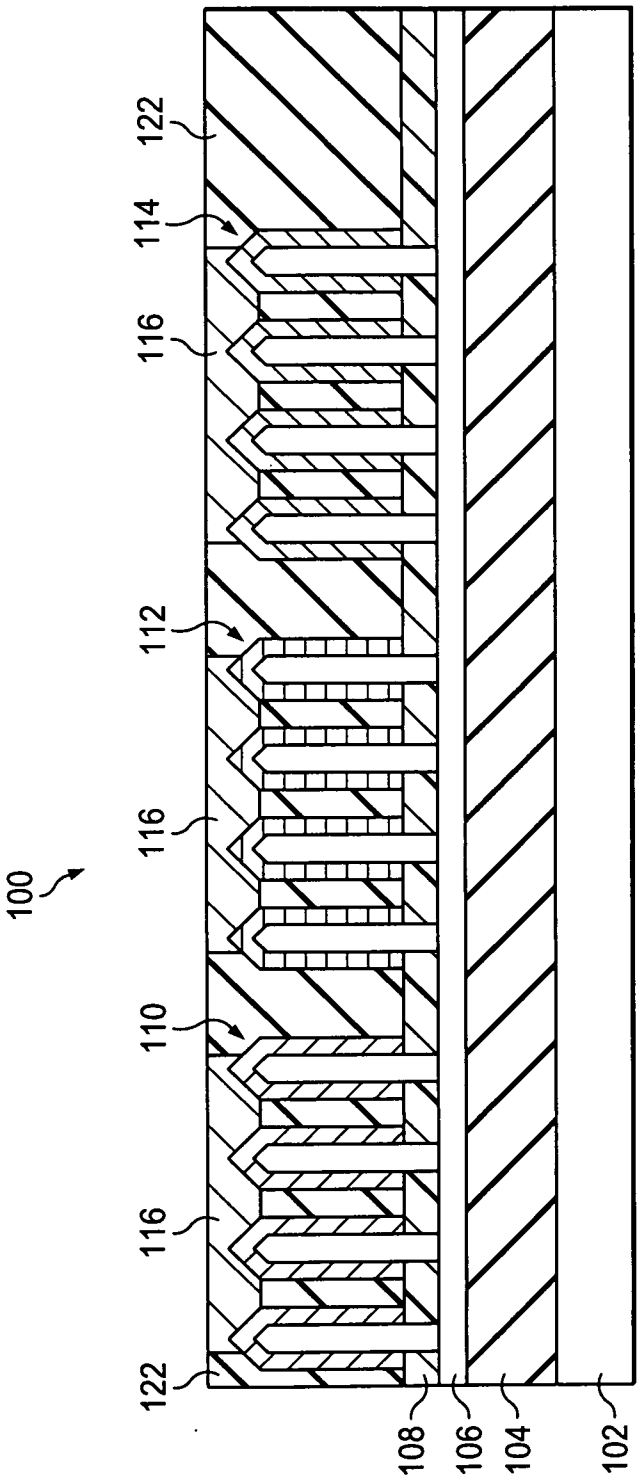

FIG. 1

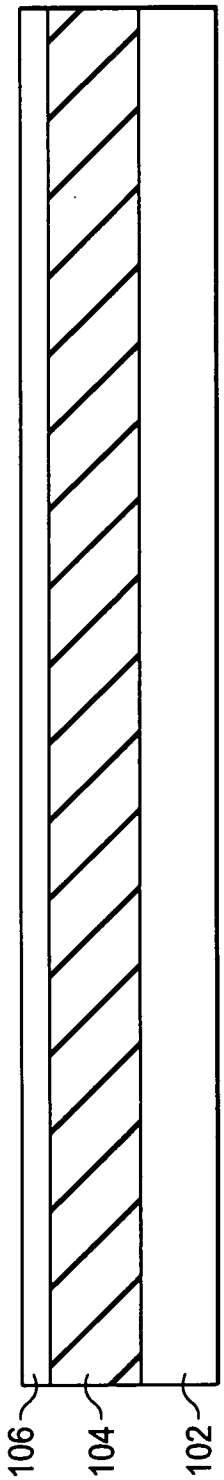

FIG. 2

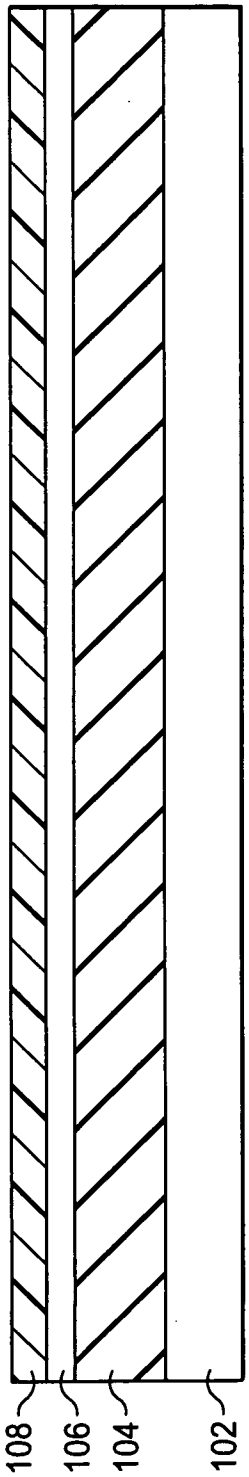

FIG. 3

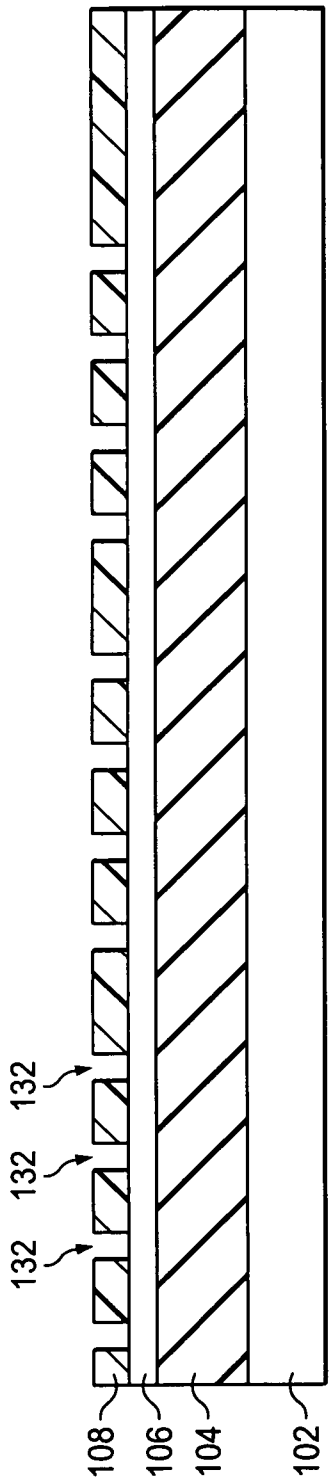
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FIG. 4

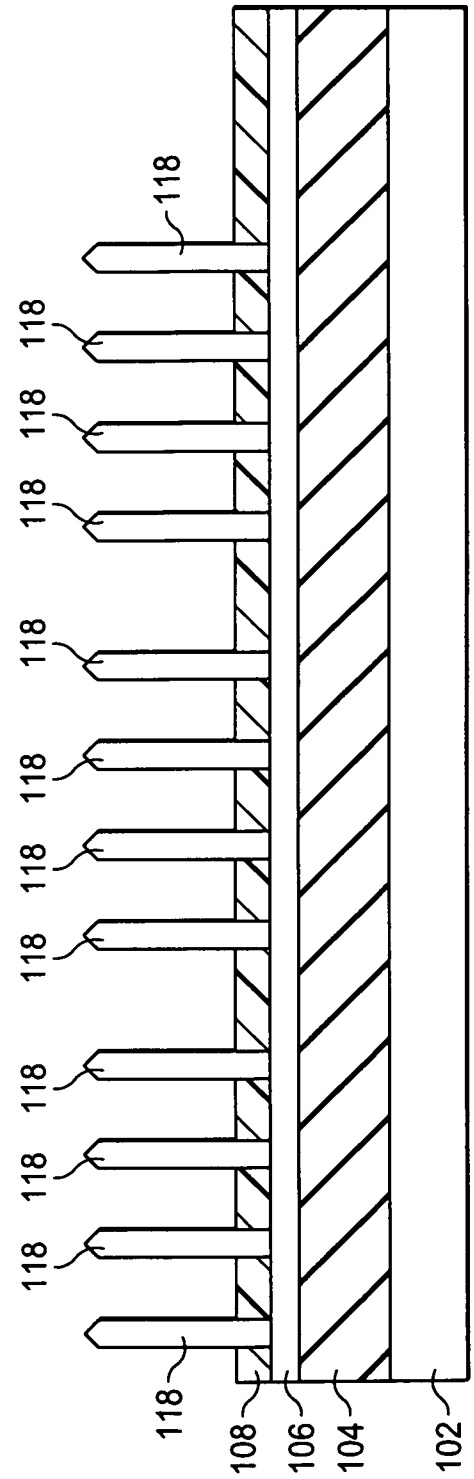
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FIG. 5

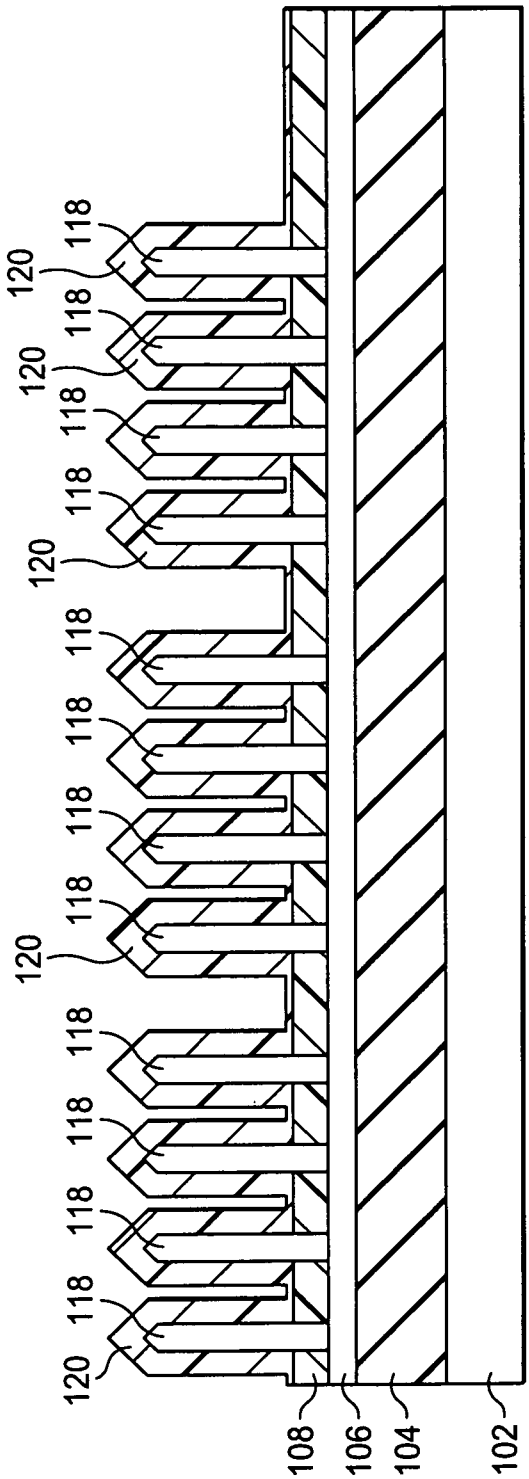
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FIG. 6

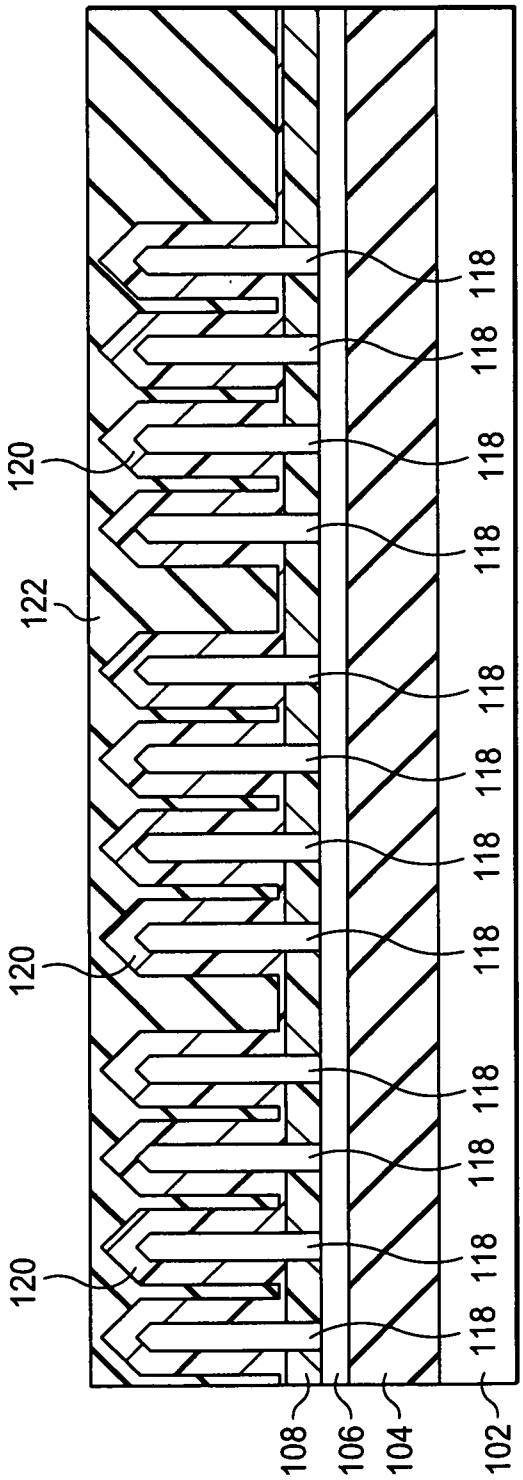
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FIG. 7

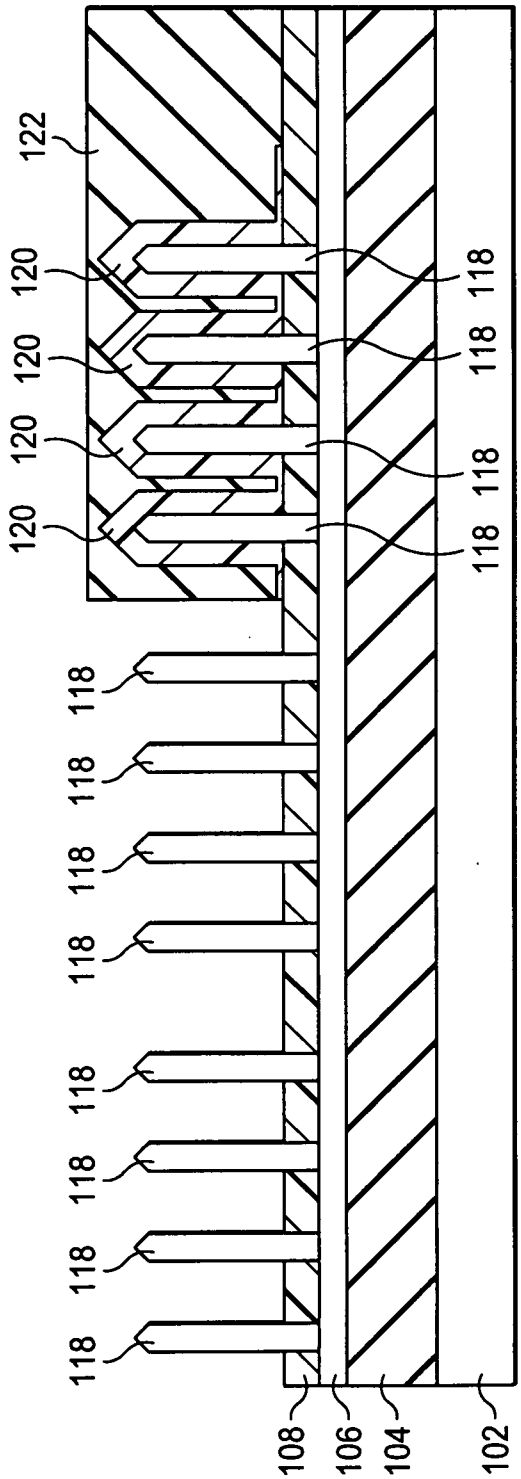
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FIG. 8

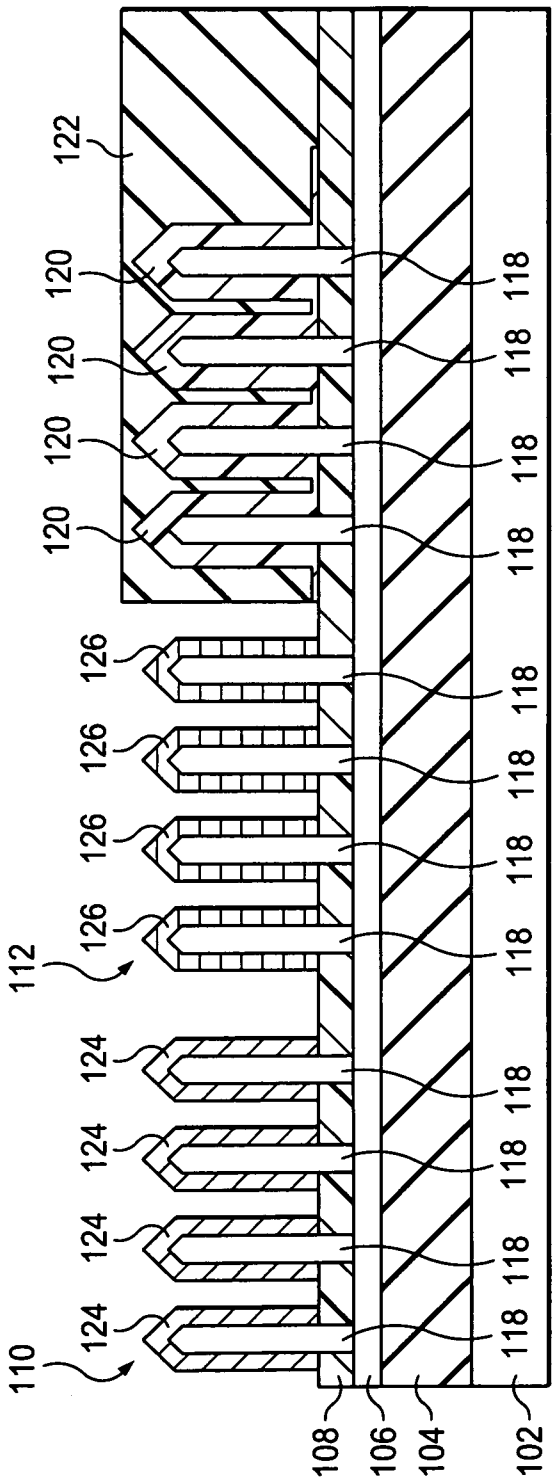
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FIG. 9

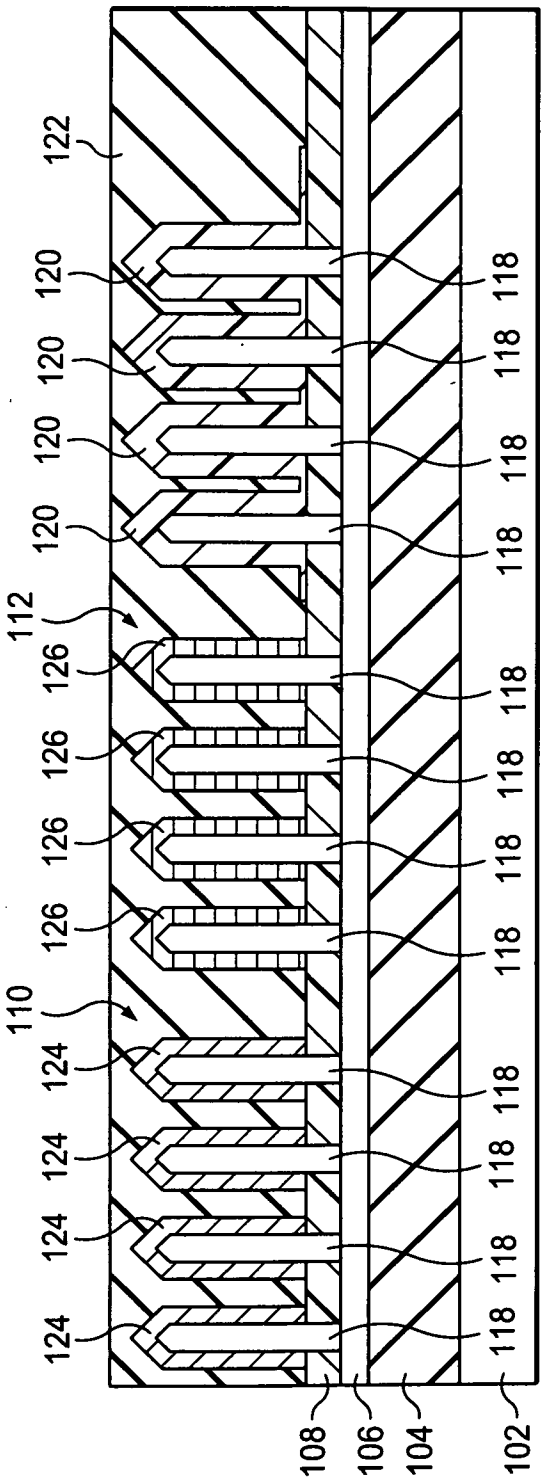
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FIG. 10

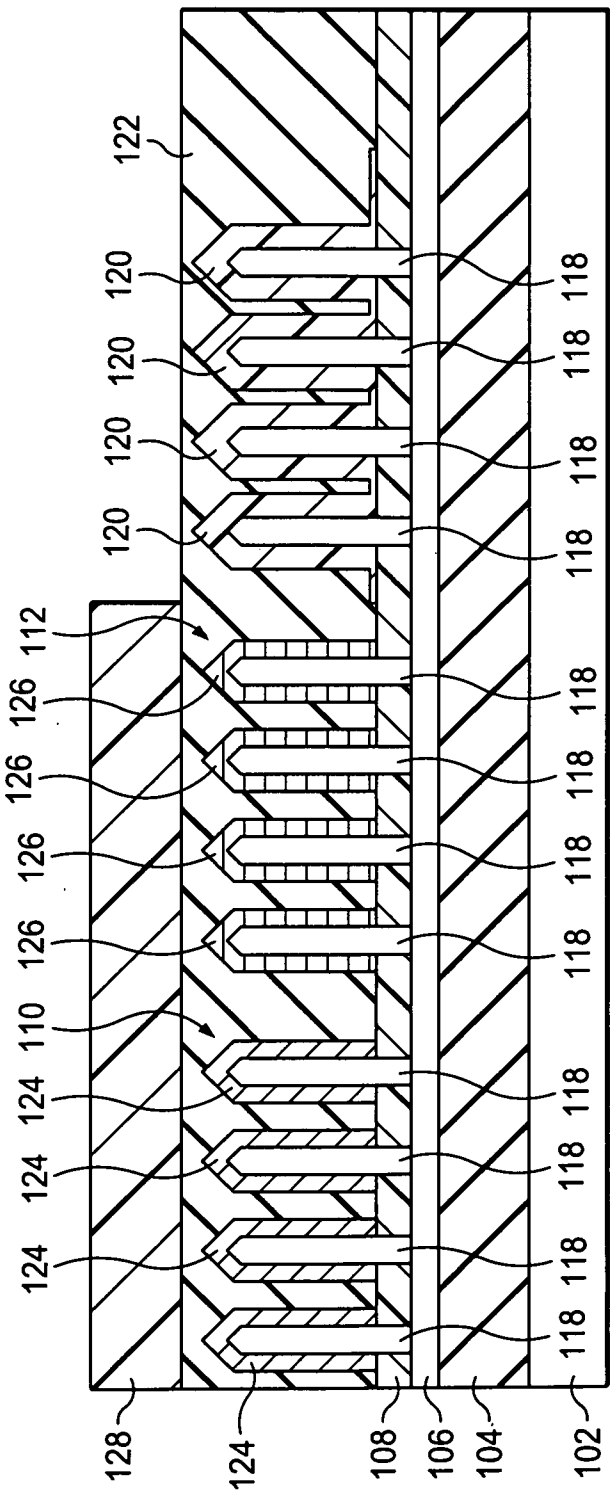
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FIG. 11

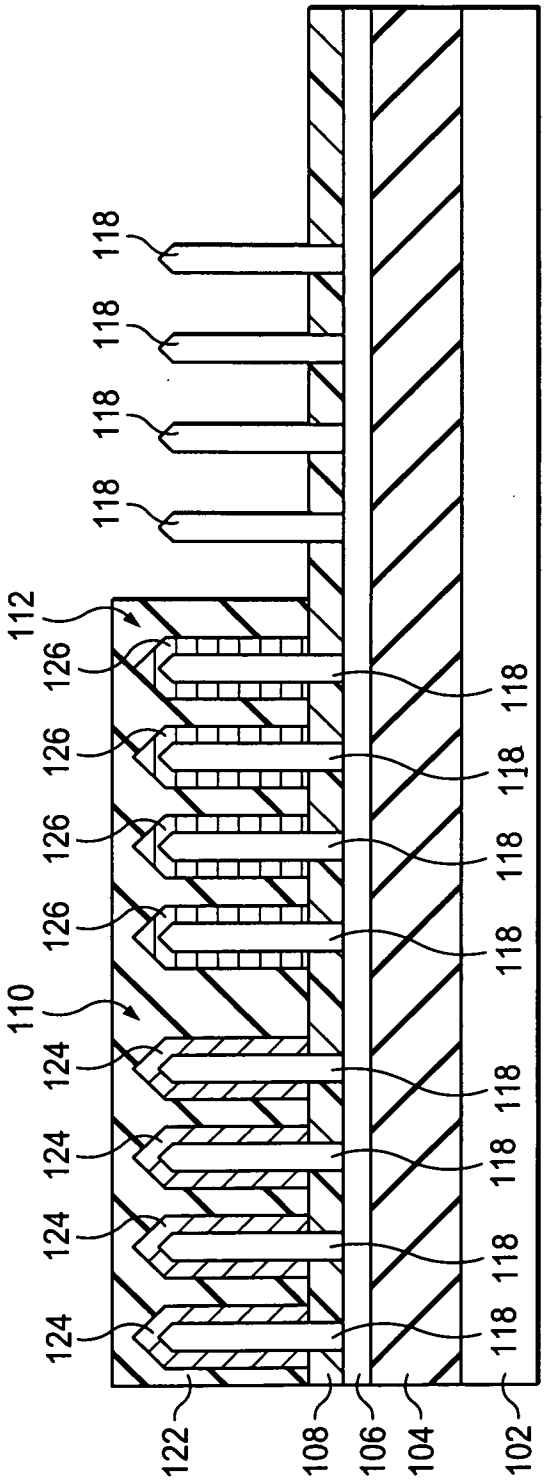
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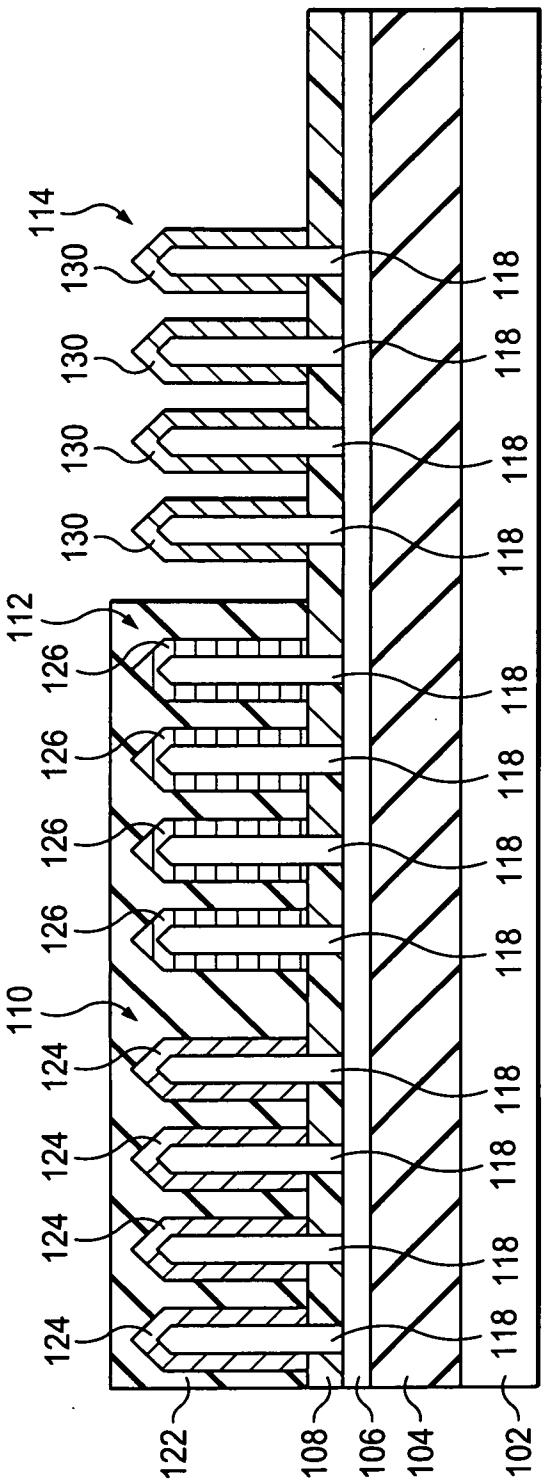
FIG. 12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102

FIG. 13

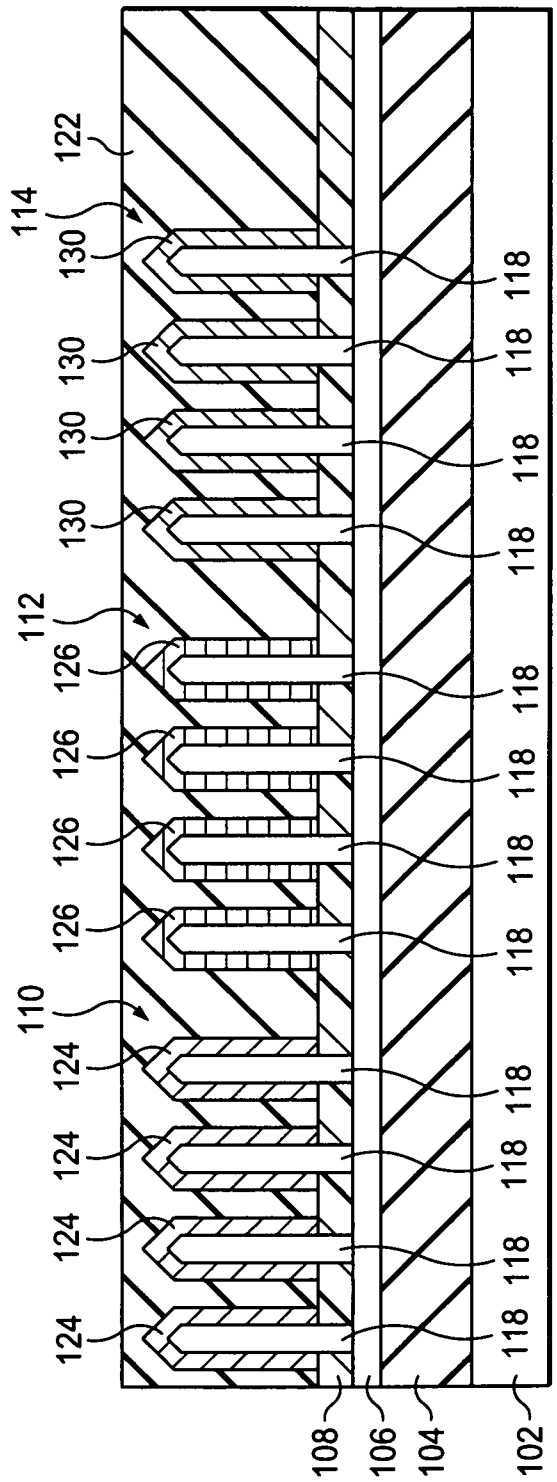
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FIG. 14

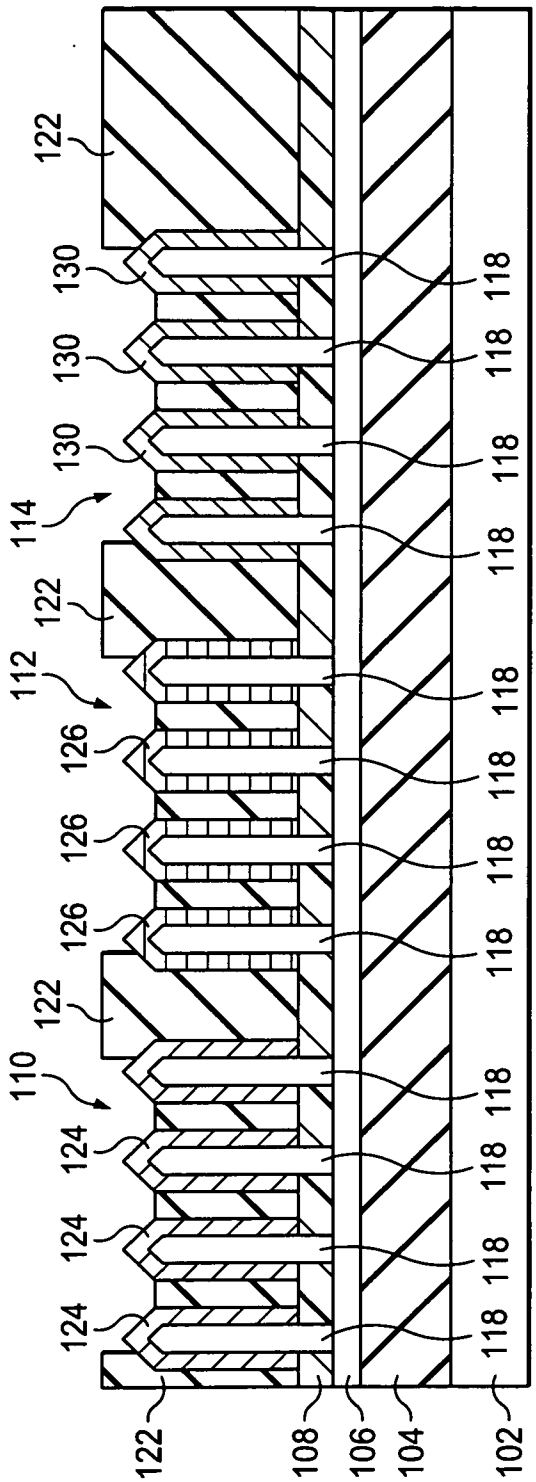
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FIG. 15

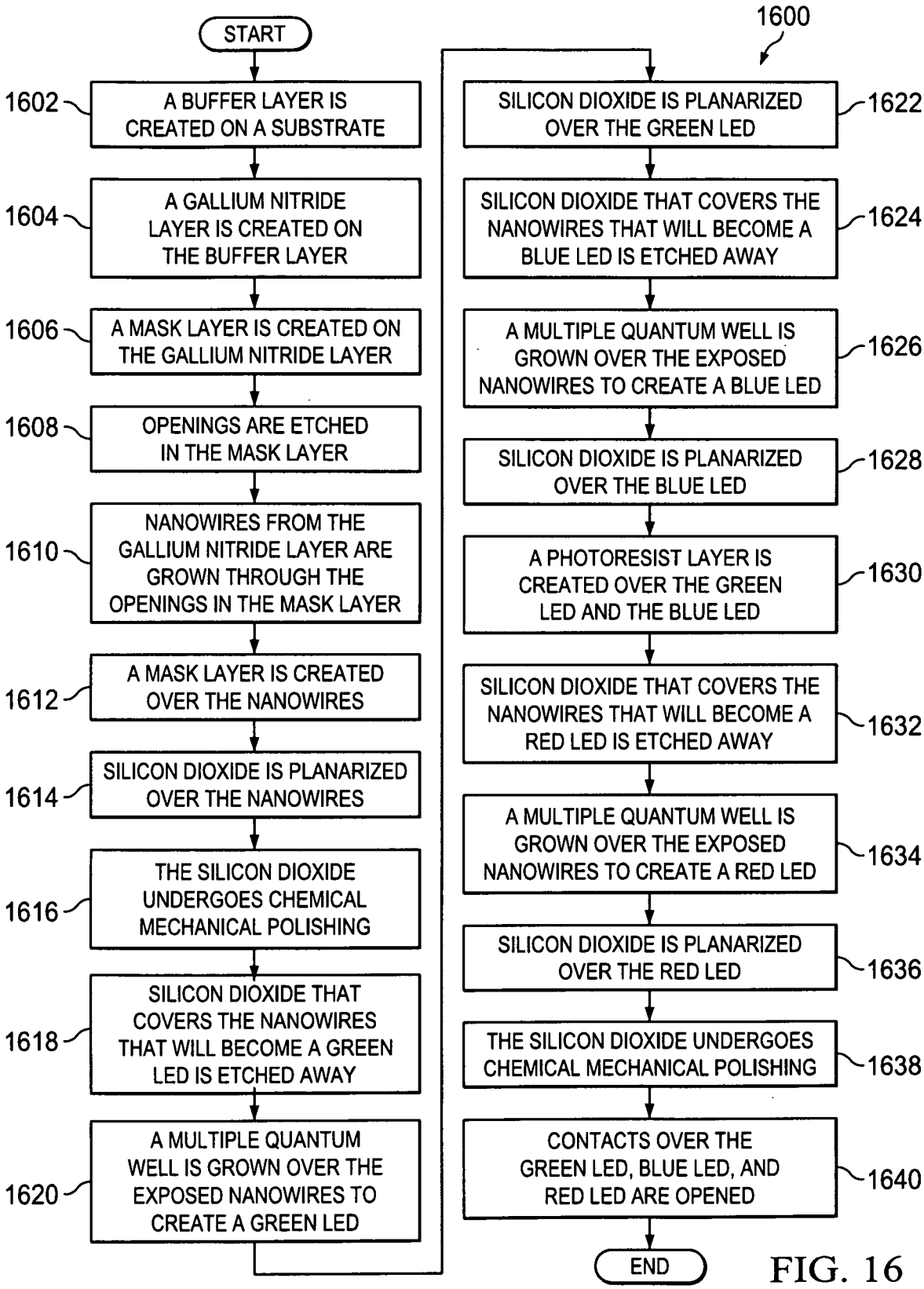

1600
START
1602
A BUFFER LAYER IS CREATED ON A SUBSTRATE
1604
A GALLIUM NITRIDE LAYER IS CREATED ON THE BUFFER LAYER
1606
A MASK LAYER IS CREATED ON THE GALLIUM NITRIDE LAYER
1608
OPENINGS ARE ETCHED IN THE MASK LAYER
1610
NANOWIRES FROM THE GALLIUM NITRIDE LAYER ARE GROWN THROUGH THE OPENINGS IN THE MASK LAYER
1612
A MASK LAYER IS CREATED OVER THE NANOWIRES
1614
SILICON DIOXIDE IS PLANARIZED OVER THE NANOWIRES
1616
THE SILICON DIOXIDE UNDERGOES CHEMICAL MECHANICAL POLISHING
1618
SILICON DIOXIDE THAT COVERS THE NANOWIRES THAT WILL BECOME A GREEN LED IS ETCHED AWAY
1620
A MULTIPLE QUANTUM WELL IS GROWN OVER THE EXPOSED NANOWIRES TO CREATE A GREEN LED
1622
SILICON DIOXIDE IS PLANARIZED OVER THE GREEN LED
1624
SILICON DIOXIDE THAT COVERS THE NANOWIRES THAT WILL BECOME A BLUE LED IS ETCHED AWAY
1626
A MULTIPLE QUANTUM WELL IS GROWN OVER THE EXPOSED NANOWIRES TO CREATE A BLUE LED
1628
SILICON DIOXIDE IS PLANARIZED OVER THE BLUE LED
1630
A PHOTORESIST LAYER IS CREATED OVER THE GREEN LED AND THE BLUE LED
1632
SILICON DIOXIDE THAT COVERS THE NANOWIRES THAT WILL BECOME A RED LED IS ETCHED AWAY
1634
A MULTIPLE QUANTUM WELL IS GROWN OVER THE EXPOSED NANOWIRES TO CREATE A RED LED
1636
SILICON DIOXIDE IS PLANARIZED OVER THE RED LED
1638
THE SILICON DIOXIDE UNDERGOES CHEMICAL MECHANICAL POLISHING
1640
CONTACTS OVER THE GREEN LED, BLUE LED, AND RED LED ARE OPENED
END

FIG. 16

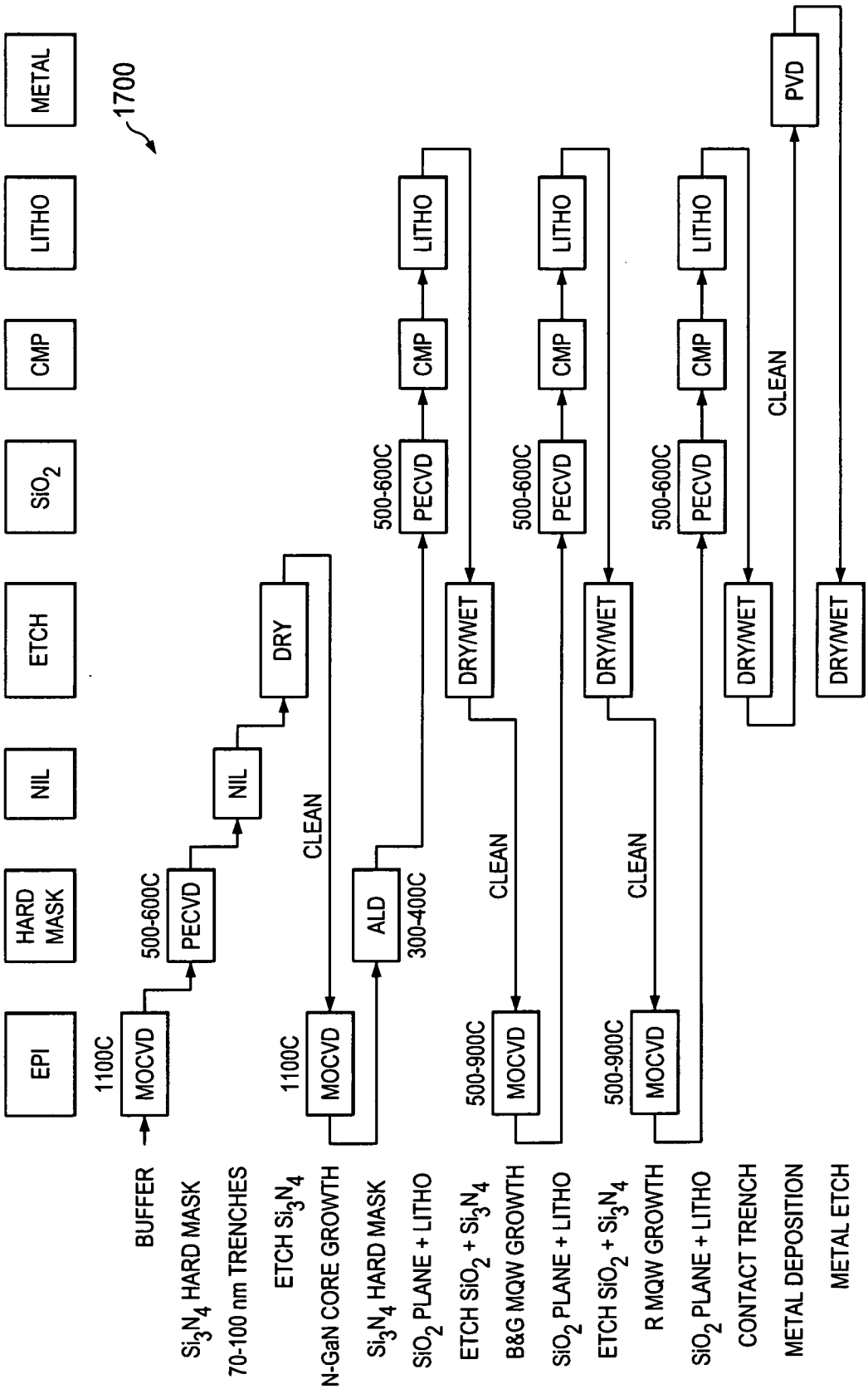
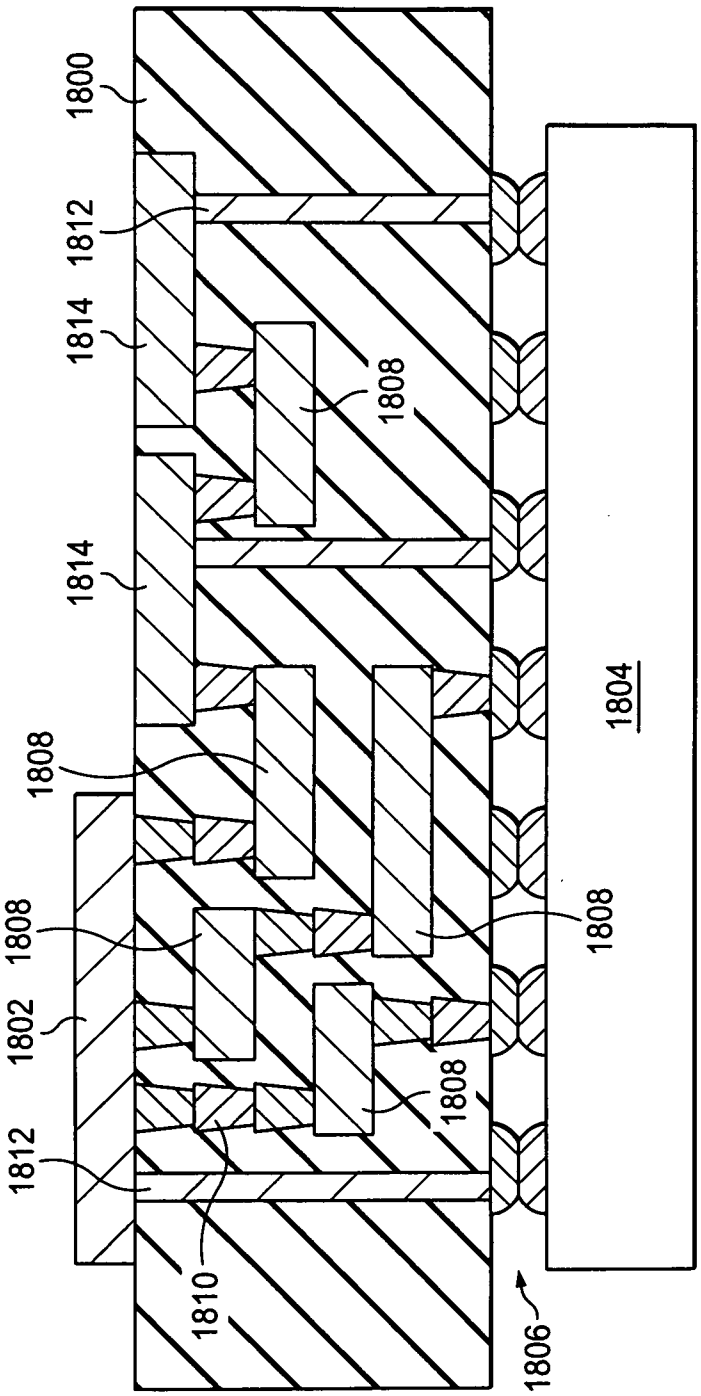

EPI
HARD MASK
NIL
ETCH
SiO_2
CMP
LITHO
METAL
1700
BUFFER
1100C MOCVD
Si_3N_4 HARD MASK
500-600C PECVD
70-100 nm TRENCHES
NIL
ETCH Si_3N_4
DRY
CLEAN
N-GaN CORE GROWTH
1100C MOCVD
Si_3N_4 HARD MASK
ALD 300-400C
SiO_2 PLANE + LITHO
500-600C PECVD
CMP
LITHO
ETCH SiO_2 + Si_3N_4
DRY/WET
CLEAN
B&G MQW GROWTH
500-900C MOCVD
SiO_2 PLANE + LITHO
500-600C PECVD
CMP
LITHO
ETCH SiO_2 + Si_3N_4
DRY/WET
CLEAN
R MQW GROWTH
500-900C MOCVD
SiO_2 PLANE + LITHO
500-600C PECVD
CMP
LITHO
CONTACT TRENCH
DRY/WET
CLEAN
METAL DEPOSITION
PVD
METAL ETCH
DRY/WET

FIG. 17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1812
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1808
1814
1808
1808
1802
1812
1810
1808
1808
1804
1806

FIG. 18

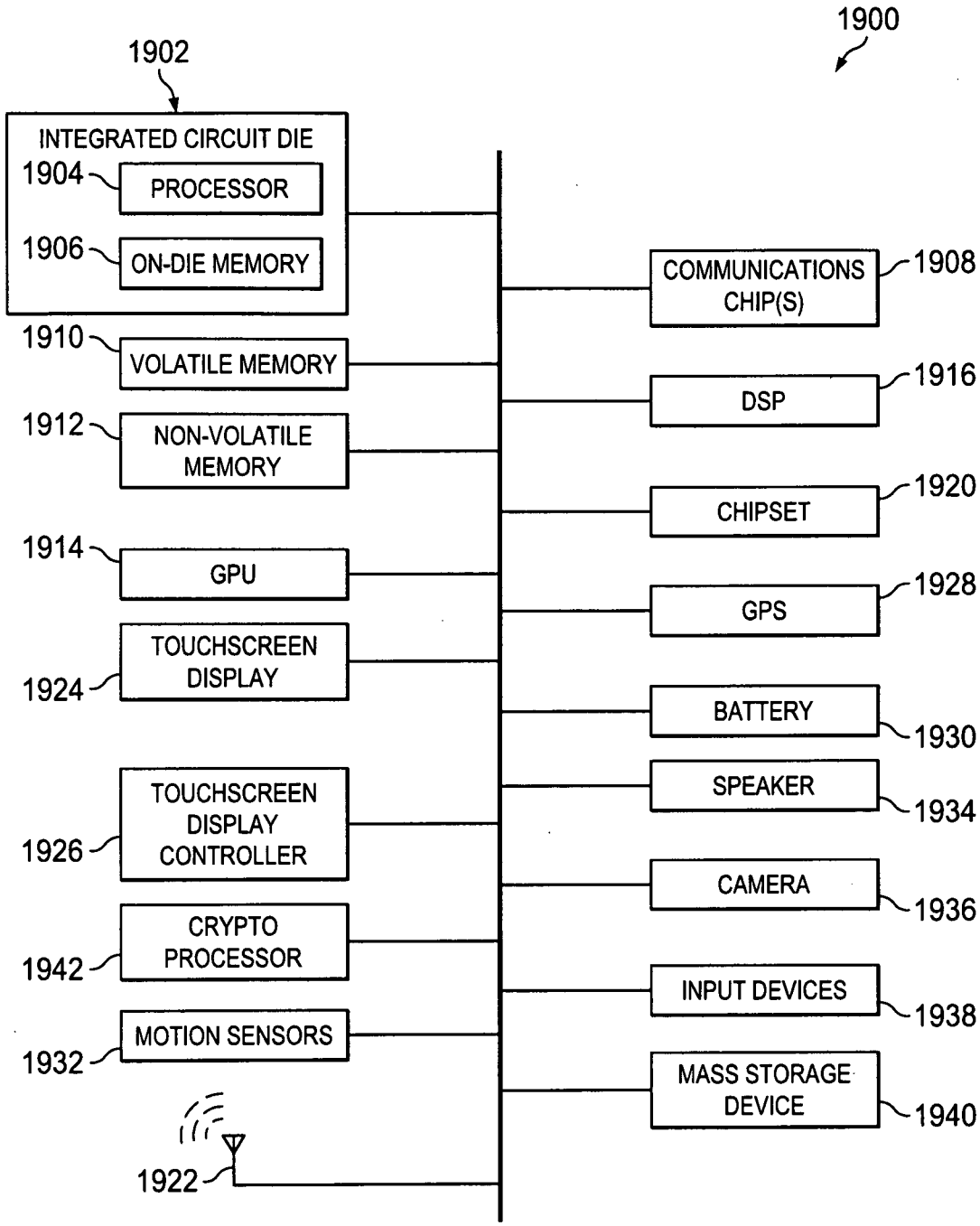
1900
1902
INTEGRATED CIRCUIT DIE
1904
PROCESSOR
1906
ON-DIE MEMORY
1910
VOLATILE MEMORY
1912
NON-VOLATILE MEMORY
1914
GPU
TOUCHSCREEN DISPLAY
1924
TOUCHSCREEN DISPLAY CONTROLLER
1926
CRYPTO PROCESSOR
1942
MOTION SENSORS
1932
1922
COMMUNICATIONS CHIP(S)
1908
DSP
1916
CHIPSET
1920
GPS
1928
BATTERY
1930
SPEAKER
1934
CAMERA
1936
INPUT DEVICES
1938
MASS STORAGE DEVICE
1940

FIG. 19

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000385

A. CLASSIFICATION OF SUBJECT MATTER

H01L 33/02(2010.01)i, H01L 33/12(2010.01)i, H01L 33/32(2010.01)i, H05B 37/00(2006.01)i, H05B 33/14(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 33/02; H01L 33/20; H01L 33/24; H01L 33/00; H01L 33/04; H01L 33/08; H01L 33/14; H01L 33/06; H01L 33/16; H01L 33/12; H01L 33/32; H05B 37/00; H05B 33/14

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: nanorod, active, display, panel, processor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0223289 A1 (SHANG-JR GWO et al.) 06 September 2012 See paragraphs 33, 47, 72-88, claims 1-14 and figure 7a.	1-25
Y	KR 10-2014-0096980 A (SAMSUNG ELECTRONICS CO., LTD.) 06 August 2014 See paragraphs 29-30, 50-56, 184, claims 1-10 and figures 1a-1e.	1-13,16-19,22-25
Y	US 2015-0187991 A1 (LUXVUE TECHNOLOGY CORPORATION) 02 July 2015 See paragraphs 75, 139-159 and claim 1.	14-25
A	KR 10-2012-0028104 A (SAMSUNG LED CO., LTD.) 22 March 2012 See paragraphs 27-38, claims 1-6 and figure 1.	1-25
A	US 2015-0221814 A1 (GLO AB.) 06 August 2015 See paragraphs 11-16, claims 1-10 and figures 1A-1B.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 September 2016 (22.09.2016)	**22 September 2016 (22.09.2016)**

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Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/000385

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