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(54) Title: PRINTED ASSEMBLIES OF ULTRATHIN, MICROSCALE INORGANIC LIGHT EMITTING DIODES FOR DEFORMABLE AND SEMITRANSPARENT DISPLAYS

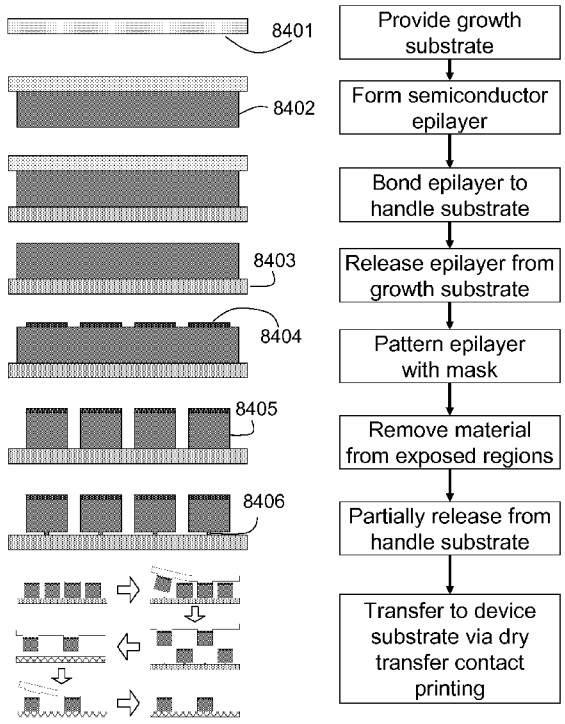


Figure 84

(57) Abstract: Described herein are printable structures and methods for making, assembling and arranging electronic devices. A number of the methods described herein are useful for assembling electronic devices where one or more device components are embedded in a polymer which is patterned during the embedding process with trenches for electrical interconnects between device components. Some methods described herein are useful for assembling electronic devices by printing methods, such as by dry transfer contact printing methods. Also described herein are GaN light emitting diodes and methods for making and arranging GaN light emitting diodes, for example for display or lighting systems.

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PRINTED ASSEMBLIES OF ULTRATHIN, MICROSCALE INORGANIC LIGHT EMITTING DIODES FOR DEFORMABLE AND SEMITRANSPARENT DISPLAYS

CROSS-REFERENCE TO RELATED APPLICATIONS

[001] This application claims the benefit of and priority to U.S. Provisional Applications 61/177,458 filed on May 12, 2009 and 61/241,465 filed on September 11, 2009 which are hereby incorporated by reference in their entireties.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[002] This invention was made with United States governmental support under Award Nos. DE-FG02-07ER46471 and DE-FG02-07ER46453 awarded by the U.S. Department of Energy and Award No. DMI-0328162 awarded by the National Science Foundation. The U.S. government has certain rights in the invention.

BACKGROUND OF INVENTION

[003] This invention is in the field of printable electronics. This invention relates generally to methods for making and assembling electronic devices and printable electronic devices.

[004] A variety of platforms are available for printing structures on device substrates and device components supported by device substrates, including nanostructures, microstructures, flexible electronics, and a variety of other patterned structures. For example, a number of patents and patent applications describe different methods and systems for making and printing a wide range of structures, including U.S. Patent Nos. 7,195,733, 7,557,367, 7,622,367 and 7,521,292, U.S. Patent Application Publication Nos. 2009/0199960, 2007/0032089, 2008/0108171, 2008/0157235, 2010/0059863, 2010/0052112 and 2010/0002402, and U.S. Patent Application Nos. 11/145,574 (filed 06/02/2005) and 11/981,380 (filed 10/31/2007); all of which are hereby incorporated by reference in their entireties to the extent not inconsistent herewith.

SUMMARY OF THE INVENTION

[005] Provided herein are methods for making electronic devices including flexible devices and arrays of light emitting diodes (LEDs). Methods are also provided for

assembling electronic devices including simultaneously embedding device components into a polymer and molding of the polymer with recessed features.

[006] In one aspect, provided herein are methods for making electronic devices. A method of this aspect comprises the steps of: providing a growth substrate having a receiving surface; forming a semiconductor epilayer on the receiving surface via epitaxial growth; the semiconductor epilayer having a first contact surface; bonding the first contact surface of the semiconductor epilayer to a handle substrate; releasing the semiconductor epilayer from the growth substrate wherein the semiconductor epilayer remains bonded to the handle substrate, thereby exposing a second contact surface of the semiconductor epilayer; patterning the second contact surface of the semiconductor epilayer with a mask, thereby generating exposed regions and one or more masked regions of the second contact surface; removing semiconductor material from the exposed regions by etching the exposed regions, thereby generating one or more semiconductor structures supported by the handle substrate; at least partially releasing the one or more semiconductor structures from the handle substrate; and transferring at least one of the one or more semiconductor structures from the handle substrate to a device substrate via dry transfer contact printing, thereby assembling the semiconductor structures on the device substrate to make the electronic device.

[007] For certain embodiments, the growth substrate is lattice matched to the semiconductor epilayer, for example to within ±3.4% or ±1.9%. In certain embodiments, the growth substrate is lattice matched to the semiconductor epilayer to within ±13.8%. Lattice matched growth substrate and epilayers are useful, for example, for growing high quality single crystalline layers via epitaxial growth. In embodiments, useful semiconductor epilayers include, but are not limited to a GaN layer, an InGaN layer, a GaAsN layer, an AlGaN layer, an AlGaAsN layer, a GaAs layer, an InGaAs layer, an AlGaAs layer, an AlGaAsP layer, a GaAsSbN layer and an InN layer. Useful growth substrates include, but are not limited to, sapphire, silicon having a (111) orientation, SiC, ZnO, Si(100), $MGAl_2O_4$ (100), $MgAl_2O_4$ (111), A-plane sapphire, M-plane sapphire, AlN, MnO, ZrB_2, $LiGaO_2$, $(La,Sr)(Al,Ta)O_3$, $LaAlO_3$, $LaTaO_3$, $SrAlO_3$ $SrTaO_3$, $LiAlO_2$, GaAs and InP.

[008] Useful semiconductor epilayers include those having thicknesses selected from the range of 5 nm to 20 μm or 1 μm to 5 μm. In some embodiments, the semiconductor epilayer is a multilayer. Useful multilayers include those comprising layers of semiconductors having different compositions, different doping levels, different dopants or any combination of these. In one embodiment of this aspect, a multilayer comprises at least one p-type semiconductor layer in electrical communication with at least one n-type semiconductor layer. In one embodiment, the multilayer comprises a plurality of light emitting diode (LED) device layers. Useful LED device layers include contact layers, spreader layers, cladding layers and barrier layers.

[009] In one embodiment, the semiconductor epilayer comprises GaN and optionally a GaN multilayer. Useful GaN layers include those having different doping levels, different dopants, different thicknesses or both. For example, in one embodiment, a GaN multilayer comprises at least one p-type GaN layer in electrical communication with at least one n-type GaN layer. In an embodiment, a GaN multilayer comprises material including GaN, InGaN, AlGaN, GaN:Mg, GaN:Si, GaN:AlN, GaN:ZnO or any combination of these.

[010] In a specific embodiment, the handle substrate comprises silicon and the step of bonding the first contact surface of the semiconductor epilayer to the handle substrate comprises contacting the first contact surface to an external surface of the handle substrate so as to establish Van der Waals bonding between the semiconductor epilayer and the handle substrate. Useful handle substrates include those comprising an adhesion layer. Useful adhesion layers include, but are not limited to, those comprising Au, Al, Pd, In, Ni and polymers such as polyurethanes, photoresists, polyimide, silicones and any combination of these.

[011] In certain embodiments, a sacrificial layer is provided between the growth substrate and the semiconductor epilayer. For these embodiments, the step of partially releasing the semiconductor epilayer optionally comprises at least partially removing the sacrificial layer, for example by etching or dissolving the sacrificial layer. Useful etching processes include electrochemical and photoelectrochemical etching processes. Useful sacrificial layers include, but are not limited to InGaN, SiO_2, AlAs, Si_3N_4, ZnO, AlN, HfN, AlInN and any combination of these.

[012] In one embodiment, the semiconductor epilayer and the growth substrate meet at an interface and the step of releasing the semiconductor layer from the growth substrate comprises exposing the interface to electromagnetic radiation. In an embodiment, the electromagnetic radiation is passed through the growth substrate. Optionally, the electromagnetic radiation comprises laser radiation. Useful electromagnetic radiation comprises electromagnetic radiation having a wavelength selected over the range of 100 to 800 nm, a fluence selected over the range of 400 to 600 mJ/cm^2 and any combination thereof. Specific examples of electromagnetic radiation include, but are not limited to: KrF pulsed excimer laser at 248 nm, 38 ns pulse time at 600 mJ/cm^2, for epilayers grown on sapphire; third harmonic of pulsed Q-switched Nd:YAG laser at 355 nm, 5 ns pulse time at 400 mJ/cm^2, for epilayers grown on sapphire; pulsed second harmonic Nd:YAG at 532 nm, 10 ns pulse time at energy greater than $12mJ/cm^2$, for epilayers grown on sapphire. In a further embodiment of this aspect, an absorbing layer is provided at the interface between the growth substrate and the semiconductor epilayer and the electromagnetic radiation is at least partially absorbed by the absorbing layer to release the semiconductor epilayer.

[013] In one embodiment, the mask provided on the second contact surface of the epilayer includes a first mask layer comprising Si_3N_4. Optionally the mask includes a second mask comprising a metal provided over the first mask layer. Useful mask layers further include those comprising a dielectric, such as Si_3N_4 and SiO_2; a metal, such as Al, Au and Cu; and any combination of these.

[014] In embodiments, the step of removing material from exposed regions of the masked semiconductor epilayer comprises etching the exposed regions. Useful etching processes include reactive ion etching, deep reactive ion etching and inductive coupled plasma reactive ion etching. In some embodiments, removing material from exposed regions of the masked semiconductor epilayer exposes side-walls of the remaining semiconductor structure. In certain embodiments, an etch block layer, a mask layer or both is deposited on at least a portion of the exposed side-walls, for example to protect the side walls from being etched during a subsequent releasing step.

[015] In some embodiments, partially releasing semiconductor epilayers from a handle substrate results in semiconductor structures anchored to the handle substrate, for example by at least one homogenous anchor or at least one heterogeneous anchor. In other embodiments, one method further comprises a step of anchoring a semiconductor structure to handle substrate, for example by at least one homogeneous anchor or at least one heterogeneous anchor.

[016] In embodiments, the step of transferring comprises a dry transfer contact printing method, for example as known in the art. A specific dry transfer contact printing technique useful for the methods described herein comprises transferring at least one semiconductor structure from a handle substrate to a device substrate via contact printing using a conformal transfer device, such as a PDMS stamp.

[017] Useful device substrates include, but are not limited to, glass substrates, polymer substrates, flexible substrates, large area substrates, pre-metalized substrates, substrates pre-patterned with one or more device components, and any combination of these.

[018] Another method of this aspect comprises the steps of: providing a growth substrate having a receiving surface; forming a semiconductor epilayer on the receiving surface via epitaxial growth; said semiconductor epilayer having a first contact surface; bonding the first contact surface of the semiconductor epilayer to a handle substrate; releasing the semiconductor epilayer from the growth substrate, wherein at least a portion of the semiconductor epilayer remains bonded to the handle substrate, thereby exposing a second contact surface of the semiconductor epilayer; processing the semiconductor epilayer on the handle substrate, thereby generating one or more semiconductor structures supported by said handle substrate; transferring at least one of the one or more semiconductor structures from the handle substrate to a device substrate via dry transfer contact printing, thereby assembling said semiconductor structures on said device substrate to make said electronic device.

[019] Another method of this aspect comprises the steps of: providing a first growth substrate having a first receiving surface; forming a first semiconductor epilayer on the first receiving surface via epitaxial growth; the first semiconductor

epilayer having a first contact surface; bonding the first contact surface of the first semiconductor epilayer to a handle substrate; releasing the first semiconductor epilayer from the first growth substrate, wherein at least a portion of the first semiconductor epilayer remains bonded to the handle substrate, thereby exposing a second contact surface of the first semiconductor epilayer; providing a second growth substrate having a second receiving surface; forming a second semiconductor epilayer on the second receiving surface via epitaxial growth; the second semiconductor epilayer having a third contact surface; bonding the third contact surface of the second semiconductor epilayer to the handle substrate, the first semiconductor epilayer or both; releasing the second semiconductor epilayer from the second growth substrate, the first semiconductor epilayer or both, wherein at least a portion of the second semiconductor epilayer remains bonded to the handle substrate, the first semiconductor epilayer or both, thereby exposing a fourth contact surface of the second semiconductor epilayer; processing the first semiconductor epilayer, the second semiconductor epilayer or both the first and the second semiconductor epilayers on the handle substrate, thereby generating one or more semiconductor structures supported by the handle substrate; transferring at least one of the one or more semiconductor structures from the handle substrate to a device substrate via dry transfer contact printing, thereby assembling the semiconductor structures on the device substrate to make the electronic device. In a specific embodiment, the step of bonding the third contact surface of the second semiconductor epilayer to the handle substrate, the first semiconductor epilayer or both comprises bonding at least a portion of the third contact surface of the second semiconductor epilayer to the second contact surface of the first semiconductor epilayer.

[020] Certain embodiments further comprise a step of processing a semiconductor epilayer on a growth substrate, for example processing a first semiconductor epilayer on a first growth substrate, a second semiconductor epilayer on a second growth substrate or processing both a first semiconductor epilayer on a first growth substrate and a second semiconductor epilayer on a second growth substrate. In embodiments, the step of processing a semiconductor epilayer on a handle substrate or a growth substrate comprises a processing method including, but not limited to, a patterning process, a lithography process, a growth process, a polishing

process, a deposition process, an implantation process, an etching process, an annealing process, a molding process, a curing process, a coating process, exposure to electromagnetic radiation or any combination of these. In specific embodiments, the step of processing a semiconductor epilayer on a handle substrate comprises forming one or more ohmic contacts on a semiconductor epilayer, forming one or more thermal management structures on a semiconductor epilayer or forming one or more ohmic contacts and forming one or more thermal management structures.

[021] In certain embodiments, the handle substrate comprises a material including, but not limited to: a doped or undoped semiconductor; a single crystal material; a polycrystalline material; a ceramic such as SiC, Si_3N_4, fused silica, alumina (Al_2O_3), ZrO_2, MgO, pyrolytic Boron nitride (PBN), aluminum nitride, aluminum silicate and titania; a polymer; glass; quartz; a semiconductor with or without a thermal oxide layer; and any combination of these. Useful handle substrates also include substrates having an adlayer or substrates coated by or deposited with a film of any of the above materials or other materials including but not limited to a polymer, a sol-gel, a polymer precursor, an incompletely cured sol-gel. Use of certain materials for the handle substrate can be advantageous as subsequent processing of devices or device components on the handle substrate can also cure, anneal or otherwise process the materials of or coated on the handle wafer. For example when the processing includes a high temperature step a handle substrate including a film comprising a thermally curable polymer or an uncured or incompletely cured sol-gel can be cured. In certain embodiments, the composition of a handle substrate is driven by the requirements for subsequent processing of device elements on the handle substrate. For example, in embodiments when processing on the handle substrate includes high temperature processing (e.g., annealing or ohmic contact formation processes), the handle substrate is selected so as to be compatible with the associated high temperatures (e.g., ceramics, semiconductors). In embodiments when processing on the handle substrate includes exposure to reactive chemicals (e.g., acids, bases, chemical etchants), the handle substrate is selected so as to be compatible with the exposure conditions (e.g., chemically inert).

[022] Methods of this aspect are useful, for example for making an array of LEDs. A specific method for making an array of LEDs comprises the steps of: providing a sapphire growth substrate having a receiving surface; forming a GaN epilayer on the receiving surface via epitaxial growth; wherein the GaN epilayer is a multilayer comprises at least one p-type GaN semiconductor layer in electrical communication with at least one n-type GaN semiconductor layer; the GaN multilayer having a first contact surface; bonding the first contact surface of the GaN multilayer to a handle substrate; releasing the GaN multilayer from the sapphire growth substrate wherein the GaN multilayer remains bonded to the handle substrate, thereby exposing a second contact surface of the GaN multilayer; patterning the second contact surface of the GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of the second contact surface; removing material from the exposed regions by etching the exposed regions, thereby generating one or more LED device structures supported by the handle substrate; at least partially releasing the one or more LED device structures from the handle substrate; and transferring at least a portion of the one or more LED device structures from the handle substrate to a device substrate via dry transfer contact printing, thereby making an array of LEDs.

[023] Another specific method for making an array of LEDs comprises the steps of: providing a silicon growth substrate having a (111) orientation and having a receiving surface; generating a GaN multilayer on the receiving surface of the growth substrate via epitaxial growth; the GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one p-type GaN layer; the GaN multilayer having a contact surface; patterning the contact surface of the GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of the GaN multilayer; removing material from the exposed regions by etching the exposed regions and into the silicon growth substrate, thereby exposing a portion of the silicon growth substrate and generating one or more LED device structures; at least partially releasing the one or more LED device structures from the growth substrate by anisotropic etching the exposed portion of the silicon growth substrate; and transferring at least a portion of the one or more LED device structures from the silicon growth substrate to a device substrate via dry transfer contact printing, thereby making the array of LEDs.

[024] For certain embodiments of methods for making an array of LEDs, the step of removing material etches a depth into the growth or host substrate greater than or equal to 5 nm, or selected over the range of 5 nm to 10 μm. In embodiments, anisotropic etching of a silicon (111) substrate occurs preferentially along <110> directions. Useful anisotropic etching methods include directional wet etching using an anisotropic etchant such as KOH or tetramethylammonium hydroxide (TMAH).

[025] Another specific method for making an array of LEDs comprises the steps of: providing a sapphire growth substrate having a receiving surface; providing a sacrificial layer on the receiving surface of the sapphire growth substrate; generating a GaN multilayer on the sacrificial layer via epitaxial growth; the GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one n-type GaN layer; the GaN multilayer having a contact surface; patterning the contact surface of the GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of the GaN multilayer; removing material from the exposed regions by etching the exposed regions, thereby exposing a portion of the sacrificial layer and generating one or more LED device structures; at least partially releasing the one or more LED device structures from the growth substrate by removing at least a portion of the sacrificial layer using directional etching, electrochemical etching or photoelectrochemical etching; and transferring at least a portion of the one or more LED device structures from the sapphire growth substrate to a device substrate via dry transfer contact printing, thereby making the array of LEDs.

[026] Useful sacrificial layers include InGaN, SiO_2, AlAs, Si_3N_4, ZnO, AlN, HfN, AlInN and any combination of these. In some embodiments, a buffer layer or an etch block layer is provided between the growth substrate and the sacrificial layer, for example a buffer layer or an etch block layer comprising GaN. Buffer layers and etch block layers are useful, for example, to prevent etching of a GaN device layer during a subsequent etching or releasing step.

[027] In a specific embodiment, a method of this aspect comprises the steps of: providing a sapphire growth substrate having a receiving surface; providing a sacrificial layer on the receiving surface of said sapphire growth substrate; providing an etch block layer on the sacrificial layer, for example via epitaxial growth;

generating a GaN multilayer on the etch block layer via epitaxial growth; patterning the contact surface of the GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of the GaN multilayer; removing material from the exposed regions by etching the exposed regions, thereby exposing a portion of the sacrificial layer and generating one or more LED device structures; at least partially releasing said one or more LED device structures from said growth substrate by removing at least a portion of the sacrificial layer using directional etching, electrochemical etching or photoelectrochemical etching; and transferring at least a portion of the one or more LED device structures from the sapphire growth substrate to a device substrate via dry transfer contact printing. In an embodiment, a method of this aspect further comprises generating an etch block layer in at least a portion of the exposed regions, for example to prevent further etching of said exposed regions during the step of at least partially releasing.

[028] In some embodiments, a sacrificial layer is removed during the releasing step by exposing the sacrificial layer to a selective etchant, for example HCl, HF, H_3PO_4, KOH, NH_4Cl, chelating amines, 1,2-diaminoethane (DAE), NaOH and any combination of these. For specific embodiments, the releasing step comprises exposing the sacrificial layer to electromagnetic radiation, for example electromagnetic radiation having wavelengths selected over the range of 100 nm to 800 nm or electromagnetic radiation from a xenon lamp. In one embodiment, the electromagnetic radiation is first passed through an undoped GaN film before exposing the sacrificial layer, for example to optically filter the electromagnetic radiation to remove at least a portion of the electromagnetic radiation absorbed by the undoped GaN film. For some embodiments, the releasing step comprises providing the sacrificial layer at an electric potential, for example an electric potential 600 mV to 800 mV greater than the potential of a buffer layer, the growth substrate or an etching solution. For some embodiments, the sacrificial layer is simultaneously exposed to an etching solution while it is held at a potential different from the etching solution. For some embodiments, the sacrificial layer is simultaneously exposed to an etching solution while it is held at a potential different from the etching solution and being exposed to electromagnetic radiation. In a specific embodiment, the GaN multilayer is grown on a sacrificial layer comprising ZnO and the step of at least partially releasing comprises etching the sacrificial layer with NH_4Cl etchant.

[029] Another specific method for making an array of LEDs comprises the steps of: providing a sapphire growth substrate having a receiving surface; generating a GaN multilayer on the sapphire growth substrate via epitaxial growth; the GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one n-type GaN layer; the GaN multilayer having a first contact surface, wherein the GaN multilayer and the sapphire growth substrate meet at an interface; bonding the first contact surface of the GaN multilayer to a handle substrate; exposing the interface between the GaN multilayer and the sapphire growth substrate to electromagnetic radiation; releasing the GaN multilayer from the sapphire growth substrate wherein the GaN multilayer remains bonded to the handle substrate, thereby exposing a second contact surface of the GaN multilayer; patterning the second contact surface of the GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of the GaN multilayer; removing material from the exposed regions by etching the exposed region, thereby generating one or more LED device structures; at least partially releasing the one or more LED device structures from the handle substrate; and transferring at least a portion of the one or more LED device structures from the handle substrate to a device substrate via dry transfer contact printing, thereby making the array of LEDs.

[030] In a specific embodiment, the interface is exposed to electromagnetic radiation, optionally laser radiation. Optionally, the electromagnetic radiation is passed through the sapphire growth substrate. In one embodiment, the handle substrate comprises an external metal film and the first contact surface of the GaN multilayer is bonded to the handle substrate when it is contacted to the external metal film. In embodiments where there is an external metal film and the interface is exposed to electromagnetic radiation, the external metal film optionally reflects at least a portion of the electromagnetic radiation, thereby exposing the interface to electromagnetic radiation.

[031] In an exemplary embodiment for making an array of LEDs, the GaN multilayer comprises at least one p-type GaN layer, at least one n-type GaN layer and a quantum well region comprising InGaN positioned between the p-type GaN layer and the n-type GaN layer. Specific methods of this aspect further comprise depositing a metal film on an exposed region of the p-type GaN layer, the n-type

GaN layer or both and optionally annealing the metal film to form an electrical contact on the p-type GaN layer, the n-type GaN layer or both. One method of this aspect comprises the optional step of etching a portion of the GaN multilayer to expose a region of the n-type GaN layer, a region of the p-type GaN layer or both, depositing a metal film on an exposed region of the n-type GaN layer, the p-type GaN layer or both and optionally annealing the metal film to form an electrical contact on the n-type GaN layer, the p-type GaN layer or both.

[032] Embodiments of specific methods of this aspect further comprise the steps of providing one or more metallic contacts in electrical contact with a portion of the one or more LED device structures; coating the one or more LED device structures and one or more metallic contacts with a photosensitive polymer layer; and exposing select portions of the photosensitive polymer layer to electromagnetic radiation, wherein the electromagnetic radiation is at least partially transmitted through the device substrate and wherein the one or more metallic contacts block at least a portion of the electromagnetic radiation from reaching at least a portion of the photosensitive polymer layer, the one or more metallic contacts thereby serving as one or more self-aligned mask elements. An optional step comprises removing portions of the photosensitive polymer layer which are masked by the one or more metallic contacts serving as self-aligned mask elements. Optionally, the step of removing portions of the photosensitive polymer layer which are masked by the one or more metallic contacts serving as self-aligned mask elements comprises developing the photosensitive polymer layer, wherein regions of the photosensitive polymer layer that were not exposed to electromagnetic radiation are dissolved by exposure to a solvent.

[033] In some embodiments, the LED device structures correspond to a vertical type LED. In embodiments, the GaN multilayer comprises a plurality of GaN layers, for example GaN layers including, but not limited to, GaN contact layers, GaN spreader layers, GaN cladding layers, GaN barrier layers, GaN etch block layers, GaN buffer layers and any combination of these.

[034] In embodiments, the mask provided on the GaN multilayer comprises a first layer of Si_3N_4 and an optional metal second layer. Optionally, methods of this aspect comprise removing at least a portion of the mask. In embodiments, the step of

removing material comprises etching exposed regions of a masked GaN multilayer via and etching method such as inductively coupled plasma reactive ion etching, reactive ion etching or deep reactive ion etching. After the removing step and/or the releasing step, some LED device structures optionally are anchored to the handle or growth substrate by at least one homogeneous anchor or at least one heterogeneous anchor. Some embodiments optionally comprise a step of anchoring one or more of the LED device structures by at least one homogeneous anchor or at least one heterogeneous anchor. In some embodiments, the step of at least partially releasing comprises photoelectrochemically or electrochemically etching at least a portion of the GaN multilayer.

[035] In embodiments, the device substrate is a glass substrate, a polymer substrate, a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components or any combination of these. Transfer of the LED device structures to the device substrate is optionally via contact printing using a conformal transfer device, for example a PDMS stamp. In certain methods of this aspect, the device substrate comprises one or more additional LED device structures and the step of transferring at least a portion of the one or more LED device structure comprises printing at least one of the one or more LED device structures on to of the one or more additional LED device structures, for example to make a stacked LED device structure. Another method of this aspect, comprises a step of printing one or more additional LED device structures on top of the one or more LED device structures on the device substrate, for example to make a stacked LED array.

[036] In some embodiments, a stacked LED comprises multiple LEDs stacked one on top of another, each capable of outputting selected wavelengths of electromagnetic radiation, for example each capable of outputting different wavelengths of electromagnetic radiation. In a specific embodiment, a stacked LED comprises multiple LEDs whose total electromagnetic spectrum is visible as white light.

[037] Optionally, multiple LEDs are connected in series, such that identical current flows through each LED. Optionally, multiple LEDs are connected in parallel, such

that each LED experiences identical voltage. Multiple LEDs connected in series provide a benefit of similar output of electromagnetic radiation from each LED.

[038] In some embodiments, an array of LEDs comprises a phosphor or an array of phosphors. A particular method embodiment comprises a step of printing phosphors over at least a portion of an LED array, for example via a contact printing method. Another method embodiment comprises making an array of phosphors, making an array of LEDs and laminating the array of phosphors over the array of LEDs.

[039] In another aspect, provided are methods for making an array of phosphors. One method of this aspect comprises the steps of molding an elastomer layer with an array of recessed regions; providing phosphor particles over the elastomer layer, wherein the phosphor particles at least partially fill in the array of recessed regions; and providing an encapsulation layer over the elastomer layer, wherein the phosphor particles are encapsulated in the array of recessed regions, thereby making an array of phosphors. In exemplary embodiments, the recessed regions have depths selected over the range of 5 nm to 10 μm.

[040] In another aspect, provided are methods for making a semiconductor device. A method of this aspect comprises the steps of providing a transparent substrate; assembling a semiconductor device on a surface of the transparent substrate via dry transfer contact printing; providing one or more metallic contacts in electrical contact with the semiconductor device; coating said semiconductor device and one or more metallic contacts with a photosensitive polymer layer; exposing select portions of the photosensitive polymer layer to electromagnetic radiation, wherein the electromagnetic radiation is at least partially transmitted through the transparent substrate and wherein the one or more metallic contacts block at least a portion of the electromagnetic radiation from reaching at least a portion of the photosensitive polymer layer, the one or more metallic contacts thereby serving as one or more self-aligned mask elements. Certain embodiments further comprises a step of removing portions of the photosensitive polymer layer which are masked by the one or more metallic contacts serving as self-aligned mask elements. In one embodiment, the step of removing portions of the photosensitive polymer layer which are masked comprises developing the photosensitive polymer layer and wherein regions of the

photosensitive polymer layer that were not exposed to the electromagnetic radiation are dissolved by exposure to a solvent.

[041] Useful transparent substrates for methods of this aspect include substrates comprising quartz, glass, sapphire and any combination of these. In certain embodiments, the transparent substrate, the semiconductor device or both transmit at least 50% of the electromagnetic radiation. In some embodiments, at least a portion of the electromagnetic radiation is reflected, absorbed or both by the one or more metallic contacts. In a specific embodiment, at least 50%, at least 75%, or at least 95% of the electromagnetic radiation received by a metallic contacts is reflected, scattered and/or absorbed by the metallic contact. Useful metallic contacts include those comprising gold, copper, nickel, aluminum, platinum and any combination of these. In specific embodiments, each of the metallic contacts has a thickness selected over the range of 5 nm to 10 μm.

[042] In specific embodiments, the photosensitive polymer has a thickness selected over the range of 5 nm to 1 mm. Useful photosensitive polymers include, but are not limited to, negative tone photopolymers, polymers at least partially crosslinked by exposure to electromagnetic radiation, BCB (Benzo Cyclo Butene), WL-5351, SU-8, polyurethanes, silicones and any combination of these.

[043] In another aspect, provided herein are methods for assembling an electronic device. A method of this aspect comprises the steps of: providing one or more electronic device components; contacting the one or more electronic device components with a conformal transfer and molding device, thereby transferring the one or more electronic device components onto the conformal transfer device; contacting a prepolymer layer disposed over a host substrate with the conformal transfer and molding device having the one or more electronic device components positioned thereon, thereby at least partially embedding the one or more electronic device components into the prepolymer layer and patterning the prepolymer layer with one or more recessed features; curing the prepolymer layer, thereby forming a polymer layer having one or more recessed features; and filling at least a portion of the one or more recessed features with a filling material.

[044] Optionally, methods of this aspect further comprise the steps of providing a filling material on a surface of the polymer and dragging or moving a scraping tool along the surface of the polymer to fill the filling material into at least a portion of the one or more recessed features.

[045] Useful filling materials include, but are not limited to, conductive materials, optical materials, heat transfer materials and any combination of these. Useful host substrates include substrates comprising polymer, glass, plastic, semiconductor, sapphire, ceramics and any combination of these. Useful prepolymer layers include, but are not limited to, those layers comprising a photocurable polymer, a thermally curable polymer, a photocurable polyurethane and any combination of these.

[046] Optionally, methods of this aspect comprise a step of curing the prepolymer layer by exposing the prepolymer layer to electromagnetic radiation, heating the prepolymer layer or both. In one embodiment, a method of this aspect further comprises a step of curing the filling material, for example by heating the filling material, exposing the filling material to electromagnetic radiation or both.

[047] In embodiments, at least one of the one or more electronic device components comprises one or more electrode contacts. Optionally, at least a portion of the polymer is etched in a further step to expose at least one of the one or more electrode contacts. In a specific embodiment, the filling material comprises a conductive material, for example in electrical communication with one or more electrode contacts. Conductive filling materials are useful, for example for providing one or more electrical interconnections to at least one of the electronic device components. Useful conductive materials include those materials having a resistivity selected over the range of 1×10^{-10} to 1×10^{-2} $\Omega\cdot$cm or 1×10^{-10} to 1×10^{-5} $\Omega\cdot$cm, for example a conductive past such as epoxies containing metallic particles, such as silver epoxy, gold epoxy, copper epoxy or aluminum epoxy; conductive carbon materials, such as carbon black, carbon nanotubes, graphite or grapheme; and any combination of these.

[048] In a specific embodiment, the filling material comprises an optical material. Optionally, the optical material forms an optical element such as a collecting optic, a concentrating optic, a reflective optic, a diffusing optic, a dispersive optic, a lens, a

phosphor, a waveguide, an optical fiber, an optical coating, a transparent optic, an optical filter, a polarizing optic and any combination of these. Useful optical materials include polymer, plastic, glass and any combination of these.

[049] Useful electronic device components include, but are not limited to, a P-N junction, a thin film transistor, a single junction solar cell, a multi-junction solar cell, a photodiode, a light emitting diode, a laser, a sensor, a photodiode, an electro-optical device, a CMOS device, a MOSFET device, a MESFET device, a photovoltaic cell, a microelectromechanical device, a HEMT device, a light-emitting transistor and any combination of these. In a specific embodiment, the electronic device component has a dimension selected over the range of 10 nm to 10 mm or 10 nm to 10 μm, for example a height, width, diameter, and/or depth. In specific embodiments, the electronic device component has a height selected over the range of 10 nm to 10 μm, a width selected over the range of 1 μm to 10 mm, a depth selected over the range of 1 μm to 10 mm and/or a diameter selected over the range of 1 μm to 10 mm.

[050] Another method of this aspect comprises the steps of: providing a conformal transfer and molding device having a contact surface comprising one or more transfer surfaces and one or more raised molding features; contacting one or more electronic device components with the conformal transfer and molding device, thereby positioning the one or more electronic device components on the one or more transfer surfaces of the conformal transfer and molding device; contacting a prepolymer layer disposed over a host substrate with the patterned conformal transfer and molding device having the one or more electronic device components positioned thereon, thereby at least partially embedding the one or more electronic device components and the one or more raised molding features into the prepolymer layer; curing the prepolymer layer, thereby forming a polymer layer, wherein the one or more raised molding features of the conformal transfer device are replicated as one or more recessed features in the polymer layer; separating the conformal transfer device from the polymer layer, wherein the one or more electronic device components are retained in the polymer layer; applying a filling material to a surface of the polymer layer; and dragging a scraping tool along the surface of the polymer to fill the filling material into at least a portion of the one or more recessed features.

[051] Another method of this aspect comprises the steps of: providing a host substrate with a prepolymer disposed thereon; at least partially embedding one or more electronic device components into the prepolymer layer, wherein one or more recessed features are patterned in the prepolymer layer during the embedding step; curing the prepolymer layer, thereby forming a polymer layer having one or more recessed features and fixing the one or more electronic device components in the polymer layer; and filling at least a portion of the one or more recessed features with a conductive material, wherein the conductive material provides one or more electrical interconnections to at least one electronic device component.

[052] In another aspect, provided are methods for making a printable electronic device on a device substrate. A method of this aspect comprises the steps of: providing a printable electronic device having a contact area, wherein the printable electronic device is anchored to a host substrate via one or more homogeneous or heterogeneous anchors; contacting the contact area of the printable electronic device with a contact surface of a conformable transfer device, wherein the contact surface of the conformable transfer device has an area smaller than the contact area of the printable electronic device, and wherein the contact area and the contact surface are aligned off center from each other, wherein contact between the contact surface and the contact area binds the printable electronic device to the contact surface; separating the printable electronic device and the host substrate, thereby releasing the one or more homogeneous or heterogeneous anchors; contacting the printable electronic device disposed on the contact surface with a receiving surface of the device substrate; and separating the contact surface of the conformable transfer device and the printable electronic device, wherein the printable electronic device is transferred onto the receiving surface, thereby assembling the printable electronic device on the receiving surface of the device substrate.

[053] In embodiments, the contact surface of the conformable transfer device is a percentage of the contact area of the printable electronic device, for example 25%, 30%, 40%, 50%, less than 50% or selected over the range of 25 to 75%. In a specific embodiment, the contact surface of the conformable transfer device and the contact area of the electronic device are aligned off center from each other, for example by 1 μm, 2 μm, 10 μm, greater than 1 μm, greater than 10 μm or selected

over the range of 1 μm to 100 μm. Optionally the contact surface of the conformable transfer device is provided on a relief feature of the conformable transfer device. In one embodiment, the conformable transfer device is a PDMS stamp.

[054] In some embodiments, the conformable transfer device comprises a plurality of relief features providing a plurality of contact areas. Optionally, in an embodiment where the conformable transfer device comprises a plurality of relief features providing a plurality of contact regions, the method comprises providing a plurality of printable electronic devices each having a contact area, wherein each of the printable electronic devices is anchored to a host substrate via one or more homogeneous or heterogeneous anchors; contacting the contact areas of the printable electronic devices with the contact areas of the conformable transfer device, wherein each of the contact regions of the conformable transfer device has an area smaller than the each of contact areas of the printable electronic device, and wherein the contact areas and the contact regions are aligned off center from each other, wherein contact between the contact regions and the contact areas binds the printable electronic devices to the contact regions; separating the printable electronic devices and the host substrate, thereby releasing the homogeneous or heterogeneous anchors; contacting the printable electronic devices disposed on the contact regions with a receiving surface of the device substrate; and separating the contact regions of the conformable transfer device and the printable electronic devices, wherein the printable electronic devices are transferred onto the receiving surface, thereby assembling the printable electronic devices on the receiving surface of the device substrate.

[055] Useful printable electronic devices include, but are not limited to a P-N junction, a thin film transistor, a single junction solar cell, a multi-junction solar cell, a photodiode, a light emitting diode, a laser, a CMOS device, a MOSFET device, a MESFET device, a photovoltaic cell, a microelectromechanical device, a HEMT device or any combination of these. In embodiments, the device substrate is a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components, or any combination of these.

BRIEF DESCRIPTION OF THE DRAWINGS

[056] Figure 1. (A) SEM image of a square array of AlInGaP LED structures (50 μm by 50 μm) created by vertical, patterned etching through an epitaxial multilayer stack grown on a GaAs wafer. (B) Cross-sectional SEM view of one of these structures, showing the LED semiconductor layers (quantum wells, as well as cladding, spreading, and contact layers) on a sacrificial epilayer of AlAs. (C) Schematic illustration of a printing-based assembly method for transferring collections of LEDs (gray) released from the GaAs wafer to a target substrate (shown here as a flexible sheet). (D) SEM image of the GaAs wafer after removing a set of LEDs (indicated by white arrows) with a stamp. (E) SEM image of a region of the target substrate printed with this stamp. (F) Angled-view SEM image of an individual LED (i.e., ILED) from the array in (D). A pair of "breakaway" photoresist (PR) anchors at the two far corners of the device holds it above the GaAs wafer in the suspended configuration of a diving board, for ease of liftoff with a stamp. The white arrow points to the region of removed AlAs. (G) SEM image of a dense collection of such devices on a piece of a GaAs wafer. The black arrow and white dot indicate, roughly, the region of this chip that corresponds to the image of (F). (H) Optical image of a target substrate printed with sparse arrays of devices at different spacings, derived from the chip shown in (G). (I) Large-scale collection of ILEDs (1600 devices, in a square array with pitch of 1.4 mm) printed onto a thin, flexible sheet of plastic, shown here wrapped onto a cylindrical glass substrate (main panel). The inset shows a similar collection of ILEDs (1600 devices, in a square array with pitch of 1.4 mm) printed onto a plate of glass. For these cases, relatively large ILEDs were selected for ease of viewing; devices with dimensions of (E) are invisible at this magnification.

[057] Figure 2. (A) Exploded view schematic illustration of an array of ILEDs contacted by a metal mesh (bottom; n contacts) and a metal film (top; p contacts). A thin adhesive layer of PDMS facilitates printing onto the glass substrate. A photopatterned layer of epoxy on top of the devices prevents shorting of the top film to the bottom mesh. (B)Optical micrographs of an array of ILEDs (top: 25 μm by 25 μm, square geometries; bottom: characters "LED") in their off state with frontside illumination (left) and in their on state without illumination (right). (C) Schematic illustration of an ILED with integrated ohmic contacts (left) and optical image of an

operating device (right), showing uniform emission characteristics at all regions not directly blocked by the contacts or probe tips. The areas delineated by yellow and white dashed boxes correspond to the contact electrodes and the device periphery, respectively. The regions labeled "PT" correspond to the probe tips used to evaluate the device operation. (D) Current-voltage-emission characteristics of a representative device before undercut etching on the GaAs wafer, and after transfer printing onto a polyurethane-coated glass slide. The inset provides a histogram of the bias voltages needed to produce currents of 0.1 mA in a collection of devices. (E) Spectral characteristics of emission for a typical device on the wafer and after transfer printing.

[058] Figure 3. (A) Schematic illustration of a planar scheme for interconnecting a printed array of ILEDs in a passive matrix layout. Coordinated control of voltages applied to the row and column electrodes allows operation in a passive matrix display mode. (B) Images of a flexible display that incorporates a 16 by 16 array of ILEDs in the layout shown in (A), on a sheet of plastic (PET), wrapped around the thumb of a mannequin hand (main panel; human scale; radius ~8 mm) and a cylindrical glass tube (inset; radius ~12 mm). External interface to control electronics occurs through ribbon cables bonded to column and row electrodes that emerge from the periphery of the display. (C) Image of a comparatively large, semitransparent display that uses a similar layout but with a sparse array of ILEDs on a glass substrate. The camera is focused on the paper in the background; the white dashed box illustrates the perimeter of the active region of the display. (D) Image of a similar device (bottom right) displaying a different pattern in front of a mirror (upper left), to illustrate the bidirectional emission property. In this system, the ILEDs represent only ~0.8% of the total area. The inset shows a magnified view of a region of the display in its off state, to illustrate the small areal coverage of the devices. The black arrow points to one of the ILEDs, which is barely visible at this magnification.

[059] Figure 4. (A) Color plots of the strain distributions (in percent) at the quantum well region and the corresponding finite element mesh used for simulation (top) and optical micrographs (bottom) of a stretchable ILED on a rubber substrate in unstrained and strained states. The bottom panels show optical micrographs in the

off (top) and on (bottom) states, with and without external illumination, respectively. (B) Passive matrix, stretchable ILED display that uses a noncoplanar mesh configuration, on a rubber substrate. Here, interconnect lines between adjacent devices are supported by arc-shaped bridge structures that can deform in response to applied strain. Both the main panel and the inset images were collected with an automated camera system that combines pictures captured at different focal depths to provide a sharp, composite image. (C) Optical micrographs of a set of four pixels in the display shown in (B). The upper and lower images show optical micrographs in the off (top) and on (bottom) states, with and without external illumination, respectively. The multiple red spots in the case of the configuration in the left result from reflections from the interconnection bridges. (D) Current (I)–voltage (V) measurements on a representative ILED in the display, at different applied strains. (E) Voltage (V) needed to generate a current of 20 μA measured after stretching cycles to 500 times at an applied strain of 22%. The inset shows the I-V behavior after these cycling tests. These devices have relatively high turn-on voltages, due to the use of nonohmic contacts.

[060] Figure 5. Schematic illustration (left) and cross sectional scanning electron microscope (SEM) image (middle) of the epitaxial semiconductor multilayer stack on a GaAs wafer. (Right) SEM image of a square array of laterally delineated, square ILEDs on a GaAs wafer. (Bottom) Details of the epi-stack.

[061] Figure 6. Schematic illustration and optical microscope/SEM images of processing steps for retrieving ILEDs from a GaAs source wafer.

[062] Figure 7. Picture of the automated printing machine, with key parts labeled.

[063] Figure 8. (A) Schematic illustration of retrieving and printing selected sets of ILEDs with a composite stamp. (B) Optical microscope image of the source wafer after three cycles of printing. (C) Optical microscope image of a substrate with sparsely printed ILEDs derived from the source wafer of (B), illustrating the concept of area expansion.

[064] Figure 9. Schematic illustration of processing steps for ILEDs of Figure 2A.

[065] Figure 10. (A) Optical microscope image of transmission line model (TLM) patterns with gaps of L_1 = 10 μm, L_2 = 20 μm, L_3 = 30 μm, L_4 = 40 μm, L_5 = 50 μm, L_6 = 60 μm, L_7 = 70 μm. (B) I (current) – V (voltage) curves associated with p contacts (Pt/Ti/Pt/Au = 10/40/10/70 nm) as a function of annealing temperature. (C) Resistance as a function of gap length, for the p contact metallization, evaluated at different annealing temperatures. (D) I-V curves associated with n contacts (Pd/Ge/Au = 5/35/70 nm) as a function of annealing temperature. (E) Resistance as a function of gap length, for the n contact metallization, evaluated at different annealing temperatures.

[066] Figure 11. (A) I-V curves of ILED devices with ohmic contacts with and without a passivation scheme to protect the sidewalls during undercut etching. (B) I-V curves of ILED devices (50x50 μm and 100x100 μm) with ohmic contacts and passivation scheme, before and after transfer.

[067] Figure 12. (A) Schematic illustration of processing steps for fabricating electrical interconnections to complete a passive matrix array. (B) Optical microscope image of an array of ILEDs array after exposing n-GaAs by wet etching. (C) Cross sectional SEM view of an ILED after exposing n-GaAs by wet etching. (D) Optical microscope image of an array of ILEDs with electrical interconnections.

[068] Figure 13. Optical images of a 16x16 ILED (100 μm x 100 μm with a pitch of 210 μm) display on a plastic substrate, wrapped onto the wrist (A) and finger (B, C) of mannequin. (Bottom right) a map of non-working pixels (indicated by 'x' symbols).

[069] Figure 14. (A) Optical image of a 16x16 ILED (50 μm x 50 μm with a pitch of 70 μm) display on a glass substrate with ACF ribbon cable connection. (B) Optical images of the display during the operation. (Left-top) a map of non-working pixels (indicated by 'x' symbols).

[070] Figure 15. Electrical properties of a 16x16 ILED (100 μm x 100 μm with a pitch of 210 μm) display on a plastic substrate. (A) Plot of voltage at 20 μA and (B) I-V curves under $R = \infty$, 17.3, 12.6, 8.8, 7.3 mm. (C) Plot of voltage at 20 μA and (D) I-V curves as a function of bending cycles up to 500 times at R = 8.8 mm. The relatively high turn-on voltages are due to the use of non-ohmic contacts.

[071] Figure 16. (A, B) Optical images of a 16x16 ILED (100 μm x 100 μm with a pitch of 1.20 mm) display on glass substrate during operation. (C) A map of non-working pixels (indicated by 'x' symbols).

[072] Figure 17. (A) Exploded schematic illustration of processing steps for wavy ILEDs ribbons. (B) Optical microscope image of wavy ILEDs ribbons with 50 μm and 100 μm width collected with a scanning focal technique. Optical microscope image of a wavy ILEDs ribbon in different strained states (from wavy to flat): (C) non-emission with illumination, (D) emission with illumination, (E) emission without illumination. (F) I-V curves under different strained states. The relatively high turn-on voltages are due to the use of non-ohmic contacts.

[073] Figure 18. (A) Optical microscope images of emission, collected without illumination, from wavy ILEDs ribbons in wavy (top) and flat (bottom) configurations. Color analysis of pixels recorded in white square box of (A) using a utilities available in a commercial software package (Photoshop, Adobe Systems): range of red values of emission from (B) the wavy and (C) flat configurations, as a function of position along the ribbon length (0 = white, 255 = full red). (D) Averaged range of red values of emission across the ribbon width from (B) and (C).

[074] Figure 19. (A) Schematic illustration of processing steps for stretchable ILEDs display. (B) A map of non-working pixels (indicated by 'x' symbols).

[075] Figure 20. Optical microscope images of a passive matrix, stretchable ILEDs display that uses a non-coplanar mesh configuration, on a flat rubber substrate.

[076] Figure 21. Optical microscope and SEM images of a passive matrix, stretchable ILEDs display that uses a non-coplanar mesh configuration, on a bent/twisted rubber substrate.

[077] Figure 22. (A) Schematic illustrations of a stretchable ILED on a rubber substrate in compressed (left) and stretched (right) configurations. Strain distributions in the device: (B) top surface, (C) middle surface (quantum well region), (D) bottom surface in a compressed state and (E) middle surface in a stretched state.

[078] Figure 23. Strain distributions of a stretchable ILED display: (A) top surface, (B) middle surface (quantum well region), and (C) bottom surface of ILED.

[079] Figure 24. Schematic illustration of procedures for printing and interconnecting microscale device components. (a) The first step involves fabrication of devices (square, dark grey blocks with rectangular, gold electrodes) on a source substrate. (b) An elastomeric stamp (light blue) retrieves a collection of these devices by van der Waals adhesion to features of relief that contact the electrode regions. (c) Bringing the stamp, 'inked' with devices in this manner, into contact with a layer of liquid prepolymer (tan), followed by curing to a solid form yields a molded structure with integrated, embedded devices. (d) Scraping a conductive paste (light grey) over this structure fills the molded features to form electrical contacts to the devices and interconnects between them.

[080] Figure 25. (a) Optical image of a collection of conducting features formed by molding a layer of PU on a PET substrate, and then filling the resulting trenches with silver epoxy. These results illustrate the range of feature sizes and shapes and areas that can be formed easily. (b) Cross-sectional SEM images of filled lines with depths of 20 μm and widths of 20 μm (left) and 200 μm (right). Higher aspect ratios and narrower features can be achieved with suitable modifications to the conductive material. (c) Interconnected arrays of metal pads (Cr/Au, 100/1000 nm; 500×500 μm; 1.5 mm pitch) with crossed, but electrically isolated conducting lines on a PET substrate. This result used a stamp/mold with lines (100 μm widths and 20 μm depths) and rectangular features (100×300 μm lateral dimensions and 40 μm depths) to form the interconnects and the contacts to the metal pads, respectively. The bottom left and right frames provide a schematic cartoon illustration and a top view optical micrograph, respectively, of the structure near a representative pad. (d) Current/voltage data collected by probing contact pads to different combinations of row (r1, r2, etc) and column (c1, c2, etc) interconnect lines verifies electrical continuity along columns and rows and electrical isolation between columns and rows.

[081] Figure 26. (a) Optical image of a set of six AlInGaP light emitting diodes (LEDs; 250x250 μm) formed in ultrathin (2.5 μm thick) layouts and pairs of molded interconnect lines leading to each. Selective printing formed the arrays; aligned

molding followed by filling with silver epoxy formed the interconnect. The top inset provides a top view optical micrograph. The three devices in the middle were connected to a power supply to cause light emission. (b) Current/voltage characteristics (non-ohmic contacts) of these LEDs.

[082] Figure 27. (a) Schematic illustration of a photovoltaic minimodule consisting of five monocrystalline bars of silicon with integrated contacts. The left and right frames show the structure before and after filling molded trenches with silver epoxy, respectively. The molded polymer (PU) is illustrated in tan; the silicon cells are black, with gold contacts. Filling the molded trenches with silver epoxy (light grey) yields the interconnected structure on the right. Each bar is 50 μm wide, 1.55 mm long and 20 μm thick, with ohmic contacts of metal (Cr/Au, 100/1000 nm; 50 μm width and 100 μm length for p contact; 50 μm width and 1.4 mm length for n contact) on p and n doped regions. (b) Optical image of a sample, with an inset that shows a cross sectional view of part of the structure. (c) Current/voltage characteristics carried out at room temperature, in light and dark. The efficiency (E_{ff}) and fill factor (FF) of this solar cell were 6.5% and 0.61 respectively.

[083] Figure 28. Epitaxial layers of GaAs LED wafer.

[084] Figure 29. Processing schematics for μ-GaAs LED.

[085] Figure 30. A. Scanning Electron Microscopy (SEM) image of isolated GaAs LED on the host wafer. B. Scanning Electron Microscopy (SEM) image GaAs LED after heterogeneous anchors are photolithographically defined. C. Scanning Electron Microscopy (SEM) image of transfer-printed GaAs LEDs on a PET substrate. D. Optical Microscopy (OM) image of GaAs LEDs before & after transfer-printing process.

[086] Figure 31. (A). A cartoon illustrating the printed μ-GaAs LED. (B) Luminance vs. current-voltage characteristic plots.

[087] Figure 32. Epitaxial layer structure of a typical GaN device on a silicon wafer.

[088] Figure 33. Processing scheme of individually printable μ-GaN LEDs.

[089] Figure 34. Scanning electron microscopy (SEM) image of an anchor of μ-GaN LED cell before (left) and after (right) KOH undercut process.

[090] Figure 35. Optical image of the donor substrate after several step-and-repeat transfer-printing process has been carried out.

[091] Figure 36. Step-and-repeat process on GaAs μ-LEDs.

[092] Figure 37. (a) Optical image (b) current-voltage characteristic and (c) emission spectrum of an individual μ-GaN LED cell under operation.

[093] Figure 38. SEM images of GaN LED devices before and after KOH undercut. Extended exposure to KOH causes moderate roughening of the GaN sidewalls.

[094] Figure 39. Sidewall passivation scheme for printable GaN devices.

[095] Figure 40. Printable GaN devices utilizing laser lift-off.

[096] Figure 41. Freestanding GaN device transfer utilizing PEC etching with InGaN sacrificial layer. SEM images* of PEC etching for freestanding GaN and AlGaN layers are inserted. (*left image: E. Habereret al. Appl. Phys. Lett. 85, 5179 (2005), right image: R. Sharma et al Appl. Phys. Lett. 87, 051107 (2005)).

[097] Figure 42. Selective etching of sacrificial layer by EC (electrochemical) etching.

[098] Figure 43. Selective etching of sacrificial layer (i.e. ZnO) with specific etchant (NH_4Cl).

[099] Figure 44. Optical Microscopy (OM) image of heterogeneous anchoring structures.

[0100] Figure 45. Various geometries of heterogeneous anchoring structures.

[0101] Figure 46. (A) Optical microscopy (OM) image of homogeneous anchors; (B) scanning electron microscopy (SEM) images of homogeneous anchors.

[0102] Figure 47. SEM images of commercially available wire-bonded LED.

[0103] Figure 48. (a) Schematic illustration of the cell design. (b) Process for encapsulation via back-side exposure.

[0104] Figure 49. (a) Scanning electron microscopy (SEM) image (b) optical microscopy (OM) image of passivated μ-GaN LED using encapsulation via back-side exposure process.

[0105] Figure 50. Scanned profile using a profilometer of μ-GaN LED after the encapsulation via back-side exposure process.

[0106] Figure 51. Five μ-GaN LEDs connected in series.

[0107] Figure 52. Two strings of five μ-GaN LEDs connected in series.

[0108] Figure 53. Fabrication schematic for the molded interconnection.

[0109] Figure 54. Fabrication schematic for the molded interconnection.

[0110] Figure 55. (a) Optical Image of 1 GaAs LED cell. 9 GaAs LED cells with 250×250 μm^2 are independently metalized with a conductive silver paste. (b) Current-Voltage (I-V) characteristic of 1 GaAs LED.

[0111] Figure 56. Molded interconnection approach with addition of reflective layers for selective curing.

[0112] Figure 57. Resolution of molded interconnection approach.

[0113] Figure 58. GaAs vertical LED structure.

[0114] Figure 59. Fabrication process for the mesh interconnection approach. Also exploded view schematic illustration of an array of ILEDs contacted by a metal mesh (bottom; n contacts) and a metal film (top; p contacts) is shown.

[0115] Figure 60. A comparison between strings of μ-LEDs connected in series and in parallel.

[0116] Figure 61. Optical Image of serially connected strings of μ-LEDs printed on a plastic substrate.

[0117] Figure 62. Planar interconnection processing schematics for passive-matrix display using printed μ-LEDs.

[0118] Figure 63. Spatially independent micro-lens array fitted to a of five□ μ-GaN LEDs display with stretchable mechanical interconnects.

[0119] Figure 64. Stretchable □μ-LEDs.

[0120] Figure 65. a) Mirror-like facets increase internal reflection, but b) roughened surfaces reduces internal reflection.

[0121] Figure 66. Formation of pyramidal structures is performed by PEC KOH etching of a fully fabricated/undercut device in the presence of UV light.

[0122] Figure 67. Light Enhancement μ-GaN LED with outcoupling: GaN cone structures.

[0123] Figure 68. GaN LED encapsulation in a polymer micro-lens increases light extraction efficiency.

[0124] Figure 69. Processing steps to form a micro-lens array fitted to a micro-LED display.

[0125] Figure 70. Processing steps to form a spatially independent micro-lens array fitted to a micro-LED display.

[0126] Figure 71. Schematics for optically enhancement with polymeric pattern.

[0127] Figure 72. Bi-directional nature of light output from the printed μ-LED on transparent substrates.

[0128] Figure 73. Integration of reflector and thermal heat sink onto printed μ-LEDs.

[0129] Figure 74. Multiple stacks of μ-LEDs

[0130] Figure 75. Thermographic images at various driving conditions of AlInGaP μ-LED.

[0131] Figure 76. Thermal management of printed μ-LED on plastic substrates.

[0132] Figure 77. Printed μ-diamond as a heat sink.

[0133] Figure 78. Integration of reflector & thermal heat sink onto printed μ-LEDs.

[0134] Figure 79. Heterogeneous integration of μ-LEDs with printed electronics.

[0135] Figure 80. Heterogeneous integration of photodiode with μ-LEDs for the *in situ* self-calibration of the light output.

[0136] Figure 81. Fabrication scheme of uniform phosphor array.

[0137] Figure 82. Phosphors in elastomer cavities.

[0138] Figure 83. Laminated Phosphor-encapsulated Elastomer on top of printed and packaged LEDs.

[0139] Figure 84. Exemplary method of making semiconductor devices.

[0140] Figure 85. Exemplary method of making GaN LED devices.

[0141] Figure 86. Exemplary method of making GaN LED devices.

[0142] Figure 87. Exemplary method of making GaN LED devices.

[0143] Figure 88. Exemplary method of making GaN LED devices.

[0144] Figure 89. Illustration of a scheme for processing electronic devices on a handle substrate.

[0145] Figure 90. A) Cross sectional view of an exemplary semiconductor structure grown on a growth substrate; B) Illustration of a transfer scheme for transferring portions of a semiconductor structure to two separate handle substrates.

[0146] Figure 91. Illustration of a scheme for assembly of electronic devices grown on separate growth substrates on a common handle substrate.

[0147] Figure 92. A) Illustration of a scheme for assembly of electronic devices grown on separate growth substrates on a common handle substrate; B) Cross sectional view of the assembled electronic devices on the handle substrate.

[0148] Figure 93. Illustration of a scheme for processing electronic devices on a handle substrate.

[0149] Figure 94. Illustration of a scheme for processing electronic devices on a handle substrate.

DETAILED DESCRIPTION OF THE INVENTION

[0150] In general the terms and phrases used herein have their art-recognized meaning, which can be found by reference to standard texts, journal references and contexts known to those skilled in the art. The following definitions are provided to clarify their specific use in the context of the invention.

[0151] "Transferable" or "printable" are used interchangeably and relates to materials, structures, device components and/or integrated functional devices that are capable of transfer, assembly, patterning, organizing and/or integrating onto or into substrates. In an embodiment, transferring or printing refers to the direct transfer of a structure or element from one substrate to another substrate, such as from a multilayer structure to a device substrate or a device or component supported by a device substrate. Alternatively, transferable refers to a structure or element that is printed via an intermediate substrate, such as a stamp that lifts-off the structure or element and then subsequently transfers the structure or element to a device substrate or a component that is on a device substrate. In an embodiment, the printing occurs without exposure of the substrate to high temperatures (i.e. at temperatures less than or equal to about 400 degrees Celsius). In one embodiment, printable or transferable materials, elements, device components and devices are capable of transfer, assembly, patterning, organizing and/or integrating onto or into substrates via solution printing or dry transfer contact printing. Similarly, "printing" is used broadly to refer to the transfer, assembly, patterning, organizing and/or integrating onto or into substrates, such as a substrate that functions as a stamp or a substrate that is itself a target (e.g., device) substrate. Such a direct transfer printing provides low-cost and relatively simple repeated transfer of a functional top-layer of a

multilayer structure to a device substrate. This achieves blanket transfer from, for example, a wafer to a target substrate without the need for a separate stamp substrate.

[0152] "Substrate" refers to a material having a surface that is capable of supporting a component, including a device, component or an interconnect. An interconnect that is "bonded" to the substrate refers to a portion of the interconnect in physical contact with the substrate and unable to substantially move relative to the substrate surface to which it is bonded. Unbonded portions, in contrast, are capable of substantial movement relative to the substrate. The unbonded portion of an interconnect generally corresponds to that portion having a "bent configuration," such as by strain-induced interconnect bending.

[0153] "Host substrate" and "handle substrate" interchangeably refer to a substrate on which an electronic device is assembled, processed or otherwise manipulated. In certain embodiments, a handle substrate is a substrate useful as a transitory substrate, for example for holding structures for subsequent transfer to another substrate, such as by transfer printing. In some embodiments, a handle substrate is useful as a processing substrate, where structures present on the handle substrate undergo additional processing steps. "Growth substrate" refers to a substrate useful for growing material, for example via epitaxial growth. In embodiments, a growth substrate comprises the same material as is being grown. In embodiments a growth substrate comprises material different from that being grown. Useful growth substrates include substrates which are lattice matched, or effectively lattice matched, to the material being grown. In some embodiments a growth substrate is a host substrate. "Device substrate" refers to a substrate useful for assembling device components. In some embodiments, a device substrate comprises functional device components. In some embodiments, a device substrate is a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components, or any combination of these. In some embodiments a device substrate is a host substrate.

[0154] The term "surface" as used herein is intended to be consistent with its plain meaning which refers to an outer boundary of an object. In embodiments, surfaces may be given specific names, such as "receiving surface", "contact surface",

"external surface". In some embodiments, named surfaces can refer to their target use and/or identify subregions of a surface. In some embodiments, named surfaces can refer to their orientation, for example relative to other nearby or adjacent components.

[0155] "Functional layer" or "device layer" refers to a layer capable of incorporation into a device or device component and that provides at least partial functionality to that device or device component. Depending on the particular device or device component, a functional layer can include a broad range of compositions. For example, a device that is a solar array can be made from a starting functional layer of III-V micro solar cells, including a functional layer that is itself made up a plurality of distinct layers as provided herein. In certain embodiments, release and subsequent printing of such layers provides the basis for constructing a photovoltaic device or device component. In contrast, a functional layer for incorporation into electronics (MESFETs), LEDs, or optical systems may have a different layering configuration and/or compositions. Accordingly, the specific functional layer incorporated into the multilayer structure depends on the final device or device component in which the functional layer will be incorporated.

[0156] "Release layer" (sometimes referred to as "sacrificial layer") refers to a layer that at least partially separates one or more functional layers. A release layer is capable of being removed or providing other means for facilitating separation of the functional layer from other layers of the multi-layer structure, such as by a release layer that physically separates in response to a physical, thermal, chemical and/or electromagnetic stimulation, for example. Accordingly, the actual release layer composition is selected to best match the means by which separation will be provided. Means for separating is by any one or more separating means known in the art, such as by interface failure or by release layer sacrifice. A release layer may itself remain connected to a functional layer, such as a functional layer that remains attached to the remaining portion of the multilayer structure, or a functional layer that is separated from the remaining portion of the multilayer structure. The release layer is optionally subsequently separated and/or removed from the functional layer.

[0157] "Buffer layer" refers to a layer of a device or device component which is useful for protecting other layers of the device component. In one embodiment, a

buffer layer protects another device layer from etching. In an embodiment, a buffer layer does not impact or has a minimal impact on the function of the device. In one embodiment, an etch block layer is a buffer layer.

[0158] "Release" and "releasing" refer to at least partially separating two layers, devices or device components from one another, for example by mechanical or physical separation, or by removal of at least a portion of one layer, device or device component. In some embodiments, removal of a sacrificial layer results in the release of a layer, device or device component. In some embodiments, layers, devices or device components are released by etching away a portion of the layer, device or device component. In certain embodiments, released components remain attached to the object with they are released from by one or more anchors. In some embodiments, released components are subsequently attached to the object they are released from by one or more anchors.

[0159] "Etch" and "etching" refer to a process by which a portion of a layer, device or device component is reacted away, dissolved or otherwise removed. In embodiments, an anisotropic etch or a directional etch refers to an etching process which preferentially removes material along a specific direction. In embodiments, a wet etch refers to removal of material by exposure to a solution. In embodiments, a selective etch refers to removal of a specific material or class of materials. In embodiments, a reactive ion etch or an inductively coupled plasma reactive ion etch refers to an etching method which utilizes a plasma to etch away material, for example by reaction with ions in the plasma. The term "etchant" is used in the present description to broadly refer to a substance which is useful for removal of material by etching. The term "electrochemical etching" refers to an etching process which utilizes an applied electric potential, electric field or electric current. The term "photoelectrochemical etching" refers to an etching process which utilizes an applied electric potential, electric field or electric current and exposure to electromagnetic radiation.

[0160] An "etch mask" refers to material useful for preventing underlying material from being etched. In some embodiments, a thick etch mask refers to an etch mask of a sufficient thickness that the majority of the mask remains after an etching process. In embodiments a thick etch mask has a thickness selected over the range

of 100 nm to 5 μm. In some embodiments a metal etch mask refers to an etch block layer.

[0161] The term "mask" refers to a material which covers or otherwise blocks portions of an underlying material. Use of the term "mask" is intended to be consistent with use of the term in the art of microfabrication. In embodiments, the term "mask" refers to an etch mask, an optical mask, a deposition mask or any combination of these.

[0162] The terms "masked region" and "exposed region" respectively refer to portions of an underlying material which are blocked and unblocked by a mask.

[0163] "Epitaxial regrowth" and "epitaxial growth" refers to a method of growing crystalline layer by deposition of material, for example gas or liquid phase deposition. The term "epilayer" refers to a layer grown via epitaxial growth.

[0164] The term "patterning" is used herein as in the art of microfabrication to broadly refer to a process by which portions of a layer, device or device component are selectively removed or deposited to create a specified structure.

[0165] "Supported by a substrate" refers to a structure that is present at least partially on a substrate surface or present at least partially on one or more intermediate structures positioned between the structure and the substrate surface. The term "supported by a substrate" may also refer to structures partially or fully embedded in a substrate.

[0166] "Printable electronic device" or "printable electronic device component" refer to devices and structures that are configured for assembly and/or integration onto substrate surfaces, for example by using dry transfer contact printing and/or solution printing methods. In embodiments, a printable electronic device component is a printable semiconductor element. In embodiments, printable semiconductor elements are unitary single crystalline, polycrystalline or microcrystalline inorganic semiconductor structures. In various embodiments, printable semiconductor elements are connected to a substrate, such as a mother wafer, via one or more bridge or anchor elements. In this context of this description, a unitary structure is a monolithic element having features that are mechanically connected. Semiconductor

elements of various embodiments may be undoped or doped, may have a selected spatial distribution of dopants and may be doped with a plurality of different dopant materials, including p- and n-type dopants. Certain microstructured printable semiconductor elements include those having at least one cross sectional dimension greater than or equal to about 1 micron and nanostructured printable semiconductor elements having at least one cross sectional dimension less than or equal to about 1 micron.

[0167] Printable semiconductor elements useful for a variety of applications comprise elements derived from "top down" processing of high purity bulk materials, such as high purity crystalline semiconductor wafers generated using conventional high temperature processing techniques. In an embodiment, a printable semiconductor element comprises a composite heterogeneous structure having a semiconductor operationally connected to or otherwise integrated with at least one additional device component or structure, such as a conducting layer, dielectric layer, electrode, additional semiconductor structure or any combination of these. In some methods and systems of the present invention, the printable semiconductor element(s) comprises a semiconductor structure integrated with at least one additional structure selected from the group consisting of: another semiconductor structure; a dielectric structure; conductive structure, and an optical structure (e.g., optical coatings, reflectors, windows, optical filter, collecting, diffusing or concentration optic etc.). In some embodiments a printable semiconductor element comprises a semiconductor structure integrated with at least one electronic device component selected from the group consisting of: an electrode, a dielectric layer, an optical coating, a metal contact pad a semiconductor channel. In some embodiments, printable semiconductor elements comprise stretchable semiconductor elements, bendable semiconductor elements and/or heterogeneous semiconductor elements (e.g., semiconductor structures integrated with one or more additional materials such as dielectrics, other semiconductors, conductors, ceramics etc.). Printable semiconductor elements include printable semiconductor devices and components thereof, including but not limited to printable LEDs, lasers, solar cells, p-n junctions, photovoltaics, photodiodes, diodes, transistors, integrated circuits, and sensors.

[0168] "Electronic device component" refers to a printable semiconductor or electrical device. Exemplary electronic device component embodiments are configured for performing a function, for example emitting electromagnetic radiation or converting electromagnetic radiation into electrical energy. In specific embodiments, multiple electronic device components are electrically interconnected and perform a more complex task or function than the individual device components perform alone. Useful electronic device components include, but are not limited to P-N junctions, thin film transistors, single junction solar cells, multi-junction solar cells, photodiodes, light emitting diodes, lasers, CMOS devices, MOSFET devices, MESFET devices, photovoltaic cells, microelectricalmechanical devices and HEMT devices.

[0169] "Vertical type LED" refers to a light emitting diode device in which the functional components or layers of the device are arranged in a stacked configuration and the electrical contacts are made at the top and bottom of the stack.

[0170] "Solution printing" is intended to refer to processes whereby one or more structures, such as transferable or printable elements, are dispersed into a carrier medium and delivered in a concerted manner to selected regions of a substrate surface. In an exemplary solution printing method, delivery of structures to selected regions of a substrate surface is achieved by methods that are independent of the morphology and/or physical characteristics of the substrate surface undergoing patterning. Solution printing methods include, but are not limited to, ink jet printing, thermal transfer printing, and capillary action printing.

[0171] "Contact printing" refers broadly to a dry transfer contact printing method such as with a stamp that facilitates transfer of features from a stamp surface to a substrate surface. In an embodiment, the stamp is an elastomeric stamp. Alternatively, the transfer can be directly to a target (e.g., device) substrate or host substrate. The following references relate to self assembly techniques which may be used in methods of the present invention to transfer, assembly and interconnect transferable semiconductor elements via contact printing and/or solution printing techniques and are incorporated by reference in their entireties herein: (1) "Guided molecular self-assembly: a review of recent efforts", Jiyun C Huie Smart Mater. Struct. (2003) 12, 264-271; (2) "Large-Scale Hierarchical Organization of Nanowire

Arrays for Integrated Nanosystems", Whang, D.; Jin, S.; Wu, Y.; Lieber, C. M. Nano Lett. (2003) 3(9), 1255-1259; (3) "Directed Assembly of One-Dimensional Nanostructures into Functional Networks", Yu Huang, Xiangfeng Duan, Qingqiao Wei, and Charles M. Lieber, Science (2001) 291, 630-633; and (4) "Electric-field assisted assembly and alignment of metallic nanowires", Peter A. Smith et al., Appl. Phys. Lett. (2000) 77(9), 1399-1401.

[0172] Useful contact printing methods for assembling, organizing and/or integrating transferable elements include dry transfer contact printing, microcontact or nanocontact printing, microtransfer or nanotransfer printing and self assembly assisted printing. Use of contact printing is beneficial because it allows assembly and integration of a plurality of transferable semiconductor in selected orientations and positions relative to each other. Contact printing also enables effective transfer, assembly and integration of diverse classes of materials and structures, including semiconductors (e.g., inorganic semiconductors, single crystalline semiconductors, organic semiconductors, carbon nanomaterials etc.), dielectrics, and conductors. Contact printing methods optionally provide high precision registered transfer and assembly of transferable semiconductor elements in preselected positions and spatial orientations relative to one or more device components prepatterned on a device substrate. Contact printing is also compatible with a wide range of substrate types, including conventional rigid or semi-rigid substrates such as glasses, ceramics and metals, and substrates having physical and mechanical properties attractive for specific applications, such as flexible substrates, bendable substrates, shapeable substrates, conformable substrates and/or stretchable substrates. Contact printing assembly of transferable structures is compatible, for example, with low temperature processing (e.g., less than or equal to 298K). This attribute allows the present optical systems to be implemented using a range of substrate materials including those that decompose or degrade at high temperatures, such as polymer and plastic substrates. Contact printing transfer, assembly and integration of device elements is also beneficial because it can be implemented via low cost and high-throughput printing techniques and systems, such as roll-to-roll printing and flexographic printing methods and systems.

[0173] "Stretchable" refers to the ability of a material, structure, device or device component to be strained without undergoing fracture. In an exemplary embodiment, a stretchable material, structure, device or device component may undergo strain larger than about 0. 5% without fracturing, preferably for some applications strain larger than about 1 % without fracturing and more preferably for some applications strain larger than about 3 % without fracturing.

[0174] The terms "flexible" and "bendable" are used synonymously in the present description and refer to the ability of a material, structure, device or device component to be deformed into a curved shape without undergoing a transformation that introduces significant strain, such as strain characterizing the failure point of a material, structure, device or device component. In an exemplary embodiment, a flexible material, structure, device or device component may be deformed into a curved shape without introducing strain larger than or equal to about 5 %, preferably for some applications larger than or equal to about 1 %, and more preferably for some applications larger than or equal to about 0.5 %.

[0175] "Semiconductor" refers to any material that is an insulator at very low temperatures, but which has an appreciable electrical conductivity at a temperatures of about 300 Kelvin. In the present description, use of the term semiconductor is intended to be consistent with use of this term in the art of microelectronics and electrical devices. Useful semiconductors include element semiconductors, such as silicon, germanium and diamond, and compound semiconductors, such as group IV compound semiconductors such as SiC and SiGe, group III-V semiconductors such as AlSb, AlAs, Aln, AlP, BN, GaSb, GaAs, GaN, GaP, InSb, InAs, InN, and InP, group III-V ternary semiconductors alloys such as AlxGa1-xAs, group II-VI semiconductors such as CsSe, CdS, CdTe, ZnO, ZnSe, ZnS, and ZnTe, group I-VII semiconductors CuCl, group IV – VI semiconductors such as PbS, PbTe and SnS, layer semiconductors such as PbI_2, MoS_2 and GaSe, oxide semiconductors such as CuO and Cu_2O.

[0176] The term semiconductor includes intrinsic semiconductors and extrinsic semiconductors that are doped with one or more selected materials, including semiconductor having p-type doping materials (also known as P-type or p-doped semiconductor) and n-type doping materials (also known as N-type or n-doped

semiconductor), to provide beneficial electrical properties useful for a given application or device. The term semiconductor includes composite materials comprising a mixture of semiconductors and/or dopants. Useful specific semiconductor materials include, but are not limited to, Si, Ge, SiC, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InP, InAs, GaSb, InP, InAs, InSb, ZnO, ZnSe, ZnTe, CdS, CdSe, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, PbS, PbSe, PbTe, AlGaAs, AlInAs, AlInP, GaAsP, GaInAs, GaInP, AlGaAsSb, AlGaInP, and GaInAsP. Porous silicon semiconductor materials are useful in the field of sensors and light emitting materials, such as light emitting diodes (LEDs) and solid state lasers. Impurities of semiconductor materials are atoms, elements, ions and/or molecules other than the semiconductor material(s) themselves or any dopants provided to the semiconductor material. Impurities are undesirable materials present in semiconductor materials which may negatively impact the electrical properties of semiconductor materials, and include but are not limited to oxygen, carbon, and metals including heavy metals. Heavy metal impurities include, but are not limited to, the group of elements between copper and lead on the periodic table, calcium, sodium, and all ions, compounds and/or complexes thereof.

[0177] In certain embodiments, the term "orientation" refers to a specific plane of a crystal structure, for example a semiconductor crystal. In certain embodiments, the term "direction" refers to a specific axis, or equivalent axes, of a crystal structure. In embodiments, use of the terms orientation and direction with a specific numeric indicator is intended to be consistent with use in the fields of crystallography and microfabrication.

[0178] "Quantum well" refers to an active layer of a light emitting diode device. In one embodiment, a quantum well is a layer of an LED device having a relatively narrow bandgap, surrounded on two sides by layers having a relatively wider bandgap. "Barrier layer" refers to a layer of a light emitting diode device which is positioned adjacent to a quantum well layer and has a larger bandgap than the quantum well material. In one embodiment, a quantum well layer is sandwiched between two barrier layers. In another embodiment, multiple quantum well layers are sandwiched between multiple barrier layers.

[0179] "Contact layer" refers to refers to a layer of a light emitting diode device, for example used to make electrical contact with external circuit components, such as electrical interconnects. "Spreader layer" refers to a layer of a light emitting diode device, for example useful for providing voltage or current from a contact layer across the area of a light emitting diode device. "Cladding layer" refers to a layer of a light emitting diode device, for example a layer surrounding the barrier layer and quantum well layer.

[0180] "Good electronic performance" and "high performance" are used synonymously in the present description and refer to devices and device components have electronic characteristics, such as field effect mobilities, threshold voltages and on – off ratios, providing a desired functionality, such as electronic signal switching and/or amplification. Exemplary printable elements exhibiting good electronic performance may have intrinsic field effect mobilities greater than or equal 100 $cm^2 V^{-1} s^{-1}$, and for some applications, greater than or equal to about 300 $cm^2 V^{-1} s^{-1}$. Exemplary transistors exhibiting good electronic performance may have device field effect mobilities great than or equal to about 100 $cm^2 V^{-1} s^{-1}$, for some applications, greater than or equal to about 300 $cm^2 V^{-1} s^{-1}$, and for other applications, greater than or equal to about 800 $cm^2 V^{-1} s^{-1}$. Exemplary transistors of exhibiting good electronic performance may have threshold voltages less than about 5 volts and/or on – off ratios greater than about 1×10^4.

[0181] "Plastic" refers to any synthetic or naturally occurring material or combination of materials that can be molded or shaped, generally when heated, and hardened into a desired shape. Useful plastics include, but are not limited to, polymers, resins and cellulose derivatives. In the present description, the term plastic is intended to include composite plastic materials comprising one or more plastics with one or more additives, such as structural enhancers, fillers, fibers, plasticizers, stabilizers or additives which may provide desired chemical or physical properties.

[0182] "Prepolymer" refers to a material which is a polymer precursor and/or a material which, when cured, is a polymer. A "liquid prepolymer" refers to a prepolymer which exhibits one or more properties of a liquid, for example flow properties. Specific prepolymers include, but are not limited to, photocurable polymers, thermally curable polymers and photocurable polyurethanes.

[0183] "Curing" refers to a process by which a material is transformed such that the transformed material exhibits one or more properties different from the original, non-transformed material. In some embodiments, a curing process allows a material to become solid or rigid. In an embodiment, curing transforms a prepolymer material into a polymer material. Useful curing processes include, but are not limited to, exposure to electromagnetic radiation (photocuring processes), for example exposure to electromagnetic radiation of a specific wavelength or wavelength range (e.g., ultraviolet or infrared electromagnetic radiation); thermal curing processes, for example heating to a specific temperature or within a specific temperature range (e.g., 150 °C or between 125 and 175 °C); temporal curing processes, for example waiting for a specified time or time duration (e.g., 5 minutes or between 10 and 20 hours); drying processes, for example removal of all or a percentage of water or other solvent molecules; and any combination of these. For example, one embodiment for curing a silver epoxy comprises heating the silver epoxy to 150 °C for a duration of 5 minutes.

[0184] "Polymer" refers to a molecule comprising a plurality of repeating chemical groups, typically referred to as monomers. Polymers are often characterized by high molecular masses. Useful polymers include organic polymers and inorganic polymers, both of which may be in amorphous, semi-amorphous, crystalline or partially crystalline states. Polymers may comprise monomers having the same chemical composition or may comprise a plurality of monomers having different chemical compositions, such as a copolymer. Cross linked polymers having linked monomer chains are also useful for some embodiments. Useful polymers include, but are not limited to, plastics, elastomers, thermoplastic elastomers, elastoplastics, thermostats, thermoplastics and acrylates. Exemplary polymers include, but are not limited to, acetal polymers, biodegradable polymers, cellulosic polymers, fluoropolymers, nylons, polyacrylonitrile polymers, polyamide-imide polymers, polyimides, polyarylates, polybenzimidazole, polybutylene, polycarbonate, polyesters, polyetherimide, polyethylene, polyethylene copolymers and modified polyethylenes, polyketones, poly(methyl methacrylate, polymethylpentene, polyphenylene oxides and polyphenylene sulfides, polyphthalamide, polypropylene, polyurethanes, styrenic resins, sulfone based resins, vinyl-based resins or any combinations of these.

[0185] "Elastomer" refers to a polymeric material which can be stretched or deformed and return to its original shape without substantial permanent deformation. Elastomers commonly undergo substantially elastic deformations. Useful elastomers may comprise polymers, copolymers, composite materials or mixtures of polymers and copolymers. An elastomeric layer refers to a layer comprising at least one elastomer. Elastomeric layers may also include dopants and other non-elastomeric materials. Useful elastomer embodiments include, but are not limited to, thermoplastic elastomers, styrenic materials, olefenic materials, polyolefin, polyurethane thermoplastic elastomers, polyamides, synthetic rubbers, PDMS, polybutadiene, polyisobutylene, poly(styrene-butadiene-styrene), polyurethanes, polychloroprene and silicones.

[0186] "Transfer device" or "transfer substrate" refers to a substrate, device or device component capable of and/or configured for receiving and/or relocating an element or array of elements, such as printable elements. Useful transfer devices include conformal transfer devices, such as devices having one or more contact surfaces capable of establishing conformal contact with elements undergoing transfer. An elastomeric stamp and/or transfer device is useful with a variety of the methods and devices described herein. Useful elastomeric transfer devices include, but are not limited to, elastomeric stamps, composite elastomeric stamps, an elastomeric layer, a plurality of elastomeric layers and an elastomeric layer coupled to a substrate such as a glass, ceramic, metal or polymer substrate.

[0187] "Target substrate" is used broadly to refer to the desired final substrate that will support the transferred structure. In an embodiment, the target substrate is a device substrate. In an embodiment, the target substrate is a device component or element that is itself supported by a substrate.

[0188] "Large area" refers to an area, such as the area of a receiving surface of a substrate used for device fabrication, greater than or equal to about 36 square inches.

[0189] "Pre-metalized" refers to a structure which includes metallic layers, components or features.

[0190] "Pre-patterned" refers to a structure which includes one or more devices, components or relief features.

[0191] "Optical communication" refers to a configuration of two or more elements wherein one or more beams of electromagnetic radiation are capable of propagating from one element to the other element. Elements in optical communication may be in direct optical communication or indirect optical communication. "Direct optical communication" refers to a configuration of two or more elements wherein one or more beams of electromagnetic radiation propagate directly from a first device element to another without use of optical components for steering and/or combining the beams. "Indirect optical communication" refers to a configuration of two or more elements wherein one or more beams of electromagnetic radiation propagate between two elements via one or more device components including, but not limited to, wave guides, fiber optic elements, reflectors, filters, prisms, lenses, gratings and any combination of these device components.

[0192] "Electrical contact" and "electrical communication" refers to the arrangement of one or more objects such that an electric current efficiently flows from one object to another. For example, in some embodiments, two objects having an electrical resistance between them less than 100 Ω are considered in electrical communication with one another. An electrical contact can also refer to a component of a device or object used for establishing electrical communication with external devices or circuits, for example an electrical interconnection.

[0193] "Electrical resistivity" refers to a property of a material characteristic of the resistance to flow of electrons through the material. In certain embodiments, the resistivity of a material (ρ) is related to the resistance (R) of a length of material (L) having a specific cross sectional area (A), e.g., $\rho = R \times A/L$.

[0194] "Electrical interconnection" and "electrical interconnect" refers to a component of an electrical device used for providing electrical communication between two or more device components. In some embodiments, an electrical interconnect is used to provide electrical communication between two device components spatially separated from one another, for example spatially separated by a distance greater than 50 nm, for some applications greater than 100 nm, for

other applications greater than 1 μm, and for yet other applications greater than 50 μm. "Electrode contact" refers to a component of an electronic device or device component to which an electrical interconnect attaches or provides electrical communication to or from.

[0195] "Embed" refers to a process by which one object or device is buried, conformally surrounded or otherwise placed or positioned within or below the surface another object, layer or material. "Encapsulate" refers to the orientation of one structure such that it is entirely surrounded by one or more other structures. "Partially encapsulated" refers to the orientation of one structure such that it is partially surrounded by one or more other structures.

[0196] "Replicate" refers to a process by which one or more relief features are transferred and/or recreated during casting, molding, embedding, or embossing processes. Replicated features generally resemble the features they originate from except that the replicated features represent the negative of the original features; that is where the original features are raised features, the replicated features are recessed features and where the original features are recessed features, the replicated features are raised features.

[0197] "Relief feature" refers to portions of an object or layer exhibiting differences in elevation and slope between the higher and lower parts of the surface of a given area or portion of the object or layer. "Raised features" refer to relief features which extend above the surface or average surface level of an object or layer or relief features which have elevations higher than other portions of the surface of an object or layer. "Recessed feature" refer to relief features which extend below the surface or average surface level of an object or layer or relief features which have elevations lower than other portions of the surface of an object or layer.

[0198] "Conformal contact" refers to contact established between surfaces, coated surfaces, and/or surfaces having materials deposited thereon which may be useful for transferring, assembling, organizing and integrating structures (such as printable elements) on a substrate surface. In one aspect, conformal contact involves a macroscopic adaptation of one or more contact surfaces of a conformal transfer device to the overall shape of a substrate surface or the surface of an object such as

a printable element. In another aspect, conformal contact involves a microscopic adaptation of one or more contact surfaces of a conformal transfer device to a substrate surface leading to an intimate contact without voids. The term conformal contact is intended to be consistent with use of this term in the art of soft lithography. Conformal contact may be established between one or more bare contact surfaces of a conformal transfer device and a substrate surface. Alternatively, conformal contact may be established between one or more coated contact surfaces, for example contact surfaces having a transfer material, printable element, device component, and/or device deposited thereon, of a conformal transfer device and a substrate surface. Alternatively, conformal contact may be established between one or more bare or coated contact surfaces of a conformal transfer device and a substrate surface coated with a material such as a transfer material, solid photoresist layer, prepolymer layer, liquid, thin film or fluid.

[0199] "Bind" and "bond" refers to the physical attachment of one object to another. Bind and bound can also refer the retention of one object on another. In one embodiment an object can bind to another by establishing a force between the objects. In some embodiments, objects are bound to one another through use of an adhesion layer. In one embodiment, an adhesion layer refers to a layer used for establishing a bonding force between two objects.

[0200] "Placement accuracy" refers to the ability of a transfer method or device to transfer a printable element, to a selected position, either relative to the position of other device components, such as electrodes, or relative to a selected region of a receiving surface. "Good placement accuracy" refers to methods and devices capable of transferring a printable element to a selected position relative to another device or device component or relative to a selected region of a receiving surface with spatial deviations from the absolutely correct position less than or equal to 50 microns, more preferably less than or equal to 20 microns for some applications and even more preferably less than or equal to 5 microns for some applications. Methods and devices described herein include those comprising at least one printable element transferred with good placement accuracy.

[0201] "Fidelity" refers to a measure of how well a selected pattern of elements, such as a pattern of printable elements, is transferred to a receiving surface of a

substrate. Good fidelity refers to transfer of a selected pattern of elements wherein the relative positions and orientations of individual elements are preserved during transfer, for example wherein spatial deviations of individual elements from their positions in the selected pattern are less than or equal to 500 nanometers, more preferably less than or equal to 100 nanometers.

[0202] "Undercut" refers to a structural configuration wherein the bottom surfaces of an element, such as a printable element, bridge element and/or anchor element, are at least partially detached from or not fixed to another structure, such as a mother wafer or bulk material. Entirely undercut refers to a refers to a structural configuration wherein the bottom surfaces of an element, such as printable element, bridge element and/or anchor element, is completely detached from another structure, such as a mother wafer or bulk material. Undercut structures may be partially or entirely free standing structures. Undercut structures may be partially or fully supported by another structure, such as a mother wafer or bulk material, that they are detached from. Undercut structures may be attached, affixed and/or connected to another structure, such as a wafer or other bulk material, at surfaces other than the bottom surfaces.

[0203] "Anchor" refers to a structure useful for connecting or tethering one device or device component to another. "Anchoring" refers to a process resulting in the connection or tethering of one device or device component to another.

[0204] "Homogeneous anchoring" refers to an anchor that is an integral part of the functional layer. In general, methods of making transferable elements by homogenous anchoring systems is optionally by providing a wafer, depositing a sacrificial layer on at least a portion of a wafer surface, defining semiconductor elements by any means known in the art, and defining anchor regions. The anchor regions correspond to specific regions of the semiconductor element. The anchor regions can correspond to a geometrical configuration of a semiconductor layer, e.g., anchors defined by relatively large surface areas and are connected to transferable elements by bridge or tether elements. Such geometry provides a means for facilitating lift-off of specific non-anchored regions for either single-layer or multi-layer embodiments. Alternatively, anchors correspond to semiconductor regions that are attached or connected to the underlying wafer. Removing the sacrificial layer

provides a means for removing or transferring semiconductor elements while the portion of semiconductor physically connected to the underlying wafer remains.

[0205] "Heterogeneous anchoring" refers to an anchor that is not an integral part of the functional layer, such as anchors that are made of a different material than the semiconductor layer or is made of the same material, but that is defined after the transferable semiconductor elements are placed in the system. One advantage of heterogeneous anchoring compared to homogeneous anchoring relates to better transfer defining strategies and further improvement to the effective useable wafer footprint. In the heterogeneous strategy embodiment, a wafer is provided, the wafer is coated with a sacrificial layer, semiconductor elements are defined, and heterogeneous anchor elements are deposited that anchor semiconductor regions. In an aspect, the anchor is a resist material, such as a photoresist or SiN (silicon nitride), or other material that has a degree of rigidity capable of anchoring and resisting a lift-off force that is not similarly resisted by non-anchored regions. The anchor may span from the top-most semiconductor layer through underlying layers to the underlying wafer substrate. Removal of sacrificial layer provides a means for removing unanchored regions while the anchored regions remain connected to the wafer, such as by contact transfer, for example. In another embodiment, for a multi-layer system, the anchor provides anchoring of a top layer to an underlying semiconductor layer. Alternatively, the anchoring system is for single-layer semiconductor layer systems.

[0206] "Carrier film" refers to a material that facilitates separation of layers. The carrier film may be a layer of material, such as a metal or metal-containing material positioned adjacent to a layer that is desired to be removed. The carrier film may be a composite of materials, including incorporated or attached to a polymeric material or photoresist material, wherein a lift-off force applied to the material provides release of the composite of materials from the underlying layer (such as a functional layer, for example).

[0207] "Dielectric" and "dielectric material" are used synonymously in the present description and refer to a substance that is highly resistant to flow of electric current. Useful dielectric materials include, but are not limited to, SiO_2, Ta_2O_5, TiO_2, ZrO_2, Y_2O_3, Si_3N_4, STO, BST, PLZT, PMN, and PZT.

[0208] "Device field effect mobility" refers to the field effect mobility of an electronic device, such as a transistor, as computed using output current data corresponding to the electronic device.

[0209] "Fill factor" refers to the percentage of the area between two elements, such as between two electrodes, that is occupied by a material, element and/or device component. In one embodiment, two electrodes are provided in electrical contact with one or more printable semiconductor elements that provide a fill factor between first and second electrodes greater than or equal to 20%, preferably greater than or equal to 50% for some applications and more preferably greater than or equal to 80% for some applications.

[0210] "Collecting" and "concentrating", as applied to optics and optical components, refers to the characteristic of optical components and device components that collect light from a first area, in some cases a large area, and optionally direct that light to another area, in some cases a relatively smaller area. In the context of some embodiments, collecting and concentrating optical components and/or optical components are useful for light detection or power harvesting by printed solar cells or photodiodes.

[0211] "Conductive material" refers to a substance or compound possessing an electrical resistivity which is typical of or equivalent to that of a metal, for example copper, silver or aluminum. In embodiments, the electrical resistivity of a conductive material is selected over the range of 1×10^{-10} to 1×10^{-2} $\Omega\cdot$cm. In the present description, use of the term conductive material is intended to be consistent with use of this term in the art of electronic devices and electric circuits. In embodiments, conductive materials are useful as electrical interconnections and/or for providing electrical communication between two devices. A "conductive paste" refers to a conductive material comprising a mixture which is generally soft and malleable. In some embodiments, cured conductive pastes lose their soft and malleable nature and generally exhibit properties of a solid or a monolithic body. Exemplary conductive pastes comprise metal micro- and/or nano-particles. Silver epoxy refers to a conductive paste comprising micro- and/or nano particles including metallic silver (Ag) and which, when cured, exhibits a low electrical resistivity, for example an

electrical resistivity lower than 1×10^{-5} Ω·cm or selected over the range of 1×10^{-10} to 1×10^{-5} Ω·cm.

[0212] "Fill" and "filling" refer to a process of depositing a material into a recessed feature. In one embodiment, a recessed region is filled by scraping material across and into the recessed feature. A filling tool generally refers to a device for moving material into a recessed feature. In an embodiment, a filling tool refers to a device for scraping material across and/or into a recessed region. In a specific embodiment, a filling tool comprises a layer or solid body of PDMS. For certain embodiments, a filling process is conceptually similar to a screen printing process where a material is scraped across a recessed feature by a tool or device having dimensions larger than the recessed feature, thereby at least partially filling the recessed feature with the material.

[0213] "Align" refers to a process by which two objects are arranged with respect to one another. "Aligned off center" refers to a process by which the centers of two objects or two areas are arranged such that the two centers are not coincident with respect to one or more spatial dimensions. For certain embodiments, the term aligned off center refers to alignment of the center of two objects such that the centers of the objects are spatially separated by a distance greater than 50 nm, for some applications greater than 100 nm, for other applications greater than 1 μm, and for yet other applications greater than 50 μm.

[0214] "Young's modulus" refers to a mechanical property of a material, device or layer which refers to the ratio of stress to strain for a given substance. Young's modulus may be provided by the expression;

$$E = \frac{(\text{stress})}{(\text{strain})} = \left(\frac{L_0}{\Delta L} \times \frac{F}{A} \right)$$

where E is Young's modulus, L_0 is the equilibrium length, ΔL is the length change under the applied stress, F is the force applied and A is the area over which the force is applied. Young's modulus may also be expressed in terms of Lame constants via the equation:

$$E = \frac{\mu(3\lambda + 2\mu)}{\lambda + \mu}$$

where μ and λ are Lame constants. High Young's modulus (or "high modulus") and low Young's modulus (or "low modulus") are relative descriptors of the magnitude of Young's modulus in a give material, layer or device. In the present description, a High Young's modulus is larger than a low Young's modulus, about 10 times larger for some applications, more preferably about 100 times larger for other applications and even more preferably about 1000 times larger for yet other applications.

[0215] Described herein are printable structures and methods for making, assembling and arranging electronic devices. A number of the methods described herein are useful for assembling electronic devices where one or more device components are embedded in a polymer which is patterned during the embedding process with trenches for electrical interconnects between device components. Some methods described herein are useful for assembling electronic devices by printing methods, such as by dry transfer contact printing methods. Also described herein are GaN light emitting diodes and methods for making and arranging GaN light emitting diodes, for example for display or lighting systems.

[0216] Figure 24 illustrates an exemplary embodiment of a method for assembling an electronic device. First, one or more electronic device components **2401** are provided. In this embodiment, the electronic device components are printable device components including electrode contacts **2402**. A transfer substrate is also provided with a patterned surface **2403**. In this embodiment, the patterned surface contains features for contacting and retrieving the device components onto the transfer substrate. The patterned surface also contains raised features **2404** which represent the orientation and configuration of electrical interconnects to be fabricated between some of the electronic device components.

[0217] Next, the patterned transfer substrate is brought into contact with the electronic device components **2401**, where they are retrieved onto the transfer substrate. A host substrate having a prepolymer layer **2405** thereon is then provided to receive the electronic device components **2401**. The patterned transfer substrate **2403** having the electronic device components **2401** thereon is brought into contact

with the prepolymer layer **2405**. The electronic device components **2401** are embedded into the prepolymer layer **2405** and, during this step, the patterned surface of the transfer substrate **2403** is also brought into contact with the prepolymer layer **2405**. The raised features **2404** of the patterned surface are also embedded into the prepolymer layer **2405**, at least partially, after which the prepolymer layer **2405** is cured into a hardened polymer layer **2406**. As the prepolymer layer **2405** is cured, the embedded electronic device components are fixed into place within the polymer **2406**, and the raised features of the patterned transfer surface are replicated as recessed features **2407** in the polymer layer **2406**. Once the polymer layer **2406** is cured, the patterned transfer substrate **2403** and the polymer layer **2406** are separated and the electronic device components **2401** are retained in the polymer layer **2406**. Further, the polymer layer includes a number of recessed features **2407**.

[0218] Next, the recessed features **2407** are filled with a conducting material to form electrical interconnects **2408** between the electronic device components **2401**. In one embodiment, a line of silver epoxy conductive paste is provided on the surface of the polymer. The silver epoxy is then filled into the recessed features by dragging a filling tool across the surface of the polymer. Optionally, the filling tool is dragged across the surface of the polymer multiple times and in multiple directions to fill the recessed features. If necessary or desired, additional silver epoxy can be provided on the surface and the dragging steps repeated to ensure that the recessed features are filled to the desired level. Once filled, the conductive paste is cured to form rigid electrical interconnections.

[0219] The invention may be further understood by the following non-limiting examples.

Example 1: Printed Assemblies of Inorganic Light-Emitting Diodes for Deformable and Semitransparent Displays

[0220] This example describes methods for creating microscale inorganic light-emitting diodes (LEDs) and for assembling and interconnecting them into unusual display and lighting systems. The LEDs use specialized epitaxial semiconductor layers that allow delineation and release of large collections of ultrathin devices. Diverse shapes are possible, with dimensions from micrometers to millimeters, in

either flat or "wavy" configurations. Printing-based assembly methods can deposit these devices on substrates of glass, plastic, or rubber, in arbitrary spatial layouts and over areas that can be much larger than those of the growth wafer. The thin geometries of these LEDs enable them to be interconnected by conventional planar processing techniques. Displays, lighting elements, and related systems formed in this manner can offer interesting mechanical and optical properties.

[0221] Display devices represent ubiquitous, central components of nearly all consumer electronics technologies. Organic light emitting diodes (OLEDs) are rapidly emerging as an attractive alternative to backlit liquid crystals due to their comparatively high refresh rates, contrast ratios, power efficiencies, and capacity for vibrant color rendering. Inorganic light emitting diodes (ILEDs) can also form displays, with properties such as brightness, lifetime, and efficiency that can exceed those possible with OLEDs. These displays exist, however, only in ultralarge-area, low-resolution formats (square meters; billboard displays), limited by processing and assembly procedures that do not scale effectively to small (< ~200 μm by 200 μm), thin (< ~200 μm) light emitters or to dense, high-pixel count arrays. An ability to replace existing methods for fabricating ILEDs (i.e., wafer sawing, serial pick-and-place, wire bonding, and packaging on a device-by-device basis) and for incorporating them into displays (i.e., robotic assembly into tiles followed by interconnection using large quantities of bulk wiring) with those that more closely resemble the planar, batch processing of OLEDs greatly expands the application opportunities. Examples include not only ILED displays for desktop monitors, home theater systems, and instrumentation gauging, but also, when implemented in flexible or stretchable forms, wearable health monitors or diagnostics and biomedical imaging devices. In microscale sizes, such ILEDs can also yield semitransparent displays, with the potential for bidirectional emission characteristics, for vehicle navigation, heads-up displays, and related uses.

[0222] This example provides routes to create ultrathin, ultrasmall ILEDs in flat or "wavy" geometries and to assemble them into addressable arrays using scalable processing techniques, on substrates ranging from glass to plastic and rubber. The strategy includes four components: (i) epitaxial semiconductor multilayers designed for lateral delineation and release from a source wafer to yield isolated arrays of

ILEDs, each of which remains tethered to the wafer by polymeric "breakaway" anchor structures; (ii) printing techniques for manipulating the resulting ILEDs in schemes that enable formation of large-scale arrays on foreign substrates and in arbitrary spatial layouts; (iii) planar processing methods for establishing electrical interconnects to the devices, in direct or matrix addressable configurations; and (iv) integration strategies capable of yielding ILED displays in flexible or stretchable formats and with conventional, semitransparent, or bidirectional emission characteristics. Certain aspects build on previously reported procedures for etching and manipulating epitaxial semiconductor layers and for fabricating flexible and stretchable electronics.

[0223] Figure 1 presents aspects of the first two of the components. The epitaxial semiconductor layers include AlInGaP quantum well structures (6-nm-thick $In_{0.56}Ga_{0.44}P$ wells, with 6-nm-thick barriers of $Al_{0.25}Ga_{0.25}In_{0.5}P$ on top and bottom), cladding films (200-nmthick layers of $In_{0.5}Al_{0.5}P$:Zn and $In_{0.5}Al_{0.5}P$:Si for the p and n sides, respectively), spreaders (800-nm-thick layers of $Al_{0.45}Ga_{0.55}As$:C and $Al_{0.45}Ga_{0.55}As$:Si for the p and n sides, respectively), and contacts (5-nm-thick layer of GaAs:C and 500-nm-thick layer of GaAs:Si for the p and n sides, respectively), for a total thickness of ~2.523 μm, all grown on AlAs (1500-nm-thick layer of $Al_{0.96}Ga_{0.04}As$:Si) on a GaAs substrate (Figure 5). The AlAs can be removed by etching with hydrofluoric (HF) acid, in procedures that do not alter the overlying layers or the underlying substrate. The process for defining the ILEDs first involves forming a pattern of vertical trenches through the epitaxial layers by inductively coupled plasma reactive ion etching through a mask of SiO_2 defined photolithographically (Figure 6). This step determines the lateral geometries of the devices (Figure 5). Figure 1, A and B, shows top and cross-sectional scanning electron microscope (SEM) images collected after this etching process for a representative case, where the device islands in Figure 1 are 50 μm by 50 μm. Creating a pattern of photoresist posts (i.e., "breakaway" anchors) located at two of the four corners of each island, followed by immersion in concentrated HF, leads to the undercut release of an organized array of ILEDs. The anchors hold the devices in their lithographically defined locations to prevent liftoff into the etching bath, even after complete undercut (Figure 6). Next, an automated printing tool (Figure 7) brings a soft elastomeric stamp with features of relief embossed onto its surface into

aligned contact with a selected set of these ILEDs. Peeling the stamp away fractures the photoresist anchors and leaves the devices adhered via Van der Waals interactions to the raised regions of relief. Figure 1, C and D, shows schematic illustrations of the printing process and an SEM image of an array of anchored ILEDs on the source wafer after one cycle of printing (Figure 8). The white arrows in Figure 1D highlight the collection of ILEDs removed by this process, corresponding to every third device along the two orthogonal axes of the square array. Figure 1E provides an SEM image of these devices printed onto a glass substrate. The engineering design of the breakaway anchors is such that they are sufficiently robust to hold the ILEDs in their lithographically defined locations during the undercut etching and drying processes but sufficiently fragile to enable high-yield liftoff during printing. Three design aspects are the use of (i) a pair of anchors on the same side of each ILED, to yield, after undercut, suspended, "diving board" layouts (Figure 1F) that enable transfer of torques large enough to fracture the photoresist upon peel-back of the stamp; (ii) stamps with relief structures that are slightly smaller than the ILEDs and are offset from the centers of the devices to maximize these torques and also to minimize overlap with the anchors; and (iii) photoresist structures that fracture more readily than the semiconductor material. This type of anchoring scheme (i.e., heterogeneous anchoring) is much more efficient in active materials utilization and versatile in design choices than corresponding methods demonstrated previously for transistors and solar cells, where peripheral parts of the devices themselves serve as the anchors (i.e., homogeneous anchoring). Conventional wafer dicing and pick-and-place methods are not suitable for devices with the thicknesses and dimensions in the range reported here, due to challenges associated with wafer utilization, device fragility, and size. Such techniques also lack the high-throughput, parallel operation of the type of printing methods described above.

[0224] Figure 1G shows a micrograph of a densely packed array of anchored, undercut ILEDs on a source wafer. Figure 1H shows sparse assemblies of these devices formed by printing in a step-and-repeat fashion from this wafer to a glass substrate, coated with a thin (~10 mm) layer of poly(dimethylsiloxane) (PDMS) to promote dry, conformal adhesion. As examples of high yields, large areas, and compatibility with plastic substrates, Figure 1I presents images of collections of ILEDs printed onto a thin sheet of polyethylene terephthalate (PET, 50 μm thick),

shown as wrapped around a cylindrical glass support (1600 devices, in a square array with pitch of 1.4 mm; radius of cylinder ~25 mm) and onto a plate of glass (inset; 1600 devices, in a square array with pitch of 1.4 mm). The overall fabrication yields, including delineation and undercut of the ILEDs and subsequent printing of them onto the target substrates, were 100% in both cases. The devices were selected to have sizes (i.e., 250 μm by 250 μm) large enough to be visible in the images; those with sizes of Figure 1D are too small to be seen clearly at these scales.

[0225] Establishing electrical connections to these printed ILEDs yields lighting elements or addressable displays. The small thickness (~2.5 μm) of the devices enables the use of conventional thin-film processing, thereby providing a route to displays and related devices that is simpler, more scalable, and applicable to much smaller pixel geometries than established wire bonding and packaging techniques. To demonstrate the most basic scheme, we printed a collection of devices onto a thin, metal mesh on a transparent substrate, to form bottom contacts, and then established separate top contacts using a planar lithographic process (Figure 9). Figure 2, A and B, shows an exploded view schematic illustration and optical micrograph of an array of small, square devices (~25 μm by 25 μm), as well as those with shapes that spell "LED." The results indicate bright emission, even out to the edges of the devices, consistent with the relatively low surface recombination velocity in AlInGaP materials. For improved performance, ohmic contacts can be implemented by using established metallization and annealing schemes. One strategy involves additional processing on the source wafer to yield released devices with integrated ohmic contacts, suitable for printing and interconnection even on low-temperature substrates such as plastic or rubber. An alternative is to use low-temperature approaches to establish the ohmics directly on such substrates. For this work, we pursued the second strategy, using processes that involve temperatures below 175 °C (see Figure 10 for transmission line model analysis of the contact resistances). Figure 2C shows the layout of an ILED with ohmic contacts printed onto a thin layer of polyurethane on a glass substrate, and an optical micrograph of emission from a directly probed device. Figure 2, D and E, presents electrical and optical characteristics of a set of such devices, recorded on the wafer before undercut etching and after printing. The processing in this case used a passivation

scheme to eliminate moderate degradation in performance associated with the HF etching step on unprotected devices (Figure 11). The resulting current-voltage-emission behavior of the printed devices is comparable to that of the devices on the wafer. Figure 3A provides a schematic illustration of an interconnect scheme for passive matrix addressing. Photolithography and electron beam evaporation define patterned metal electrodes [Ti (20 nm)/Au (300 nm)] that connect p and n contacts (nonohmic for the cases of Figures 3 and 4) of devices in common columns and rows, respectively. Two spin-cast, photopatterned layers of epoxy (1.2 μm thick) provide openings to these contacts; the top layer electrically separates the column and row electrodes at their crossing points. Connecting terminal pads at the ends of these electrode lines to external computer control systems via ribbon cables that use anisotropic conductive films (ACFs) enables passive matrix addressing (see Figure 12 for details). Figure 3B shows images of a small display that uses this design, formed on a thin sheet of plastic (PET, 50 μm thick) with a layer of a photocurable polyurethane as an adhesive. The ILEDs have dimensions of 100 μm by 100 μm and are configured into a 16 by 16 square array. The yields on the individual pixels for the case of Figure 3B are 100%; at the level of the display, one column and two rows do not function, due to breaks in the contacts to the ACF ribbon cable [Figure 13; see Figure 14 for an example of similar display with even smaller ILEDs (50 μm by 50 μm)]. Such systems can be bent to radii of curvature of ~7 mm, with no observable degradation, even for several hundred cycles of bending (Figure 14). Analytical calculation shows that even at the minimum bend radius investigated here, the maximum strain in the ILED is 0.21%, with a somewhat smaller strain (0.19%) in the quantum well region. Analysis using literature parameters to determine the dependence of the bandgap on strain suggests changes in emission wavelength of ~2.4 nm for the smallest bend radius. As shown in Figure 1, step-and-repeat printing can yield systems that cover areas much larger than those of the constituent ILEDs or the source wafer. One important outcome is the ability to form displays that can offer an effectively high level of transparency, where only the ILEDs (and the electrodes, if they are not made with transparent conductors) are opaque. Figure 3, C and D, shows examples of a 16 by 16 array, formed on glass. Here the area of the display is ~325 mm^2; the cumulative area of all the ILEDs is only ~2.5 mm^2, corresponding to less than ~1% of the display area. Figure 3C illustrates the operation of such a system positioned above a sheet of paper with printed logos; the

focus of the image is on the paper, thereby illustrating a practical level of transparency for application in a heads-up display, for example. Figure 3D shows the same device (lower right), operating in front of a mirror (upper left) to demonstrate bidirectional emission characteristics. The inset provides a magnified view of a region of this display, in its off state to show the small sizes of the ILEDs compared to the unit cells. These layouts are important for many applications, due to the efficient utilization of the LED material, for reduced cost. For the examples shown, we achieved ~98% yields on the individual devices, and ~80% yields on the interconnections, limited by breaks in the metal lines and failed contacts to the ACF ribbon cable (Figure 16).

[0226] The devices and integration methods reported here are compatible with strategies to produce stretchable electronics, thereby providing a route to conformable displays and lighting systems of the type that might be interesting for integration with the human body and other curvilinear, deformable surfaces, all of which demand more than simple bending (e.g., Figure 3B). Figure 4A shows an example of a stretchable ILED with the shape of a ribbon. This device was formed by transfer printing and bonding to a prestrained, rubber substrate of PDMS. Relaxing the prestrain creates a device with a "wavy," sinusoidal profile; this structure responds elastically to applied strain with a physics similar to that of an accordion bellows to yield a stretchable ILED device. The top panels provide finite element simulation of the mechanics of the system in compressed (left) and stretched (right) configurations. The results indicate maximum strains in the ILED and the quantum well region of 0.36 and 0.053%, respectively (see SOM for details). The bottom panels show optical micrographs in the off (top) and on (bottom) states, with and without external illumination, respectively, in configurations similar to those illustrated in Figure 22A. The emission characteristics show no noticeable change in color with applied strain or associated changes in device geometry from "wavy" to flat (see Figures 17 and 18 for details). This observation is consistent with a calculated change in emission wavelength of less than ~0.7 nm based on our computed strain values and analysis similar to that performed for the flexible display.

[0227] The "wavy" strategy of Figure 4A can accommodate only a relatively modest range of applied strains (i.e., up to a few percent, for the designs reported here). A

path to displays with high levels of stretchability uses non-coplanar mesh designs adapted from schemes reported for integrated circuits. Figure 4B presents optical micrographs of such a system, composed of a 16 by 16 square array of ILEDs bonded to a PDMS substrate and interconnected by electrodes supported by arc-shaped bridges, with a fraction of the pixels turned on (overall yield >80%) (see Figure 19 for details). The shapes of these bridges change in response to deformations of the display, in a way that isolates the ILEDs from any significant strains (Figures 20 and 21). In particular, calculation shows that for strains of 24%, as defined by the change in separation between inner edges of adjacent device islands, the maximum strains in the ILED and quantum well are only 0.17 and 0.026%, respectively. The computed change in emission wavelength is less than ~0.3 nm. Figure 4C provides optical micrographs of four pixels in this display, in their off and on states, with (top) and without (bottom) external illumination, respectively, in compressed and stretched configurations. The images show the expected reduction in the heights of the arc-shaped bridges that lie in the direction of the applied tensile force (i.e., along the interconnects that run from lower left to upper right), together with an increase in the heights of the bridges in the orthogonal direction, due to the Poisson effect. This mechanical response is fully elastic – the bending-induced strains in the interconnects are small, the strains in the ILEDs are negligible, and the strain in the PDMS is well within its linear response regime. The data in Figure 4, D and E, are consistent with this mechanics, as are the associated mechanics calculations. In particular, the current-voltage characteristics of a typical device do not change in a measurable way for applied strains up to ~22%, and we observe no degradation on cycling up to a few hundred times (500 times). Recent work demonstrates the use of smaller collections of large, conventional ILEDs in deformable devices that use different designs.

[0228] The schemes reported here for creating thin, small inorganic LEDs and for integrating them into display and lighting devices create design options that are unavailable with conventional procedures. The planar processing approaches for interconnect resemble those that are now used for organic devices and, for example, large-area electronics for liquid crystal displays, thereby conferring onto inorganic LED technologies many of the associated practical advantages. In large area, high–pixel count systems (e.g., 1 million pixels per square meter), the ability to use LEDs

with sizes much smaller than those of the individual pixels is important to achieve efficient utilization of the epitaxial semiconductor material, for reasonable cost. The minimum sizes of devices reported here are limited only by the resolution and registration associated with manual tools for photolithography.

MATERIALS AND METHODS

[0229] The materials and methods for this project, including epitaxial semiconductor multilayer design, polymeric anchor structures, large scale printing techniques, and electrical interconnection in direct or matrix addressable configurations, are described in the following, for the flexible display, the large area display, the array of inorganic light emitting diode (ILED) devices with ultrasmall sizes/arbitrary shapes, the wavy ribbon devices, and the stretchable display.

Preparation of ILEDs

[0230] Figure 5 shows the epi-stack design for our ILEDs, capable of release from a source wafer by undercut etching, grown on a GaAs wafer (Epiworks, Inc.). The sequence of processing steps used to retrieve ILEDs array appears below. Polymeric anchor structures support the ILEDs during undercut etching of the $Al_{0.96}Ga_{0.04}As$ sacrificial layer (Figure 6).

Processing Scheme for Preparing ILEDs from a Source Wafer

[0231] Delineating the ILEDs

[0232] 1. Clean an epi-stack ILED wafer chip (acetone, isopropyl alcohol (IPA), deionized (DI) water).

[0233] 2. Deposit 800 nm SiO_2 by plasma enhanced chemical vapor deposition (plasma enhanced chemical vapor deposition (PECVD); PlasmaTherm SLR).

[0234] 3. Pretreat with hexamethyldisilazane (HMDS) for 1 min.

[0235] 4. Pattern photoresist (PR; Clariant AZ5214, 3000 rpm, 30 sec) with 365 nm optical lithography through an iron oxide mask (Karl Suss MJB3). Develop in aqueous base developer (Clariant AZ327 MIF) and bake on hot plate (110 °C, 3 min).

[0236] 5. Etch oxide with buffered oxide etchant (BOE; Fisher, 130 sec).

[0237] 6. Etch with an inductively coupled plasma reactive ion etcher (ICP-RIE; Unaxis SLR 770 System, 2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W, ~21 min).

Undercut etching of the ILEDs

[0238] 7. Clean the processed wafer chip from step 6 above with HF (Fisher, 49%, diluted 10:1, 2 sec).

[0239] 8. Pattern PR and bake at 110 °C for 5 min to form polymeric anchors at the corners of the μ-ILEDs.

[0240] 9. Dip the wafer chip in diluted HF (Fisher, 49%, diluted 100:1) for an appropriate time (μ-ILEDs with 50 μm x 50 μm dimension: ~4 hrs, 100 μm x 100 μm: ~5.5 hrs) to remove the $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the ILEDs. Rinse by-product using DI water at 1.5 hr intervals.

Device Fabrication

[0241] Processing Scheme for ILED devices of Figure 2A; schematic illustration of these steps appears in Figure 9.

[0242] Preparing a substrate with metal mesh

[0243] 1. Deposit 300 nm SiO_2 with PECVD onto a silicon wafer

[0244] 2. Pretreat surface with HMDS for 1 min, and then pattern PR.

[0245] 3. Deposit 7/70 nm of Cr/Au by electron beam evaporation.

[0246] 4. Lift-off PR in acetone to yield a pattern of Cr/Au in the geometry of a mesh.

[0247] 5. Etch oxide with HF (49%, 38 sec).

[0248] 6. Transfer print mesh to a glass substrate coated with poly(dimethylsiloxane) (PDMS; Sylgard 184, Dow Corning, spun at 600 rpm/5 sec, 3000 rpm/30 sec, cured in oven at 70 °C for 90 min) formed by mixing the base and curing agent with a ratio of 10:1 followed by thermal curing.

[0249] Printing the ILEDs

[0250] 7. Liftoff ILEDs using a flat PDMS stamp formed by mixing the base and curing agent with a ratio of 8.5:1.5, and then thermally cure.

[0251] 8. Print ILEDs onto the glass substrate with Cr/Au mesh (n-contact).

[0252] 9. Remove PR by washing in acetone.

[0253] Forming the interlayer and p-contact metallization

[0254] 10. Spin coat the substrate from step 9 with a photodefinable epoxy (SU8-2, Microchem, spun at 1,500 rpm for 30 s). Soft bake at 65 °C and 95 °C for 1 min and 1.5 min, respectively.

[0255] 11. Pattern epoxy by exposing to ultraviolet (UV) light in a mask aligner for 14 sec, baking at 95 °C for 2 min, developing (SU8 developer, Microchem) for 15 sec, rising (IPA), and curing (110 °C, 35 min, slow cooling).

[0256] 12. Pattern PR.

[0257] 13. Deposit 7 nm of Pd-Au by sputtering.

[0258] 14. Lift-off PR in acetone to leave a thin layer of Pd-Au on the top surfaces of the ILEDs (pcontact).

[0259] Processing Scheme for ILED devices with ohmic contacts of Figure 2C

[0260] Preparing the substrate

[0261] 1. Clean a glass slide (25 mm X 25 mm) (acetone, IPA, DI water)

[0262] 2. Expose to ultraviolet induced ozone (UVO) for 5 min.

[0263] 3. Spin coat with polyurethane (NOA61; Norland Products Inc., spun at 5000 rpm/60 sec).

[0264] Delineating the ILEDs

[0265] 4. Clean an epi-stack ILED wafer chip (acetone, IPA, DI water).

[0266] 5. Deposit 800 nm SiO_2 with PECVD.

[0267] 6. Pretreat with HMDS for 1 min.

[0268] 7. Pattern PR and bake on hot plate (110°C, 3 min).

[0269] 8. Etch oxide with BOE (130 sec).

[0270] 9. Etch with ICP-RIE (2 mTorr, Cl_2 4 sccm, H_2 2 sccm, Ar 4 sccm, RF1: 100 W, RF2: 500 W, ~16 min) to expose $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the ILEDs.

[0271] Forming a passivation layer and undercut etching of the ILEDs

[0272] 10. Clean the processed wafer chip from step 9 above (acetone, IPA, DI water).

[0273] 11. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65°C and 110°C each for 1 min and 1 min, respectively.

[0274] 12. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing. The pattern includes a passivation structure to protect μ-ILEDs and an anchor structure to suspend ILEDs during the undercut etching.

[0275] 13. Dip the wafer chip in diluted HF (49%, diluted 100:1) for ~2 hrs to remove the $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the μ-ILEDs.

[0276] Printing the ILEDs

[0277] 14. Liftoff ILEDs using a flat PDMS stamp formed by mixing the base and curing agent with a ratio of 10:1, followed by thermal curing. Contact 'inked' stamp against the substrate from step 13.

[0278] 15. Retrieve the stamp after UV exposure (through the stamp) for 20 min. Cure the polyurethane layer by UV exposure for 2 hours.

[0279] Defining the n-contact regions

[0280] 16. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, ~12 min) to remove the epoxy on the top surface of the ILEDs.

[0281] 17. Pattern PR and bake at 110 °C for 2 min.

[0282] 18. Wet etch C-doped p-GaAs/p-spreader($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (volume ratio 1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped nspreader ($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

[0283] 19. Remove PR by washing in acetone.

[0284] Defining the n-ohmic contact metallization

[0285] 20. Pattern PR.

[0286] 21. Clean the surface of n-GaAs with HCl : DI water (1:1) for 30 sec.

[0287] 22. Deposit 5/35/70 nm of Pd/Ge/Au by electron beam evaporation.

[0288] 23. Lift-off PR in acetone to remain Pd/Ge/Au on the top surface of n-GaAs.

[0289] 24. Anneal at 175 °C for 60 min under N_2 ambient

[0290] Defining the p-ohmic contact metallization

[0291] 25. Pattern PR.

[0292] 26. Clean the surface of p-GaAs with HCl : DI water (1:1) for 30 sec.

[0293] 27. Deposit 10/40/10/70 nm of Pt/Ti/Pt/Au by electron beam evaporation.

[0294] 28. Lift-off PR in acetone to remain Pt/Ti/Pt/Au on the top surface of p-GaAs.

Processing Scheme for Flexible ILED Displays of Figure 3B

[0295] Preparing the substrate

[0296] 1. Clean a glass slide (30 mm X 30 mm) (acetone, IPA, DI water).

[0297] 2. Treat with ultraviolet induced ozone (UVO) for 5 min.

[0298] 3. Spin coat with PDMS (spun at 600 rpm/5 sec, 3000 rpm/30 sec), formed by mixing the base curing agent with a ratio of 10:1.

[0299] 4. Cure PDMS in an oven (70 °C, 90 min).

[0300] 5. Clean a sheet of polyethylene terephthalate (PET; Grafix DURA-LAR, 32 mm X 32 mm X 50 μm) (IPA, DI water).

[0301] 6. Laminate the PET sheet onto the PDMS coated glass slide, as a carrier for the following processing steps.

[0302] 7. Spin coat with polyurethane (NOA61; Norland Products Inc., spun at 5000 rpm/60 sec).

[0303] Printing the ILEDs

[0304] 8. Liftoff an array of ILEDs (16x16 array of devices with dimensions of 100μm x 100μm) using a flat PDMS stamp. Contact 'inked' stamp against the substrate from step 7.

[0305] 9. Retrieve the stamp after UV exposure (through the stamp) for 20 min.

[0306] 10. Remove PR by washing in acetone and then cure the polyurethane layer by UV exposure for 2 hours.

[0307] Defining the n-contact regions

[0308] 11. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, 8 min) to remove the polyurethane layer covering the ILEDs.

[0309] 12. Pattern PR and bake at 110 °C for 2 min.

[0310] 13. Wet etch C-doped p-GaAs/p-spreader($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (volume ratio 1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped nspreader ($Al_{0.45}Ga_{0.55}As$) by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

[0311] 14. Remove PR by washing in acetone.

[0312] Defining the n-contact metallization

[0313] 15. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65°C and 110°C each for 1 min and 1 min, respectively.

[0314] 16. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing.

[0315] 17. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

[0316] 18. Pattern PR and bake at 110 °C for 2 min.

[0317] 19. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant (Transene, Inc.).

[0318] 20. Remove PR by washing in acetone.

[0319] Defining the p-contacts and p-contact metallization

[0320] 21. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65 °C and 110°C for 1 min and 1 min, respectively.

[0321] 22. Pattern epoxy by exposing to UV, developing, rising, and curing.

[0322] 23. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

[0323] 24. Pattern PR and bake at 110 °C for 2 min.

[0324] 25. Wet etch Ti/Au for 45/90s by BOE and Au etchant.

[0325] 26. Remove PR by washing in acetone.

[0326] Forming an encapsulation layer

[0327] 27. Spin coat with epoxy (SU8-5, Microchem, spun at 3,000 rpm for 30 s). Soft bake at 65°C and 110°C for 1 min and 1.5min, respectively.

[0328] 28. Pattern epoxy by exposing to UV for 14 sec, baking at 95°C for 2 min, developing (SU8 developer) for 18 sec, rising (IPA), and curing (110 °C, 35 min, slow cooling)

Processing Scheme for Large Area ILEDs Displays of Figures 3, C and D

[0329] Preparing the substrate

[0330] 1. Clean a glass slide (50 mm X 50 mm) (acetone, IPA, DI water)

[0331] 2. Deposit 50 nm of Ti by electron beam evaporation.

[0332] 3. Pattern PR and bake on a hot plate (110 °C, 2 min) to form guide lines to assist in registration of ILEDs printed with an automated printer system.

[0333] 4. Wet etch Ti with BOE (70 sec).

[0334] 5. Remove PR by washing in acetone.

[0335] 6. Expose to ultraviolet induced ozone (UVO) for 15 min.

[0336] 7. Spin coat with PDMS (spun at 600 rpm/5 sec, 2500 rpm/30 sec) formed by mixing the base and curing agent with a ratio of 10:1.

[0337] 8. Cure PDMS in an oven (70 °C, 90 min)

[0338] Printing the ILEDs

[0339] 9. Selectively liftoff ILEDs (100μm x 100μm lateral dimensions) using a composite stamp in automated printing machine (Figures 7, 8) and print them onto the substrate from step 8, in a step and repeat fashion to form a 16x16 array.

[0340] 10. Remove PR by washing in acetone.

[0341] Patterning the p-contact metallization

[0342] 11. Spin coat with epoxy (SU8-2, spun at 1,500 rpm for 30 s). Soft bake at 65 °C and 110 °C for 1 min and 1min, respectively.

[0343] 12. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

[0344] 13. Deposit 10/70 nm of Ti/Au by electron beam evaporation.

[0345] 14. Pattern PR and bake at 110 °C for 2 min.

[0346] 15. Wet etch Ti/Au with BOE and gold etchant for 35/20 sec.

[0347] 16. Remove PR by washing in acetone.

[0348] 17. Reactive ion etch (RIE, 50 mTorr, 20 sccm O_2, 100 W, 13 min) to remove remaining epoxy around the sidewalls of the ILEDs (Figure 12).

[0349] Defining the n-contact regions

[0350] 18. Pattern PR and bake at 110 °C for 2 min.

[0351] 19. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

[0352] 20. Remove PR by washing in acetone.

[0353] Patterning the n-contact metallization

[0354] 21. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65 °C and 110 °C for 1 min and 1 min, respectively.

[0355] 22. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

[0356] 23. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

[0357] 24. Pattern PR and bake at 110 °C for 2 min.

[0358] 25. Wet etch Ti/Au for 45/90 sec with BOE and Au etchant.

[0359] 26. Remove PR by acetone rinse.

[0360] Defining the p-contact regions and metallization

[0361] 27. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65 °C and 110 °C for 1 min and 1 min, respectively.

[0362] 28. Pattern epoxy with exposing UV, developing, rising, and curing.

[0363] 29. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

[0364] 30. Pattern PR and bake at 110 °C for 2 min.

[0365] 31. Wet etch Ti/Au for 45/90s by BOE and Au etchant.

[0366] 32. Remove PR by acetone.

[0367] Forming an encapsulation layer

[0368] 33. Spin coat with epoxy (SU8-5, spun at 3,000 rpm for 30 s). Soft bake at 65 °C and 110°C for 1 min and 1.5min, respectively.

[0369] 34. Pattern epoxy by exposing to UV, baking, developing, rising, and curing.

Processing Scheme for stretchable ILEDs of Figure 4A

[0370] Exploded view schematic illustration of the processing step appears in Figure 18.

[0371] Preparing ribbon shaped ILEDs

[0372] 1. Clean an epi-stack ILED wafer chip (acetone, IPA, DI water).

[0373] 2. Pattern PR and bake for 2 min.

[0374] 3. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 35 sec to expose $Al_{0.96}Ga_{0.04}As$ (sacrificial layer) underneath the μ-ILEDs.

[0375] 4. Remove PR by washing in acetone.

[0376] Forming an encapsulation layer and undercut etching

[0377] 5. Pattern PR on the top surface of the ribbons.

[0378] 6. Deposit 3/15 nm of Ti/Au by electron beam evaporation.

[0379] 7. Lift-off PR in acetone to remain Ti/Au on the top surface of the ribbons.

[0380] 8. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65 °C and 95 °C for 1 min and 1.5min, respectively.

[0381] 9. Pattern epoxy by exposing to UV, baking, developing, rising (IPA), and curing.

[0382] 10. Dip the ILED in diluted HF (100:1) for 1 hr to release the ribbons from the wafer.

[0383] 11. Rinse in DI water for 5 min.

[0384] 12. Print ribbons onto a pre-strained substrate of PDMS with prepatterned metal lines.

Processing Scheme for Stretchable ILED Display of Figures 4, B and C

[0385] Schematic illustration of the processing steps appears in Figure 20.

[0386] Preparing the carrier substrate

[0387] 1. Clean a glass slide (25 mm X 25 mm) (acetone, IPA, DI water).

[0388] 2. UVO treatment for 5 min.

[0389] 3. Spin coat with PMMA (A2, Microchem, spun at 3,000rpm for 30 sec).

[0390] 4. Anneal at 180 °C for 3 min.

[0391] 5. Spin coat with polyimide (PI, poly(pyromellitic dianhydride-co-4,4' -oxydianiline), amic acid solution, Sigma-Aldrich, spun at 4,000 rpm for 60 sec).

[0392] 6. Anneal at 110 °C for 3 min and 150 °C for 10 min.

[0393] 7. Anneal at 250 °C for 50 min in N_2 atmosphere.

[0394] 8. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65 °C and 95 °C for 1 min and 1 min, respectively.

[0395] Printing the ILEDs

[0396] 9. Liftoff ILEDs (16x16 array of devices with dimensions of 50 μm x 50 μm) using a flat PDMS stamp and contact the 'inked' stamp with the substrate from step 8.

[0397] 10. Remove the stamp after UV exposure (through the stamp) for 60 sec and baking at 110 °C for 10 min.

[0398] 11. Remove PR by washing with acetone. Fully cure the epoxy layer at 150 °C for 20 min.

[0399] Forming the sidewall region

[0400] 12. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65 °C and 95 °C for 1 min and 1 min, respectively.

[0401] 13. Expose to UV for 14 sec and bake at 110 °C for 1 min.

[0402] 14. Anneal at 150 °C for 20 min.

[0403] 15. Reactive ion etch (RIE; PlasmaTherm 790 Series, 50 mTorr, 20 sccm O_2, 100 W, 13 min) to remove remaining epoxy around the sidewalls of the ILEDs.

[0404] Defining the n-contact regions

[0405] 16. Pattern PR and bake at 110 °C for 5 min.

[0406] 17. Wet etch C-doped p-GaAs/p-spreader by $H_3PO_4/H_2O_2/H2O$ (1:13:12) for 25 sec, InGaP-based active region by HCl/H_2O (2:1) for 15 sec and Si-doped n-spreader by $H_3PO_4/H_2O_2/H_2O$ (1:13:12) for 23 sec to expose Si-doped n-GaAs.

[0407] 18. Remove PR by washing with acetone.

[0408] Defining the n- and p-contact metallization

[0409] 19. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65 °C and 95°C for 1 min and 2 min, respectively.

[0410] 20. Pattern epoxy by exposing to UV for 14 sec, developing for 15 sec, rising, and curing (110 °C, 35 min, slow cooling).

[0411] 21. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

[0412] 22. Pattern PR and bake at 110 °C for 2 min to define n-contact electrodes, designed as line patterns connected to n-GaAs, and p-contact electrodes, designed as line patterns that avoid crossing over the n-contact electrodes (Figure 20).

[0413] 23. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant.

[0414] 24. Remove PR by washing with acetone.

[0415] Interconnecting the p-contact metallization

[0416] 25. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 sec). Soft bake at 65 °C and 95 °C for 1 min and 2min, respectively.

[0417] 26. Pattern epoxy by exposing to UV, developing, rising, and curing.

[0418] 27. Deposit 20/300 nm of Ti/Au by electron beam evaporation.

[0419] 28. Pattern PR and bake at 110 °C for 2 min.

[0420] 29. Wet etch Ti/Au for 45/90 sec by BOE and Au etchant.

[0421] 30. Remove PR by washing with acetone.

[0422] Forming and encapsulation layer

[0423] 31. Spin coat with epoxy (SU8-2, spun at 3,000 rpm for 30 s). Soft bake at 65 °C and 95 °C for 1 min and 1.5min, respectively.

[0424] 32. Pattern epoxy by exposing to UV, developing, rising, and curing.

[0425] Forming the island/bridge structures

[0426] 33. Deposit 150 nm SiO_2 by PECVD.

[0427] 34. Pattern PR and bake at 110 °C for 2 min.

[0428] 35. RIE (50 mTorr, CF_4/O_2 40/1.2 sccm, 150 W, 8 min) to etch SiO_2.

[0429] 36. RIE (150 mTorr, O_2 20 sccm, 150 W, 50 min) to etch epoxy/PI layers.

[0430] 37. Etch oxide with BOE (20 sec).

[0431] Transferring the mesh

[0432] 38. Immerse the ILEDs array mesh from step 37 in acetone (80 °C) for ~10 min to dissolve the PMMA.

[0433] 39. Lift off the mesh using a PDMS stamp formed by mixing a base and agent with a ratio of 8.5:1.5.

[0434] 40. Selectively deposit 5/30 nm of Ti/SiO_2 by electron beam evaporation on the bottom of island regions through a shadow mask.

[0435] 41. Transfer the ILED mesh to a biaxially pre-strained PDMS substrate.

[0436] 42. Anneal in an oven at 70 °C and release the strain.

Measurement of Emission Spectra

[0437] Emission spectra were measured using a spectrometer (Oceanoptics, HR4000) which enabled signal collected through an optical fiber directly mounted in an electrical probing station.

Measurement of Surface Profile of Wavy ILEDs

[0438] The wavelength and amplitude of stretchable ILEDs of Figure 4A were measured by a surface profiler (Sloan Dektak3). A diamond stylus in contact with a sample surface scans along the length of ribbon and measures physical surface variation at different positions.

Bending Test

[0439] To evaluate the bending performance of flexible ILEDs displays, bending test were performed (Figures 16A, B). The displays were bent and released, with bend radii down to ~ 7.3 mm. The electrical properties of 32 different pixels in the display were measured and averaged to assess the performance.

Fatigue Test

[0440] To evaluate the fatigue performance of flexible ILED displays, multiple cycling tests were performed under repetitive bending and releasing up to 500 times (Figure 16C, D). Electrical measurements were performed on 16 different pixels, for a bend radius of ~ 8.8 mm. Stretching tests were performed with mechanical stages capable of applying uniaxial strain to evaluate the performance of stretchable ILED display under repetitive stretching and releasing up to 500 times (Figure 4). Electrical properties of 14 different pixels in the display were measured and averaged. In all cases, the testing was performed at a rate of roughly one cycle per second.

Modeling of Flexible ILED Displays of Figure 3B

[0441] The encapsulation, electrode, ILED, adhesive and plastic shown in Figure 12 can be modeled as a composite beam subject to a bend curvature. The distance between the neutral mechanical plane and the top surface in each cross section is given by $\sum_{i=1}^{N}\overline{E}_i h_i\left(\sum_{j=1}^{i}h_j-\frac{h_i}{2}\right)\Big/\sum_{i=1}^{N}\overline{E}_i h_i$, where N is the total number of layers, h_i is the thickness of the i^{th} layer (from the top), and $\overline{E}_i h_i/1-\nu_i^2$ is related to the Young's modulus E_i and Poisson's ratio ν_i of the i^{th} layer. The strain in the μ-ILED, including the quantum well, is given by y/R, where R is the bend radius, and y is the distance from the neutral mechanical plane. The elastic properties and layer thicknesses used for bendable display are (1) $E_{encapsulation}$ = 4.4 GPa, $\nu_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 4.0 μm and $h_{encapsulation2}$ = 0.877 μm for the two encapsulation layers above and below the electrode, respectively; (2) $E_{electrode}$ = 78 GPa, $\nu_{electrode}$ = 0.44, and $h_{electrode}$ = 300 nm; (3) E_{ILED} = 77.5 GPa, ν_{ILED} = 0.312, and h_{ILED} = 2.523 μm; (4) $E_{adhesive}$ = 1 GPa, $\nu_{adhesive}$ = 0.3, and $h_{adhesive}$ = 2.5 μm; and (5) $E_{plastic}$ = 4 GPa, $\nu_{plastic}$ = 0.44 and $h_{plastic}$ = 50 μm. These give the neutral mechanical plane 19.76 μm below the top surface. The maximum distance from the ILED is then 14.58 μm to the neutral mechanical plane, which gives the maximum strain 0.21% in the ILED for the bend radius R = 7 mm. The quantum well is 1.011 μm below the top surface of ILED (Figure 5), and is therefore 13.57 μm to the neutral mechanical plane. This gives the maximum strain 0.19% for the bent radius R = 7 mm.

Modeling and Simulation of Stretchable ILEDs of Figure 4A: the Wavy Design

[0442] As shown in Figure 18A, the stretchable ILED consists of the encapsulation, electrode and μ-ILED, and can be modeled as a composite beam with the effective tensile stiffness $\overline{EA}=\sum_{i=1}^{3}\overline{E}_i h_i$ and bending stiffness $\overline{EI}=\sum_{i=1}^{3}\overline{E}_i h_i\left[\left(\sum_{j=1}^{i}h_j\right)^2-\left(\sum_{j=1}^{i}h_j\right)h_i+\frac{h_i^2}{3}\right]-\frac{\left[\sum_{i=1}^{3}\overline{E}_i h_i\left(\sum_{j=1}^{i}h_j-\frac{h_i}{2}\right)\right]^2}{\overline{EA}}$, where the summation is for the 3 layers of encapsulation, electrode and ILED, h_i is the thickness of the i^{th}

layer (from the top), and $\overline{E}_i = E_i/(1-\nu_i^2)$ is related to the Young's modulus E_i and Poisson's ratio ν_i of the i^{th} layer. The distance between the neutral mechanical plane and the top surface in each cross section is given by $\sum_{i=1}^{3}\overline{E}_i h_i\left(\sum_{j=1}^{i}h_j - \frac{h_i}{2}\right)\Big/\overline{EA}$.

[0443] The device was formed by transfer printing and bonding to a pre-strained substrate of PDMS. Relaxing the pre-strain creates a device with a 'wave' of the amplitude A and wavelength λ. The bending energy and membrane energy of the wavy device are $U_{bending} = \frac{4\pi^4 \overline{EI} L A^2}{\lambda^4}$ and $U_{membrane} = \frac{1}{2}\overline{EA}L\left[\pi^2\left(\frac{A}{\lambda}\right)^2 + \varepsilon_{pre}\right]^2$, where L is the length of device and ε_{pre} (<0) is the compressive strain on the device upon the release of the pre-strain in the PDMS.

[0444] The strain energy in the PDMS substrate due to the sinusoidal displacement profile on its top surface is $U_{substrate} = \overline{E}_s L\frac{\pi A^2}{4\lambda}$, where $\overline{E}_s = E_s/(1-\nu_s^2)$ is related to the Young's modulus E_s and Poisson's ratio ν_s of the PDMS substrate. The minimization of the total energy $U_{total} = U_{bending} + U_{membrane} + U_{substrate}$ gives analytically the wave length and amplitude as

$$\lambda = 2\pi\left(\frac{4\overline{EI}}{\overline{E}_s}\right)^{1/3}, \qquad (1)$$

$$A = \frac{\lambda}{\pi}\sqrt{|\varepsilon_{pre}| - \varepsilon_{crit}}, \qquad (2)$$

where $\varepsilon_{crit} = \frac{3}{2}\left[\frac{\overline{EI}\,\overline{E}_s^2}{2(\overline{EA})^3}\right]^{1/3}$ is the critical strain for buckling.

[0445] The strain in the ILED, including the quantum well, is given by $4\pi^2\frac{A}{\lambda^2}y$, where y is the distance from the neutral mechanical plane. The elastic properties and layer thicknesses used for the device are (1) $E_{encapsulation}$ = 4.4 GPa, $\nu_{encapsulation}$ = 0.44, and $h_{encapsulation1}$ = 1 μm; (2) $E_{electrode}$ = 78 GPa, $\nu_{electrode}$ = 0.44, and $h_{electrode}$ = 10 nm; and (3) E_{ILED} = 77.5 GPa, ν_{ILED} = 0.312, and h_{ILED} = 2.523 μm. These give the neutral mechanical plane 2.22 μm below the top surface. The maximum distance

from the ILED is then 1.31 μm from the neutral mechanical plane, which gives the maximum strain 0.36% in the ILED for the experimentally measured wavelength 275 μm and amplitude 5.15 μm. The quantum well is 1.011 μm below the top surface of ILED (Figure 5), and is therefore 0.2 μm to the neutral mechanical plane, which gives a very small strain 0.053% in the quantum well.

[0446] The finite element method has also been used to determine the strains in the 1.0 μm-thick SU8 encapsulation, 10 nm-thick Au thin film and 2.523 μm-thick ILED on 1 mm-thick PDMS substrate. Eight-node, hexahedral brick elements (C3D8) and four-node multi-layer shell elements (S4R) in the finite element analysis software ABAQUS (2007) are used for the substrate and the thin film, respectively. The multi-layer shell is bonded to the substrate by sharing the nodes. Each layer of thin film is linear elastic, while the PDMS substrate is modeled as a hyper-elastic material. The eigenvalues and eigenmodes of the system are first obtained. The eigenmodes are then used as initial small geometrical imperfections to trigger buckling of the system. The imperfections are always small enough to ensure that the solution is accurate. As shown in Figure 4A and Figure 23, the numerical results give strains that agree very well with the analytical model.

Simulation of Stretchable ILED of Figures 4, B and C: the Island-Bridge Design

[0447] The finite element method has also been used to determine the strains in island-bridge design of stretchable ILED shown in Figure 20. Eight-node, hexahedral brick elements (C3D8) in the finite element analysis software ABAQUS (2007) are used for the substrate, which is modeled as a hyper-elastic material. Four-node, multi-layer shell elements (S4R) are used for the islands and bridges, which are linear elastic. The islands are bonded to the substrate by sharing the nodes, but the bridges do not. Figure 24 shows the strain distribution in the top, middle and bottom surfaces of the ILED as the bridge length is reduced from 310 μm to 250 μm. The maximum strain is 0.17%, and that in the quantum well is only 0.026%.

Analysis of Flexible/Stretchable ILED System for Strain Sensitivity of Emission Wavelength

[0448] The calculated maximum uniaxial strains in the quantum well of the ILED system are 0.19% tensile in flexible ILED displays, 0.053% tensile in stretchable ILED, and 0.026% compressive in stretchable ILED displays. On the basis of the *kp*

perturbation theory *(S1, 2)* for strain induced effect on semiconductor band structures, emission wavelength shift of the ILED associated with bending or stretching can be evaluated.

[0449] The bending and stretching deformations explored correspond to in-plane uniaxial stress defined as in the x direction here, and the stresses in the y and z directions are zero ($\sigma_{yy} = \sigma_{zz} = 0$) due to free contraction by Poisson's effect. Thus the strains in these directions are given by $\varepsilon_{yy} = \varepsilon_{zz} = -\nu\varepsilon_{xx}$, where $\frac{\nu}{1-\nu} = \frac{C_{12}}{C_{11}}$, and ν is Poisson's ratio, C_{11} and C_{12} are elastic stiffness constants. For the small stress range examined here, the strain induced bandgap shifts for heavy hole (HH) and light hole (LH) are given by $\delta Eg^{LH} = \delta E_H + \delta E_S$, $\delta Eg^{HH} = \delta E_H - \delta E_S$, where $\delta E_H = a(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz})$, $\delta E_S = \frac{b}{2}(\varepsilon_{xx} + \varepsilon_{yy} - 2\varepsilon_{zz})$, and δE_H, and δE_S are the hydrostatic pressure shift and the uniaxial stress-induced valence-band splitting, respectively *(S1-3)*, and *a* and *b* are the corresponding deformation potentials.

[0450] For the quantum well ($In_{0.56}Ga_{0.44}P$) in the ILED structure, the parameters used for the present calculation are *a* = -7.42 eV, *b* = 1.91 eV, C_{11}= 11.936x10^{11} dyne/cm^2, and C_{12} = 5.975x10^{11} dyne/cm^2 *(S4)*. Assuming HH is the ground state for the quantum well *(S4)*, the maximum uniaxial mechanical stress induced bandgap shift in the ILED system studied here is calculated to be ~7.1 meV (or ~2.4 nm). This small shift can be considered negligible for most applications.

Example 2: Electrically Interconnected Assemblies of Microscale Device Components by Printing and Molding

[0451] This example presents approaches for deterministic assembly and electrical interconnection of micro/nanoscale devices into functional systems with useful characteristics. Transfer printing techniques provide deterministic control over an assembly process that occurs prior to or simultaneously with a soft lithographic molding step that defines relief features in a receiving polymer. Filling these features with conducting materials that are processable in the form of liquids or pastes yields integrated interconnects and contacts aligned to the devices. Studies of the underlying aspects and application to representative systems in photovoltaics and solid state lighting indicators provide insights into the process and its practical use.

[0452] Unusual microsystems for electronics/optoelectronics, solid state lighting and photovoltaics can be formed with assemblies of micro/nanoscale components or material elements to achieve system level outcomes that are not possible using conventional approaches. Examples include flexible/stretchable designs, curvilinear layouts and systems that exploit heterogeneous materials integration in two or three dimensional layouts. The assembly process can occur either by deterministic methods based on transfer printing or guided approaches based on fluidic delivery and surface/shape recognition. In all cases, electrically interconnecting the assembled devices to form integrated systems represents a practically challenging aspect of the fabrication, particularly for systems in solid state lighting and photovoltaics where long interconnect wiring traces with minimal resistances are preferred. The most straightforward and widely explored approaches rely on conventional techniques, such as photolithography, to pattern uniform layers of metal formed by vacuum deposition (possibly followed by electroplating). The cost structures, however, preclude their use in many systems of interest. Conventional soft lithographic methods can be used, but their application over surface topography associated with assembled device components can be difficult. Screen printing or ink jet printing of pastes or liquid suspensions of conductive particles provide alternatives, but their modest resolution limits the utility. Newer techniques that rely on electrohydrodynamic jet printing or direct writing avoid these problems. Achieving adequate throughput with these serial methods and developing them into forms suitable for realistic application are subjects of this example. The research described here provides a simple scheme designed specifically to address the classes of systems described above; it combines aspects of transfer printing for assembly, with soft imprint lithography and certain aspects of screen printing for contacts and interconnect. In the following, the basic features of this method are described, and its applications to representative systems of interest in monocrystalline silicon photovoltaics and AlInGaP lighting indicators are demonstrated.

[0453] Figure 24 presents a schematic illustration of the process, in which transfer printing for device placement and molding for electrical interconnect occur simultaneously. The first step involves fabricating the devices (i.e. square blocks with rectangular electrode pads; Figure 24a) on a source substrate using procedures discussed subsequently in the context of different demonstration examples. Next,

techniques for transfer printing lift these devices onto an elastomeric stamp/mold with relief that defines contacts to the electrode regions and trenches for interconnect. In this example (Figure 24b), the relief consists of two different levels such that the devices rest with their electrodes in contact with the highest features; the others are associated with interconnect. The stamp/mold 'inked' with devices then contacts a thin layer of a liquid prepolymer cast on a target substrate. Allowing this liquid to flow and conform to the relief, photochemically or thermally curing it into a solid form and then removing the stamp/mold yields the structure illustrated in Figure 24c. The polymer acts as an adhesive and an encapsulant for the devices, with molded features that define the geometry of the interconnect wiring. Scraping a conductive paste over the top surface using methods conceptually similar to those for screen printing fills the recessed regions in the molded polymer to form these interconnects (Figure 24d). For the experiments described in the following, a photocurable polyurethane (PU; NOA61, Norland Products Inc.) and a silver epoxy (H20E Epo-Tek®, Ted Pella Inc.) served as the mold material and the conductive paste, respectively. In certain cases, we found that a thin residue of the PU remained on the contacts of the devices, necessitating a short reactive ion etching step (50 mtorr, O_2 20 sccm, 100W, 3-5 min; Plasmatherm) to remove this residue just before application of the conductive paste. The silver epoxy underwent a thermal cure at 150 °C for 5 minutes to obtain low electrical resistivity. The casting and curing procedures of soft lithography were used to form stamps/molds of the elastomer poly(dimethylsiloxane) (PDMS; Sylgard, Dow Corning).

[0454] In a first set of experiments, the basic features of this method as applied to interconnects and contacts to test structures were examined. The molding step relies on established methods for soft imprint lithography. Concepts for using the molded features as trenches to be filled with conductive pastes, and accomplishing the molding at the same time as printing are both unusual aspects of the process reported here. The filling procedures involve first dispensing a line of silver epoxy along one edge of a flat region of the substrate, located a short (e.g. 3-5 mm) distance away from the molded features. As an implement for scraping this epoxy over the surface, we used a slab of PDMS roughly 3 cm long, 1 cm thick and with a width somewhat larger than that of the molded substrate. This element has a ~45° beveled edge, similar to squeegees used for screen printing. Scraping this edge

across the substrate at an angle of ~30 degrees several times filled the trenches with epoxy and left only small amounts of residue on the top surfaces. Scraping several additional times with another PDMS element soaked in acetone removed these residues. Figure 25a shows a pattern of conducting features formed in this fashion on a molded layer of PU (20 μm depth) on a substrate of polyethylene terephthalate (PET). These results illustrate the range of feature sizes (line widths 20-200 μm, lengths 0.2-2.0 mm, in straight, curved and zig-zag geometries, and in text) and shapes that can be formed easily, and the good levels of uniformity that are possible. The limit of resolution is determined by the sizes of particles in the silver epoxy (10-15 μm), rather than by the fidelity in the molding step. Figure 25b shows cross sectional views of lines formed with aspect ratios (depth to width) of 1 and 0.1. The limits at the high and low ends of this range are defined, respectively, by inability to push epoxy into deep, narrow features, and tendency to scrape it completely away from the center regions of shallow, wide features. Decreasing the viscosity and particle sizes in the epoxy can improve the former aspect; increasing the stiffness of the slab of material (PDMS in this case) used to scrape the epoxy into the grooves can improve the latter. Independent of dimension in the acceptable range, we found values of electrical resistivity ($3.0\text{-}6.0\times10^{-4}$ Ω·cm) roughly two orders of magnitude higher than bulk silver (1.6×10^{-6} Ω·cm), for curing temperatures of 150 and times of 5 minutes, consistent with specifications from the vendor. Contacts to devices and electrical crossovers can be formed in the manner of Figure 24. Figure 25c shows such an example, where metal pads (Cr/Au, 100/1000 nm; 500×500 μm) formed in a square array (1.5 mm pitch) on a PET substrate provide an equivalent of the devices in Figure 24. Defining trenches in PU using a stamp/mold with a design similar to that of Figure 24 followed by filling with silver epoxy yielded the structure shown in the image of Figure 25(c). The bottom left and right frames provide a schematic cartoon illustration and a top view optical micrograph, respectively. The lines here have widths of 100 μm and depths of 20 μm. The contacts to the electrode pads are defined by molded features with depths of 40 μm and lateral dimensions of 100×300 μm. Current/voltage data (Figure 25(d)) collected by probing contact pads to different combinations of row (r1, r2, etc) and column (c1, c2, etc) electrodes verifies electrical continuity along given columns and rows and electrical isolation (i.e. >GΩ) between all other pairs of lines.

[0455] To demonstrate this concept in real devices, AlInGaP light emitting diodes (LEDs; 250x250 μm) formed in ultrathin (2.5 μm thick) layouts were used. Here, the printing step to transfer these devices from a GaAs wafer to a glass substrate occurred first, followed by molding to define contacts and interconnect. Figure 26(a) shows a set of six such LEDs, with an independent pair of electrical leads to each. The top inset provides a top view optical micrograph. The three devices in the middle were connected to a power supply to induce light emission, for the purpose of illustration. The current/voltage characteristics shown in Figure 26b are similar to those observed in devices (non-ohmic contacts) interconnected with conventional procedures of photolithography and liftoff.

[0456] Microscale monocrystalline silicon solar cells provide another device example. Here, collection of five such cells were formed into interconnected arrays for a mini-module using the schemes as shown in Figure 24, where printing and molding occurred simultaneously. See Figure 27a. The process steps for fabricating the cells appear elsewhere. Each cell consists of a bar of monocrystalline silicon (width, length and thickness of 50 μm, 1.55 mm and 20 μm, respectively) with ohmic contacts of metal (Cr/Au, 100/1000 nm; 50 μm width and 100 μm length for the p contact; 50 μm width and 1.4 mm length for the n contact). Figure 27(b) shows a sample, with an inset that provides a cross sectional view of part of the structure. In these systems, illumination occurs through the backside surface of the transparent substrate; the interconnect lines and metal layers serve as reflectors. Figure 27(c) gives current/voltage characteristics carried out at room temperature using a DC source meter (Model 2400, Keithley) operated by Labview5®, and a 1000 W full spectrum solar simulator (Model 91192, 4×4 inch source diameter, ±4° collimation, Oriel) equipped with AM 0 and AM 1.5 direct filter. The efficiency (E_{ff}) and fill factor (FF) of this solar cell, corresponding to measurement on all five interconnected cells in the module, were 6.5 % and 0.61 respectively, obtained using standard procedures and considering only the geometrical sizes of the cells (not explicitly separating flux from the sidewalls). These properties are in the same range as those of arrays of similar devices interconnected using conventional procedures.

[0457] In summary, the procedures reported here might provide an attractive solution to electrical interconnection of classes of systems that incorporate

assemblies of micro/nanoscale devices or material elements. Although their use in prototype devices for photovoltaics and lighting indicators demonstrates the key aspects, the same methods can also be used to establish electrodes and/or interconnects in related systems that use micro/nanoscale material elements, such as nanowires, nanomembranes, nanotubes, and others. The printing and molding can occur either sequentially or simultaneously, depending on requirements. The final, embedded configurations of the devices that result from this process have practical advantages for encapsulation. The ultimate limits in the resolution are defined by the soft imprint molding procedures (e.g. ~1-2 nm for PDMS molds) and the conductive pastes (e.g. 5-100 nm for Au or Ag nanoparticles). Their use in realistic applications will also be limited by achievable registration of the stamp/mold elements to the device components or material elements. Flexible sheets of plastic or glass can form support structures for thin layers of PDMS, to reduce distortions to one or two micron levels over areas of hundreds of square centimeters, or larger. The characteristics of the methods described here, their simplicity and potential for low cost operation over large areas, and the diversity of materials and devices with which they can be applied suggest a potential for broad utility.

Example 3: Printed GaAs LEDs

[0458] GaAs LED device fabrication starts out with the epitaxially grown LED wafer. Epitaxial layers of GaAs wafers are shown in Figure 28. The stack structures of this particular GaAs LED wafer used for the experiments are also listed in Table 1 below.

[0459] From the multi-quantum well (MQW) which is shown as layer 5 in Figure 28 and Table 1, barrier, cladding, spreading, and contact layers symmetrically distributed to form a Vertical-type LED (VLED). Epitaxial structures for GaAs LED are, however, not restricted to this particular structures. There are many variant structure designs for different purposes and applications, and transfer-printing technology should be compatible regardless of this epitaxial structure designs.

[0460] The processing schematics for μ-GaAs LED is shown in Figure 29. The fabrication process starts out with the commercially available GaAs LED epitaxial wafer with an embedded sacrificial layer as shown in Figure 28. First, SiO_2 layer is deposited onto the GaAs LED wafer and photolithographically patterned SiO_2 layer serves as an etch mask for the isolation step which is carried out by dry-etching (i.e.

ICP RIE with Cl_2). GaAs can also be isolated using wet etchant (i.e. HCl), and Photo-resist (PR) can be sufficient as an etch mask in this case. The point is that SiO_2 can be any other etch mask depending which isolation route is considered. Once GaAs LED cells are isolated on the host wafer, heterogeneous anchors are photolithographically defined as illustrated in Figure 29. Scanning Electron Microscopy (SEM) images along with Optical Microscopy (OM) images of these GaAs LEDs after isolation (A), anchoring (B), and printing (C) processes are shown in Figure 30.

Table 1. Epitaxial Layers of GaAs LED wafer

Layer	Layer Name	Material	Thickness (nm)	Type	Dopant	Concentration (cm^{-3})
1	Contact	GaAs	5	P	C	1.00E+19
2	Spreader	$Al_{0.45}Ga_{0.55}As$	800	P	C	1.00E+18
3	Clad	$In_{0.5}Al_{0.5}P$	200	P	Zn	3E17 to 6E17
4	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
5	Well	$In_{0.56}Ga_{0.44}P$	6	-	-	<1E16
6	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
7	Clad	$In_{0.5}Al_{0.5}P$	200	N	Si	1.00E+18
8	Spreader	$Al_{0.45}Ga_{0.55}As$	800	N	Si	1.00E+18
9	Contact	GaAs	500	N	Si	4.00E+18
10		$Al_{0.96}Ga_{0.04}As$	1500	N	Si	1.00E+17
11		GaAs	1500	N	Si	1.00E+17
12		$Al_{0.96}Ga_{0.04}As$	500	N	Si	1.00E+17
13	Substrate	GaAs		N	Si	>1E18

Example 4: Printed GaN LEDs from Silicon

[0461] GaN device fabrication begins with a host wafer with a suitable epitaxial layer stack as shown in Figure 32. This particular GaN LED structures are epitaxially grown on Si (111) wafer. However, similar fabrication process can be employed on GaN LED structures grown on Sapphire or any other host substrates.

[0462] Following from Figure 33, access to the n-GaN is achieved by a) ICP-RIE etching of the p-GaN and quantum well region. Mixed metal ohmic contacts, first n-contacts then p-contacts, are subsequently deposited and annealed with a standard high temperature rapid thermal annealing process. Device isolation is achieved via

patterning Si_3N_4 and a thick metal etch mask and ICP-RIE etching for the isolation. Since this system is concerned with utilizing the anisotropic etching characteristics of the underlying Si(111) substrate, sufficient etch depth into the Si substrate must be obtained. Potassium hydroxide (KOH) or Tetramethylammonium hydroxide (TMAH) is used as the anisotropic etchant of Si(111) which results in suspended devices tethered to the host wafer via anchor bars as shown in Figure 34. It is, however, not restricted to used KOH or TMAH. As a matter of fact, drying etching silicon using gases such as SF_6, CF_6, and XeF_2, could isotropically etch underlying silicon to generate free-standing μ-LEDs chiplets. For KOH-based etching system, Si_3N_4 is used in the previous etch mask to serve as a protective barrier to ohmic contacts from the harsh conditions of the strongly alkaline KOH solution. Individual devices are removed from the host substrate via contacting with a soft elastomeric stamp, namely PDMS, and pulling the stamp quickly in the vertical direction. This device is then transferred to a secondary substrate coated with a thin polymer adhesive layer (i.e. PDMS, SU-8, polyimide, BCB, sol-gel silica, etc) or without any such layer.

[0463] Utilizing a step-and-repeat process, devices can be removed from a very dense array and be printed to a sparse array of any desired spacing. An optical image of a donor substrate during the step-and-repeat process is shown in Figure 35. It shows retrieved LED cells which are transferred onto the foreign substrate. This step-and-repeat concept is not restricted to GaN LED, but can be employed in wide variety of materials including GaAs LED, which is shown in Figure 36. The transfer can be accomplished with a patterned or an un-patterned stamp. The transfer can be facilitated by the use of specialized relief structures, embedded actuators (balloons, local heaters, and the like) or by externally applied forces or radiation (laser exposure, etc). In some cases, it is possible, for example, to print the LEDs directly onto a pre-metalized substrate to achieve transfer and, at the same time, electrical interconnect and interface with heat spreading structures. In addition to these variants in printing, the processing sequence of Figure 33 can be implemented in different orders – e.g. the ohmic contacts can be defined on the foreign substrate, after printing.

[0464] Current-voltage (I-V) characteristics of undercut and printed devices were measured using an Agilent 4155C Semiconductor Parameter Analyzer as shown in

Figure 37(b). Light emission spectrum was collected using a spectrometer from Ocean Optics and according to Figure 37(c) the peak emission wavelength is 472.3 nm. As shown in Figure 37(b), an individual μ-GaN LED exhibits forward bias voltage of ~4.2V at the forward current of 50mA with an emission wavelength at around 470nm.

[0465] Experimental results have shown slight etching of the GaN stack upon extended exposure (~20 min) to KOH. Figure 38 shows two SEM images of a 100 μm x 100 μm device immediately following the ICP-RIE deep etching with the Ni/Si_3N_4 etch mask still intact. Slight sidewall striations can be noticed due to the anisotropic etching of the ICP-RIE. Following KOH undercut of the device, moderate roughening of the device sidewall is observed.

[0466] Etching of GaN is very slow and is considered negligible in the context of LED fabrication, i.e. sidewall roughening has no effect on device performance. If pristine sidewalls are desired, an additional passivation step can be included in the fabrication process, Figure 39. Following ICP-RIE deep etching, a) Ni etch mask is removed followed by Si_3N_4 deposition by PECVD. A b) timed RIE etch then removes Si_3N_4 from the trench "floors" and c) SF_6 RIE treatment will etch the underlying Si substrate. The device e) can then be undercut in KOH then f) transfer printed to a secondary substrate followed by buffered oxide etchant removal of the remaining Si_3N_4.

Printed GaN LEDs from Sapphire

[0467] Due to the relatively large mismatch in lattice constants of GaN and Si(111), sapphire has always been the predominant substrate for GaN growth. Sapphire, however, is very inert, making etching of the material very difficult. Grinding, polishing and other process approaches might be suitable. An alternative route to printed devices from a sapphire substrate (also applicable to SiC and other substrates) utilizes the laser lift-off method, which is shown in Figure 40. Alternatively, releasing the GaN stack from handle wafer by selective etching of a sacrificial layer are also shown in Figure 41 and 42.

Laser lift off with wafer-LED layer bonding

[0468] Figure 40 shows steps for processing GaN LEDs grown on a sapphire substrate then wafer-bonded to a Si (111) substrate and removed from the sapphire via laser lift-off. The first steps include b) n-contact deposition and annealing then c) wafer bonding and laser lift-off. Exposed interface between GaN and sapphire is easily delaminated and transferred from sapphire to receiver wafer, as can be shown in c),d). Freestanding GaN layers are fabricated for LED devices by silicon undercut etching with KOH (similar to procedures described in the previous sections), GaN buffer layer elimination (via polishing, as illustrated here, or by etching or related procedures) and e) n-contact electrode patterning. The inset image shows experimental results of sections of GaN epimaterial bonded to a Si (111) wafer coated with Au. GaN structures here are composed of 5×5 mm^2 squares on 2 inch sapphire. Receptor wafer is 3 inch diameter with <111> direction. Trench etching and other approaches, not explicitly indicated here, are often necessary to achieve high yields in this overall process flow.

Sacrificial layer for undercut etching: PEC etching

[0469] As mentioned above, sacrificial layer inserted in GaN stack can be used as an alternative to wafer bonding. Various sacrificial layers (InGaN, SiO_2, AlAs, Si_3N_4, ZnO, and etc.) can be used which are etched selectively in solutions (i.e. HF, HCl, and H_3PO_4). Etching methods are various. Directional wet etching, PEC (photoelectrochemical) etching and EC (electrochemical) etching can be utilized to form freestanding GaN LED layers suitably configured for printing. Figure 41 presents one example.

[0470] Figure 41 presents InGaN sacrificial layer and selectively etching of this layer by the PEC etching method. Here, a sacrificial layer such as InGaN layer is inserted between GaN stack and GaN buffer layer. Selective etchants (such as HCl, KOH, and etc) can be utilized for PEC etching (i.e. GaN etching rate ~0). After dry etched a), entire device substrates on sapphire are etched with PEC etching. The metal in the field serves as a cathode during PEC etching b) in diluted HCl (0.004M) with 1000 W Xe lamp. The lamp photo-generates carriers and associated PEC etching, while an intentionally doped GaN film filters out the light with energy higher than band gap of GaN, thereby limiting etching to the lower band gap InGaN

sacrificial layer. Selectively undercut GaN devices are transferred by protruding PDMS mold, d).

Sacrificial layer for undercut etching with EC (electrochemical etching)

[0471] Figure 42 explains one of examples of an EC etching method. It is quite similar with PEC etching, however, photo irradiation is not needed in this system. The electrolyte can help a sacrificial layer be decomposed and etched. In panel (a) of Figure 42, GaN/InGaN multilayer structures are covered with a passivation layer, such as SiN_x or SiO_2, and a cathode (e.g., Ti/Au) is fabricated on the InGaN sacrificial layer. Panel (b) of Figure 42 shows connection of the cathode to power supply in an electrolyte (e.g., 0.008 M HCl). As shown in panel (c) of Figure 42, the sacrificial layer can be removed, followed by removal of the passivation layer, for example with buffered oxide etchant (BOE). Finally, as shown in panel (d) of Figure 42, the structures are selectively transferred by transfer/contact printing

Sacrificial layer for undercut etching: selectively wet etching

[0472] Sacrificial layers that can be removed without PEC or related schemes for selectively are also possible.

[0473] Figure 43 presents an example of wet etching strategy for freestanding GaN LED cells. ZnO buffer layer can be used for template of GaN epitaxial process. ZnO layer is selectively etched by 5% diluted NH_4Cl in water. Materials such as SiO_2 can be used for passivation, as they are not removed by this etchant.

Example 5: Anchoring Structures

[0474] During the process of generating free-standing μ-LEDs structures (i.e. μ-GaAs LED, μ-GaN LED, and etc), anchoring structures were used to hold μ-LED chiplets in place preventing them from being disturbed or being displaced. Various anchoring schemes are proposed in this example. In large, the anchoring structures can be divided into two different categories: Heterogeneous anchoring and Homogeneous anchoring.

Heterogeneous Anchoring Structures

[0475] Heterogeneous anchoring represents anchor structures that are different materials than the chiplet materials. (i.e. polymer anchor, and etc). One type of heterogeneous anchoring system is shown in Figure 44.

[0476] In this particular heterogeneous anchoring structure shown in Figure 44, photolithographically defined photoresist (PR) is used as an anchor. It is, however, not restricted to photoresist. In fact, any material (i.e. organic, inorganic, ceramic, and etc) that withstands the etchant or etching species can be served as an anchor. As illustrated in the Figure 45, various geometries of heterogeneous anchoring structures can be employed depending on process conditions. Anchoring geometries shown in Figure 45 are only few examples from many possible variances.

Homogeneous Anchoring Structures

[0477] In the case of μ-GaN LED chiplets on silicon (111), natural homogeneous anchors are formed if chiplets are aligned parallel to the [110] direction of the silicon (111) wafer. Anisotropic Si etchant (i.e. KOH, TMAH, and etc) exhibits significant etch rate variation depending on crystalline direction they are etching. For example, KOH etches [110] and [100] direction several hundred times faster than [111] direction. In other words, if μ-GaN LED chiplets are aligned parallel to [110] direction, etch rate difference between (110) and (111) planes produces a natural anchoring system as shown in Figure 46. Since these anchors are same material as the μ-GaN LED chiplets, we refer them as Homogeneous anchors.

Example 6: Encapsulation & Interconnection

[0478] Once μ-LED cells are transfer printed onto a foreign substrate, the cells can be passivated and encapsulated in a manner that leaves the contact regions exposed for electrical interconnection. On conventional LED process, electrical connection from LED to the external pins are often realized via wire bonding. Wire bonding process requires the ball size of about 100 μm in diameter as shown in Figure 47.

[0479] Consequently, the light-emitting area effectively gets reduced by the size of the ball required for the wire bonding process. Unless the ball size for the wire bonding is dramatically reduced, reducing the LED die size simply becomes unrealizable. Recent work with GaAs based devices demonstrates the ability to use planar processing techniques to establish interconnects that are much smaller than those possible with wire bonding. These strategies can also be implemented with

GaN devices, alone or in combination with wire bonding, screen printing, transfer printing/molding and other approaches.

Encapsulation Via Back-Side Exposure (EBSE)

[0480] This example describes a self-aligned process that is referred to herein as Encapsulation via Back-Side Exposure, as illustrated in Figure 48.

[0481] First, photosensitive polymers (negative tone) can be spin-coated or spray-deposited onto the transferred μ-GaN LEDs on a transparent substrate. Photosensitive polymers with a sufficient thickness can encapsulate the entire substrate conformally as illustrated in Figure 48. P-ohmic contact metal composition can be selected to have a high transparency in the emission wavelength and but only partial transparency at the UV wavelengths for the process of Figure 48. Thick contact pads are deposited on P-ohmic contact metal. By taking advantage of transparent nature of the substrate and reflective nature of the P-contact pads, the photosensitive polymer layer can be exposed from the backside of the substrate with the optimum exposure dose. During the back-side (flood) exposure step, thick contact pads on the LED chiplet simply serve as self-aligned masking layers such that the photosensitive polymer in these regions is not exposed by the backside irradiation. These regions can be selectively removed during a subsequent developing step. After the final curing step, conventional photolithography or related approaches can be used for the interconnection between LEDs. Many variations of these basic concepts are possible.

[0482] Scanning Electron Microscopy (SEM) and Optical Microscopy (OM) images of μ-GaN LED after Encapsulation via Back-Side Exposure process are shown in Figure 49 above. Profilometer data on μ-GaN LED after the process appears in Figure 50 below. Blue and Black profiles represent the as-printed μ-GaN LED cell before the encapsulation process and printed μ-GaN LED cell after the encapsulation process, respectively.

[0483] A fully interconnected string of μ-GaN LEDs are shown in Figure 51 above. Incorporating a series connection between μ-GaN LEDs results in highly uniform light output from one μ-GaN LED to another because of identical current flowing

through these μ-GaN LEDs. Furthermore, two strings of five□ μ-GaN LEDs connected in series are shown in Figure 52 below.

Example 7: Molded Interconnection for μ-LEDs

[0484] As an alternative to the process of Figure 48, LED isolation and interconnection can be done in a single step (or multiple, sequential steps) using the molded interconnection method as illustrated in the Figure 53 and Figure 54.

[0485] As illustrated in Figure 53 above, selectively transferred LEDs can serve as a template for creating a master for the PDMS mold. By photolithographically patterning photosensitive polymer (i.e. Su-8 from Microchem), trenched patterns can be fabricated leading from the LED contacts. These trenched patterns can be designed following the desired interconnection patterns. Therefore, the molded elastomer stamp using this master would have protruded interconnection structures. 3D patterned elastomer stamp can be used to selectively pick up LEDs from their donor substrate, and transfer them onto the target substrate using photo-curable polymer such as NOA (Norland Optical Adhesive) creating embossed structures. Elastomer stamp can be simply peeled off after photo-curing adhesive polymer resulting in trenched patterns for the interconnection between LEDs similar to the master substrate. When applied silver paste would simply fill up the previously created trenches and silver paste on the top surface can simply be scrapped off leaving silver paste only in the trenched regions. Resulted silver paste in the trenched regions can now serve as an interconnection between LEDs and external contacts as illustrated in Figure 54.

[0486] An optical image and the electrical measurement on metalized LEDs are illustrated in Figure 55.

[0487] Furthermore, this molded interconnection approach can be slightly modified to generate by including the opaque or reflective layers on the areas of stamp that contact the device electrodes as illustrated in Figure 56. In this way, the photo-curable molding material would not be exposure to irradiation and hence be left uncured only on those locations enabling easy removal with appropriate solvent. In Figure 56(a), metal is deposited or transferred only on the surface of PDMS relief features which is supposed to be in contact with electrodes of devices. Another

approach is depicted in Figure 56(b) where patterned mask which corresponds to electrodes of device is place on the backside of PDMS stamp during the UV curing effectively serving as a masking layer.

[0488] The ultimate limits in the resolution of the molded interconnection approach are defined by the soft imprint molding procedures and the Ag particle size. Average Ag particle size used in the experiment above is about 10~15μm, which makes it difficult to generate finer interconnection. Using Ag nano-particles with the average size of 5nm ~100nm, the resolution of molded interconnection could improve dramatically down to sub-micron regime.

[0489] Besides the molded interconnection approach, e-jet printing approach and direct-ink writing approaches can also be used as alternative interconnection schemes.

Example 8: Mesh Interconnection for Vertical LED (V-LED)

[0490] Interconnection for a vertical LED (a type of LED where electrical contact for N and P are made top and bottom as shown in Figure 58) can be accomplished by Mesh Interconnection approach, which is illustrated in Figure 59.

[0491] Fabrication Process for the Mesh Interconnection is illustrated in Figure 59. As shown in Figure 59, metal mesh gets transfer printed onto the plastic substrate with the adhesive layer. Since metal-mesh structure is only partially covering the adhesive layer underneath, μ-LEDs can effectively be transfer-printed onto the substrate. These metal mesh can not only serve as a electrical connection to the printed μ-LEDs, but also as a heat sink. A thin adhesive layer of PDMS (although it is not restricted to PDMS) facilitates printing onto the glass substrate. A photo-patterned layer of epoxy on top of the devices prevents shorting of the top film to the bottom mesh.

Serial Interconnection vs. Parallel Interconnection for μ-LEDs

[0492] μ-LED, like any diode, has an exponential relationship between current and voltage. In other words, a slight variation in the forward voltage between cells could result in a much larger difference in the operating current, and hence different luminescence. When a large number of μ-LEDs are connected in parallel, a μ-LED

with a smaller forward voltage, or turn-on voltage, would draw most of the supplied current instead of all μ-LEDs receiving the same amount of current. In a series connection, however, all μ-LEDs would receive equal amount of current since there's only one possible current path in a serially connected string of μ-LEDs as illustrated in Figure 60. As shown in Figure 60 and 61, combination of series/parallel connection generates more uniform light output from large number of interconnected μ-LEDs.

Planar Interconnection

[0493] As mentioned in previous section, the ultrathin property of these printed μ-LEDs enable a conventional planar interconnection schemes as illustrated in Figure 62. Conventional LEDs with vertical thickness in an order of several hundred μm, simple planar interconnection scheme suggested here becomes extremely challenging or almost impossible to achieve due to the extremely high step coverage, which is why the wire-bonding approach has become the main stream approach as shown in Figure 47 earlier.

Example 9: Stretchable Lighting System based on Printed μ-LEDs

[0494] The interconnects of the spatially independent micro-lens array can be fabricated in a serpentine-like (not shown) or accordion-like (shown in Figure 63) fashions to serve as a force dampening mechanism. With such a design, the module can be stretched and bent but the interconnect will stretch and flex so as to absorb the lateral forces exerted due the change in relative position of each pixel keeping the curvature of the micro-lens unchanged. Furthermore the surface of these micro-lens can be roughened to serve as the diffusion stage.

[0495] The approach in Figure 63 is used for creating a stretchable interconnection, while that of Figure 64 is used for creating stretchable μ-LED, per se, for possible outcoupling of the light output via strain-induced modification of the band structures of μ-LEDs.

Example 10: Enhancement in Light Extraction from μ-GaN LEDs

[0496] Recent research on GaN blue LEDs has led to a rapid development of the quality of the devices, pushing the performance to ever higher levels. GaN based LEDs are expected to soon take over conventional (incandescent, fluorescent, and

compact fluorescent) lighting systems but progress has been slowed by the relatively poor light extraction. Due to the high refractive index (~2.5) of GaN, the critical angle for light escape into air is ~23.6°, as calculated by Snell's law. Light incident upon the inside surface outside of this angle is reflected back into the device where absorption in the epi-layers subsequently quench the light. To this end, several technologies can be applied to this flexible array of GaN LEDs which will enhance the optical performance of the system.

Example 11: Textured and/or Roughened Surface for Improved Light Extraction

[0497] The normal, "mirror-like" surface of a GaN LED leads to a large fraction of light to be internally reflected thereby decreasing the light extraction efficiency of the device. A method to increasing light extraction is to roughen to the bottom surface serving as a means to reducing internal reflection and scattering the light outwards from the LED as shown in Figure 65.

[0498] Fabrication of a roughened surface will closely follow established μ-GaN LED fabrication methods, as described previously. Following complete device fabrication individual pixels will be undercut by anisotropic potassium hydroxide (KOH) etching of the silicon substrate, performed in an environment free of ultra-violet (UV) light (i.e. cleanroom). Upon complete undercut, a plasma enhanced chemical vapor deposition (PECVD) passivation layer of Si_3N_4 is deposited to protect ohmic contacts and sidewalls of the fabricated device. Further etching in KOH in the presence of UV light will promote the photoelectrochemical (PEC) etching of the exposed (bottom) side of the μ-GaN LED, forming pyramidal shaped structures that serve as efficient light scattering centers as shown in Figure 66.

[0499] These LEDs are well suited for bottom emission, with the potential to enhance light extraction by 100% or more. Bottom emission can be efficiently achieved by using a thick, reflective p-contact. Contact schemes utilizing Pt/Ag as the p-contacts have reportedly shown reflectance values of 80%. Additional reflectance can be realized by the addition of a top-side reflector made of thick Al or Ag which demonstrate very high reflectivity at 470nm.

[0500] Schematics for optically enhancement with outcoupling is shown in Figure 67 below. Although schematics in Figure 67 is illustrated with μ-GaN LED from

Sapphire substrate using Laser Lift-off approach, the concept of using GaN cones structures for outcoupling the light is not restricted to this particular process. After the wafer bonding ((a)~(d)), residual GaN buffer layer could be selectively etched by crystallographic wet etching, (e). GaN buffer layer can be etched by H_3PO_4 etchant and PEC etching. Inset SEM image shows an example of GaN cones made by the crystallographic wet etching (D. A. Stocker et al Appl. Phys. Lett. 73, 2654 (1998)). Below two illustrations demonstrate the light emission path comparison between LEDs with GaN cones and without GaN cones. By Snell's law, impinged light by the interface is randomly emitted. On the other hands, with GaN cones device light can be emitted with straight propagation after impinged on surface.

Micro-lens, Polymeric Molded Structures for Improved Light Extraction

[0501] Towards the realization of highly efficient top emitting LEDs, micro-lens arrays can be incorporated into the final device. Lens structures, being fabricated from a higher index material (typically a polymer of n~1.5) increase the light extraction cone at the GaN/polymer interface. The lens shape is better capable of extracting light from the polymer medium to surrounding air.

[0502] Micro-lens arrays can be fabricated through a series of established photolithographic techniques. Processing begins with patterning of a photoresist. Elevated temperatures will cause the photoresist to reflow in a manner that reduces surface energy, resulting in a lens-like shape. This pattern can be captured by molding an uncured polymer such as PDMS to the micro-lens array. Final lens geometry is obtained by molding an optically clear polymer (i.e. Norland Optical Adhesive) to the PDMS mold. The lens can be removed from the mold, aligned, and laminated to the LED array.

[0503] The above micro-lens geometry can be optimized to an LED array when the array is left in an un-bent state. Upon bending, lateral forces in the lens array will cause deformation in the individual lens structures thereby decreasing the optical performance of the lens. In an effort to achieve total flexibility the following system is proposed that offers a spatially independent lens array in which the movement of a pixel does not exert lateral forces conducive to lens deformation on its neighbor pixel.

[0504] Processing of a spatially independent lens array follows a similar fabrication route as above. Pixel interconnects are patterned along with each micro-lens feature. The independent nature of this array arises in molding the polymer encapsulant (step "e" in Figure 70) when a sufficiently thin polymer film is spun such that only the depressed (lens and interconnect) features are filled. Upon removal from the mold the spatially independent lens array is then aligned and laminated to the micro-LED array.

[0505] Processing schematics for fabricating polymeric patterns for optical enhancement of μ-GaN LED is shown in Figure 71. After wafer bonding ((a)~(d)) and residual GaN polishing, polymeric patterns can be formed by molding, imprint, colloidal lithography, etc. Patterned polymeric structures can manipulate light intensity, light wave length shift. Duty ratio and polymeric beads size can control emission properties.

[0506] Fabrication of micro-lens and polymeric structures are not restricted only to the above processes. Micro-lens can also be fabricated in various approaches such as casting, molding, imprint, colloidal lithography, screen printing, ink-jet printing, E-jet printing, and etc. These micro-lens and polymeric structures can be either fabricated on the already-printed μ-GaN LED, or can be fabricated on the different substrate and be transfer-printed onto the μ-GaN LED afterwards.

[0507] Furthermore, besides those added modifications (i.e. micro-lens, cone structures, and etc), the thin and small geometries of these printed μ-LED results in higher extraction efficiency per unit area. These printed μ-LED have a size much smaller (100 μm^2 to 10,000 μm^2) than conventionally LEDs (100,000 μm^2 to 1,000,000 μm^2). In other words, μ-LEDs fabricated here are as much as 10,000 times smaller than conventional LEDs. Attributing to its micro-size effects as well as to more efficient usage of the injected current, light from the quantum well is more likely to be escaped from the LED because of smaller number of internal reflections and larger surface-to-volume ratio.

Example 12: Merging the Light Output from the Bi-direction LED

[0508] μ-LED printed onto a transparent substrate such as a glass or a plastic exhibits bi-axial illumination as shown in Figure 72. In other words, light from the printed μ-LED can be emitted from the top as well as from the bottom.

[0509] Highly reflective metals (e.g. Al, Ag, Pt, and etc) can be deposited on the top of the printed μ-LED or μ-LED can printed on highly reflective metal foil to reflect the light to merge the light emission into one-direction, which in turn increases the light output.

[0510] As illustrated in Figure 73, a micro-lens can be fabricated or placed on the printed μ-LED. These micro-lenses can simply be molded using photo-curable resin as illustrated in the figure above or be fabricated elsewhere and be transfer-printed onto μ-LED. Highly reflective and thermally conductive metals, such as Ag, can be plated, evaporated, or sputtered on top of the these structures to create a mirror-like structures to reflect the light emitted from the printed μ-LED. These reflectors can also be placed on the side to direct the light emitting from the edges of printed μ-LED. As mentioned in this example, the above system is suited for the margining the bi-directional light output into the bottom emission. However, a similar system can be incorporated into top emission system simply by transfer-printing μ-LED onto the already fabricated the micro-lens system with a reflective mirror. Additionally, re-directed light output using various approaches mentioned above, optical fibers can be incorporated in various ways to manipulate the focused light direction arbitrary. Furthermore, these reflectors can also be served as a heat sink due to its high thermal conductivity.

Example 13: Multiple Stacks of μ-LEDs

[0511] Epitaxial wafer of compound material is a considerably more expensive process than the Cz process of silicon. Cost saving process for generating epitaxial wafer is proposed in Figure 74. As shown in Figure 74, multiple μ-LED layers can be grown initially. Although the schematic in Figure 74 illustrates the multi-layer GaAs LED structures, the similar concept can be employed in GaN-based LED or any other structures from III-V and III-N compound materials. After the lattice mismatch issue between the substrate and the epitaxial layers is resolved by the growth of a

buffer layer, an appropriate sacrificial layer and active LED layer can be grown in alternating fashion as illustrated in the figure. This growth process can be repeated several times to generate multiple layers of identical sacrificial layer and the active layers. μ-LEDs from the top most layer (or the 1st layer of μ-LEDs as depicted in the figure) can be defined in the free-standing fashion by undercutting the sacrificial layer as shown in the figure. These μ-LEDs can be transfer printed in various ways as we have mentioned in previous sections. Once the 1st layer is fully processed and transfer printed onto the foreign substrate, the 2nd layer is exposed and is ready to be processed identically as the 1st layer was processed. Hence, we can generate much more μ-LEDs from the single wafer. Hence, the total cost of fabricating μ-LEDs can get effectively reduced.

Example 14: Thermal Management for μ-LEDs

[0512] When a plastic substrate is used, thermal management of μ-LEDs is important because a plastic substrate is intrinsically an insulator. Printed μ-LED, however, has a size much smaller (100 μm^2 to 10,000 μm^2) than conventionally LEDs (100,000 μm^2 to 1,000,000 μm^2). In other words, μ-LEDs fabricated here are as much as 10,000 times smaller than conventional LEDs. Sparse array of smaller μ-LEDs could exhibit better thermal distribution than one larger LED because generated heat for a smaller μ-LED is far less than a larger conventional LED. Furthermore, sparser array geometry enables better heat dissipation than a larger conventional LED simply because heat generated for a larger conventional LED is more concentrated around the LED itself.

[0513] Figure 75 illustrates the thermographic images of printed μ-LED on a plastic substrate without any heat sink in the proximity. The baseline temperature is fixed at 70°C for this particular experiment.

Metallic Heat Sink on Top of μ-LEDs

[0514] Placing a thermally conductive heat sink in a proximity of the printed μ-LED can significantly improve the thermal dissipation from the printed μ-LEDs. A cross-sectional schematic of such a system is illustrated in the Figure 76.

[0515] An electrical insulating dielectric layer with a higher thermal conductivity than organic polymer (i.e. SiN with thermal conductivity of 30W/mK compared to

0.24W/mK of PET), can be deposited on top of the printed μ-LEDs on a plastic substrate. A material with a high thermal conductivity, such as Ag and Cu, can be deposited on top of the μ-LED with an dielectric layer (i.e. SiN) in between for electrical isolation. Furthermore, a dielectric layer such as SiN can be controlled such that a very thin layer of a SiN layer is enough for electrical isolation.

Transfer Printing Materials with High Thermal Conductivity on Top of μ-LEDs

[0516] The materials for the heat sink can be metals, or any other material with a high thermal conductivity, such as a polycrystalline diamond shown in Figure 77. These materials can be transfer-printed via either active or passive system.

[0517] Use of printed μ-Diamond as a heat sink is shown in Figure 77. μ-Diamond can be easily formulated in Chemical Vapor Deposition (CVD) process at a low cost. Grown μ-Diamond layer can be patterned and be lifted off from the mother wafer similar to μ-LED process described previously. These μ-Diamonds can be transfer printed on top of already-printed μ-LED serving as a efficient heat spreader & heat sink due to its exceptionally high thermal conductivity (>1000 W/mK). As shown in Figure 75, thermal dissipation is not uniform, rather it is concentrated in a certain part of the printed μ-LED. Thermal management strategy described here can be designed such that the heat sink is placed strategically on the hot spot.

Placing a Heat Sink on Micro-lens used for Merging the Light Output from the Bi-direction LED

[0518] A μ-LED printed onto a transparent substrate such as a glass or a plastic exhibits bi-axial illumination. Highly reflective metals (e.g. Al, Ag, Pt, and etc) can be deposited on the top of the printed μ-LED or μ-LED can be printed on highly reflective metal foil to reflect the light to merge the light emission as discussed previously.

[0519] As illustrated in Figure 78, a micro-lens can be fabricated or placed on the printed μ-LED. These microlenses can simply be molded using photo-curable resin as illustrated in Figure 78. Highly reflective and thermally conductive metals, such as Ag, can be plated, evaporated, or sputtered on top of the these structures to create a mirror-like structures to reflect the light emitted from the printed μ-LED.

Furthermore, these reflector can also be served as a heat sink due to its high thermal conductivity.

Example 15: Heterogeneous Integration of μ-LEDs with Printed Electronics

[0520] Utilizing step-and-repeat process, different classes of materials (i.e. μ-GaAs LEDs, μ-GaN LEDs, and printed μ-Si electronics, and etc) can be printed in a sequence into a single substrate for combining advantages of those different materials. For example, μ-Si is well suited for developing a complex electronics based on its stable electronic properties and matured processing technologies on both digital and analog circuits. Instead of μ-Si, μ-GaAs chiplets or μ-GaN chiplets could be used as a building block for developing high-frequency operating analog circuits for Radio Frequency (RF) optoelectronics on unusual substrates such as a plastic. In Figure 79, one example of combing μ-GaAs LED, μ-GaN LEDs, and μ-Si electronics for developing full-colored inorganic active-matrix display is proposed.

[0521] Furthermore, carbon-based materials such as Carbon Nanotube (CNT) or Graphene films can be grown on another substrate and be transfer-printed onto already-printed μ-LEDs for developing a transparent electrodes and interconnection (as an alternative to ITO or ZnO transparent electrodes) to prevent the interconnection lines from blocking the light output. Additionally, a photodiode can also be heterogeneously integrated onto the printed μ-LEDs as illustrated in Figure 80. A photodiode would simply detect the light intensity from the printed μ-LED and the output response of the photodiode can be fed back to the driving ICs for the μ-LEDs for the real-time self-calibration purpose.

Example 16: Integration of Phosphors and μ-GaN LEDs

[0522] White LED produced by combination of phosphor and a blue LED has several challenges to hurdle. One major challenge is the color uniformity. Due to the lack of uniformity in phosphor coverage, the resulting emission from the underlying blue LED and the phosphor varies considerably. As a result, the edges appear to be yellow whereas the center of the beam appear to be blue. LUMILED has developed a patented process on conformal coating of phosphor technology and thus far is the only LED manufacturer that can produce white LED with high uniformity.

[0523] Figure 81 illustrates a new technique to disperse phosphor particles in uniform and array-like fashion. As illustrated in Figure 81, elastomer is molded with an array of cavities. Geometries of these cavities can easily be controlled by patterning the master substrate into the desirable shapes and depths. Phosphor particles which have the diameter in the range of several microns can be mixed in the solvent, and poured onto the elastomer. Phosphors on the surface of the elastomer can be scrapped away by the elastomer blade leaving phosphors only in the cavities. By bonding the thin elastomer onto the molded elastomer, phosphors can effectively be bound inside the cavities in array-like fashion. Packaged elastomer with encapsulated phosphors can be directly laminated against the packaged μ-GaN LEDs on the flexible substrate as illustrated in Figure 81(E). The distance between phosphors and LEDs and spacing between phosphor cells can be precisely controlled resulting in the highest level of uniformity. 3D cartoons are shown in Figure 82 and Figure 83 for more clear illustrations. Micro-lens structures mentioned in a previous example can be incorporated as well simply by lamination.

Example 17: Methods for Making μ-LEDs

[0524] Figure 84 illustrates an exemplary embodiment for making an array of semiconductor devices. A growth substrate **8401** is provided and a semiconductor epilayer **8402** is grown on the surface via epitaxial growth. The epilayer **8402** is bonded to a handle substrate **8403** and is subsequently released from the growth substrate **8401**. Next, a mask **8404** is patterned over the epilayer **8402** to define masked regions and exposed regions. Material is removed from the exposed regions to define the array of semiconductor devices **8405**. The semiconductor devices **8405** are partially released from the handle substrate **8403**, and remain connected by anchors **8406**. Optionally, the patterned mask is removed (not shown). The partially released semiconductor devices **8405** are subsequently selectively printed onto a device substrate via a contact printing method.

[0525] Figure 85 illustrates an exemplary embodiment for making an array of GaN LED devices. A sapphire growth substrate **8501** is provided and a GaN multilayer **8502** is grown on the surface via epitaxial growth. The multilayer **8502** is bonded to a handle substrate **8503** and is subsequently released from the sapphire substrate **8501**. Next, a mask **8504** is patterned over the multilayer **8502** to define masked

regions and exposed regions. Material is removed from the exposed regions to define the array of GaN LED devices **8505**. The GaN LED devices **8505** are partially released from the handle substrate **8503**, and remain connected by anchors **8506**. Optionally, the patterned mask is removed (not shown). The partially released GaN LED devices **8505** are subsequently selectively printed onto a device substrate via a contact printing method.

[0526] Figure 86 illustrates an exemplary embodiment for making an array of GaN LED devices. A silicon (111) growth substrate **8601** is provided and a GaN multilayer **8602** is grown on the surface via epitaxial growth. Next, a mask **8603** is patterned over the multilayer **8602** to define masked regions and exposed regions. Material is removed from the exposed regions to define the array of GaN LED devices **8604**. In this embodiment, a portion of the silicon substrate **8601** is removed from the exposed region by the etching process. The GaN LED devices **8604** are partially released from the silicon substrate **8601**, for example by a direction etch along <110> directions of the silicon substrate **8601**. In this embodiment, the GaN LED devices remain connected to the substrate by anchors **8605**. Optionally, the patterned mask is removed (not shown). The partially released GaN LED devices **8604** are subsequently selectively printed onto a device substrate via a contact printing method.

[0527] Figure 87 illustrates an exemplary embodiment for making an array of GaN LED devices. A sapphire growth substrate **8701** is provided and a sacrificial layer **8702** is deposited thereon. A GaN multilayer **8703** is grown over the sacrificial layer **8602** via epitaxial growth. Next, a mask **8704** is patterned over the multilayer **8703** to define masked regions and exposed regions. Material is removed from the exposed regions to define the array of GaN LED devices **8705**. The GaN LED devices **8505** are partially released from the sapphire substrate **8701** by etching portions of the sacrificial layer. In this embodiment, the GaN LED devices remain connected to the substrate by anchors **8706**. Optionally, the patterned mask is removed (not shown). The partially released GaN LED devices **8705** are subsequently selectively printed onto a device substrate via a contact printing method.

[0528] Figure 88 illustrates an exemplary embodiment for making an array of semiconductor devices. A sapphire growth substrate **8801** is provided and a GaN multilayer **8802** is grown on the surface via epitaxial growth. The GaN multilayer **8802** is bonded to a handle substrate **8803**. To release the GaN multilayer **8802** from the sapphire substrate **8801**, the interface **8805** between the sapphire substrate **8801** and the GaN multilayer **8802** is exposed to laser radiation **8804**, thereby releasing the GaN multilayer **8802** from the sapphire substrate **8801**. Next, a mask **8806** is patterned over the GaN multilayer **8802** to define masked regions and exposed regions. Material is removed from the exposed regions to define the array of GaN LEDs **8807**. The GaN LED devices **8807** are partially released from the handle substrate **8803**, and remain connected by anchors **8808**. Optionally, the patterned mask is removed (not shown). The partially released semiconductor devices **8808** are subsequently selectively printed onto a device substrate via a contact printing method (not shown).

Example 18: Handle Substrate Processing

[0529] In some embodiments, a handle substrate is useful as an intermediate processing platform. For example, devices transferred to a handle substrate may undergo one or more patterning, growth, polishing, deposition, implantation, etching, annealing or other processing steps. Processing of electronic devices on a handle substrate may be useful, for example, if the handle substrate is capable of withstanding high temperatures or chemically inert. Such advantages are further advantageous if the growth and/or device substrates are, for example, not capable of withstanding high temperatures or not chemically inert. A handle substrate may also be useful, for example, as an assembly stage, where multiple electronic device components are positioned relative to one another to reduce the number of overall process steps and/or to limit processing steps on a device or growth substrate.

[0530] Figure 89 illustrates a scheme for processing electronic devices on a handle substrate. In this embodiment, electronic devices **8901** are grown and patterned on a growth substrate **8902**. At least a portion of the electronic devices **8901** are transferred to a handle substrate **8903**, for example using methods described above, where they undergo additional processing. In this embodiment, handle substrate is capable of withstanding high temperature processing, for example for patterning

ohmic contacts **8904** onto electronic devices **8901**. After electronic devices **8901** are patterned with ohmic contacts **8904**, they are transferred to a device substrate **8905** via a contact printing method. Additional processing of electronic devices **8901** while on the handle substrate **8903** is further contemplated.

[0531] Figures 90A and 90B illustrates another scheme for processing electronic devices on a handle substrate. In this embodiment, multilayer devices **9001** are grown on a growth substrate **9002**. The multilayer device **9001** shown in Figure 90A comprises a seed/buffer layer **9003** separating a lower active device layer(s) **9004** from the growth substrate **9002**. A sacrificial layer **9005** separates the lower active device layer(s) **9004** from an upper active device layer(s) **9006**. Figure 90B illustrates a useful transfer scheme for such multilayer devices **9001** via transfer to handle substrates **9007** and **9008**. The prepared multilayer devices **9001** are first processed to transfer upper active device layers **9006** to a first handle substrate **9007,** for example by at least partially removing sacrificial layers **9005** followed by a transfer step. Lower active device layers **9004** are then left exposed and still attached to growth substrate **9002**, after which they are transferred to a second handle substrate **9008**, for example using methods described above.

[0532] Figure 91illustrates another scheme for processing electronic devices on a handle substrate. In this embodiment, electronic devices **9101** and **9102** are prepared on separate growth substrates **9103** and **9104**, respectively. After growth and any necessary processing on the growth substrate (not shown), portions of each of the electronic devices **9101** and **9102** are transferred to a handle substrate **9105**. Methods such as these allow for heterogeneously integrated electronic devices in a lateral configuration to be assembled onto a handle substrate. Optionally, electronic devices **9101** and **9102** undergo additional processing while on handle substrate **9105** before transfer to an appropriate device substrate (not shown). In one embodiment, electronic devices **9101** are first transferred to handle substrate **9105** followed by transfer of electronic devices **9102** to handle substrate **9105**. In an embodiment, electronic devices **9101** and **9102** are transferred to handle substrate **9105** in a step-wise fashion, where one or more of electronic devices **9101** are transferred to handle substrate **9105** in one step, followed by transfer of one or more electronic devices **9102** to handle substrate **9105** in another step; additional transfer

steps for electronic devices **9101** and **9102** are further contemplated, as are transfer of additional electronic devices to handle substrate **9105**.

[0533] Alternative to or in addition to lateral configuration, devices can be heterogeneously integrated in a vertical configuration. Such a scheme for processing is shown in Figures 92A and 92B. In this embodiment, two different light emitting diode devices **9201** and **9202** are prepared on two different growth substrates, **9203** and **9204**, respectively. At least a portion of light emitting diode devices **9201** are first transferred to a handle substrate **9205**. At least a portion of light emitting diode devices **9202** are subsequently transferred to handle substrate **9205** on top of light emitting diode devices **9201**. Optionally, intermediate processing of light emitting diode devices **9201** take place before transfer of light emitting diode devices **9202**. Figure 92B illustrates a cross sectional view of the vertically configured heterogeneously integrated devices on handle substrate **9205**. Optionally, additional devices are further vertically integrated on handle substrate **9205**. In a specific embodiment, light emitting diode devices **9201** emit blue light and light emitting diode devices **9202** emit red light.

[0534] Figure 93 shows another example of processing an electronic device on a handle substrate. In this embodiment, buffer layer **9301** and electronic device **9302** are grown and optionally pre-processed on growth substrate **9303**. In this specific embodiment, electronic device 9302 is a vertical type LED comprising n-type GaN region **9304**, quantum well region **9305** and p-type GaN region **9306**. Buffer layer **9301** and electronic device **9302** are detached from growth substrate **9303** and transferred to handle substrate **9307**, for example using methods described above. While on handle substrate **9307**, buffer layer **9301** is removed and, optionally, a portion of electronic device **9302** is also removed. Buffer layer **9301** and portions of electronic device **9302** are optionally removed by methods known in the art, such as chemical-mechanical polishing (CMP). The polished devices **9308** may subsequently be transferred to a device substrate and/or undergo additional processing while on the handle substrate (not shown).

[0535] Figure 94 shows another example of processing an electronic device on a handle substrate. In this embodiment, electronic devices 9401 are grown and optionally patterned on a growth substrate **9402**. At least a portion of the electronic

devices **9401** are transferred to a handle substrate **9403**, for example using methods described above. Here, heat management structures **9404** are patterned over the electronic devices **9401** on the handle substrate **9403**. After patterning of heat management structures **9404**, at least a portion of electronic devices **9401** and heat management structures **9404** are transferred to a device substrate **9405**, for example via a contact printing method. In specific embodiments, patterning of heat management structures **9404** is a high temperature process and handle substrate **9403** is capable of withstanding the associated processing conditions with would otherwise damage or destroy growth substrate **9402** or device substrate **9405**.

STATEMENTS REGARDING INCORPORATION BY REFERENCE AND VARIATIONS

[0536] All references throughout this application, for example patent documents including issued or granted patents or equivalents; patent application publications; and non-patent literature documents or other source material; are hereby incorporated by reference herein in their entireties, as though individually incorporated by reference, to the extent each reference is at least partially not inconsistent with the disclosure in this application (for example, a reference that is partially inconsistent is incorporated by reference except for the partially inconsistent portion of the reference).

[0537] The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding any equivalents of the features shown and described or portions thereof, but it is recognized that various modifications are possible within the scope of the invention claimed. Thus, it should be understood that although the present invention has been specifically disclosed by preferred embodiments, exemplary embodiments and optional features, modification and variation of the concepts herein disclosed may be resorted to by those skilled in the art, and that such modifications and variations are considered to be within the scope of this invention as defined by the appended claims. The specific embodiments provided herein are examples of useful embodiments of the present invention and it will be apparent to one skilled in the art that the present invention may be carried out using a large number of variations of the devices, device components, methods

steps set forth in the present description. As will be obvious to one of skill in the art, methods and devices useful for the present methods can include a large number of optional composition and processing elements and steps.

[0538] When a group of substituents is disclosed herein, it is understood that all individual members of that group and all subgroups are disclosed separately. When a Markush group or other grouping is used herein, all individual members of the group and all combinations and subcombinations possible of the group are intended to be individually included in the disclosure. Specific names of compounds or materials are intended to be exemplary, as it is known that one of ordinary skill in the art can name the same compounds or materials differently.

[0539] Every formulation or combination of components described or exemplified herein can be used to practice the invention, unless otherwise stated.

[0540] Whenever a range is given in the specification, for example, a temperature range, a time range, or a composition or concentration range, all intermediate ranges and subranges, as well as all individual values included in the ranges given are intended to be included in the disclosure. It will be understood that any subranges or individual values in a range or subrange that are included in the description herein can be excluded from the claims herein.

[0541] All patents and publications mentioned in the specification are indicative of the levels of skill of those skilled in the art to which the invention pertains. References cited herein are incorporated by reference herein in their entirety to indicate the state of the art as of their publication or filing date and it is intended that this information can be employed herein, if needed, to exclude specific embodiments that are in the prior art. For example, when composition of matter are claimed, it should be understood that compounds known and available in the art prior to Applicant's invention, including compounds for which an enabling disclosure is provided in the references cited herein, are not intended to be included in the composition of matter claims herein.

[0542] As used herein, "comprising" is synonymous with "including," "containing," or "characterized by," and is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. As used herein, "consisting of" excludes any

element, step, or ingredient not specified in the claim element. As used herein, "consisting essentially of" does not exclude materials or steps that do not materially affect the basic and novel characteristics of the claim. In each instance herein any of the terms "comprising", "consisting essentially of" and "consisting of" may be replaced with either of the other two terms. The invention illustratively described herein suitably may be practiced in the absence of any element or elements, limitation or limitations which is not specifically disclosed herein.

[0543] One of ordinary skill in the art will appreciate that starting materials, reagents, synthetic methods, purification methods, analytical methods, assay methods and methods other than those specifically exemplified can be employed in the practice of the invention without resort to undue experimentation. All art-known functional equivalents, of any such materials and methods are intended to be included in this invention. The terms and expressions which have been employed are used as terms of description and not of limitation, and there is no intention that in the use of such terms and expressions of excluding any equivalents of the features shown and described or portions thereof, but it is recognized that various modifications are possible within the scope of the invention claimed. Thus, it should be understood that although the present invention has been specifically disclosed by preferred embodiments and optional features, modification and variation of the concepts herein disclosed may be resorted to by those skilled in the art, and that such modifications and variations are considered to be within the scope of this invention as defined by the appended claims.

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We claim:

1. A method for making an electronic device, said method comprising the steps of:

providing a growth substrate having a receiving surface;

forming a semiconductor epilayer on said receiving surface via epitaxial growth, said semiconductor epilayer having a first contact surface;

bonding said first contact surface of said semiconductor epilayer to a handle substrate;

releasing said semiconductor epilayer from said growth substrate wherein said semiconductor epilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said semiconductor epilayer;

patterning said second contact surface of said semiconductor epilayer with a mask, thereby generating exposed regions and one or more masked regions of said second contact surface;

removing material from said exposed regions by etching said exposed regions, thereby generating one or more semiconductor structures supported by said handle substrate;

at least partially releasing said one or more semiconductor structures from said handle substrate; and

transferring at least one of said one or more semiconductor structures from said handle substrate to a device substrate via dry transfer contact printing, thereby assembling said semiconductor structures on said device substrate to make said electronic device.

2. A method of making an electronic device, the method comprising the steps of:

providing a growth substrate having a receiving surface;

forming a semiconductor epilayer on said receiving surface via epitaxial growth, said semiconductor epilayer having a first contact surface;

bonding said first contact surface of said semiconductor epilayer to a handle substrate;

releasing said semiconductor epilayer from said growth substrate, wherein at least a portion of said semiconductor epilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said semiconductor epilayer;

processing said semiconductor epilayer on said handle substrate, thereby generating one or more semiconductor structures supported by said handle substrate;

transferring at least one of said one or more semiconductor structures from said handle substrate to a device substrate via dry transfer contact printing, thereby assembling said semiconductor structures on said device substrate to make said electronic device.

3. A method of making an electronic device, the method comprising the steps of:

providing a first growth substrate having a first receiving surface;

forming a first semiconductor epilayer on said first receiving surface via epitaxial growth, said first semiconductor epilayer having a first contact surface;

bonding said first contact surface of said first semiconductor epilayer to a handle substrate;

releasing said first semiconductor epilayer from said first growth substrate, wherein at least a portion of said first semiconductor epilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said first semiconductor epilayer;

providing a second growth substrate having a second receiving surface;

forming a second semiconductor epilayer on said second receiving surface via epitaxial growth; said second semiconductor epilayer having a third contact surface;

bonding said third contact surface of said second semiconductor epilayer to said handle substrate, said first semiconductor epilayer or both;

releasing said second semiconductor epilayer from said second growth substrate, wherein at least a portion of said second semiconductor epilayer remains bonded to said handle substrate, said first semiconductor epilayer or both, thereby exposing a fourth contact surface of said second semiconductor epilayer;

processing said first semiconductor epilayer, said second semiconductor epilayer or both said first and said second semiconductor epilayers on said handle substrate, thereby generating one or more semiconductor structures supported by said handle substrate;

transferring at least one of said one or more semiconductor structures from said handle substrate to a device substrate via dry transfer contact printing, thereby assembling said semiconductor structures on said device substrate to make said electronic device.

4. The method of claim 2 or claim 3, wherein said step of processing a semiconductor epilayer on said handle substrate comprises a processing method selected from the group consisting of: a patterning process, a growth process, a polishing process, a deposition process, an implantation process, an etching process, an annealing process, a molding process, a curing process, a coating process and any combination of these.

5. The method of claim 2 or claim 3, wherein said step of processing a semiconductor epilayer on said handle substrate comprises forming one or more ohmic contacts on said semiconductor epilayer.

6. The method of claim 2 or claim 3, wherein said step of processing a semiconductor epilayer on said handle substrate comprises forming one or more thermal management structures on said semiconductor epilayer.

7. The method of claim 1, 2 or 3, wherein said growth substrate and said semiconductor epilayer are lattice matched.

8. The method of claim 7, wherein said growth substrate and said semiconductor epilayer are lattice matched to within ± 3.4%.

9. The method of claim 1, 2 or 3, wherein said semiconductor epilayer is selected from the group consisting of: a GaN layer, an InGaN layer, a GaAsN layer, an AlGaN layer, an AlGaAsN layer, a GaAs layer, an InGaAs layer, an AlGaAs layer, an AlGaAsP layer, a GaAsSbN layer and an InN layer; and wherein said growth substrate is selected from the group consisting of: sapphire, Si (111), SiC, ZnO, Si (100), $MgAl_2O_4$ (100), $MgAl_2O_4$ (111), A-plane sapphire, M-plane sapphire, AlN, MnO, ZrB_2, $LiGaO_2$, $(La,Sr)(Al,Ta)O_3$, $LiAlO_2$, GaAs and InP.

10. The method of claim 1, 2 or 3, wherein said semiconductor epilayer has a thickness selected from the range of 1 μm to 5 μm.

11. The method of claim 1, 2 or 3, wherein said semiconductor epilayer is a multilayer comprising a plurality of semiconductor layers having different compositions, doping or both.

12. The method of claim 11, wherein said semiconductor epilayer is a multilayer comprising at least one p-type semiconductor layer in electrical contact with at least one n-type semiconductor layer.

13. The method of claims 11, wherein said multilayer comprises a plurality of LED device layers selected from the group consisting of: contact layers, spreader layers, cladding layers and barrier layers.

14. The method of claim 11, wherein said multilayer comprises a plurality of GaN layers having different doping, thicknesses or both.

15. The method of claim 11, wherein said multilayer comprises at least one p-type GaN layer in electrical contact with at least one n-type GaN layer.

16. The method of claim 11, wherein said multilayer comprises a plurality of GaN layers selected from the group consisting of: InGaN, GaN, AlGaN, GaN:Mg, GaN:Si, GaN:AlN and GaN:ZnO.

17. The method of claim 11, wherein said multilayer comprises a plurality of GaN layers corresponding to a vertical type GaN LED.

18. The method claim 1, 2 or 3, wherein said handle substrate comprises silicon, said semiconductor epilayer comprises GaN and wherein said step of bonding said first contact surface of said semiconductor epilayer to said handle substrate comprises contacting said first contact surface of said semiconductor epilayer to an external surface of said handle substrate so as to establish Van der Waals bonding between said semiconductor epilayer and said handle substrate.

19. The method claim 1, 2 or 3, wherein said step of bonding said first contact surface of said semiconductor epilayer to said handle substrate comprises contacting said first contact surface of said epilayer to an external surface of said handle substrate having an adhesion layer provided thereon.

20. The method of claim 19, wherein said adhesion layer is selected from the group consisting of Au, Al, Pd, In, Ni, polyurethane, polyimide, silicone and any combination of these.

21. The method claim 1, 2 or 3, wherein said step of at least partially releasing said semiconductor epilayer from said growth substrate comprises at least partially removing a sacrificial layer provided between said growth substrate and said semiconductor epilayer.

22. The method claim 21, wherein said sacrificial layer is removed by etching or dissolving said sacrificial layer.

23. The method claim 22, wherein said sacrificial layer is removed by electrochemical etching.

24. The method claim 22, wherein said sacrificial layer is removed by photoelectrochemical etching.

25. The method claim 21, wherein said semiconductor epilayer comprises GaN, said growth substrate comprises sapphire, and said sacrificial layer comprises SiO_2, AlAs, Si_3N_4, ZnO, AlN, HfN or AlInN.

26. The method of claim 1, 2 or 3, wherein said semiconductor epilayer and said growth substrate meet at an interface and wherein said step of releasing said semiconductor epilayer from said growth substrate comprises exposing said interface to electromagnetic radiation.

27. The method of claim 26, wherein said electromagnetic radiation is passed through said growth substrate.

28. The method of claim 26, wherein said semiconductor epilayer is GaN and said growth substrate is sapphire and wherein said electromagnetic radiation comprises electromagnetic radiation from a laser.

29. The method of claim 26, further comprising providing an absorbing layer at said interface, wherein said electromagnetic radiation is at least partially absorbed by said absorbing layer, thereby releasing said semiconductor epilayer from said growth substrate.

30. The method of claim 1, wherein said mask comprises a first mask layer of Si_3N_4 provided on at least a portion of said second contact surface of said epilayer and a second mask layer of metal provided on said first mask layer.

31. The method of claim 1, wherein said step of removing material from said exposed regions comprises etching said exposed regions via inductively coupled plasma reactive ion etching.

32. The method of claim 1, 2 or 3, further comprising a step of anchoring said one or more semiconductor structures to said handle substrate by at least one homogenous anchor or at least one heterogeneous anchor.

33. The method of claim 1, 2 or 3, wherein said step of transferring comprises transferring at least a one of said semiconductor structures from said handle substrate to a device substrate via contact printing using a conformal transfer device.

34. The method of claim 33, wherein said step of transferring comprises transferring at least one of said semiconductor structures from said handle substrate to a device substrate using a PDMS stamp.

35. The method of claim 1, 2 or 3, wherein said device substrate is a glass substrate or a polymer substrate.

36. The method of claim 1, 2 or 3, wherein said device substrate is a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components or any combination of these.

37. The method of claim 1, 2 or 3, wherein said handle substrate comprises a material selected from the group consisting of: a doped or undoped semiconductor; a single crystal material, a polycrystalline material, a ceramic, SiC, Si_3N_4, fused silica, alumina (Al_2O_3), ZrO_2, MgO, pyrolytic Boron nitride (PBN), aluminum nitride, aluminum silicate, titania, a polymer, glass, quartz, a semiconductor with or without a thermal oxide layer and any combination of these.

38. The method of claim 2 or 3, further comprising a step of processing said semiconductor epilayer on said growth substrate.

39. The method of claim 38, wherein said step of processing said semiconductor epilayer on said handle substrate comprises a processing method selected from the group consisting of: a patterning process, a growth process, a polishing process, a deposition process, an implantation process, an etching process, an annealing process, a molding process, a curing process, a coating process and any combination of these.

40. A method for making an array of LEDs, said method comprising the steps of:

providing a sapphire growth substrate having a receiving surface;

forming a GaN epilayer on said receiving surface via epitaxial growth; wherein said GaN epilayer is a multilayer comprising at least one p-doped GaN semiconductor layer in electrical contact with at least one n-doped GaN semiconductor layer, said GaN multilayer having a first contact surface;

bonding said first contact surface of said GaN multilayer to a handle substrate;

releasing said GaN multilayer from said growth substrate, wherein said GaN multilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said GaN multilayer;

patterning said second contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said second contact surface;

removing material from said exposed regions by etching said exposed regions, thereby generating one or more LED device structures supported by said handle substrate;

at least partially releasing said one or more LED device structures from said handle substrate; and

transferring at least a portion of said one or more LED device structures from said handle substrate to a device substrate via dry transfer contact printing, thereby making said array of LEDs.

41. A method for making an array of LEDs, said method comprising the steps of:

providing a silicon growth substrate having a (111) orientation and having a receiving surface;

generating a GaN multilayer on said receiving surface of said growth substrate via epitaxial growth, said GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one n-type GaN layer, said GaN multilayer having a contact surface;

patterning said contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said GaN multilayer;

removing material from said exposed regions by etching said exposed regions and into said growth substrate, thereby exposing a portion of said growth substrate and generating one or more LED device structures;

at least partially releasing said one or more LED device structures from said growth substrate by anisotropic etching said exposed portion of said growth substrate; and

transferring at least a portion of said one or more LED device structures from said growth substrate to a device substrate via dry transfer contact printing, thereby making said array of LEDs.

42. The method of claim 41, wherein said step of removing material etches a depth into said growth substrate greater than or equal to 5 nm.

43. The method of claim 41, wherein said step of removing material etches an average depth into said growth substrate selected from the range of 5 nm to 10 μm.

44. The method of claim 41, wherein said anisotropic etching occurs preferentially along <110> directions of said growth substrate.

45. The method of claim 41, wherein said anisotropic etching comprises directional wet etching using an anisotropic etchant.

46. The method of claim 45, wherein said anisotropic etchant is potassium hydroxide or tetramethylammonium hydroxide (TMAH).

47. The method of claim 41 wherein said step of removing material from said exposed regions exposes sides walls of said LED device structures, said method further comprising masking at least a portion of said side walls prior to said step of at least partially releasing said LED device structures from said growth substrate.

48. A method for making an array of LEDs, said method comprising the steps of:

providing a sapphire growth substrate having a receiving surface;

providing a sacrificial layer on said receiving surface of said growth substrate;

generating a GaN multilayer on said sacrificial layer via epitaxial growth, said GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one n-type GaN layer, said GaN multilayer having a contact surface;

patterning said contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said GaN multilayer;

removing material from said exposed regions by etching said exposed regions, thereby exposing a portion of said sacrificial layer and generating one or more LED device structures;

at least partially releasing said one or more LED device structures from said growth substrate by removing at least a portion of said sacrificial layer using directional etching, electrochemical etching or photoelectrochemical etching; and

transferring at least a portion of said one or more LED device structures from said growth substrate to a device substrate via dry transfer contact printing, thereby making said array of LEDs.

49. The method of claim 48, wherein said sacrificial layer comprises SiO_2, AlAs, Si_3N_4, ZnO, AlN, HfN or AlInN.

50. The method of claim 48, wherein a buffer layer or an etch block layer is provided between said GaN multilayer and said sacrificial layer.

51. The method of claim 50 wherein said buffer layer or said etch block layer comprises GaN.

52. The method of claim 48, wherein said step of at least partially releasing comprises exposing said sacrificial layer to a selective etchant.

53. The method of claim 52, wherein said selective etchant is HCl, HF, H_3PO_4, potassium hydroxide, tetramethylammonium hydroxide, ethylenediamine,

pyrcatechol, hydrazine chelating amines, 1,2-diaminoethane, NaOH or any combination of these.

54. The method of claim 52, wherein said releasing step comprises exposing said sacrificial layer to electromagnetic radiation having wavelengths selected over the range of 100 nm to 800 nm.

55. The method of claim 54, wherein said sacrificial layer is exposed to electromagnetic radiation from a xenon lamp.

56. The method of claim 54 further comprising passing said electromagnetic radiation through an undoped GaN film prior to exposing said sacrificial layer, thereby optically filtering said electromagnetic radiation to remove at least a portion of electromagnetic radiation absorbed by said undoped GaN film.

57. The method of claim 48, wherein said releasing step comprises providing said sacrificial layer at an electric potential selected over the range of 600 mV to 800 mV.

58. The method of claim 48, wherein said GaN multilayer is grown on a sacrificial layer comprising ZnO and wherein said step of at least partially releasing comprises etching said sacrificial layer with NH_4Cl etchant.

59. A method for making an array of LEDs, said method comprising the steps of:

providing a sapphire growth substrate having a receiving surface;

generating a GaN multilayer on said sapphire growth substrate via epitaxial growth, said GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one n-type GaN layer, said GaN multilayer having a first contact surface, wherein said GaN multilayer and said sapphire growth substrate meet at an interface;

bonding said first contact surface of said GaN multilayer to a handle substrate;

exposing said interface between said GaN multilayer and said sapphire growth substrate to electromagnetic radiation;

releasing said GaN multilayer from said growth substrate wherein said GaN multilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said GaN multilayer;

patterning said second contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said GaN multilayer;

removing material from said exposed regions by etching said exposed region, thereby generating one or more LED device structures;

at least partially releasing said one or more LED device structures from said handle substrate; and

transferring at least a portion of said one or more LED device structures from said handle substrate to a device substrate via dry transfer contact printing, thereby making said array of LEDs.

60. The method of claim 59, wherein said interface is exposed to electromagnetic radiation from a laser.

61. The method of claim 59, wherein said interface is exposed to electromagnetic radiation passing through said sapphire growth substrate.

62. The method of claim 59, wherein said handle substrate comprises an external metal film, wherein said first contact surface of said GaN multilayer is contacted with said external metal film of said handle substrate, thereby bonding said GaN multilayer to said handle substrate.

63. The method of claim 62, wherein said external metal film of said handle substrate reflects said electromagnetic radiation, thereby exposing said interface to said electromagnetic radiation.

64. A method for making an array of LEDs, said method comprising the steps of:

providing a sapphire growth substrate having a receiving surface;

providing a sacrificial layer on said receiving surface of said sapphire growth substrate;

providing an etch block layer on said sacrificial layer;

generating a GaN multilayer on said etch block layer via epitaxial growth, said GaN multilayer comprising at least one p-type GaN layer in electrical contact with at least one n-type GaN layer, said GaN multilayer having a contact surface;

patterning said contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said GaN multilayer;

removing material from said exposed regions by etching said exposed regions, thereby exposing a portion of said sacrificial layer and generating one or more LED device structures;

at least partially releasing said one or more LED device structures from said growth substrate by removing at least a portion of said sacrificial layer using directional etching, electrochemical etching or photoelectrochemical etching; and

transferring at least a portion of said one or more LED device structures from said growth substrate to a device substrate via dry transfer contact printing, thereby making said array of LEDs.

65. The method of claim 64, wherein said sacrificial layer comprises SiO_2, AlAs, Si_3N_4, ZnO, AlN, HfN or AlInN.

66. The method of claim 64 wherein said etch block layer comprises GaN.

67. The method of claim 66, wherein said etch block layer is generated via epitaxial growth.

68. The method of claim 64, wherein said step of at least partially releasing comprises exposing said sacrificial layer to a selective etchant.

69. The method of claim 68, wherein said selective etchant is HCl, HF, H_3PO_4, potassium hydroxide, tetramethylammonium hydroxide, ethylenediamine, pyrcatechol, hydrazine chelating amines, 1,2-diaminoethane, NaOH or any combination of these.

70. The method of claim 64, wherein said releasing step comprises exposing said sacrificial layer to electromagnetic radiation having wavelengths selected over the range of 100 nm to 800 nm.

71. The method of claim 70, wherein said sacrificial layer is exposed to electromagnetic radiation from a xenon lamp.

72. The method of claim 70 further comprising passing said electromagnetic radiation through an undoped GaN film prior to exposing said sacrificial layer, thereby optically filtering said electromagnetic radiation to remove at least a portion of electromagnetic radiation absorbed by said undoped GaN film.

73. The method of claim 64, wherein said releasing step comprises providing said sacrificial layer at an electric potential selected over the range of 600 mV to 800 mV.

74. A method for making an array of stacked LEDs, said method comprising the steps of:

providing a sapphire growth substrate having a receiving surface;

forming a GaN epilayer on said receiving surface via epitaxial growth, wherein said GaN epilayer is a multilayer comprising at least one p-doped GaN semiconductor layer in electrical contact with at least one n-doped GaN semiconductor layer, said GaN multilayer having a first contact surface;

bonding said first contact surface of said GaN multilayer to a handle substrate;

releasing said GaN multilayer from said growth substrate, wherein said GaN multilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said GaN multilayer;

patterning said second contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said second contact surface;

removing material from said exposed regions by etching said exposed regions, thereby generating one or more LED device structures supported by said handle substrate;

at least partially releasing said one or more LED device structures from said handle substrate;

transferring at least a portion of said one or more LED device structures from said handle substrate to a device substrate via dry transfer contact printing, thereby making an array of LED device structures; and

transferring one or more additional LED device structures on top of at least a portion of the array of LED device structures, thereby making said array of stacked LEDs.

75. A method for making an array of stacked LEDs, said method comprising the steps of:

providing a sapphire growth substrate having a receiving surface;

forming a GaN epilayer on said receiving surface via epitaxial growth, wherein said GaN epilayer is a multilayer comprises at least one p-doped GaN semiconductor layer in electrical contact with at least one n-doped GaN semiconductor layer, said GaN multilayer having a first contact surface;

bonding said first contact surface of said GaN multilayer to a handle substrate;

releasing said GaN multilayer from said growth substrate wherein said GaN multilayer remains bonded to said handle substrate, thereby exposing a second contact surface of said GaN multilayer;

patterning said second contact surface of said GaN multilayer with a mask, thereby generating exposed regions and one or more masked regions of said second contact surface;

removing material from said exposed regions by etching said exposed regions, thereby generating one or more LED device structures supported by said handle substrate;

at least partially releasing said one or more LED device structures from said handle substrate;

transferring at least a portion of said one or more LED device structures from said handle substrate to a device substrate via dry transfer contact printing, wherein said device substrate comprises an array of LED device structures and said transferring step transfers said one or more LED device structures on top of at least a portion of said array of LED device structures, thereby making said array of stacked LEDs.

76. The method of any of claims 40-75, wherein said GaN multilayer comprises at least one p-type GaN layer, at least one n-type GaN layer and a quantum well region comprising an InGaN layer positioned between said p-type GaN layer and said n-type GaN layer.

77. The method of claim 76, further comprising the steps of:

depositing a metal film on an exposed region of said p-type GaN layer or said n-type GaN layer; and

annealing said metal film; thereby forming an electrical contact on said p-type GaN layer or said n-type GaN layer.

78. The method of claim 76, further comprising the steps of:

etching a portion of said GaN multilayer so as to expose a region of said n-type GaN layer or said p-type GaN layer;

depositing a metal film on said exposed region of said n-type GaN layer or said p-type GaN layer; and

annealing said metal film, thereby forming an electrical contact on said n-type GaN layer or said p-type GaN layer.

79. The method of any of claims 40-75, wherein said GaN multilayer comprises a plurality of GaN layers selected from the group consisting of: GaN contact layers, GaN spreader layers, GaN cladding layers, GaN barrier layers, GaN etch block layers and GaN buffer layers.

80. The method of any of claims 40-75, wherein said LED device structures correspond to a vertical type LED.

81. The method of any of claims 40-75, wherein said step of removing material comprises etching said exposed regions via inductively coupled plasma reactive ion etching.

82. The method of any of claims 40-75, wherein said mask comprises a first mask layer of Si_3N_4 provided on a portion of said external surface of said GaN multilayer.

83. The method of claim 82, wherein said mask further comprises a second mask layer of metal provided on said first mask layer.

84. The method of any of claims 40-75, further comprising a step of anchoring said LED device structures by at least one homogenous anchor or at least one heterogeneous anchor.

85. The method of any of claims 40-75, wherein said transferring step comprises transferring at least a portion of said one or more LED device structures to a device substrate via contact printing using a conformal transfer device.

86. The method of claim 85, wherein said transferring step comprises transferring at least a portion of said one or more LED device structures to a device substrate via contact printing using a PDMS stamp.

87. The method of any of claims 40-75, wherein said device substrate is a glass substrate or a polymer substrate.

88. The method of any of claims 40-75, wherein said device substrate is a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components or any combination of these.

89. The method of any of claims 40-75, further comprising a step of removing at least a portion of said mask.

90. The method of any of claims 40-75, wherein said device substrate comprises one or more additional LED device structures and said step of transferring at least a portion of said one or more LED device structures comprises printing at least one of said one or more LED device structures on top of said one or more additional LED device structures.

91. The method of any of claims 40-75, further comprising a step of printing one or more additional LED device structures on top of said one or more LED device structures on said device substrate.

92. The method of any of claims 40-75, further comprising the steps of:

providing one or more metallic contacts in electrical contact with a portion of said one or more LED device structures;

coating said one or more LED device structures and one or more metallic contacts with a photosensitive polymer layer; and

exposing portions of said photosensitive polymer layer to electromagnetic radiation, wherein said electromagnetic radiation is at least partially transmitted through said device substrate and wherein said one or more metallic contacts block at least a portion of said electromagnetic radiation from reaching at least a portion of said photosensitive polymer layer, said

one or more metallic contacts thereby serving as one or more self-aligned mask elements.

93. The method of claim 92, further comprising a step of removing portions of said photosensitive polymer layer which are masked by said one or more metallic contacts serving as self-aligned mask elements.

94. The method of claim 93, wherein said step of removing portions of said photosensitive polymer layer which are masked by said one or more metallic contacts serving as self-aligned mask elements comprises developing said photosensitive polymer layer, wherein regions of the photosensitive polymer layer that were not exposed to said electromagnetic radiation are dissolved by exposure to a solvent.

95. The method of any of claims 40-75, wherein said step of at least partially releasing said one or more LED device structures comprises photoelectrochemically or electrochemically etching at least a portion of said GaN multilayer.

96. The method of any of claims 40-75, further comprising a step of printing phosphors over at least a portion of said array of LEDs.

97. The method of claim 96, wherein said phosphors are printed over said array of LEDs via a contact printing method.

98. A method of making a semiconductor device, the method comprising the steps of:

providing a transparent substrate;

assembling a semiconductor device on a surface of said transparent substrate via dry transfer contact printing;

providing one or more metallic contacts in electrical contact with said semiconductor device;

coating said semiconductor device and one or more metallic contacts with a photosensitive polymer layer;

exposing portions of said photosensitive polymer layer to electromagnetic radiation, wherein said electromagnetic radiation is at least partially transmitted through said transparent substrate and wherein said one or more metallic contacts block at least a portion of said electromagnetic radiation from reaching at least a portion of said photosensitive polymer layer, said one or more metallic contacts thereby serving as one or more self-aligned mask elements.

99. The method of claim 98, further comprising a step of removing portions of said photosensitive polymer layer which are masked by said one or more metallic contacts serving as self-aligned mask elements.

100. The method of claim 99, wherein said step of removing portions of said photosensitive polymer layer which are masked by said one or more metallic contacts serving as self-aligned mask elements comprises developing said photosensitive polymer layer and wherein regions of the photosensitive polymer layer that were not exposed to said electromagnetic radiation are dissolved by exposure to a solvent.

101. The method claim 98, wherein said transparent substrate comprises a material selected from the group consisting of: glass, quartz, sapphire, PET, mylar, PDMS, kapton, polycarbonate, silicone, polyurethane, ethylene tetrafluoroethylene, diamond and any combination of these

102. The method of claim 98, wherein said electromagnetic radiation has wavelengths selected over the range of 100 nm to 800 nm.

103. The method of claim 98, wherein said semiconductor device transmits at least 1% of said electromagnetic radiation.

104. The method of claim 98, wherein at least a portion of said electromagnetic radiation provided to said transparent substrate is reflected, scattered or absorbed by said one or more metallic contacts.

105. The method of claim 98, wherein at least 50% of said electromagnetic radiation received by said one or more metallic contacts is reflected, scattered or absorbed by said one or more metallic contacts.

106. The method of claim 98, wherein at least 75% of said electromagnetic radiation received by said one or more metallic contacts is reflected, scattered or absorbed by said one or more metallic contacts.

107. The method of claim 98, wherein at least 95% of said electromagnetic radiation received by said one or more metallic contacts is reflected, scattered or absorbed by said one or more metallic contacts.

108. The method of claim 98, wherein each of said one or more metallic contacts comprises a material selected from the group consisting of: gold, nickel, copper, palladium, platinum, silver, titanium, aluminum, molybdenum and any combination of these.

109. The method of claim 98, wherein each of said one or more metallic contacts has a thickness selected over the range of 4 nm to 10 μm.

110. The method of claim 98, wherein said photosensitive polymer layer has a thickness selected from the range of 5 nm to 1 mm.

111. The method of claim 98, wherein said photosensitive polymer is a negative tone photopolymer.

112. The method of claim 98, wherein portions of said photosensitive polymer exposed to electromagnetic radiation are at least partially crosslinked.

113. The method of claim 98, wherein said photosensitive polymer comprises a material selected from the group consisting of: BCB, SU8, WL-5351, polyurethane, silicon, spin-on-glass, polyimide and any combination of these.

114. The method of claim 98, wherein said semiconductor device comprises a LED, a P-N junction, a thin film transistor, a single junction solar cell, a multi-junction solar cell, a photodiode, a laser, a sensor, a photodiode, an electro-optical device, a CMOS device, a MOSFET device, a MESFET device, a

photovoltaic cell, a microelectromechanical device, a nanoelectromechanical device, a HEMT device, a light-emitting transistor or any combination of these.

115. A method for making an array of phosphors, said method comprising the steps of:

molding an elastomer layer with an array of recessed regions;

providing phosphor particles over said elastomer layer, wherein said phosphor particles at least partially fill in said array of recessed regions; and

providing an encapsulation layer over said elastomer layer, wherein said phosphor particles are encapsulated in said array of recessed regions, thereby making said array of phosphors.

116. A method for making a packaged array of LEDs, said method comprising the steps of:

molding an elastomer layer with an array of recessed regions;

providing phosphor particles over said elastomer layer, wherein said phosphor particles at least partially fill in said array of recessed regions;

providing an encapsulation layer over said elastomer layer, wherein said phosphor particles are encapsulated in said array of recessed regions, thereby making an array of phosphors; and

laminating said array of phosphors over an array of LED device structures, thereby making said packaged array of LEDs.

117. The method of claim 115 or 116, wherein said recessed regions have depths selected over the range of 5 nm to 10 mm.

118. The method of claim 116, further comprising a step of making said array of LED device structures.

119. The method of claim 118, wherein said step of making said array of LED device structures comprises the method of any of claims 40-75.

120. The method of claim 116, wherein said step of laminating comprises printing said array of phosphors onto a device substrate comprising an array of LED device structures.

121. A method of making an electronic device, said method comprising the steps of:

providing one or more electronic device components;

contacting said one or more electronic device components with a conformal transfer and molding device, thereby transferring said one or more electronic device components onto said conformal transfer and molding device;

contacting a prepolymer layer disposed over a host substrate with said conformal transfer and molding device having said one or more electronic device components positioned thereon, thereby at least partially embedding said one or more electronic device components into said prepolymer layer and patterning said prepolymer layer with one or more recessed features;

curing said prepolymer layer, thereby forming a polymer layer having one or more recessed features; and

filling at least a portion of said one or more recessed features with a filling material selected from the group consisting of: a conductive material, an optical material, a heat transfer material and any combination of these.

122. The method of claim 121, wherein said filling step comprises the steps of:

providing a filling material on a surface of said polymer; and

dragging a scraping tool along said surface of said polymer to fill said filling material into at least a portion of said one or more recessed features.

123. The method of claim 121, wherein said host substrate comprises a material selected from the group consisting of: polymer, glass, plastic, semiconductor, sapphire, ceramic and any combination of these.

124. The method of claim 121, wherein said prepolymer layer comprises a material selected from the group consisting of: a photocurable polymer, a thermally curable polymer, a photocurable polyurethane, SU8, PDMS, NOA series, photosensitive polyimide, photosensitive silicone and any combination of these.

125. The method of claim 121, wherein said step of curing said prepolymer layer comprises exposing said prepolymer layer to electromagnetic radiation or heating said prepolymer layer.

126. The method of claim 121, further comprising a step of curing said filling material.

127. The method of claim 126, wherein said step of curing said filling material comprises heating said filling material or exposing said filling material to electromagnetic radiation.

128. The method of claim 121, wherein at least one of said one or more electronic device components comprises one or more electrode contacts.

129. The method of claim 128, further comprising a step of etching at least a portion of said polymer to expose said one or more electrode contacts.

130. The method of claim 121, wherein said filling material comprises a conductive material.

131. The method of claim 130, wherein said conductive material provides one or more electrical interconnections to at least one electronic device component.

132. The method of claim 130, wherein said conductive material is in electrical communication with one or more electrode contacts of said one or more electronic device components.

133. The method of claim 130, wherein, after curing, said conductive material has a resistivity selected over the range of 1×10^{-10} to 1×10^{-2} $\Omega\cdot$cm.

134. The method of claim 130, wherein said conductive material comprises a conductive paste selected from the group consisting of: silver epoxy, gold epoxy, copper epoxy, aluminum epoxy and any combination of these.

135. The method of claim 121, wherein said filling material comprises an optical material.

136. The method of claim 135, wherein said optical material forms an optical element selected from the group consisting of: a collecting optic, a concentrating optic, a reflective optic, a diffusing optic, a dispersive optic, a lens, a phosphor, a waveguide, an optical fiber, an optical coating, a transparent optic, an optical filter, a polarizing optic and any combination of these.

137. The method of claim 135, wherein said optical material comprises a material selected from the group consisting of: polymer, plastic, glass, phosphor and any combination of these.

138. The method of claim 121, wherein at least one of said one or more electronic device components is selected from the group consisting of: a P-N junction, a thin film transistor, a single junction solar cell, a multi-junction solar cell, a photodiode, a light emitting diode, a laser, a sensor, a photodiode, an electro-optical device, a CMOS device, a MOSFET device, a MESFET device, a photovoltaic cell, a microelectromechanical device, a HEMT device and any combination of these.

139. The method of claim 121, wherein at least one of said one or more electronic device components has a vertical dimension selected over the range of 10 nm to 10 μm.

140. The method of claim 121, wherein at least one of said one or more electronic device components has a lateral dimension selected over the range of 1 μm to 10 mm.

141. A method of making an electronic device, said method comprising the steps of:

providing a conformal transfer and molding device having a contact surface comprising one or more transfer surfaces and one or more raised molding features;

contacting one or more electronic device components with said conformal transfer and molding device, thereby positioning said one or more electronic device components on said one or more transfer surfaces of said conformal transfer and molding device;

contacting a prepolymer layer disposed over a host substrate with said conformal transfer and molding device having said one or more electronic device components positioned thereon, thereby at least partially embedding said one or more electronic device components and said one or more raised molding features into said prepolymer layer;

curing said prepolymer layer, thereby forming a polymer layer, wherein said one or more raised molding features of said conformal transfer and molding device are replicated as one or more recessed features in said polymer layer;

separating said conformal transfer and molding device from said polymer layer, wherein said one or more electronic device components are retained in said polymer layer;

applying a filling material to a surface of said polymer layer; and

dragging a scraping tool along said surface of said polymer to fill said filling material into at least a portion of said one or more recessed features.

142. The method of claim 141, wherein said filling material is selected from the group consisting of: a conductive material, an optical material, a heat transfer material and any combination of these.

143. A method of making an electronic device, said method comprising the steps of:

providing a host substrate with a prepolymer disposed thereon;

at least partially embedding one or more electronic device components into said prepolymer layer, wherein one or more recessed features are patterned in said prepolymer layer during said embedding step;

curing said prepolymer layer, thereby forming a polymer layer having one or more recessed features and fixing said one or more electronic device components in said polymer layer; and

filling at least a portion of said one or more recessed features with a conductive material, wherein said conductive material provides one or more electrical interconnections to at least one electronic device component.

144. A method for making a printable electronic device on a device substrate, said method comprising the steps of:

providing a printable electronic device having a contact area, wherein said printable electronic device is anchored to a host substrate via one or more homogeneous or heterogeneous anchors;

contacting said contact area of said printable electronic device with a contact surface of a conformable transfer device, wherein said contact surface of said conformable transfer device has an area smaller than said contact area of said printable electronic device, and wherein said contact area and said contact surface are aligned off center from each other, wherein contact between said contact surface and said contact area binds said printable electronic device to said contact surface;

separating said printable electronic device and said host substrate, thereby releasing said one or more homogeneous or heterogeneous anchors;

contacting said printable electronic device disposed on said contact surface with a receiving surface of said device substrate; and

separating said contact surface of said conformable transfer device and said printable electronic device, wherein said printable electronic device is transferred onto said receiving surface, thereby assembling said printable electronic device on said receiving surface of said device substrate.

145. The method of claim 144, wherein said contact surface of said conformable transfer device is less than 50% of said contact area of said electronic device.

146. The method of claim 144, wherein said contact surface of said conformable transfer device is 25% to 75% of said contact area of said electronic device.

147. The method of claim 144, wherein said contact area and said contact surface are aligned off center from each other by at least 1 μm.

148. The method of claim 144, wherein said contact area and said contact surface are aligned off center from each other by 1 μm to 100 μm.

149. The method of claim 144, wherein said contact surface is provided on a relief feature of said conformable transfer device.

150. The method of claim 144, wherein said conformable transfer device comprises a plurality of relief features providing a plurality of contact regions; said method comprising:

providing a plurality of printable electronic devices each having a contact area, wherein each of said printable electronic devices is anchored to a host substrate via one or more homogeneous or heterogeneous anchors;

contacting said contact areas of said printable electronic devices with said contact regions of said conformable transfer device, wherein each of said contact regions of said conformable transfer device has an area smaller than said each of contact areas of said printable electronic device, and wherein said contact areas and said contact regions are aligned off center from each other, wherein contact between said contact regions and said contact areas binds said printable electronic devices to said contact regions;

separating said printable electronic devices and said host substrate, thereby releasing said homogeneous or heterogeneous anchors;

contacting said printable electronic devices disposed on said contact regions with a receiving surface of said device substrate; and

separating said contact surfaces of said conformable transfer device and said printable electronic devices, wherein said printable electronic devices are transferred onto said receiving surface, thereby assembling said printable electronic devices on said receiving surface of said device substrate.

151. The method of claim 144, wherein said conformable transfer device is a PDMS stamp.

152. The method of claim 144, wherein said electronic device is a P-N junction, a thin film transistor, a single junction solar cell, a multi-junction solar cell, a photodiode, a light emitting diode, a laser, a CMOS device, a MOSFET device, a MESFET device, a photovoltaic cell, a microelectromechanical device, a HEMT device or any combination of these.

153. The method of claim 144, wherein said device substrate is a glass substrate, a polymer substrate, a semiconductor substrate, a metal substrate or a ceramic substrate.

154. The method of claim 144, wherein said device substrate is a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components, or any combination of these.

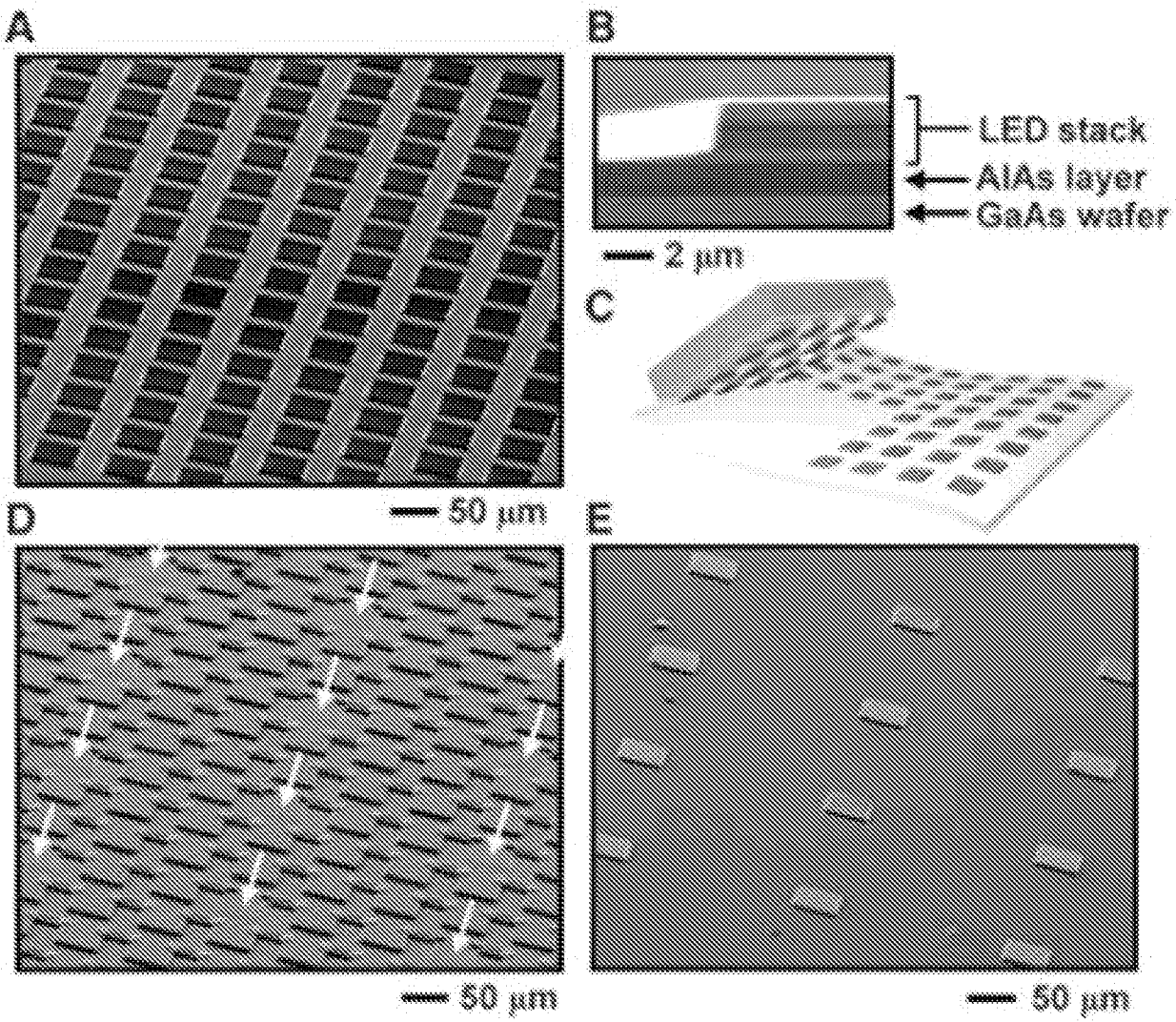
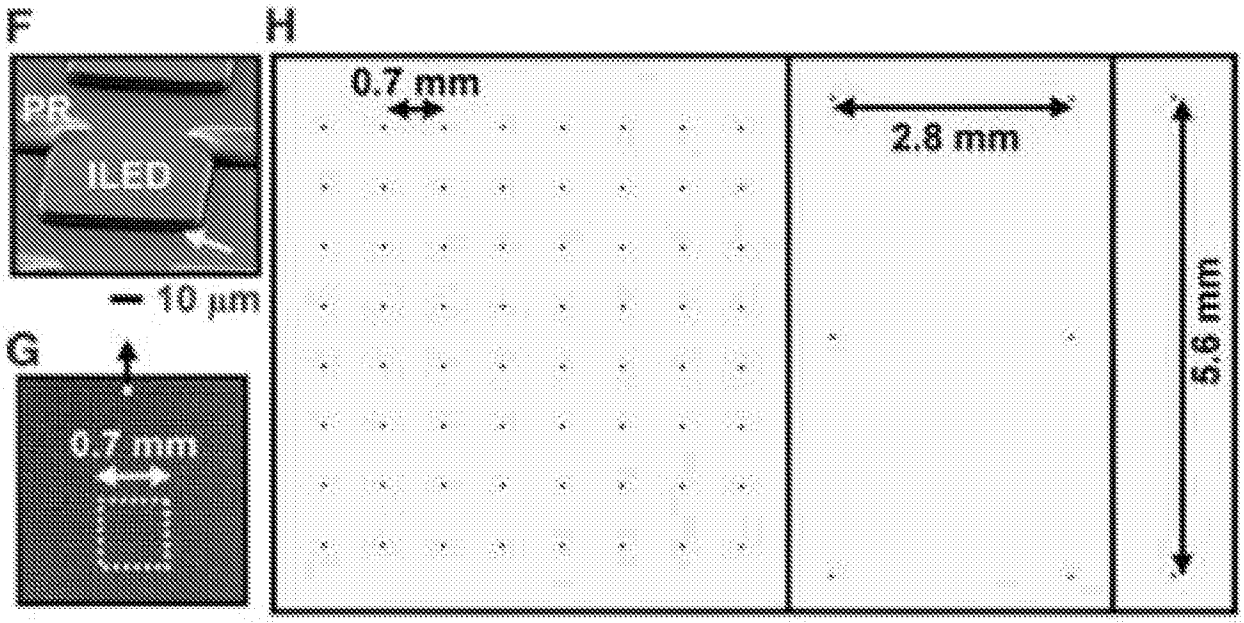


Figure 1



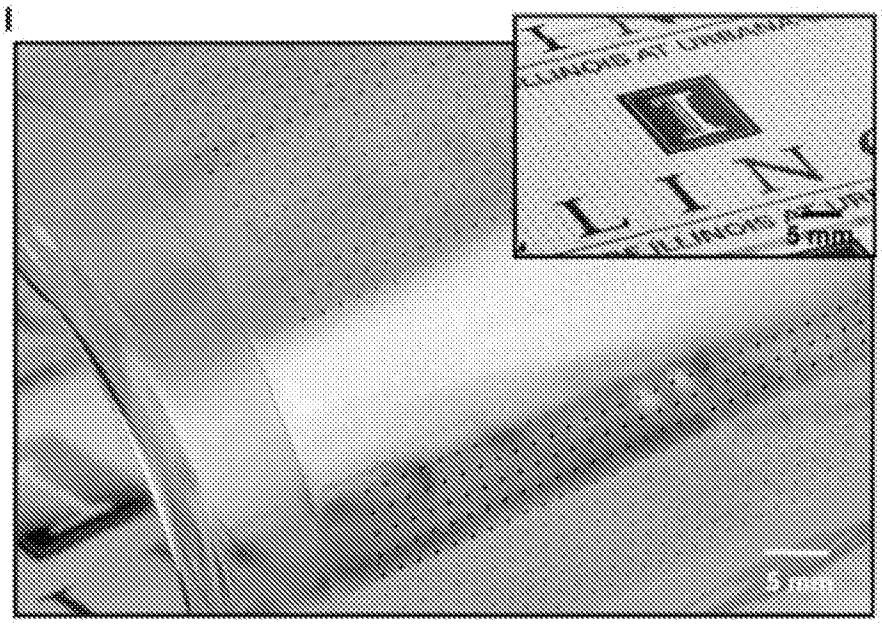


Figure 1 (cont'd)

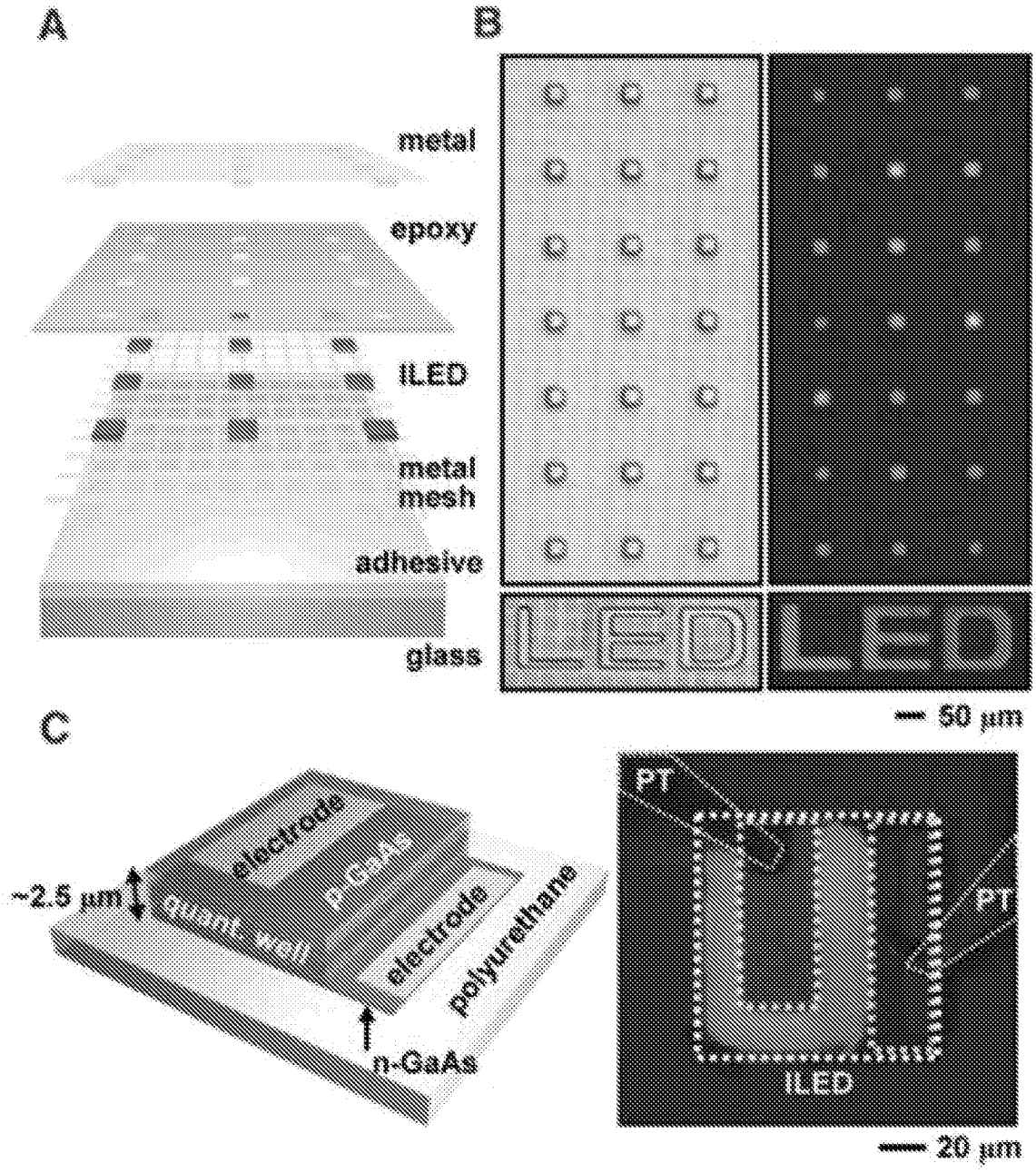

A
B
metal
epoxy
ILED
metal mesh
adhesive
glass
50 μm
C
~2.5 μm
electrode
quant. well
n-GaAs
electrode
polyurethane
n-GaAs
Pt
Pt
ILED
20 μm

Figure 2

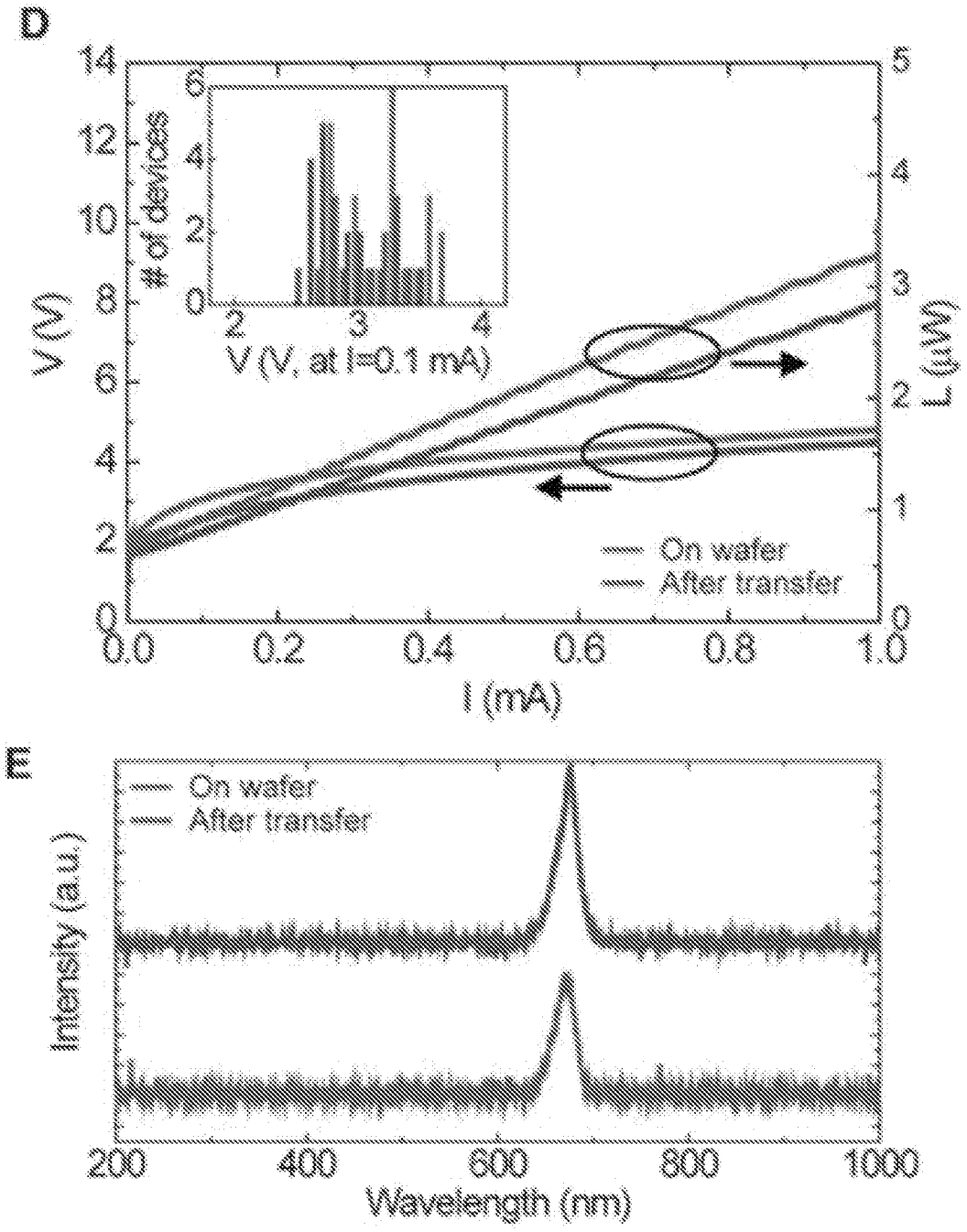


Figure 2 (cont'd)

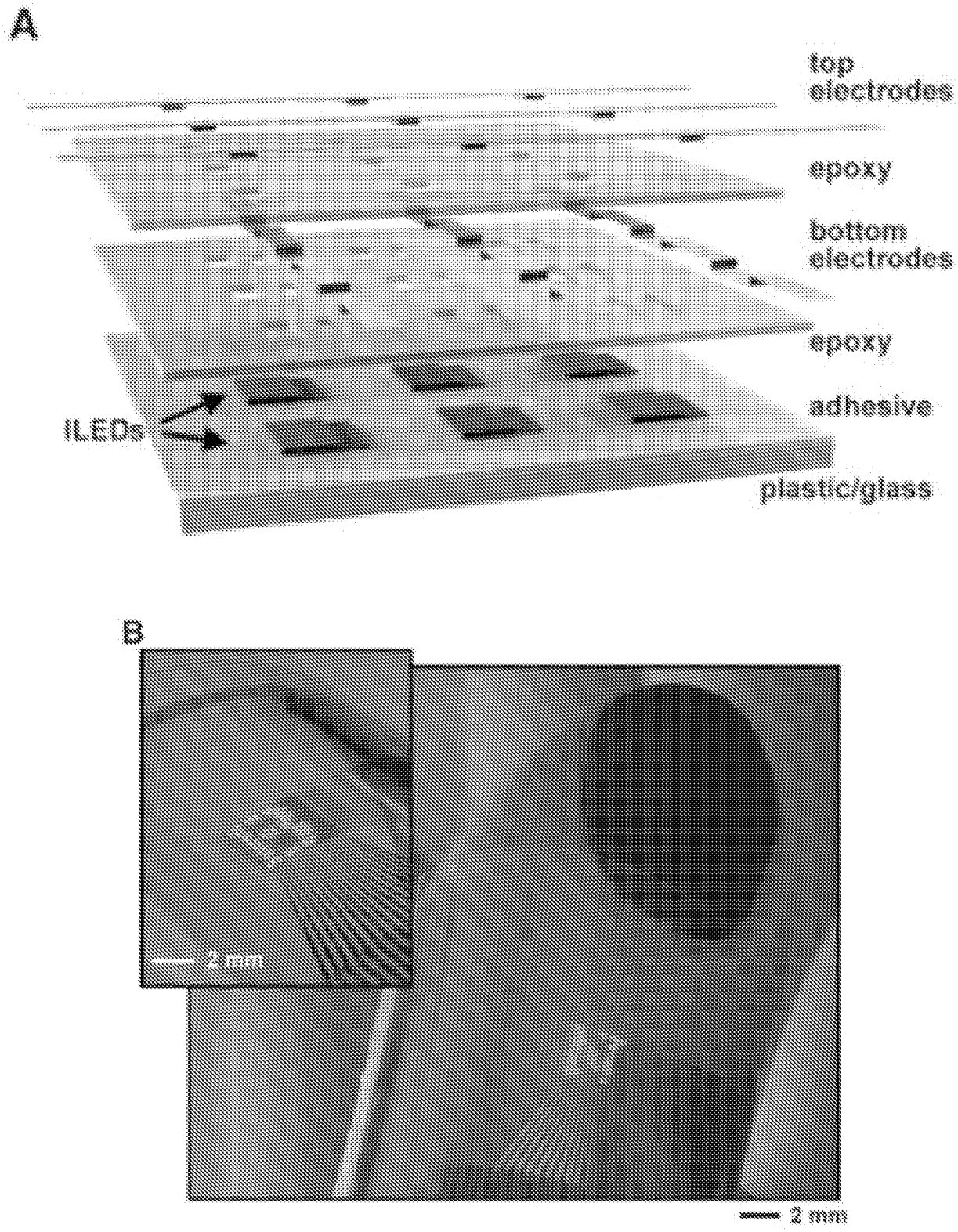

A
top electrodes
epoxy
bottom electrodes
epoxy
adhesive
ILEDs
plastic/glass
B
2 mm
2 mm

Figure 3

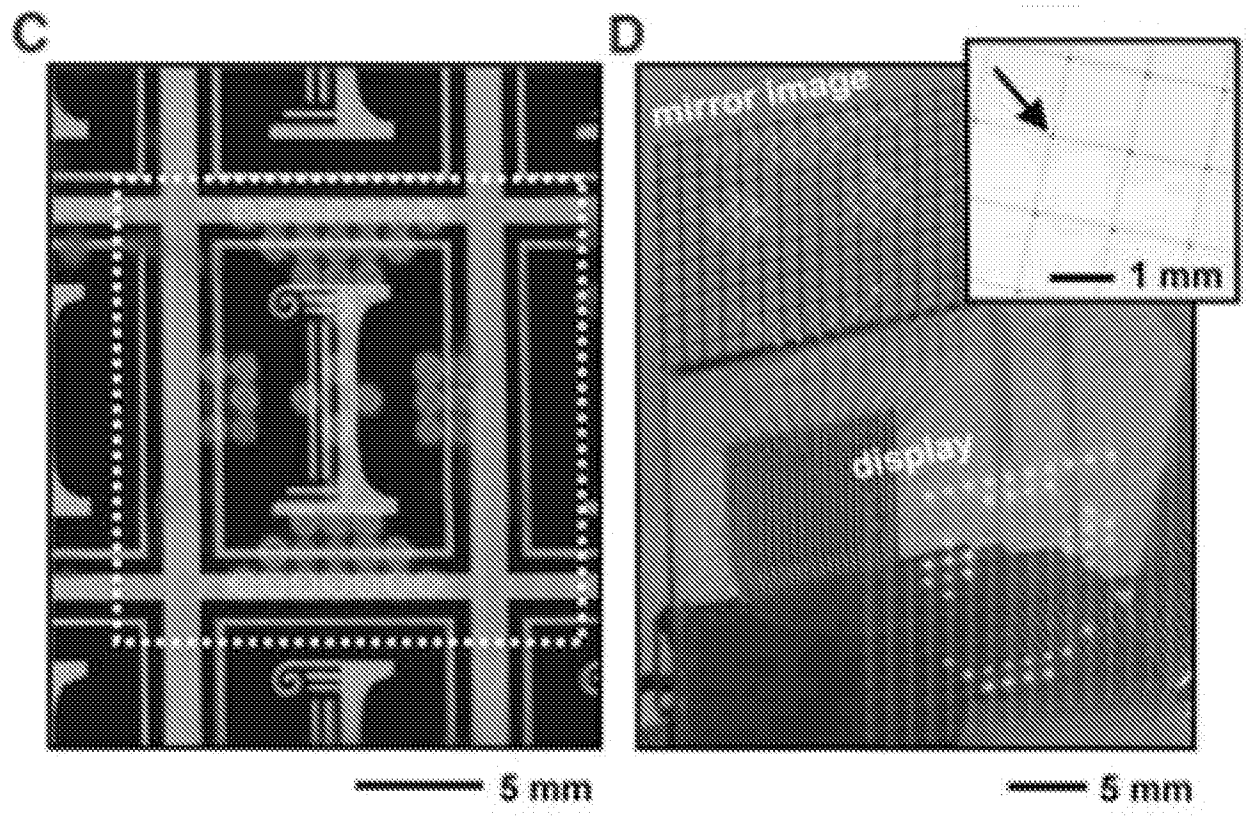
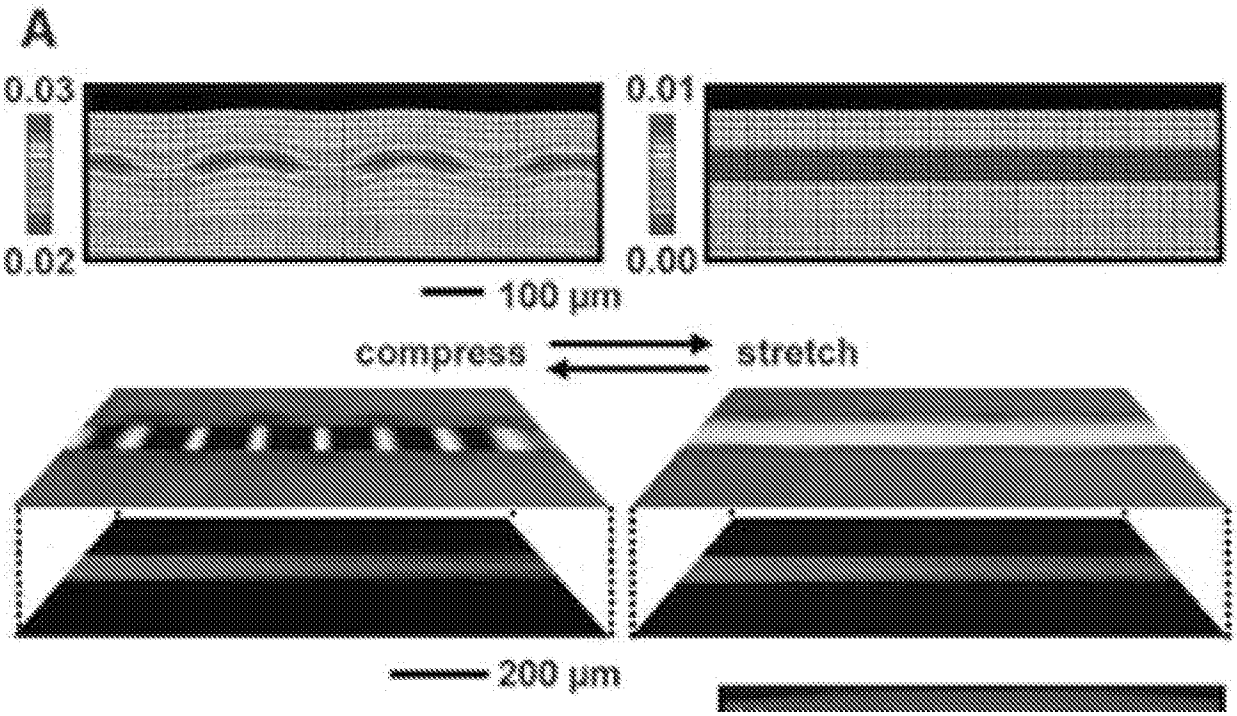


Figure 3 (cont'd)



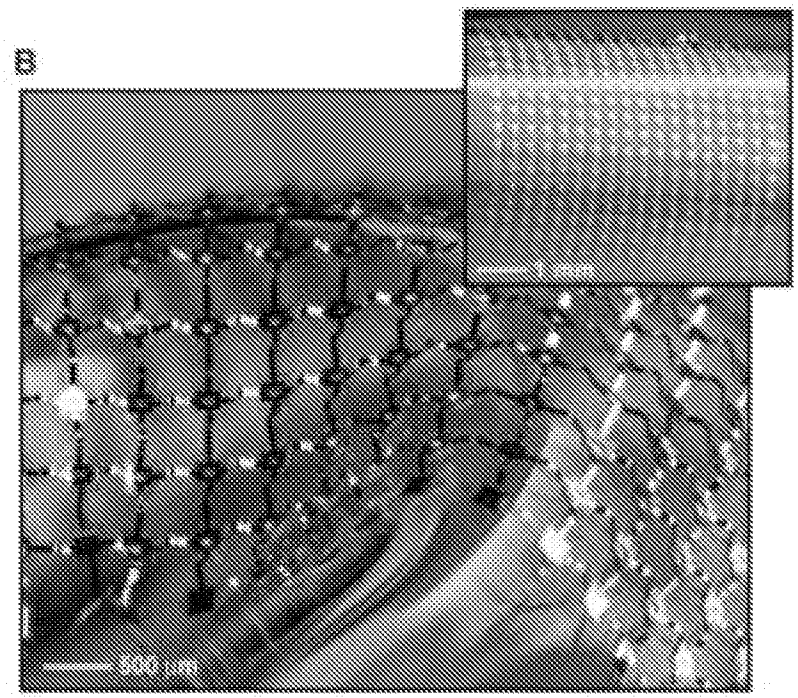


Figure 4

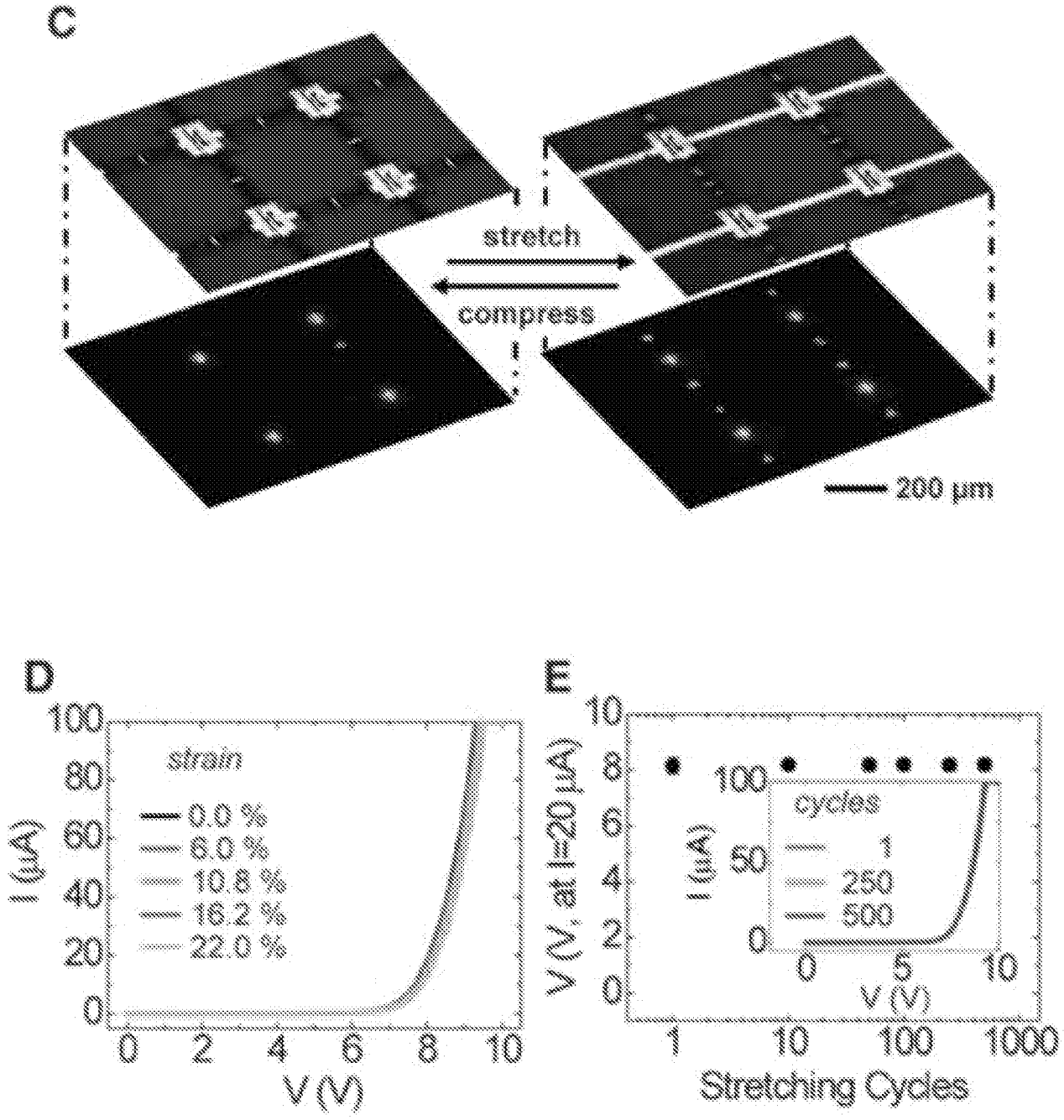
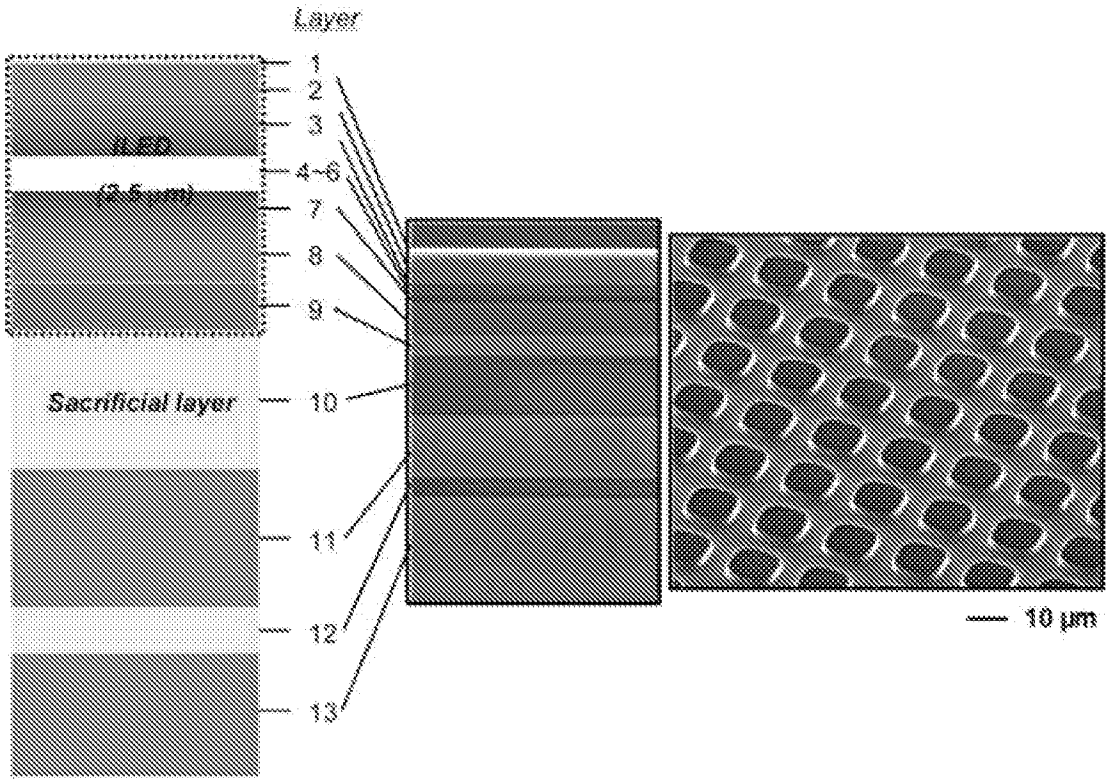


Figure 4 (cont'd)



Layer	Layer Name	Material	Thickness (nm)	Type	Dopant	Concentration (cm^{-3})
1	Contact	GaAs	5	P	C	1.00E+19
2	Spreader	$Al_{0.45}Ga_{0.55}As$	800	P	C	1.00E+18
3	Clad	$In_{0.5}Al_{0.5}P$	200	P	Zn	3E17 to 6E17
4	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
5	Well	$In_{0.56}Ga_{0.44}P$	6	-	-	<1E16
6	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
7	Clad	$In_{0.5}Al_{0.5}P$	200	N	Si	1.00E+18
8	Spreader	$Al_{0.45}Ga_{0.55}As$	800	N	Si	1.00E+18
9	Contact	GaAs	500	N	Si	4.00E+18
10		$Al_{0.95}Ga_{0.05}As$	1500	N	Si	1.00E+17
11		GaAs	1500	N	Si	1.00E+17
12		$Al_{0.95}Ga_{0.05}As$	500	N	Si	1.00E+17
13	Substrate	GaAs		N	Si	>1E18

Figure 5

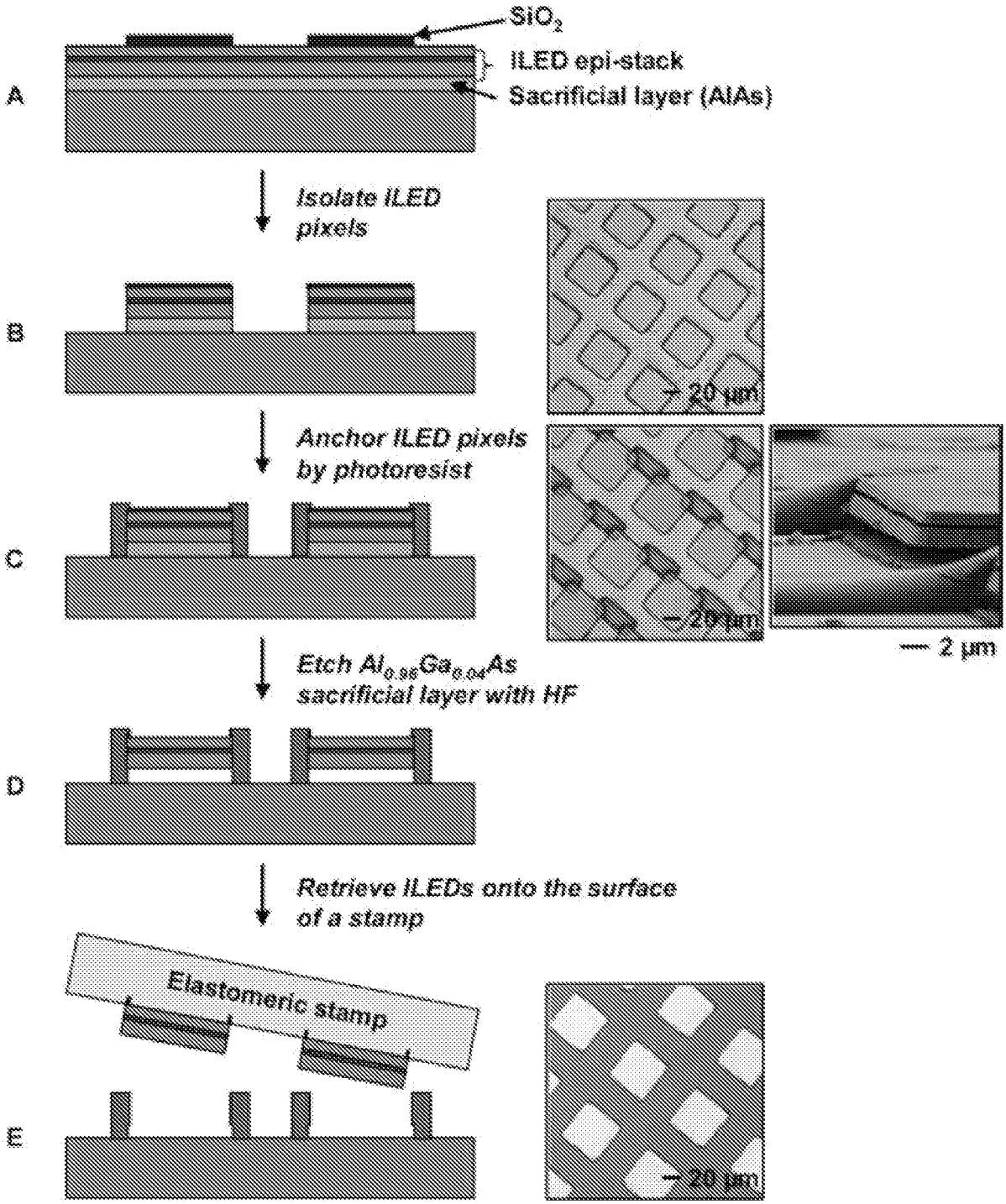

SiO_2
ILED epi-stack
Sacrificial layer (AlAs)
A
Isolate ILED pixels
B
~ 20 μm
Anchor ILED pixels by photoresist
C
~ 20 μm
~ 2 μm
Etch $Al_{0.96}Ga_{0.04}As$ sacrificial layer with HF
D
Retrieve ILEDs onto the surface of a stamp
Elastomeric stamp
E
~ 20 μm

Figure 6

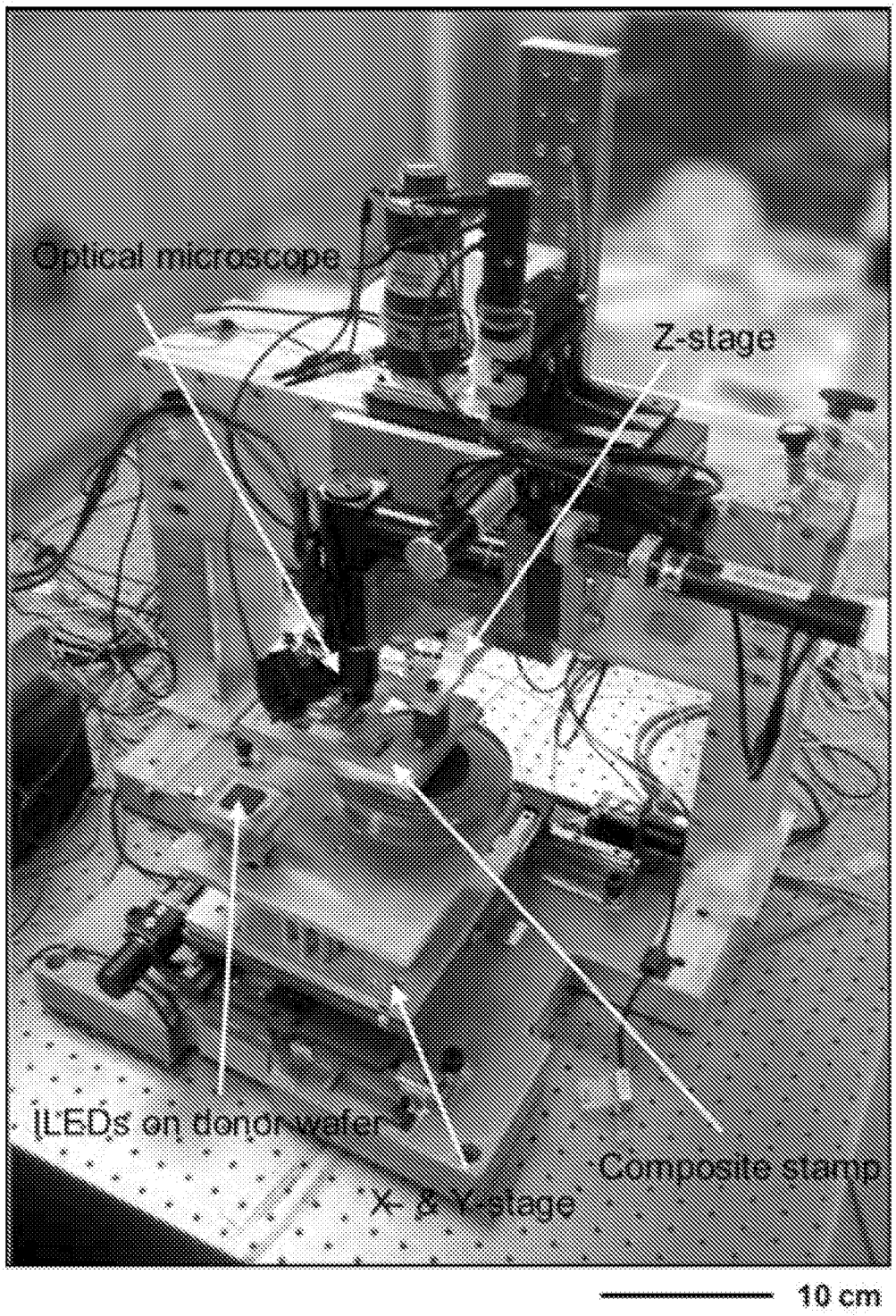

Optical microscope
Z-stage
LEDs on donor wafer
Composite stamp
X- & Y-stage
10 cm

Figure 7

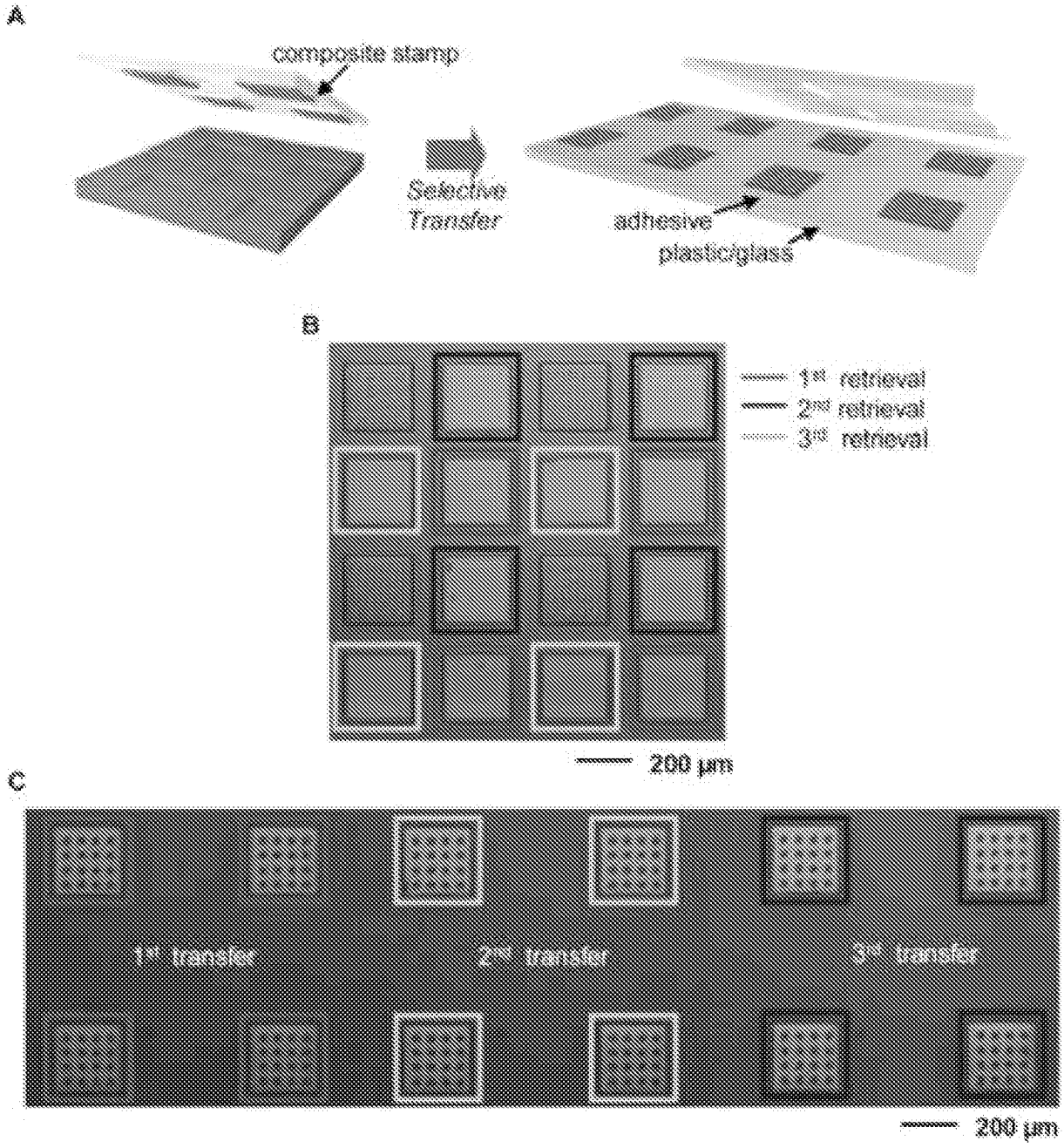

A
composite stamp
Selective Transfer
adhesive
plastic/glass
B
1st retrieval
2nd retrieval
3rd retrieval
200 μm
C
1st transfer
2nd transfer
3rd transfer
200 μm

Figure 8

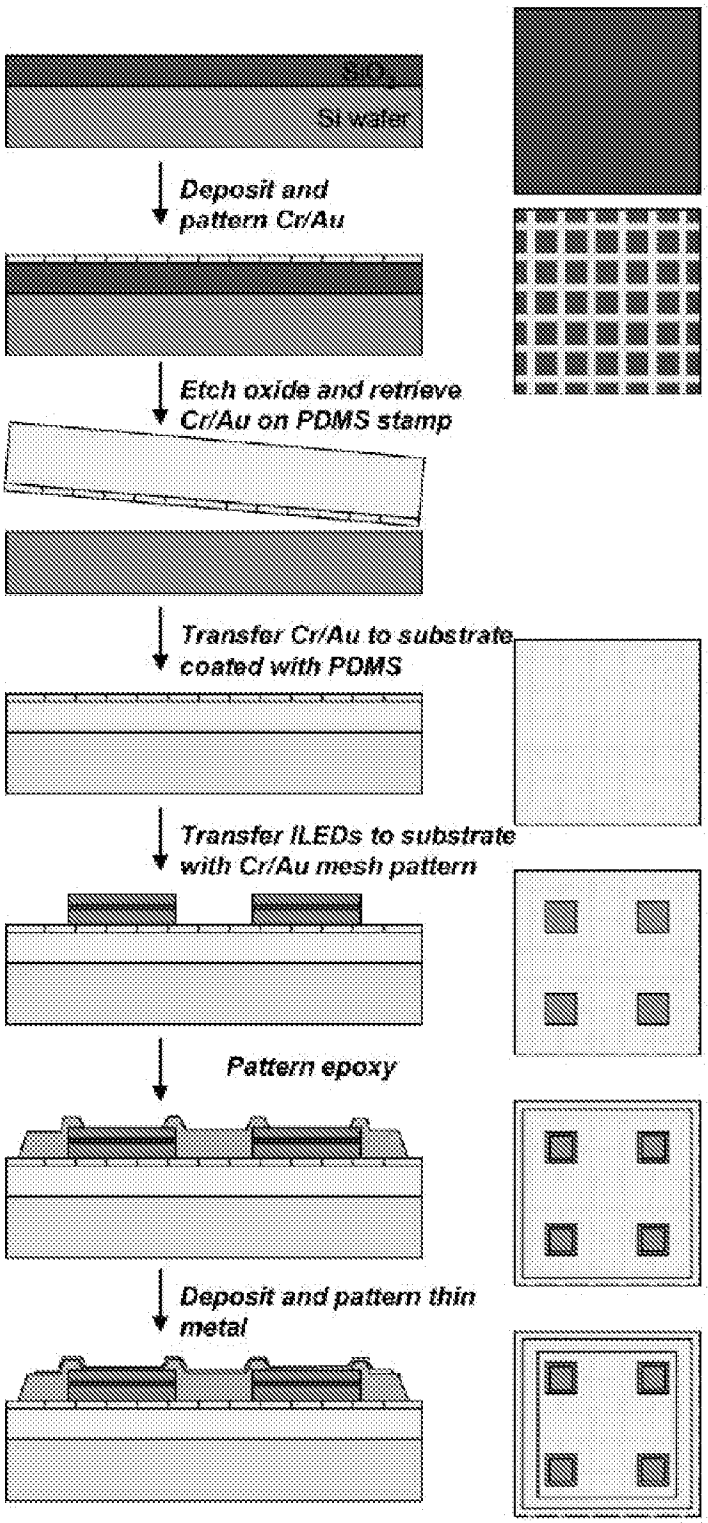

Si wafer
Deposit and pattern Cr/Au
Etch oxide and retrieve Cr/Au on PDMS stamp
Transfer Cr/Au to substrate coated with PDMS
Transfer ILEDs to substrate with Cr/Au mesh pattern
Pattern epoxy
Deposit and pattern thin metal

Figure 9

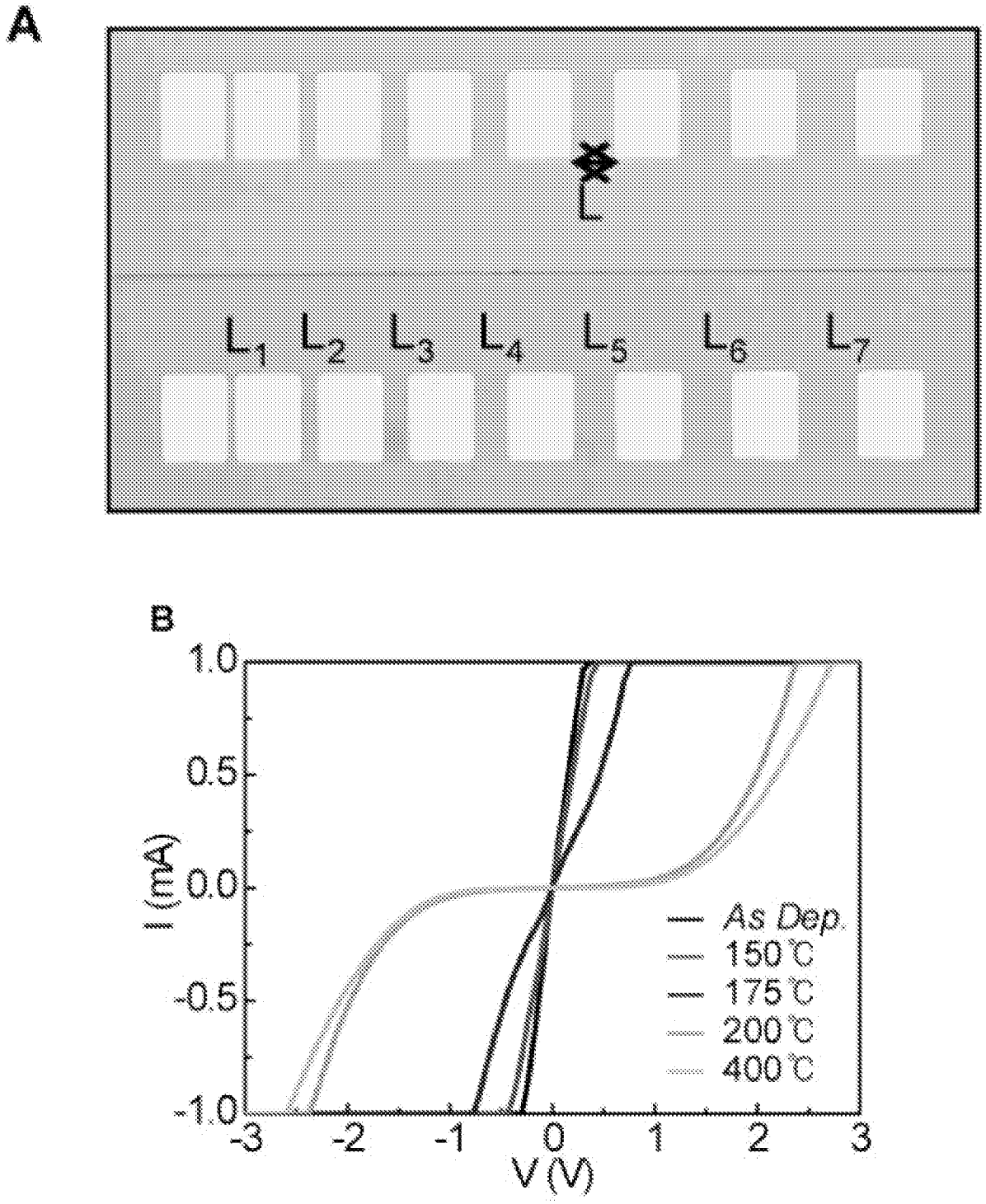

A
L
L1 L2 L3 L4 L5 L6 L7
B
1.0
0.5
0.0
-0.5
-1.0
I (mA)
-3 -2 -1 0 1 2 3
V (V)
As Dep.
150 ℃
175 ℃
200 ℃
400 ℃

Figure 10

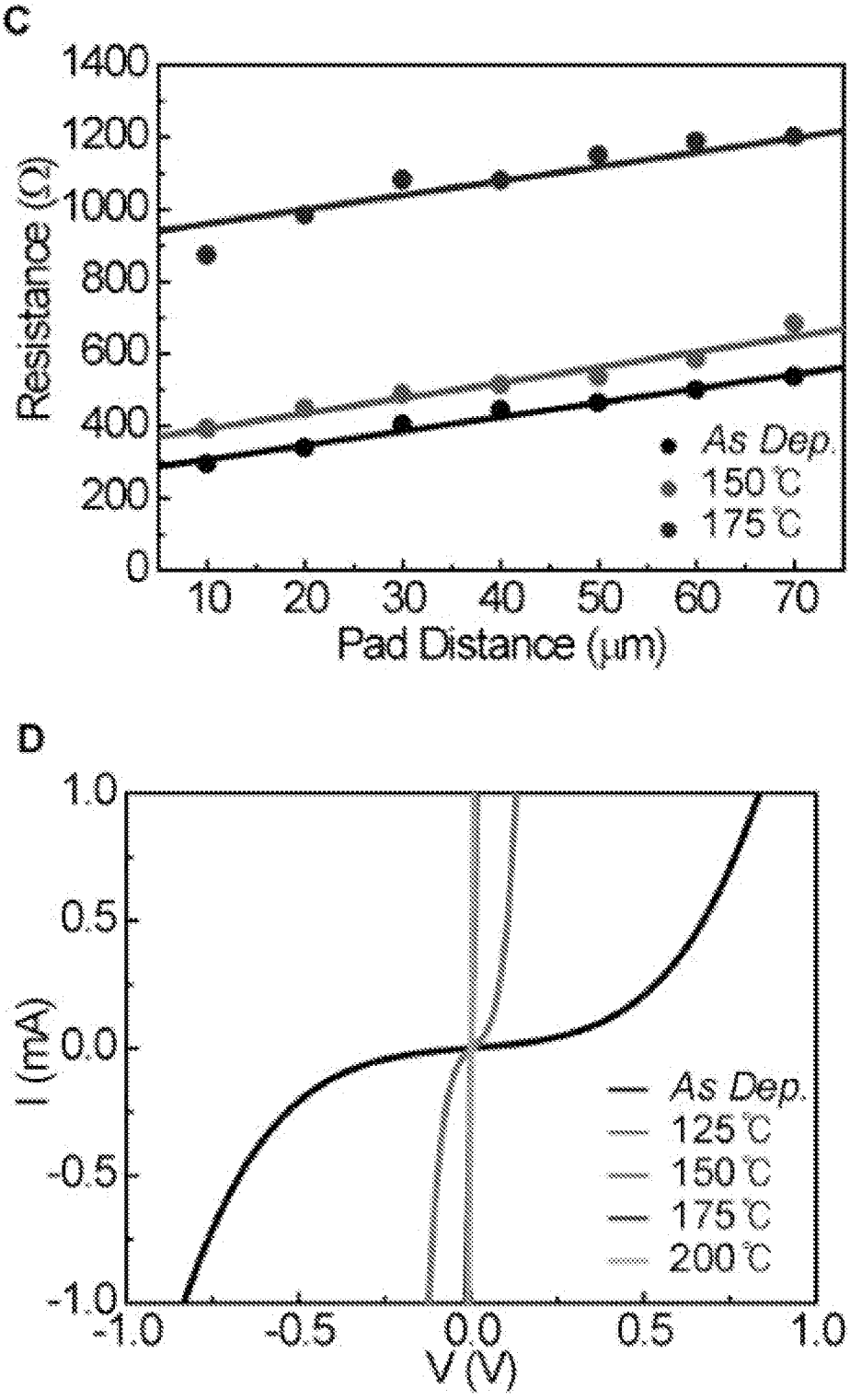


Figure 10 (cont'd)

E

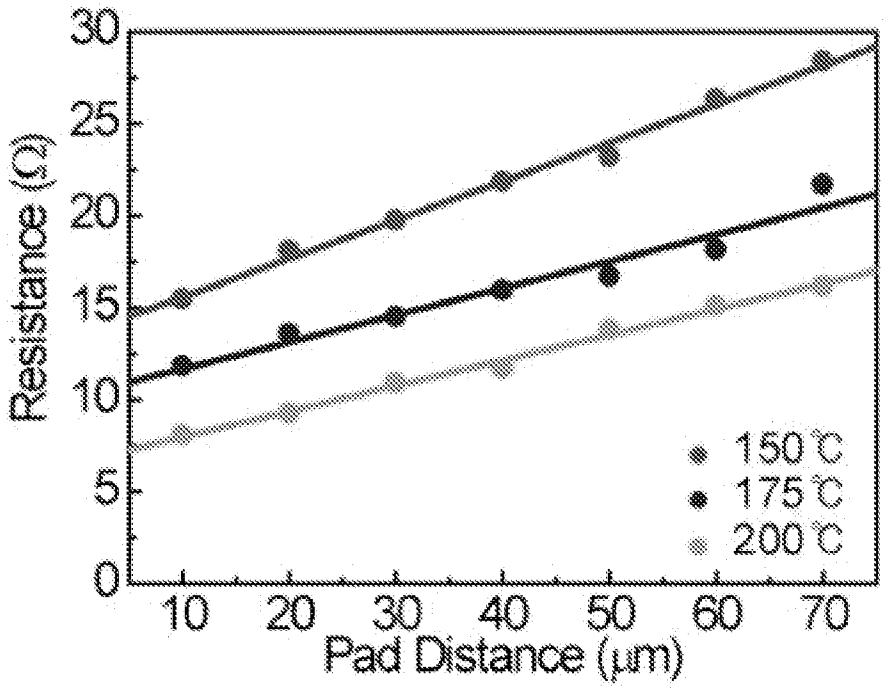


Figure 10 (cont'd)

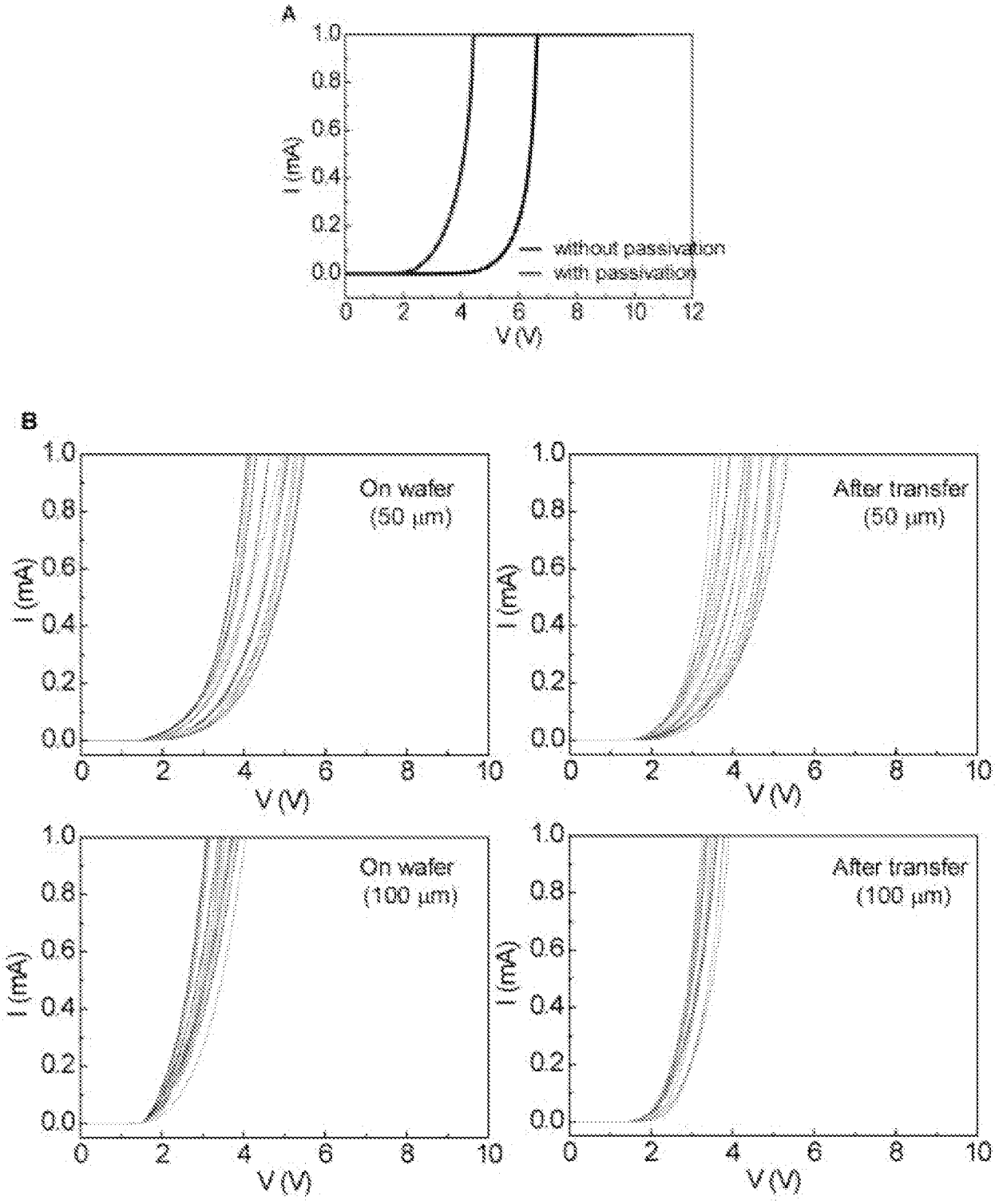

A
I (mA)
V (V)
without passivation
with passivation
B
On wafer
(50 μm)
After transfer
(50 μm)
On wafer
(100 μm)
After transfer
(100 μm)

Figure 11

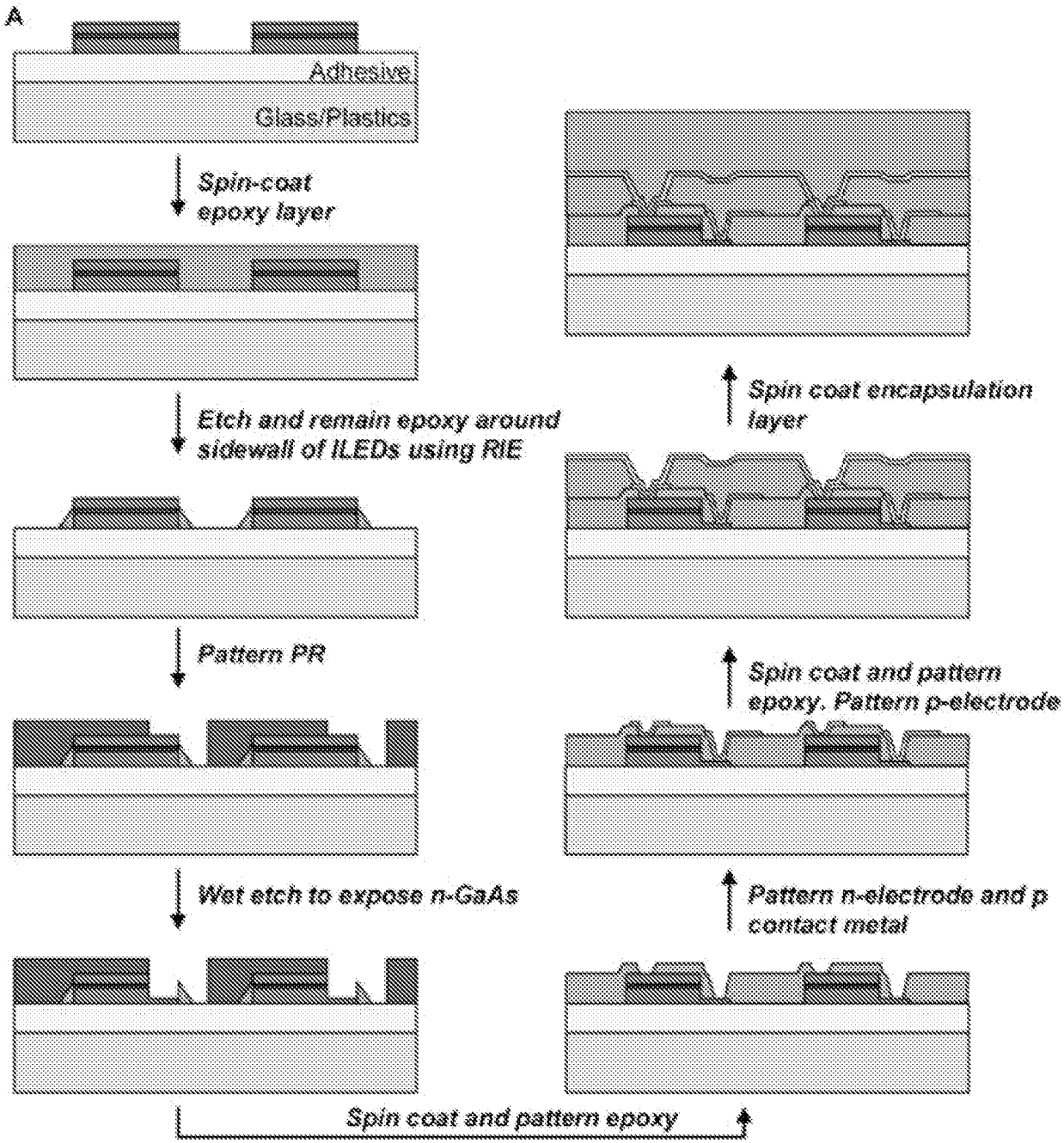

A
Adhesive
Glass/Plastics
Spin-coat epoxy layer
Etch and remain epoxy around sidewall of ILEDs using RIE
Pattern PR
Wet etch to expose n-GaAs
Spin coat and pattern epoxy
Pattern n-electrode and p contact metal
Spin coat and pattern epoxy. Pattern p-electrode
Spin coat encapsulation layer

Figure 12

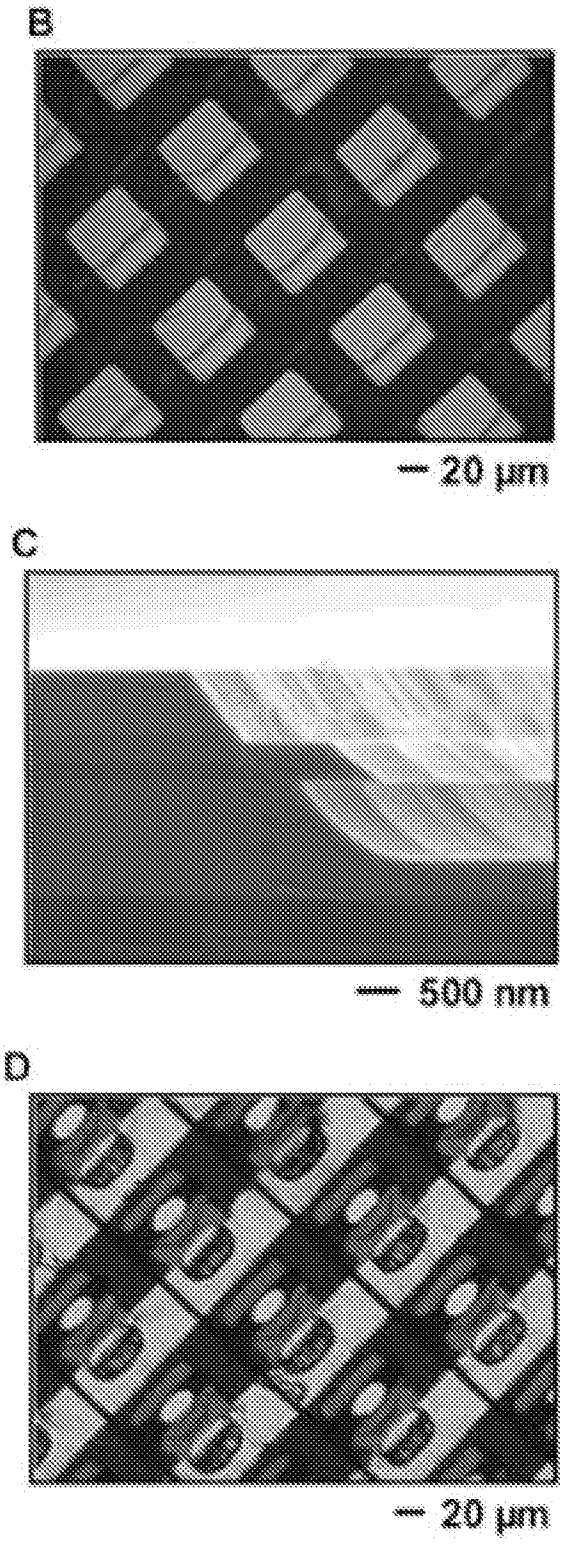


Figure 12 (cont'd)

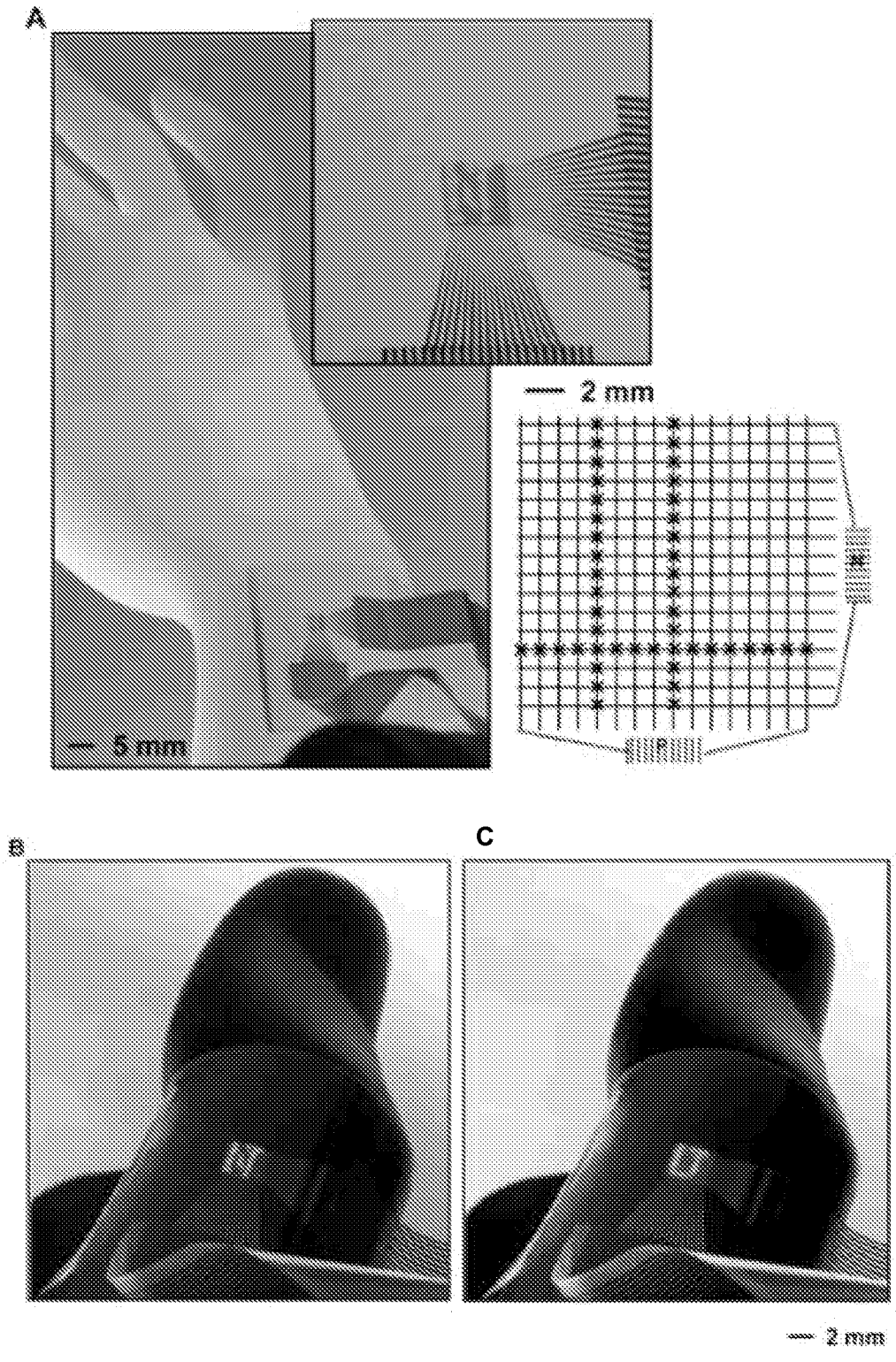


Figure 13

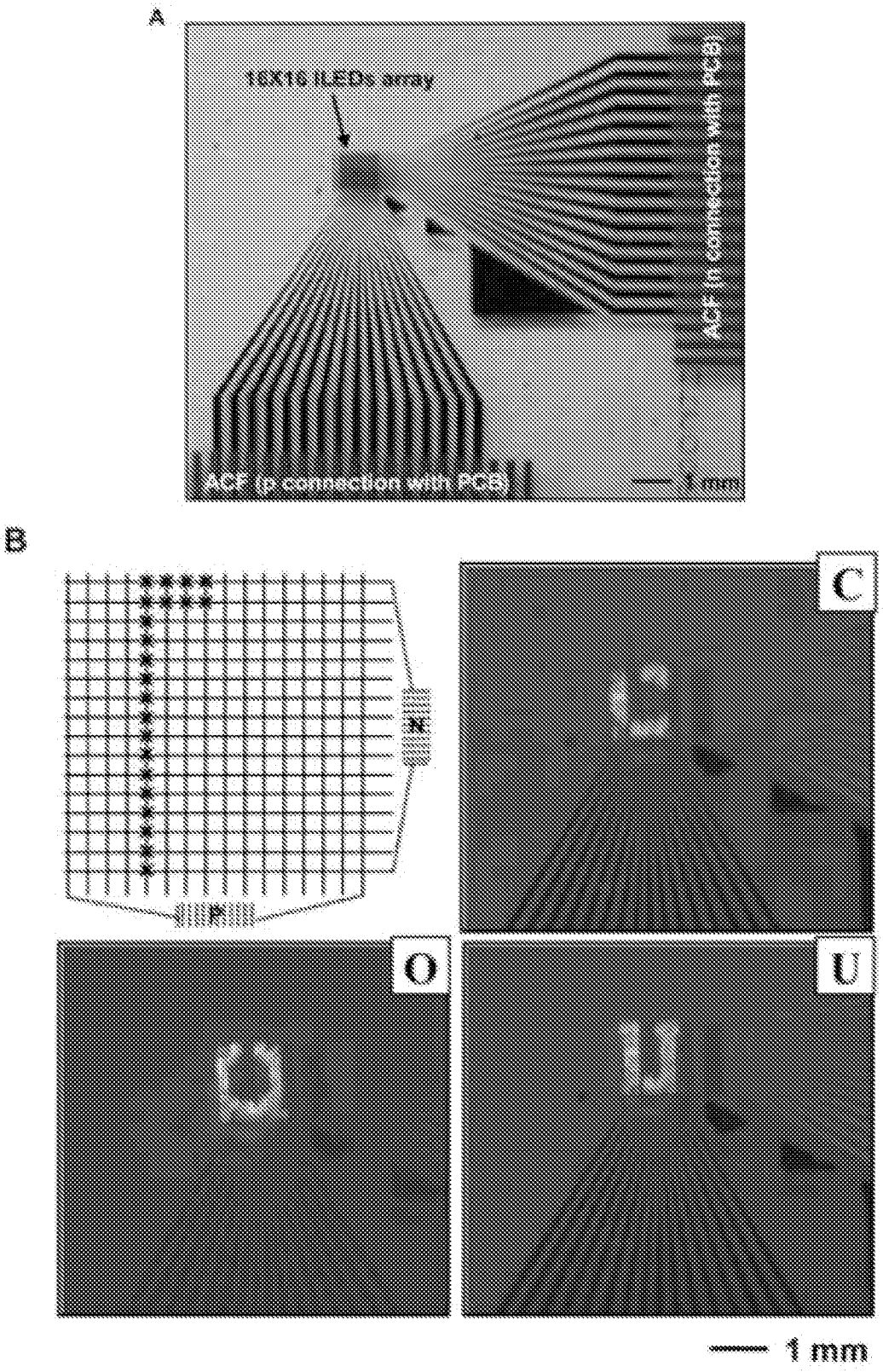

A
16X16 ILEDs array
ACF (in connection with PCB)
ACF (in connection with PCB)
1 mm
B
N
P
C
O
U
1 mm

Figure 14

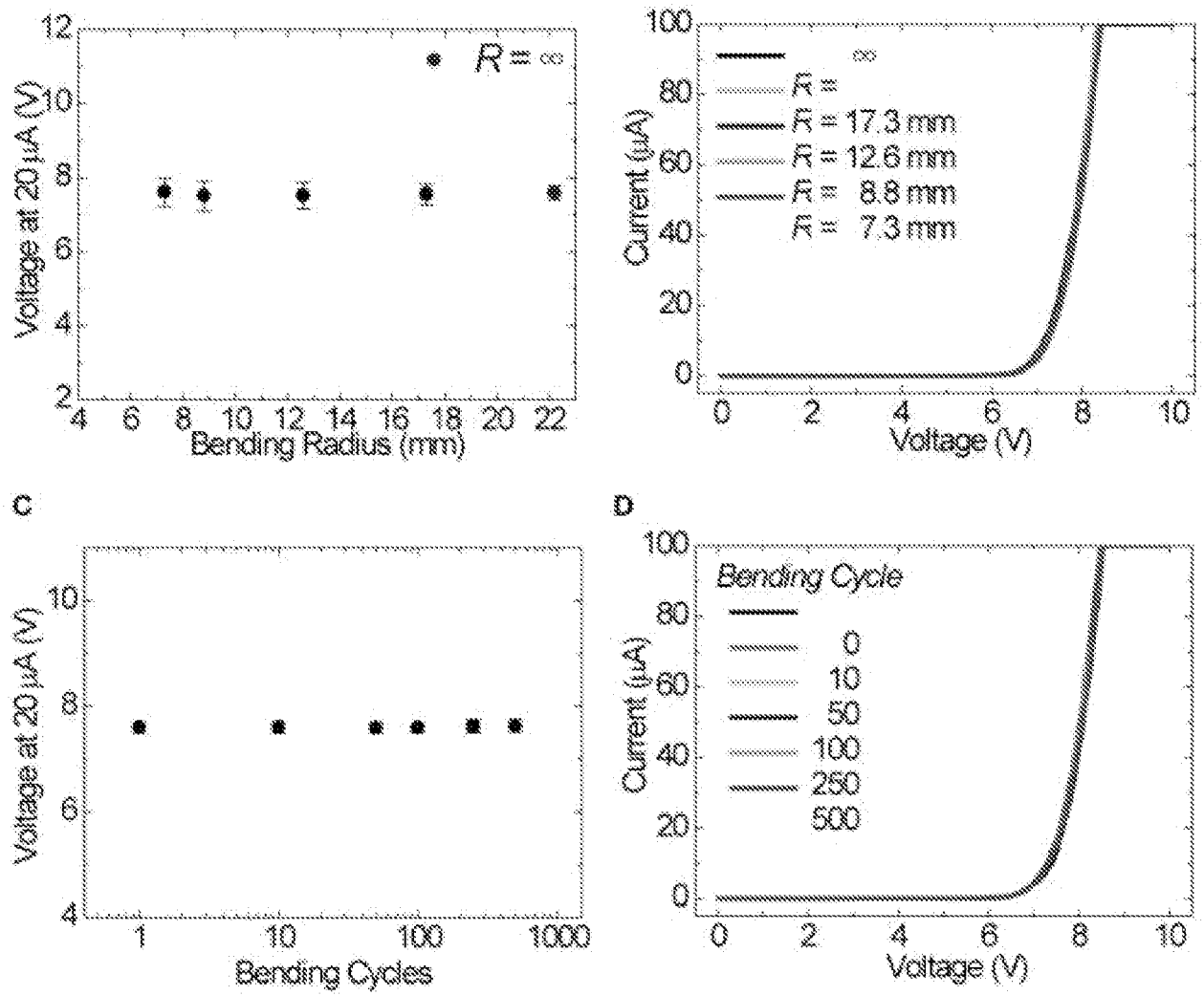

Voltage at 20 μA (V)
Bending Radius (mm)
R = ∞
Current (μA)
Voltage (V)
R = ∞
R = 17.3 mm
R = 12.6 mm
R = 8.8 mm
R = 7.3 mm
C
Voltage at 20 μA (V)
Bending Cycles
D
Current (μA)
Voltage (V)
Bending Cycle
0
10
50
100
250
500

Figure 15

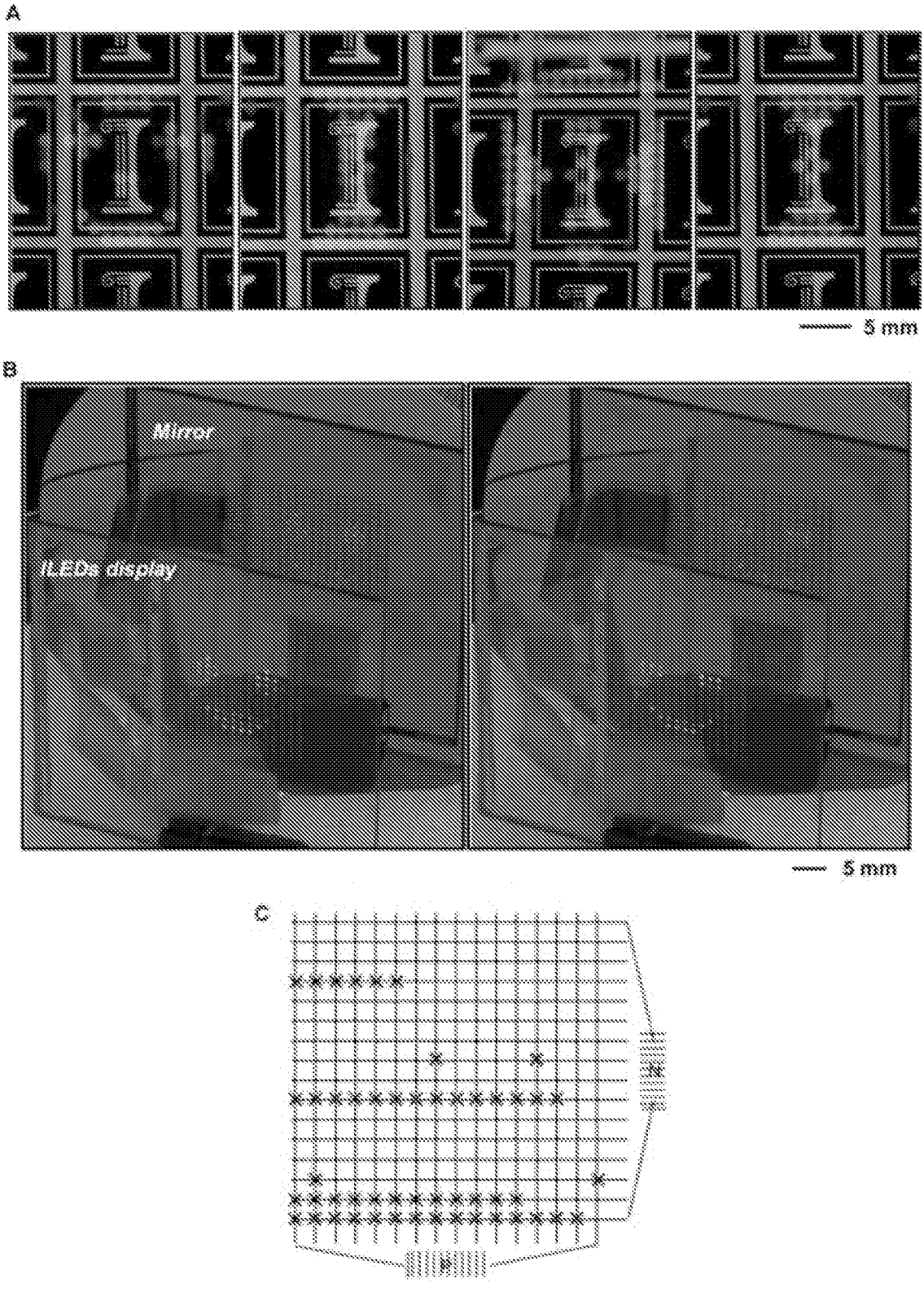


Figure 16

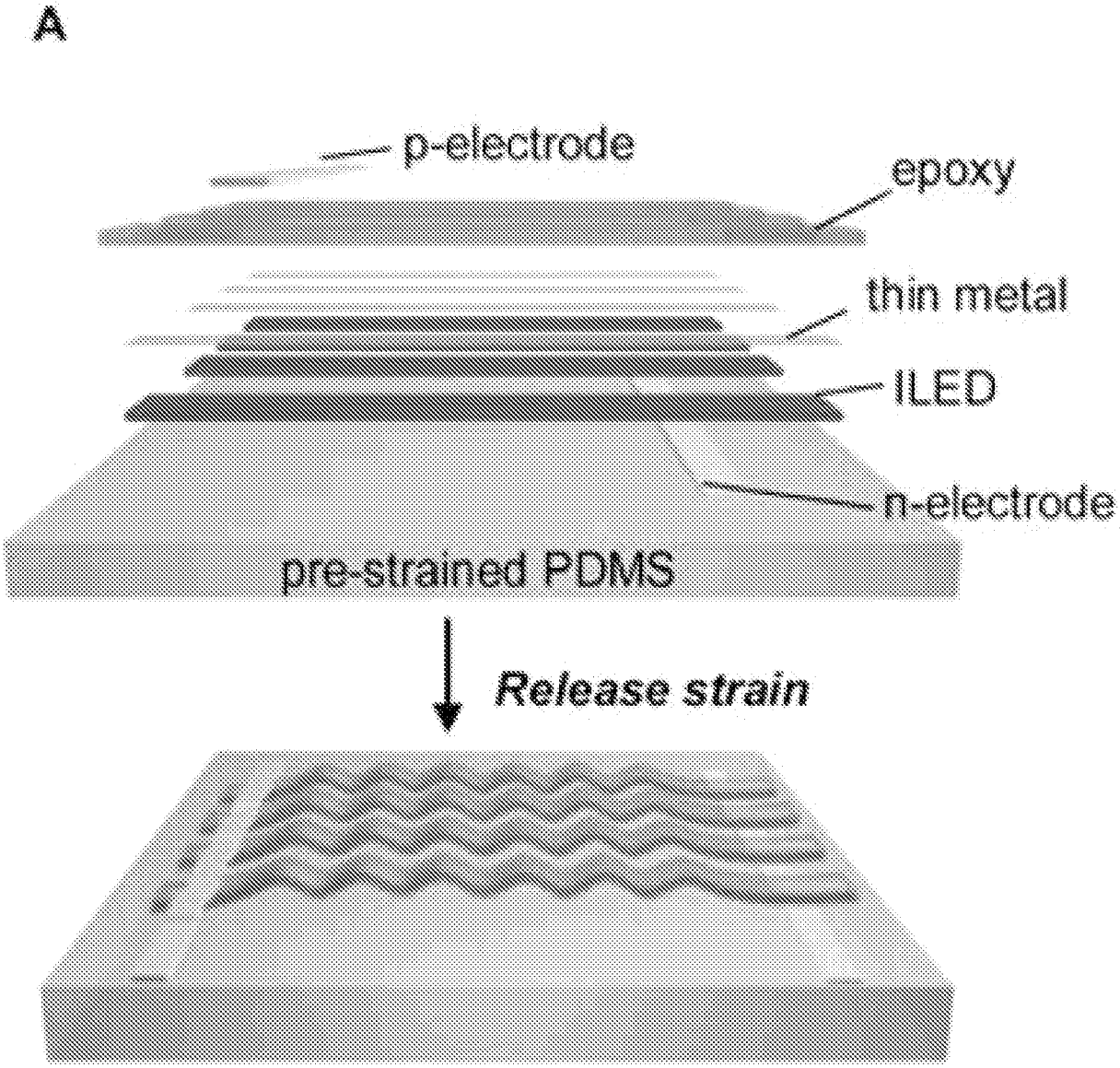

A
p-electrode
epoxy
thin metal
ILED
n-electrode
pre-strained PDMS
Release strain

Figure 17

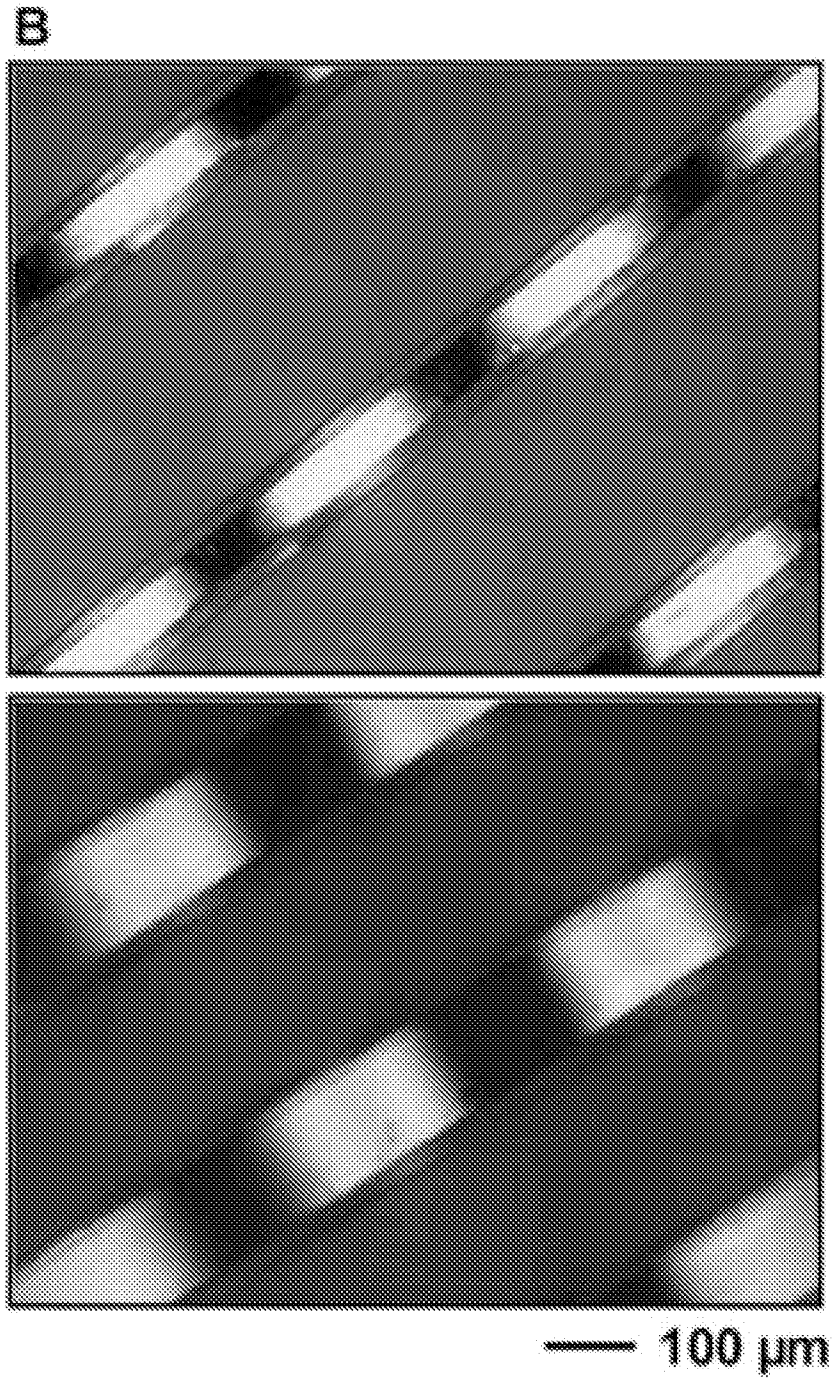
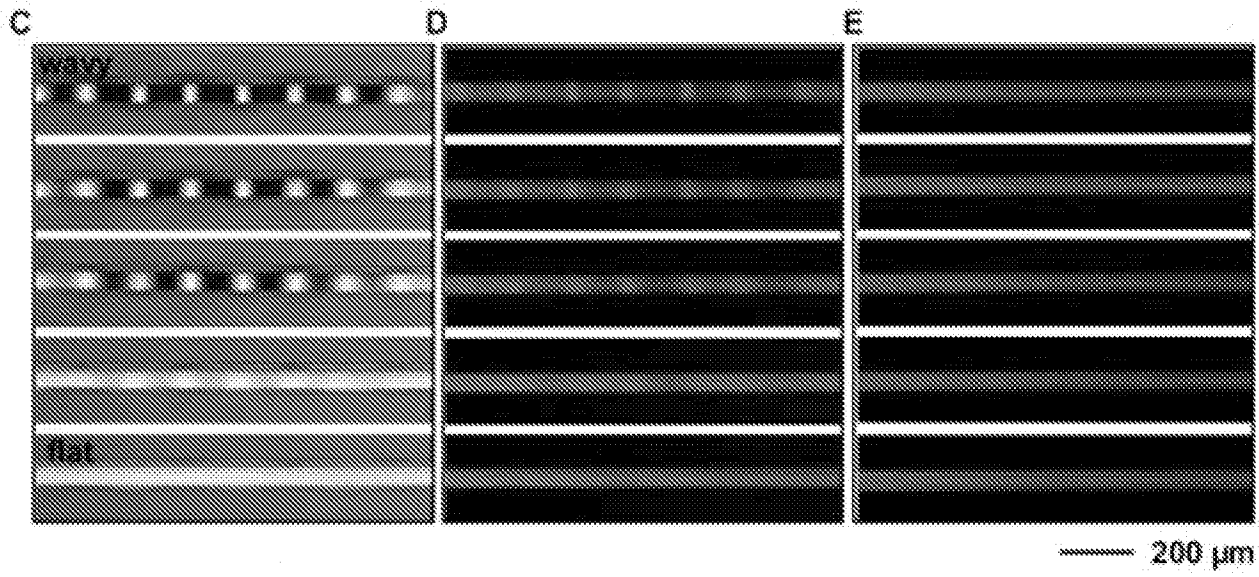


Figure 17 (cont'd)



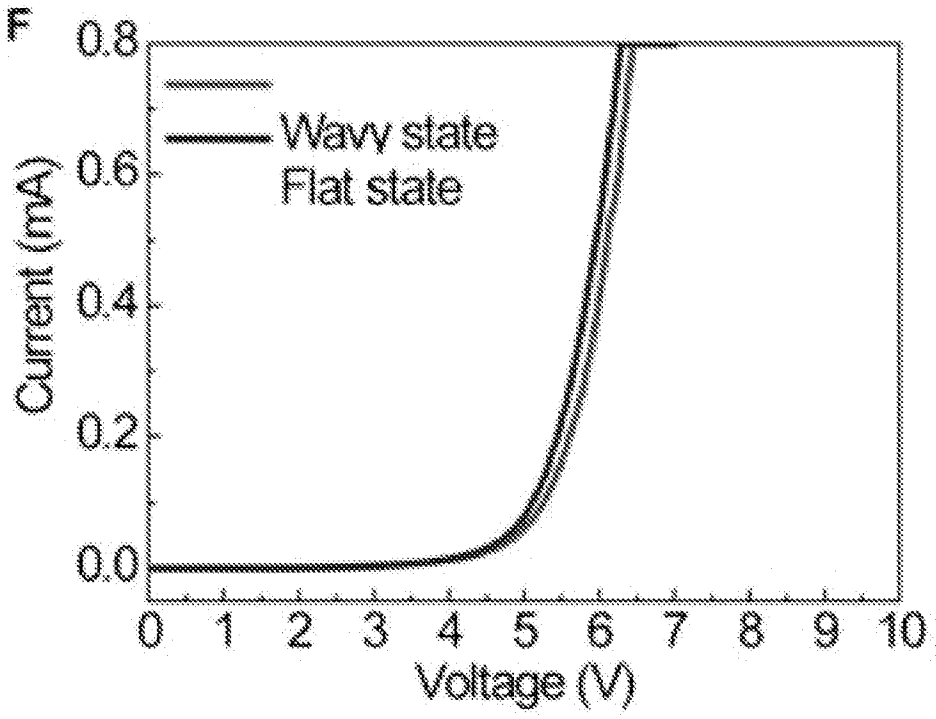


Figure 17 (cont'd)

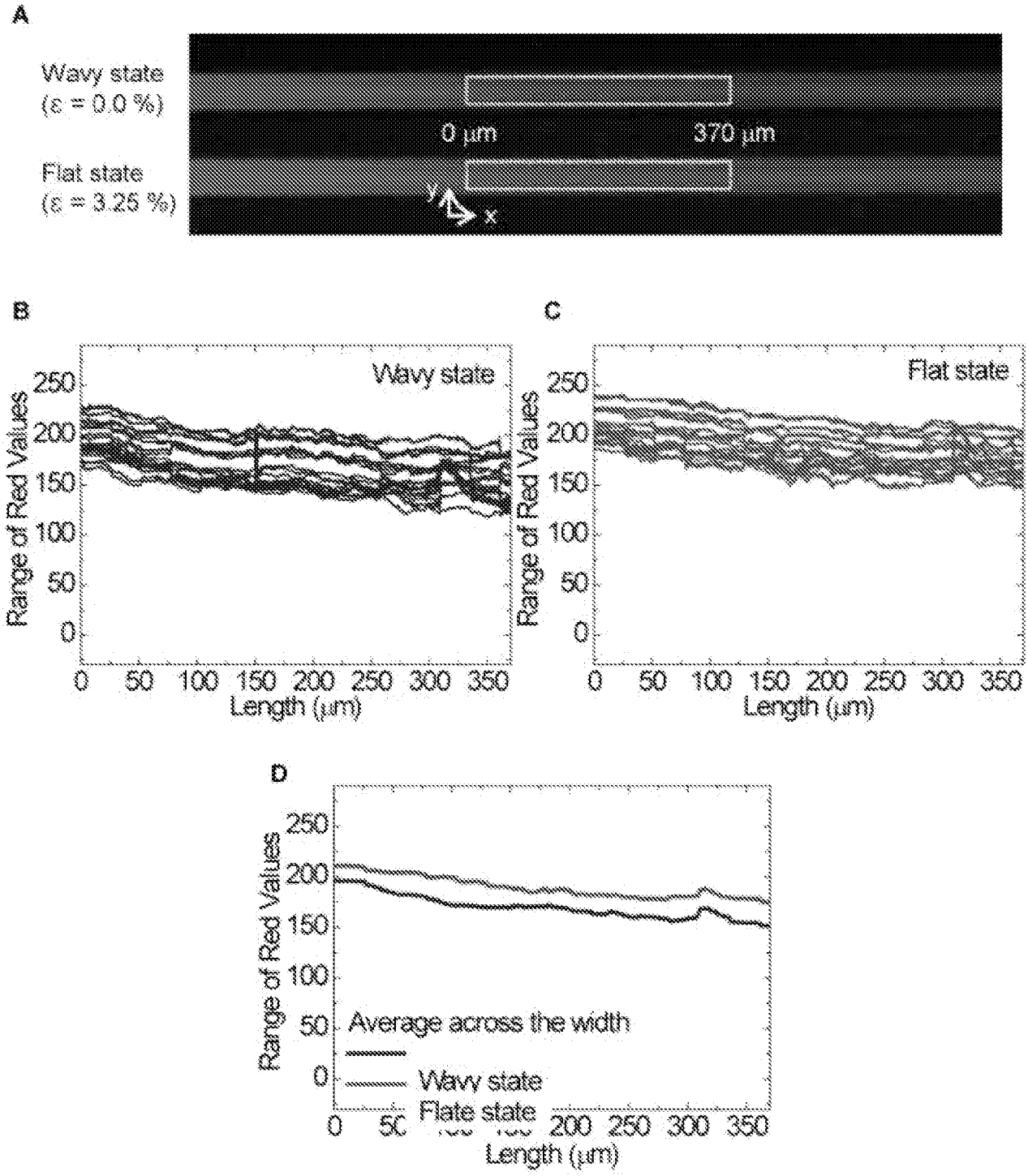

A
Wavy state
(ε = 0.0 %)
Flat state
(ε = 3.25 %)
0 μm
370 μm
y
x
B
Wavy state
Range of Red Values
Length (μm)
C
Flat state
Range of Red Values
Length (μm)
D
Range of Red Values
Average across the width
Wavy state
Flate state
Length (μm)

Figure 18

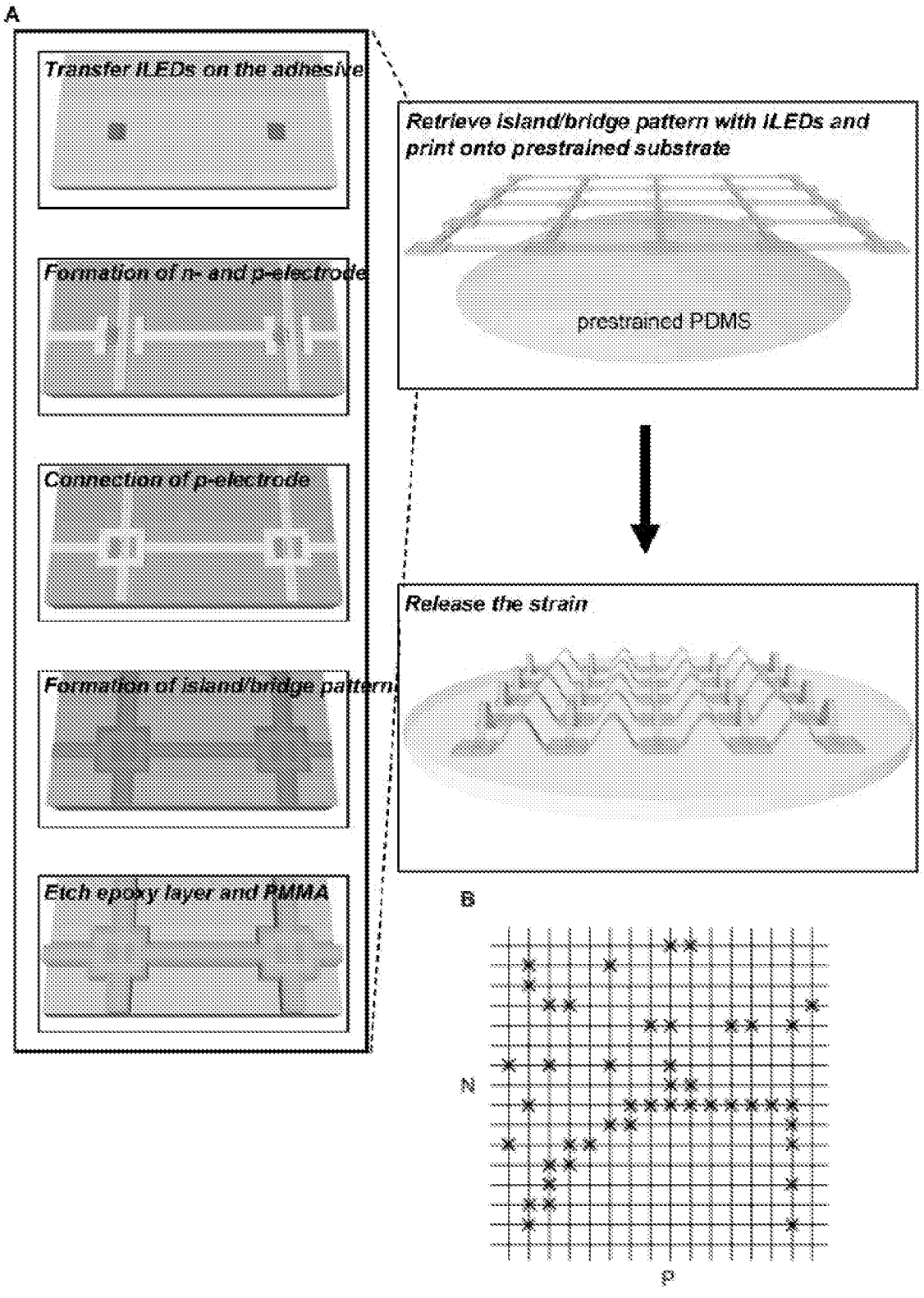

A
Transfer ILEDs on the adhesive
Formation of n- and p-electrode
Connection of p-electrode
Formation of island/bridge pattern
Etch epoxy layer and PMMA
Retrieve island/bridge pattern with ILEDs and print onto prestrained substrate
prestrained PDMS
Release the strain
B
N
P

Figure 19

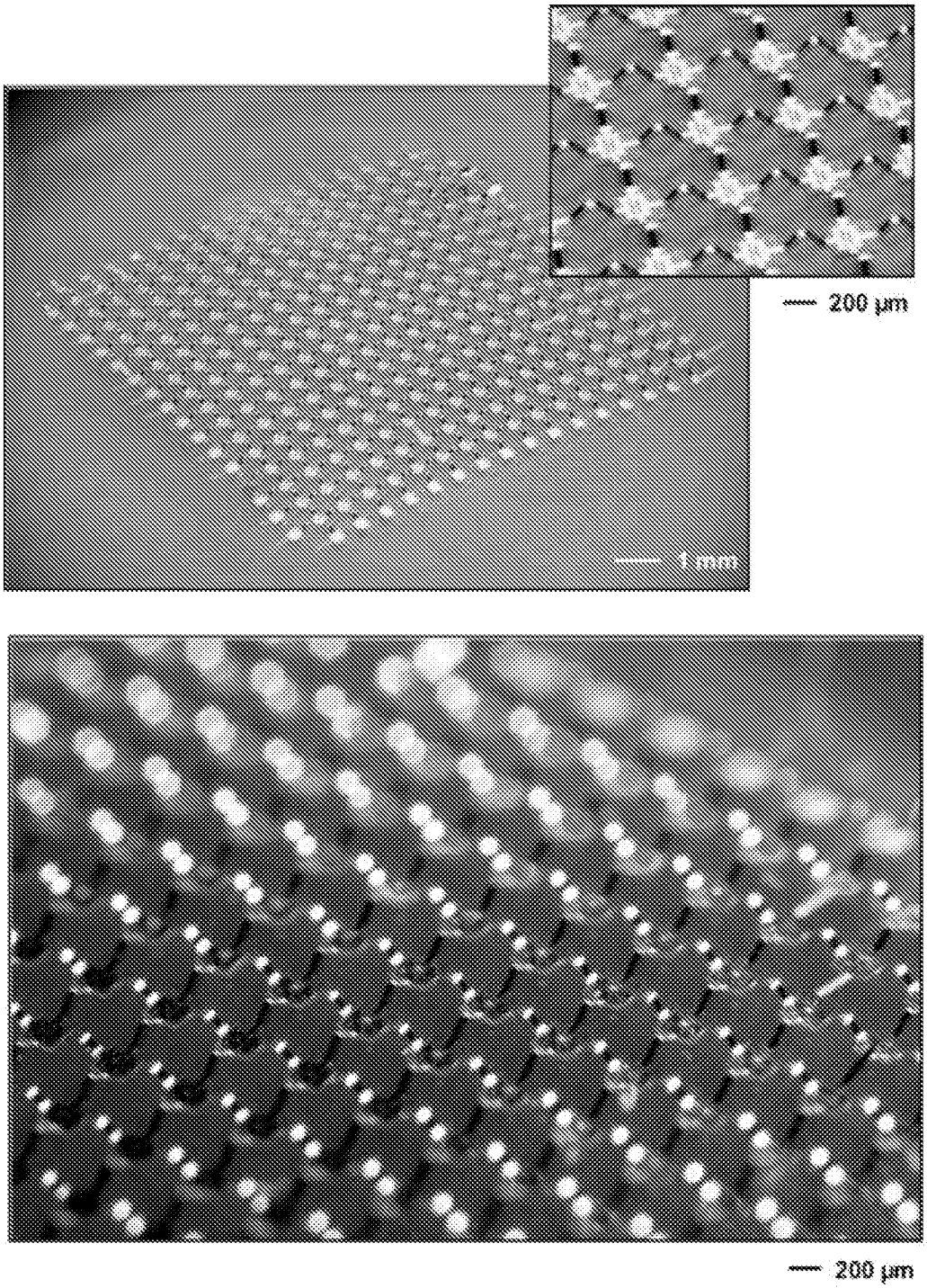


Figure 20

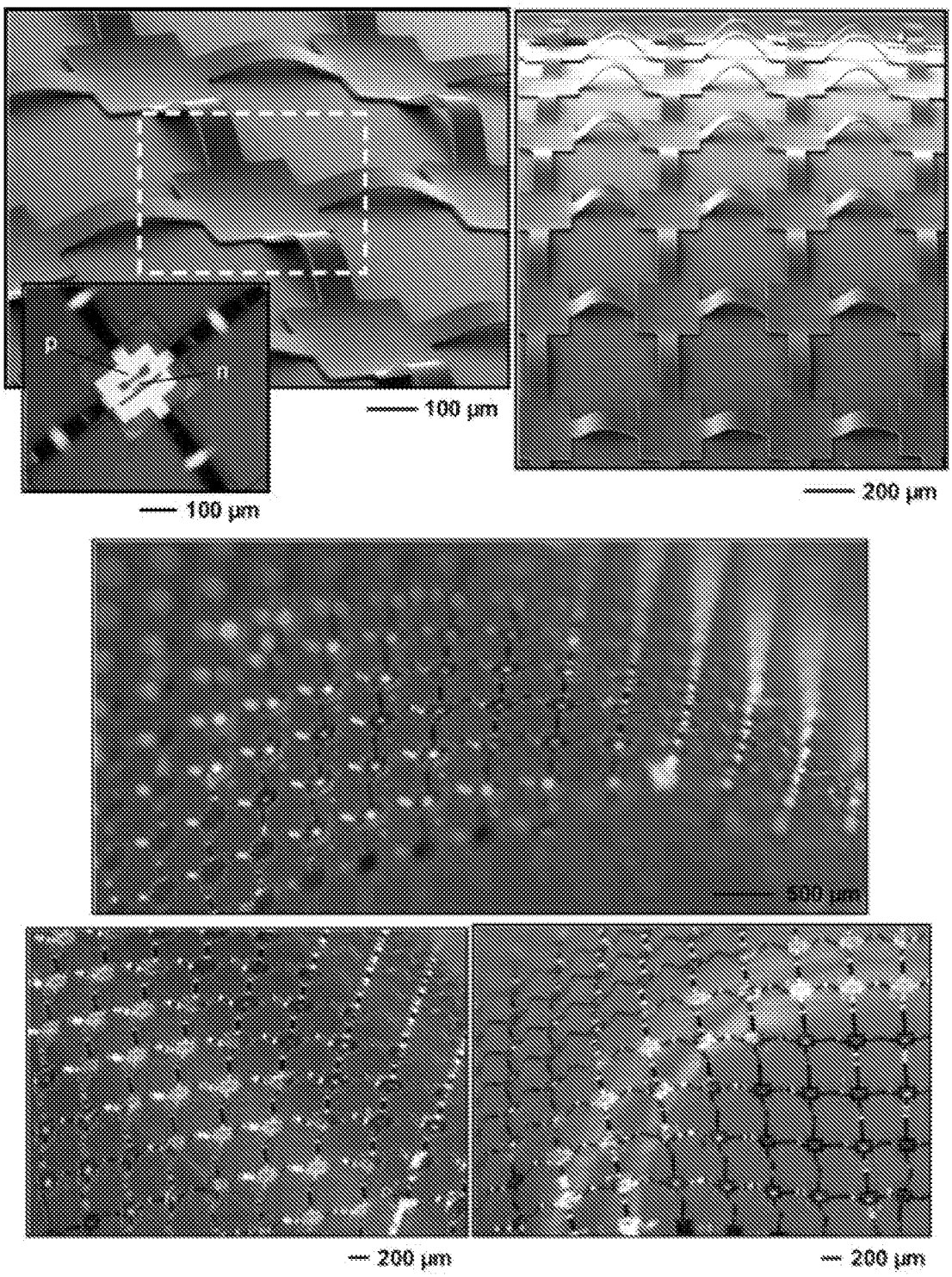


Figure 21

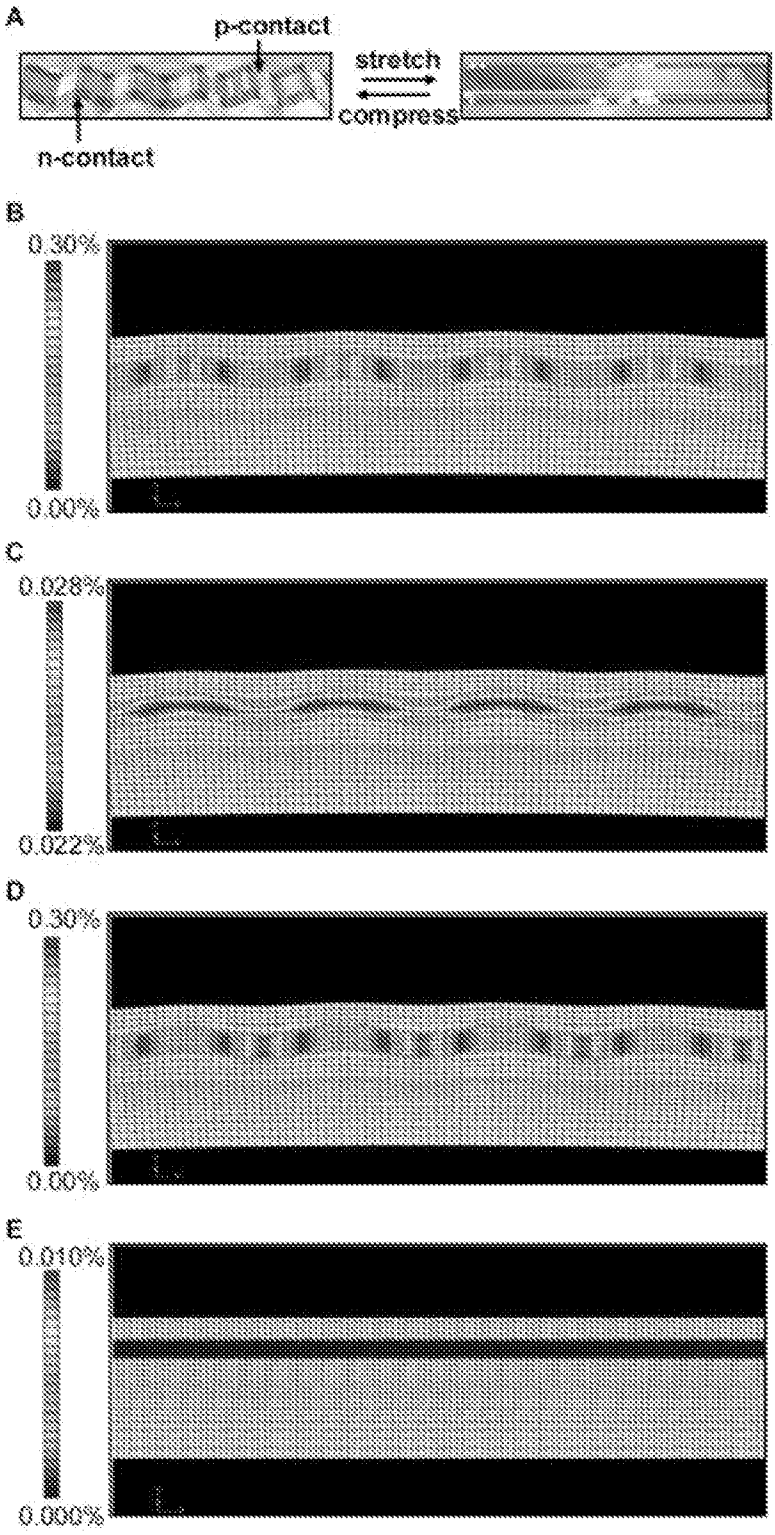

A
p-contact
stretch
compress
n-contact
B
0.30%
0.00%
C
0.028%
0.022%
D
0.30%
0.00%
E
0.010%
0.000%

Figure 22

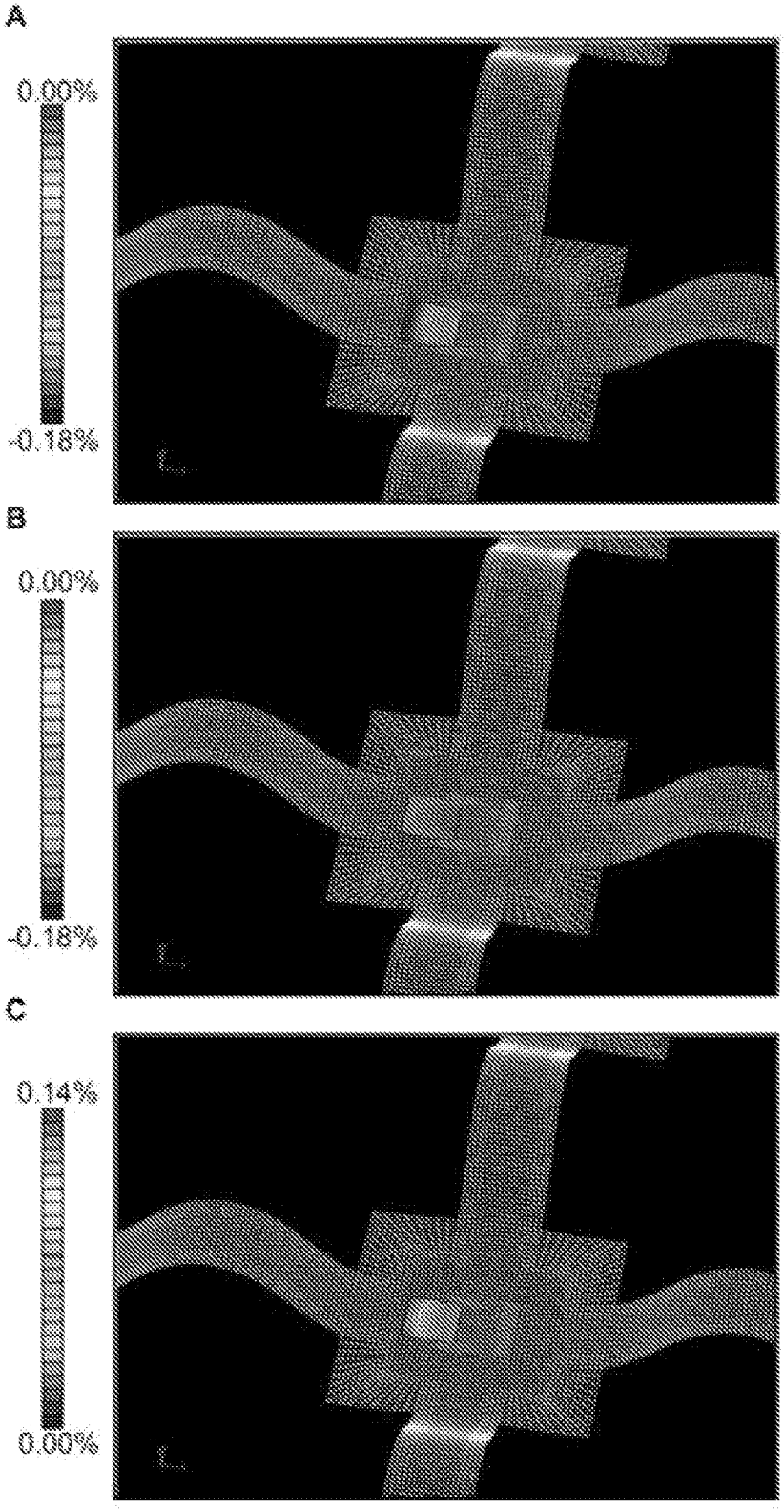


Figure 23

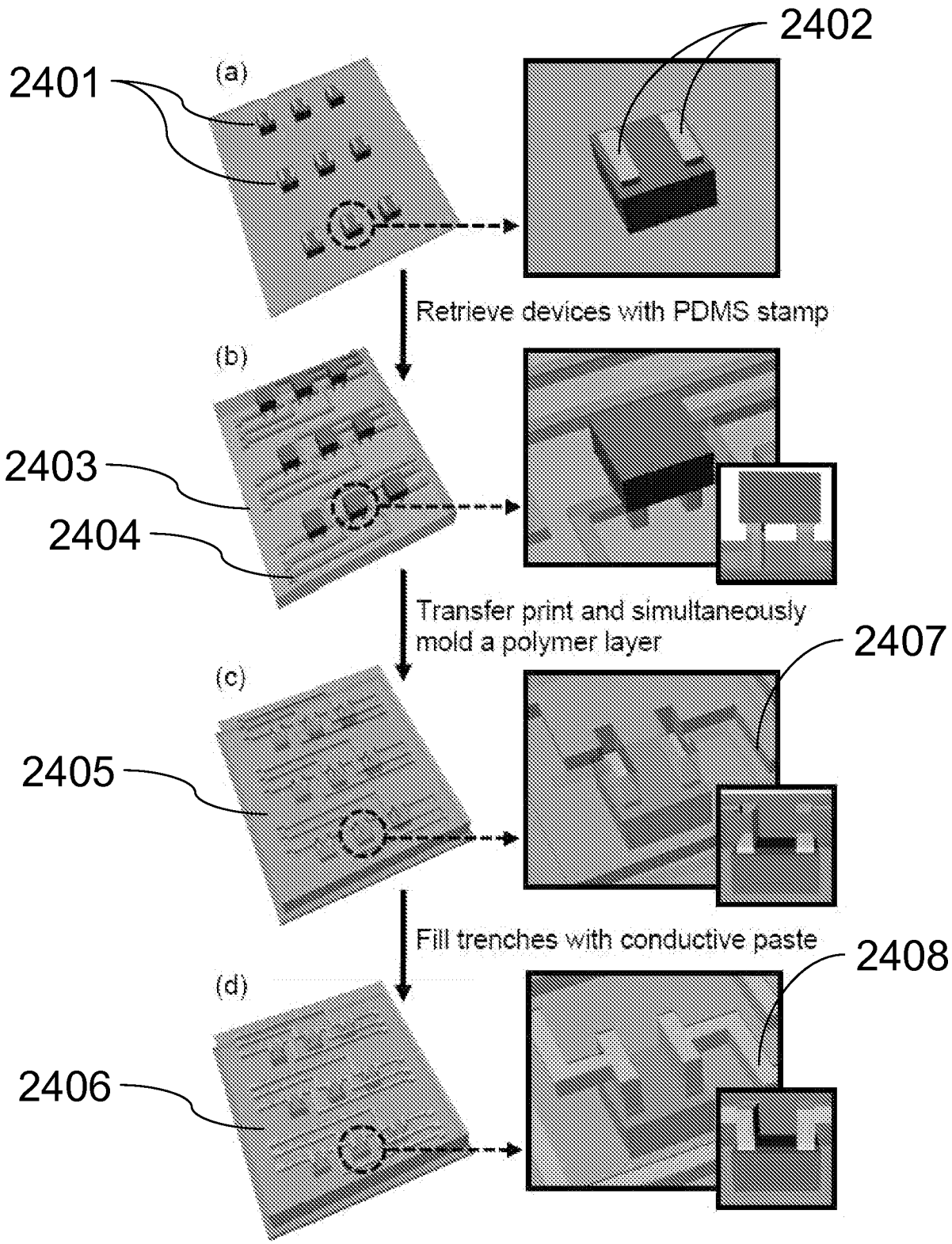

2401
(a)
2402
Retrieve devices with PDMS stamp
(b)
2403
2404
Transfer print and simultaneously mold a polymer layer
2407
(c)
2405
Fill trenches with conductive paste
2408
(d)
2406

Figure 24

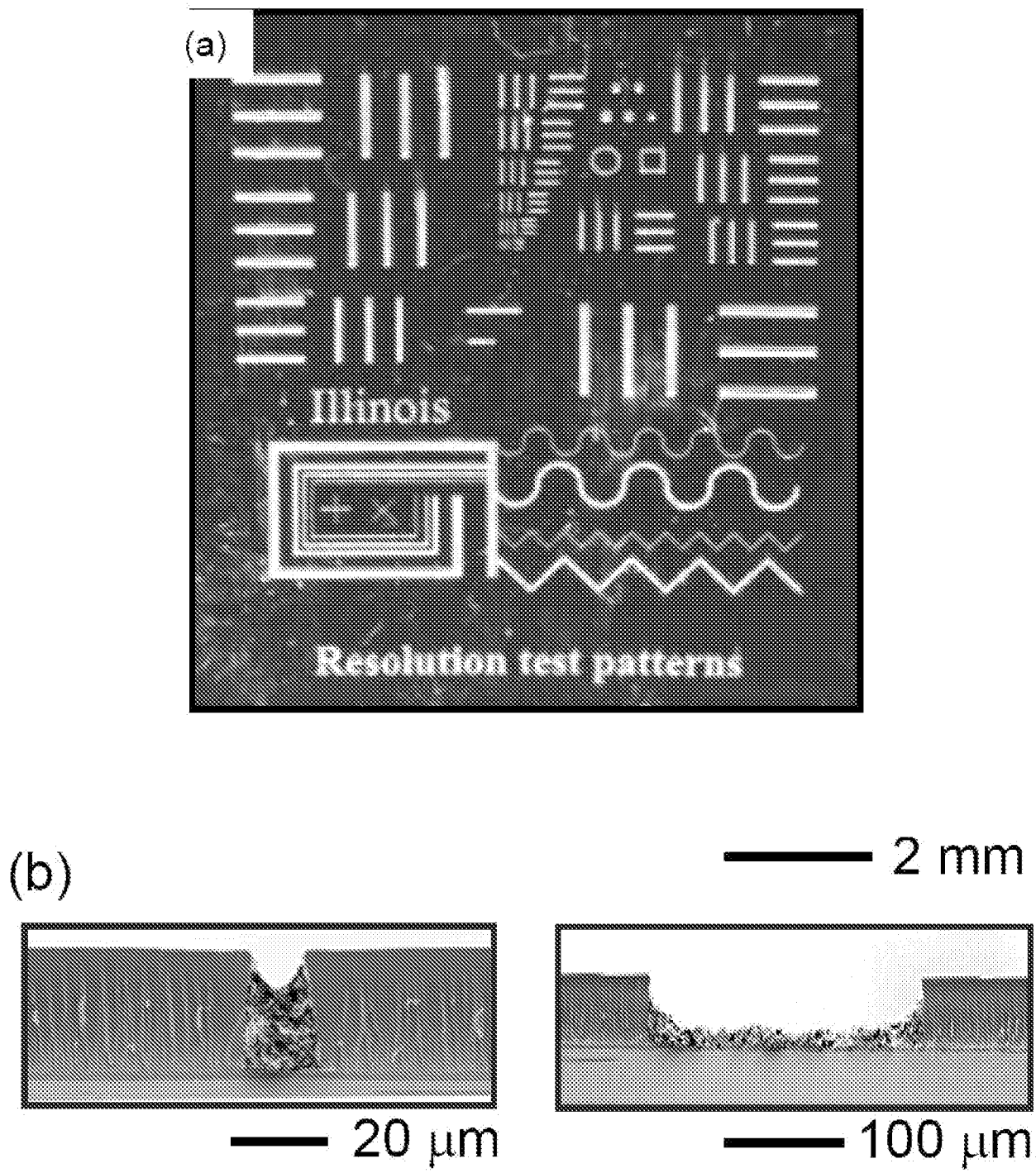


Figure 25

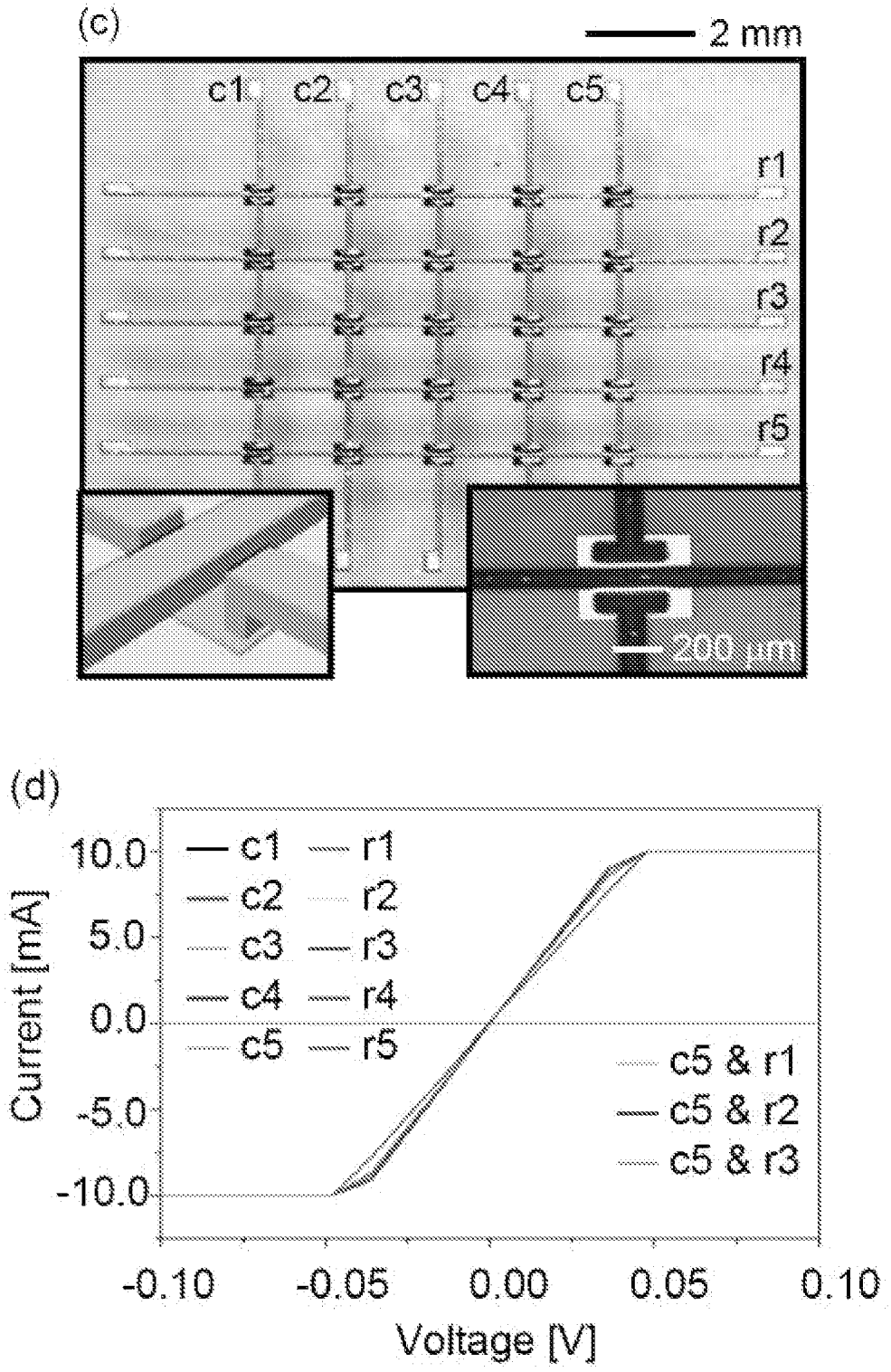


Figure 25 (cont'd)

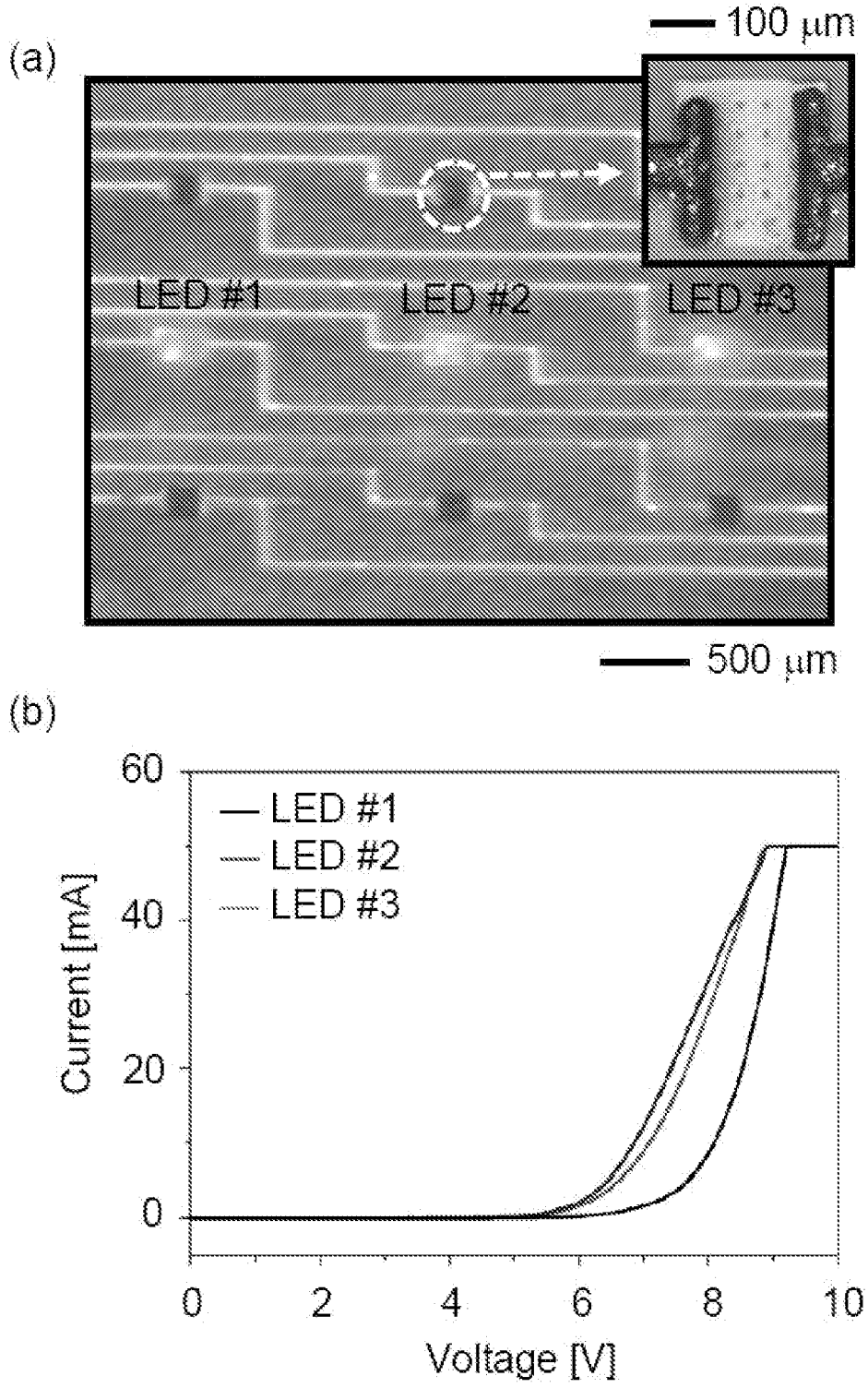

(a)
100 μm
LED #1
LED #2
LED #3
500 μm
(b)
60
40
20
0
Current [mA]
LED #1
LED #2
LED #3
0
2
4
6
8
10
Voltage [V]

Figure 26

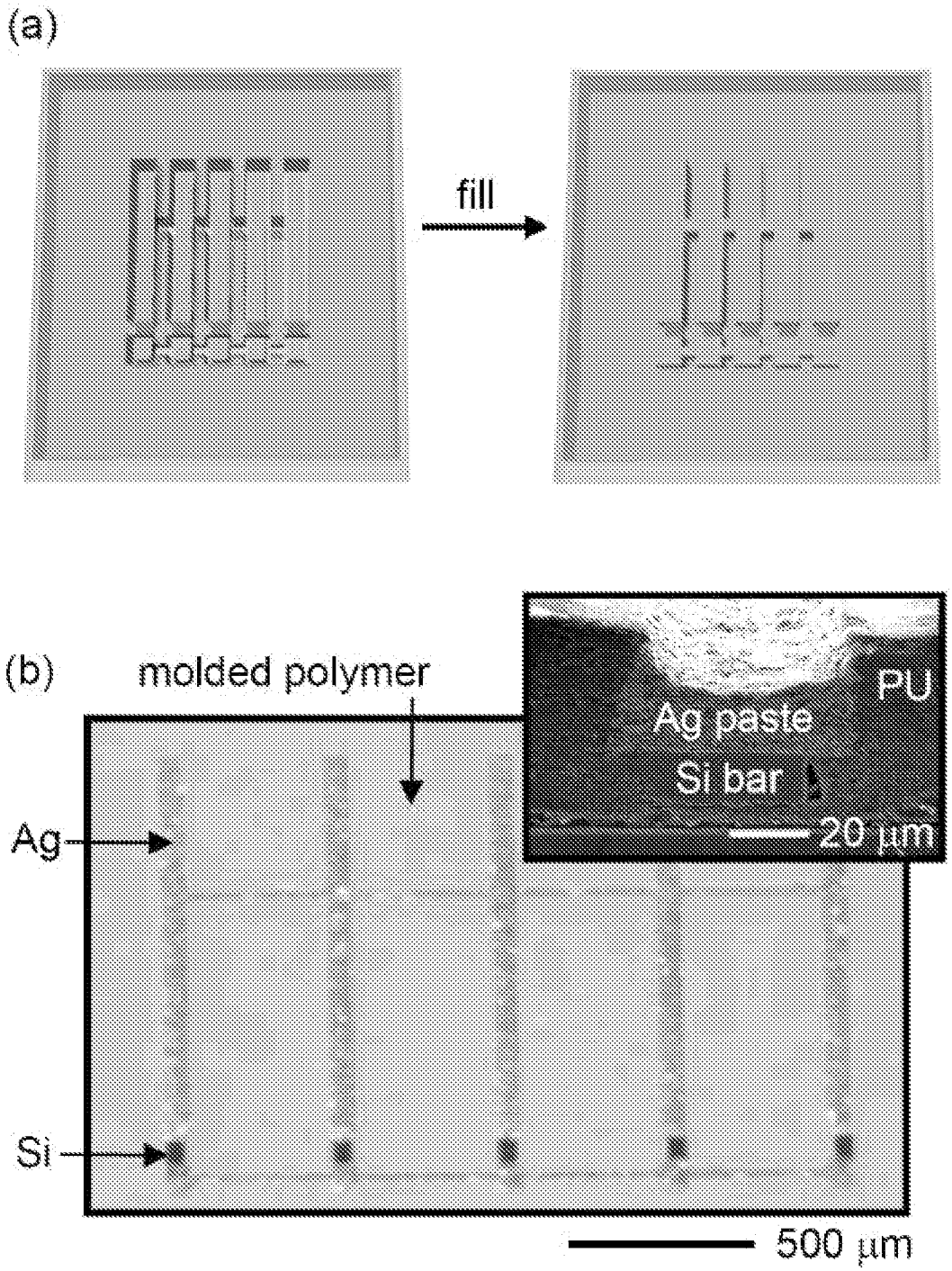


Figure 27

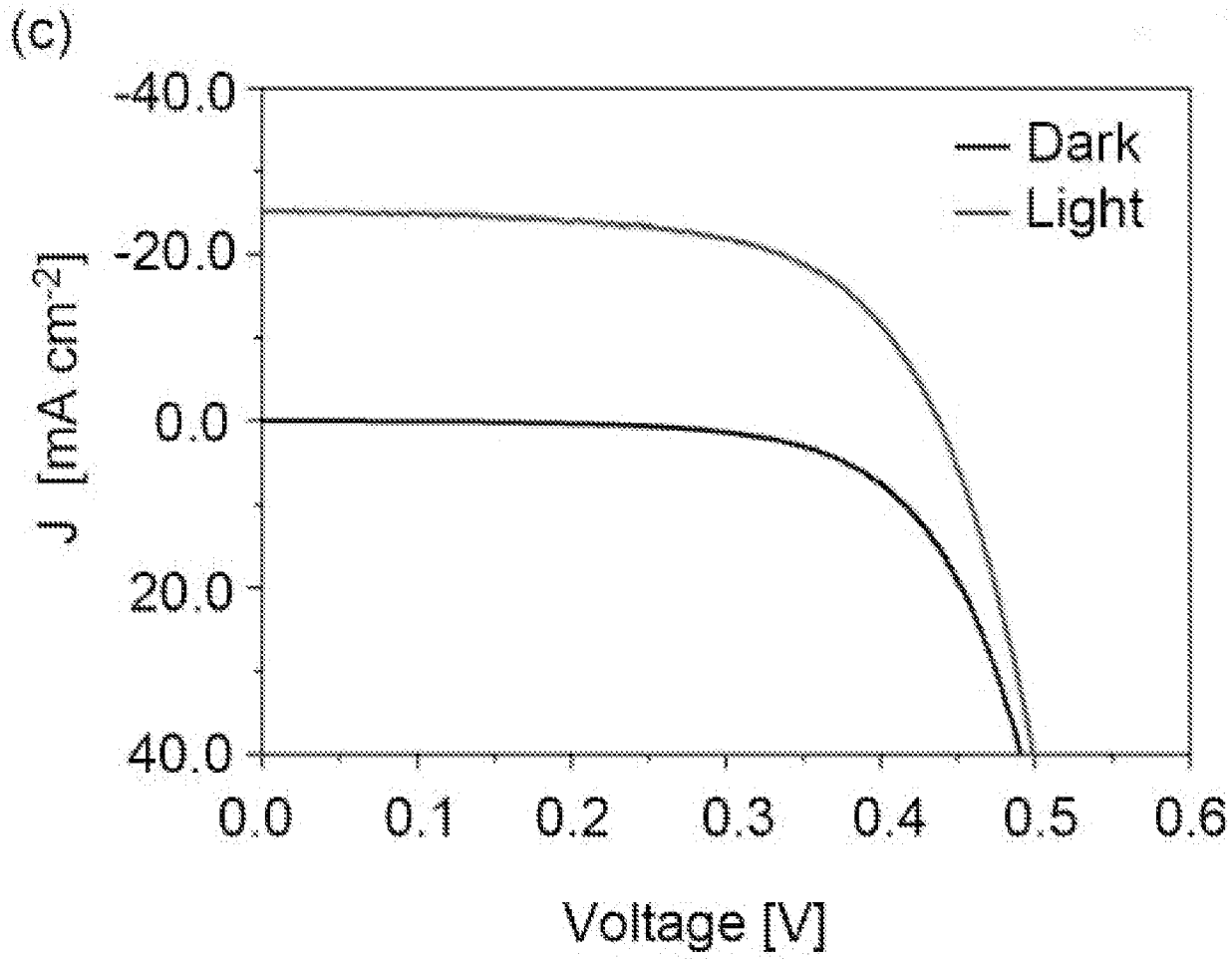


Figure 27 (cont'd)

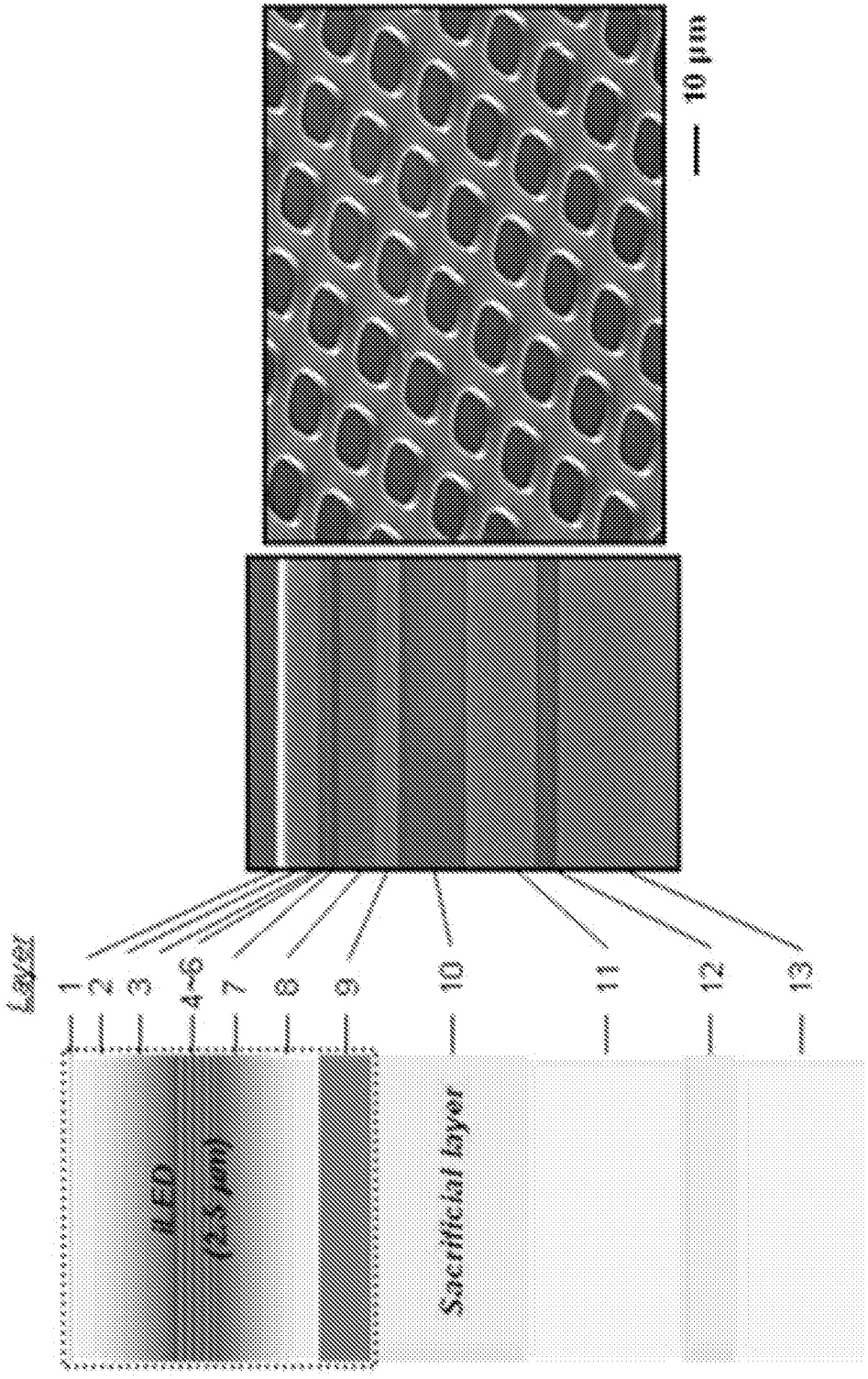

10 μm
Layer
1
2
3
4
5
6
7
8
9
10
11
12
13
ILED
(2.5 μm)
Sacrificial layer

Figure 28

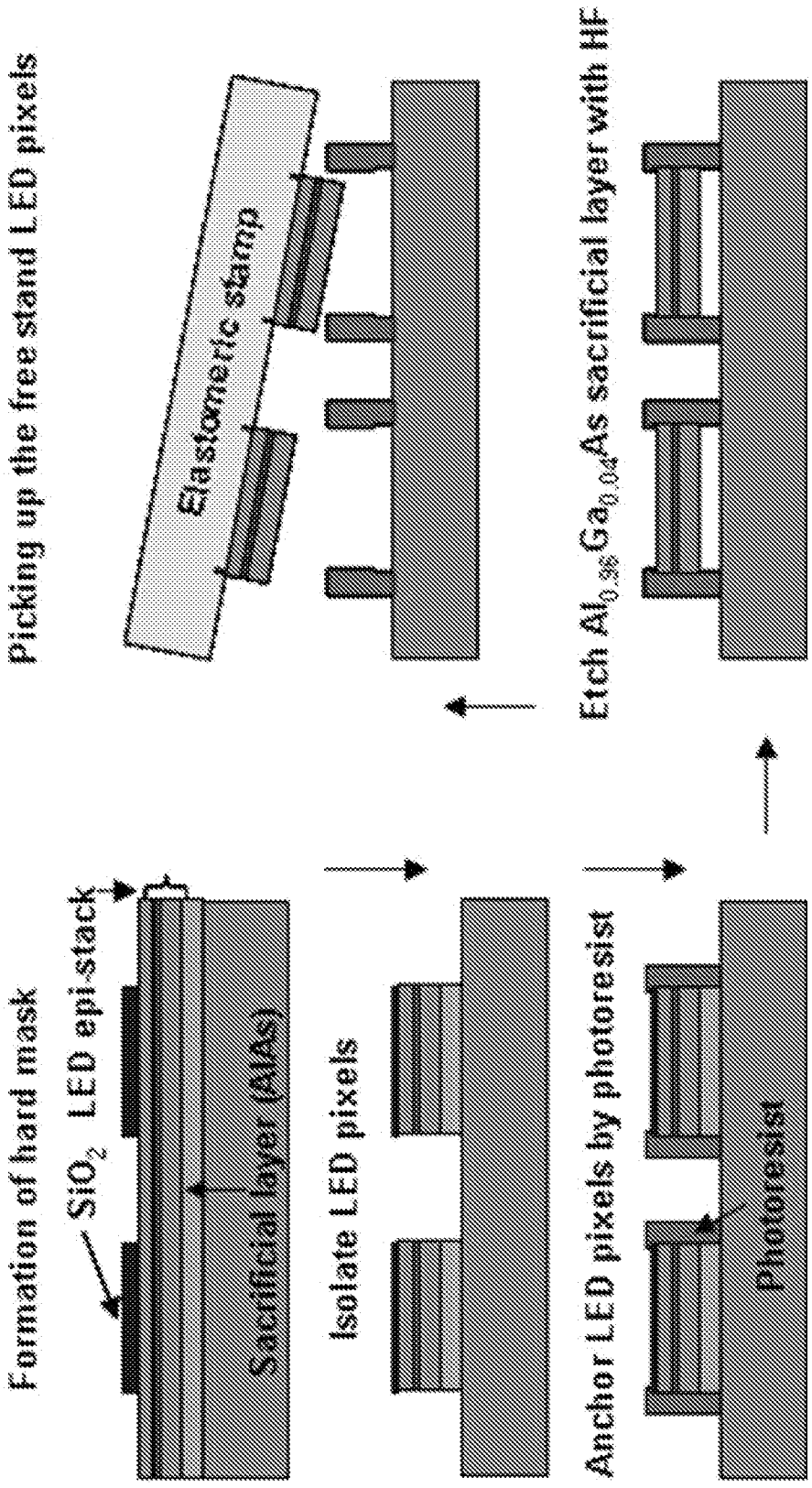

Formation of hard mask
SiO_2 LED epi-stack
Sacrificial layer (AlAs)
Isolate LED pixels
Anchor LED pixels by photoresist
Photoresist
Etch $Al_{0.96}Ga_{0.04}As$ sacrificial layer with HF
Picking up the free stand LED pixels
Elastomeric stamp

Figure 29

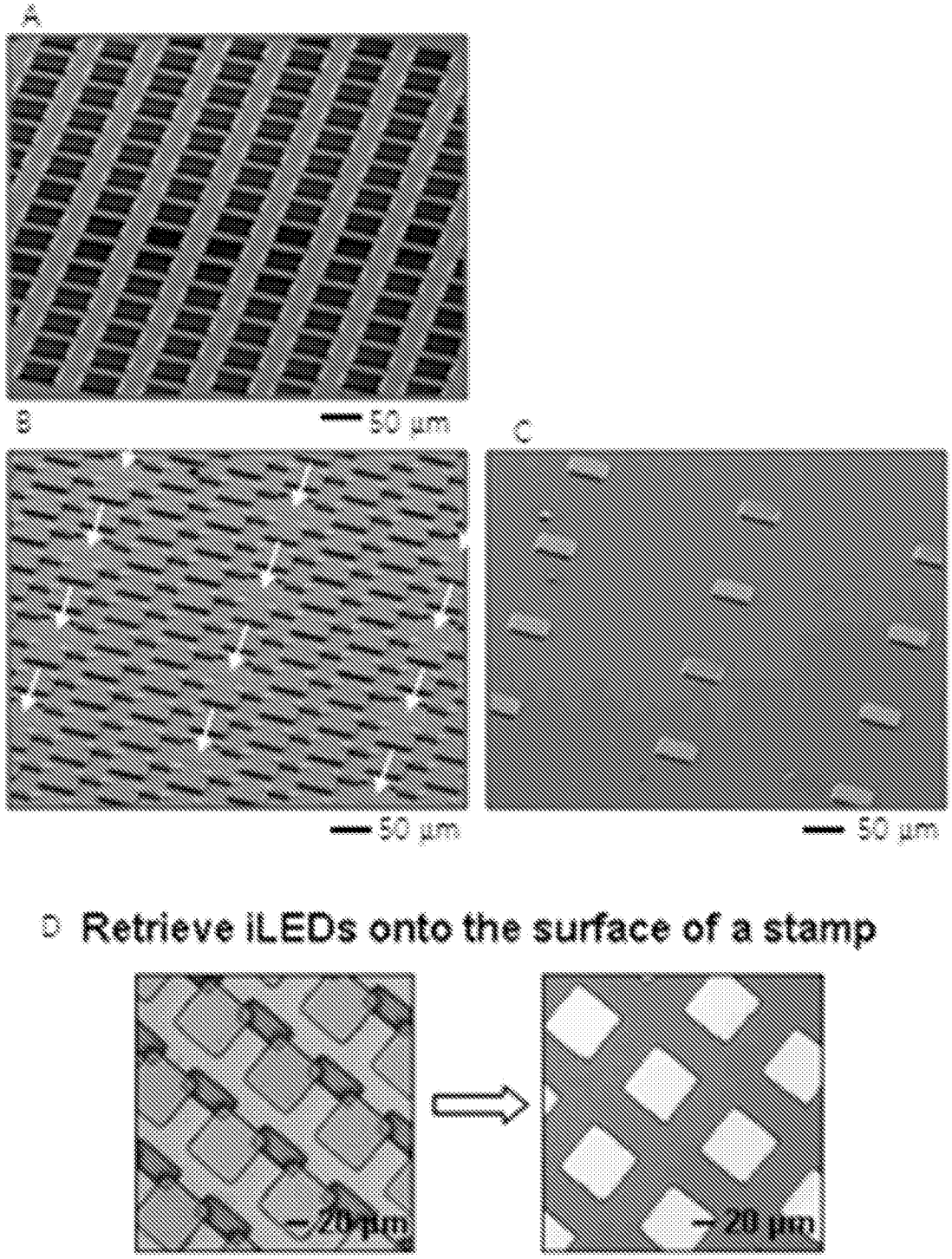

A
B
50 μm
C
50 μm
50 μm
D Retrieve iLEDs onto the surface of a stamp
~20μm
~20 μm

Figure 30

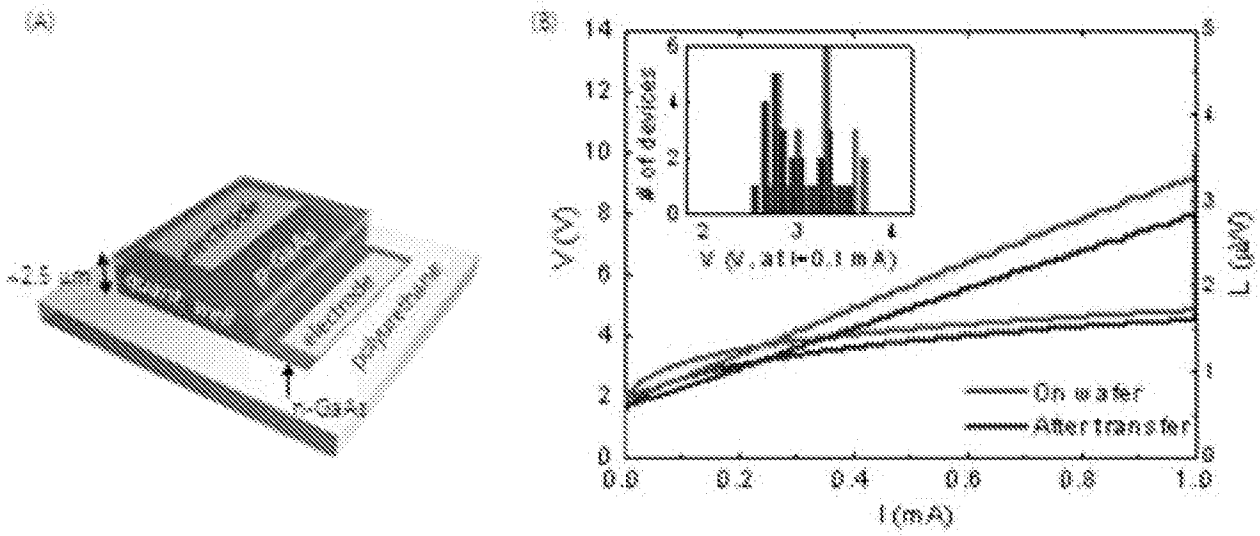


Figure 31

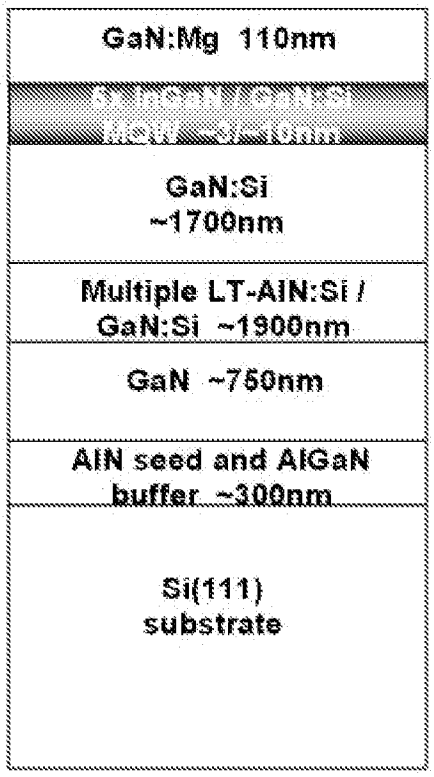


Figure 32

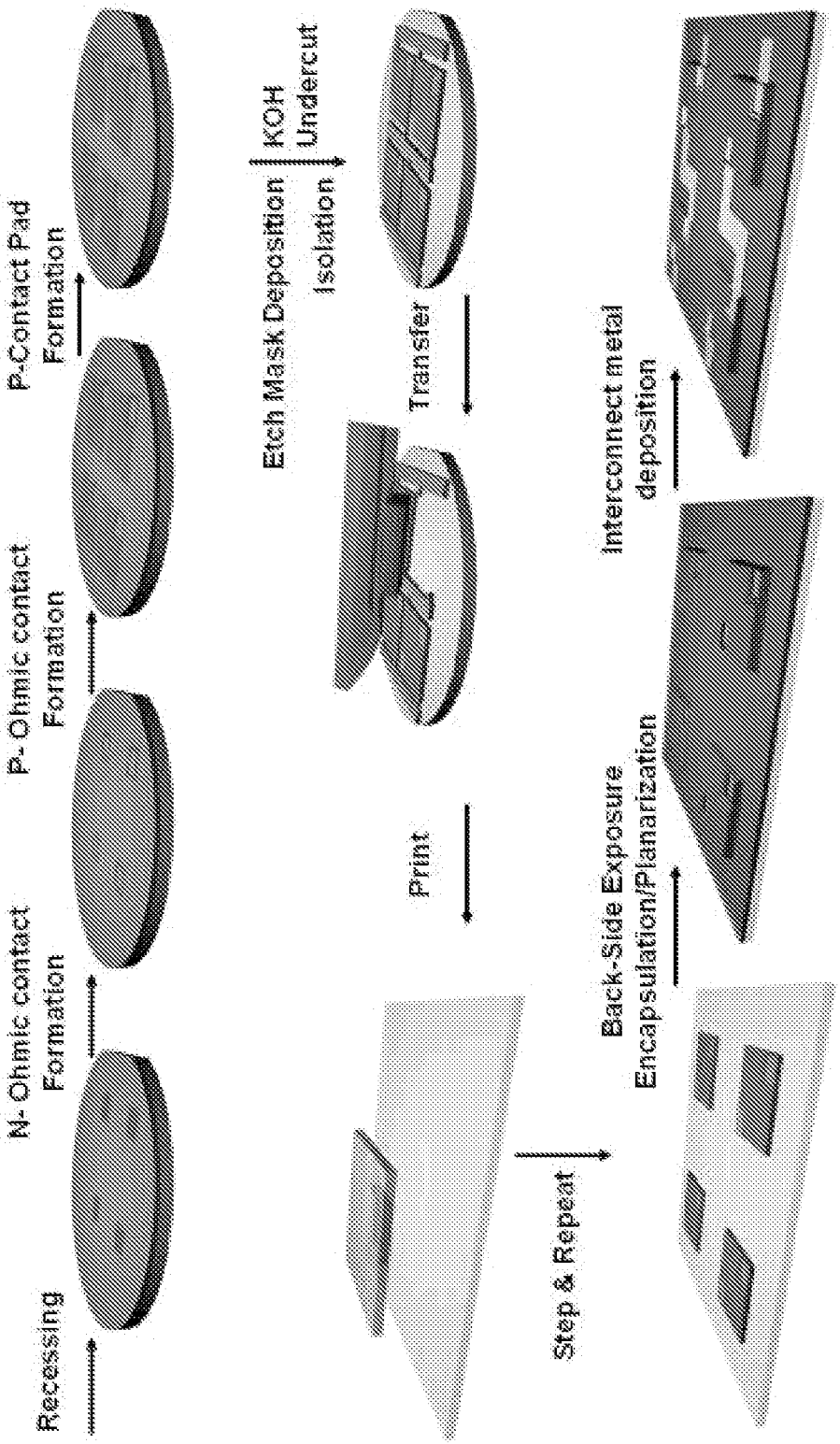

Recessing
N- Ohmic contact Formation
P- Ohmic contact Formation
P-Contact Pad Formation
Etch Mask Deposition
KOH Undercut
Isolation
Transfer
Print
Step & Repeat
Back-Side Exposure Encapsulation/Planarization
Interconnect metal deposition

Figure 33

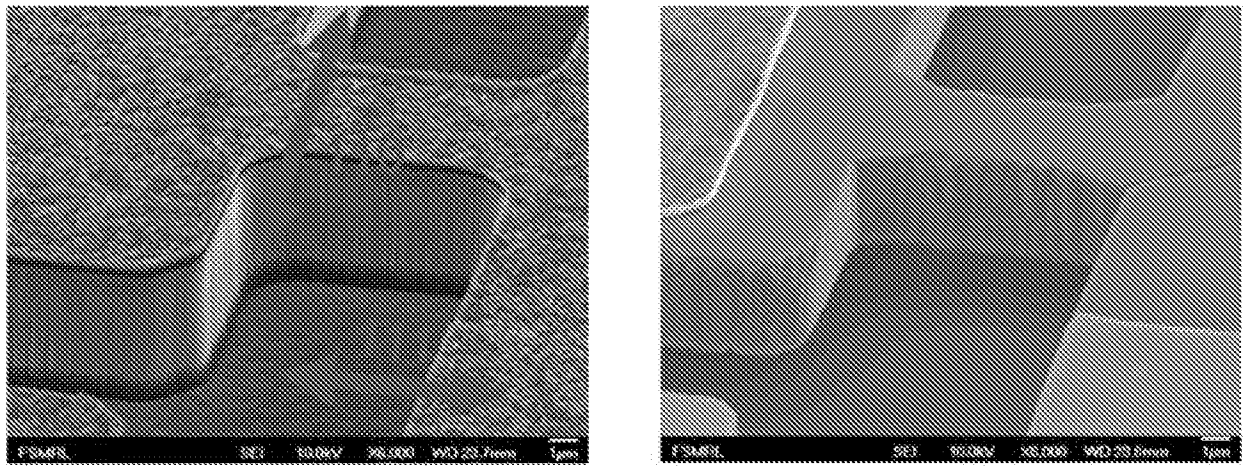


Figure 34

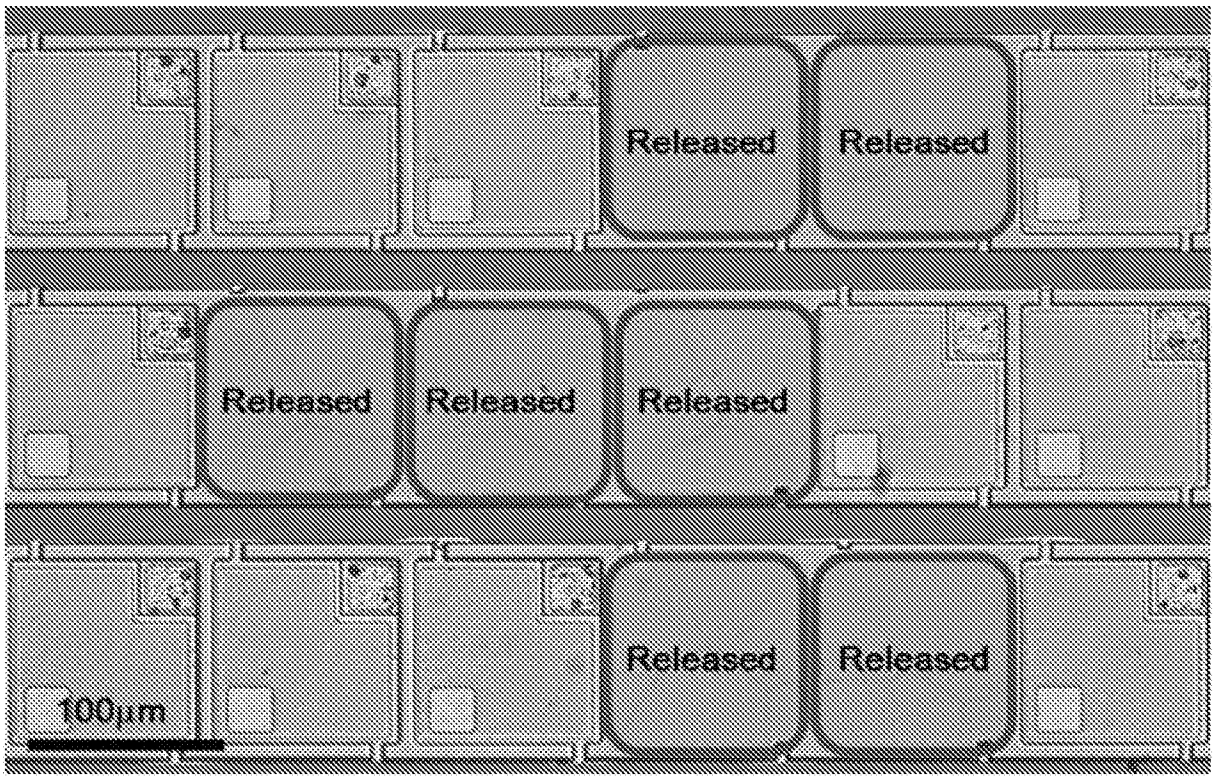


Figure 35

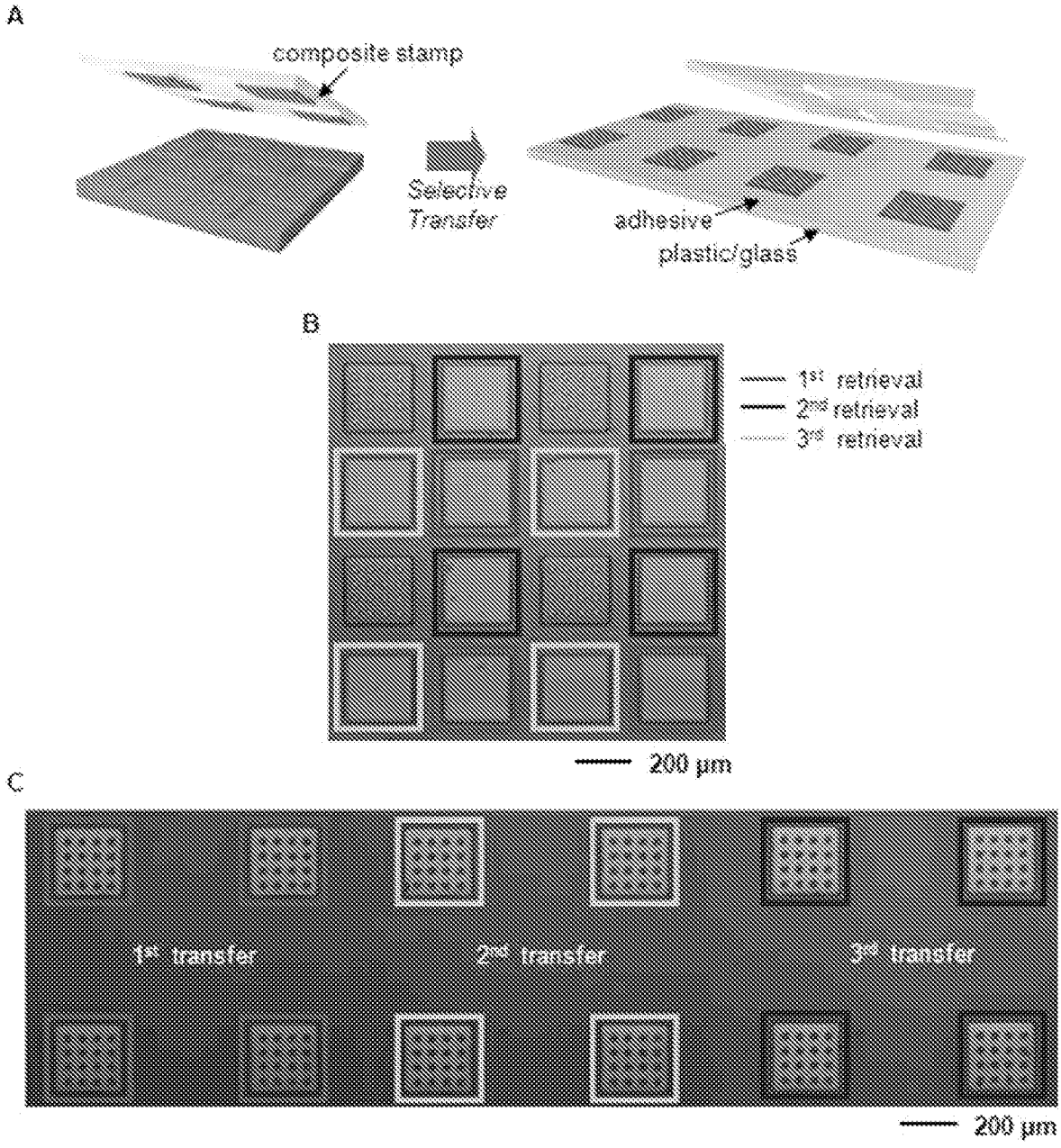
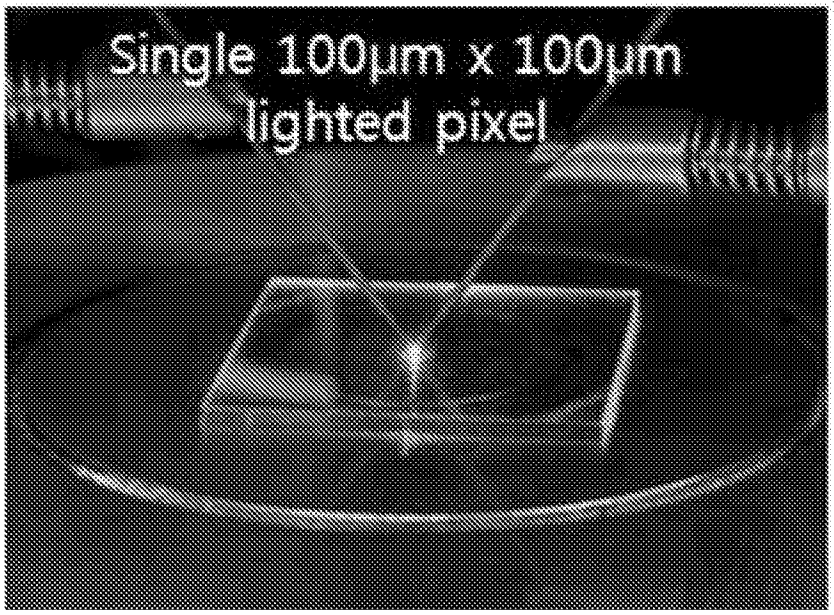

A
composite stamp
Selective Transfer
adhesive
plastic/glass
B
1st retrieval
2nd retrieval
3rd retrieval
200 μm
C
1st transfer
2nd transfer
3rd transfer
200 μm

Figure 36

(a)


Single 100µm x 100µm
lighted pixel

(b)

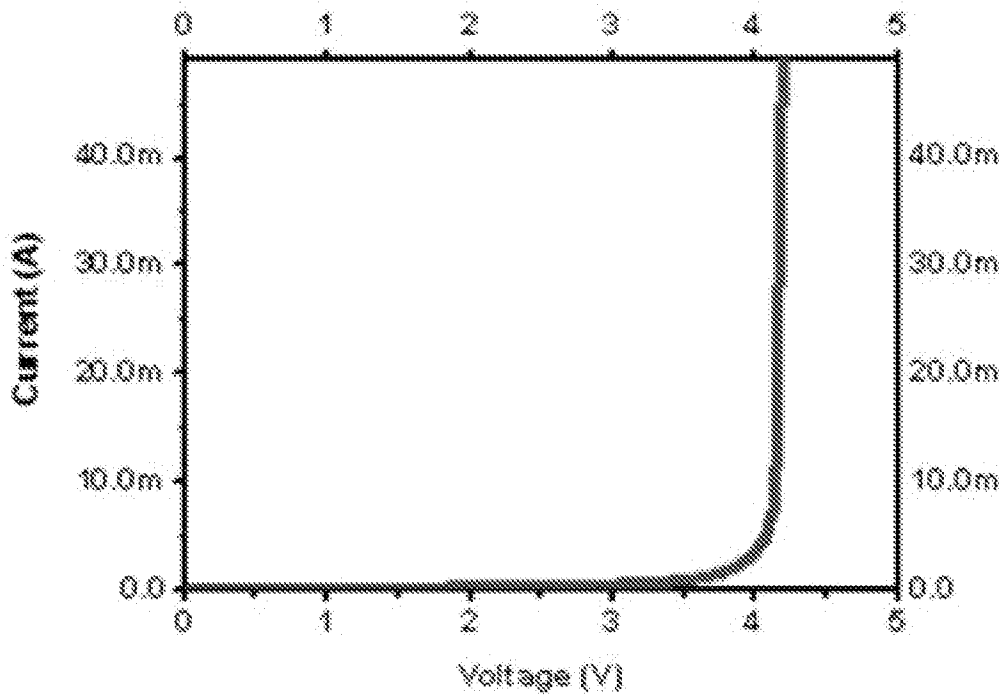

0
1
2
3
4
5
40.0m
30.0m
20.0m
10.0m
0.0
Current (A)
Voltage (V)

Figure 37

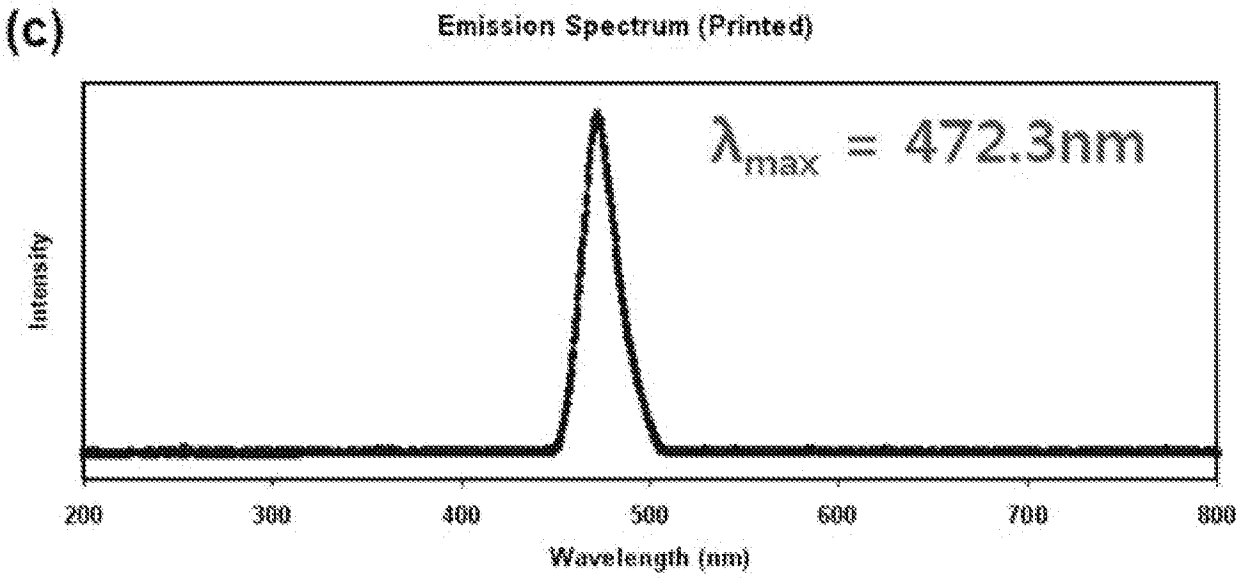


Figure 37 (cont'd)

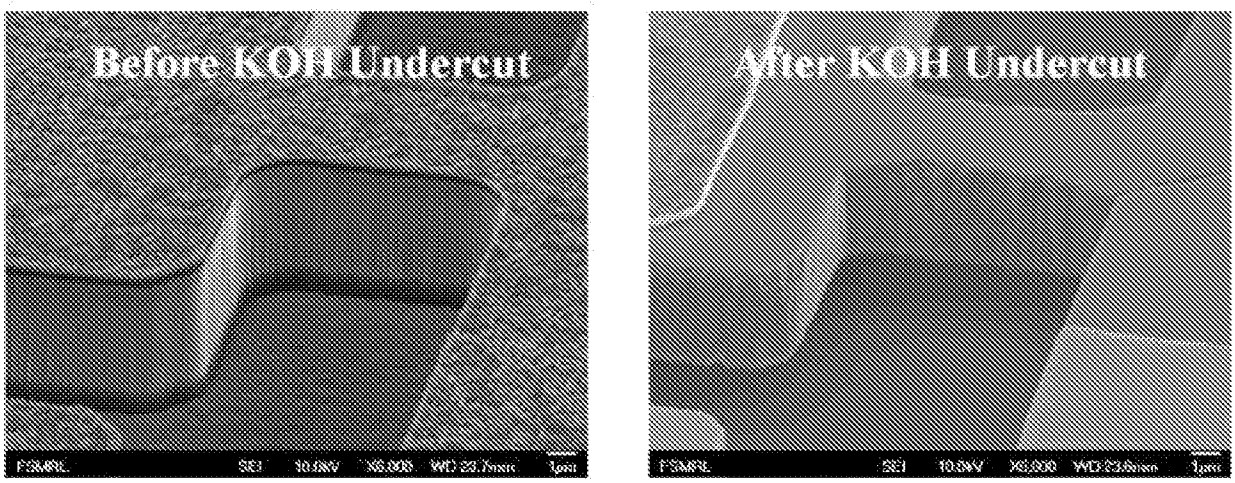


Figure 38

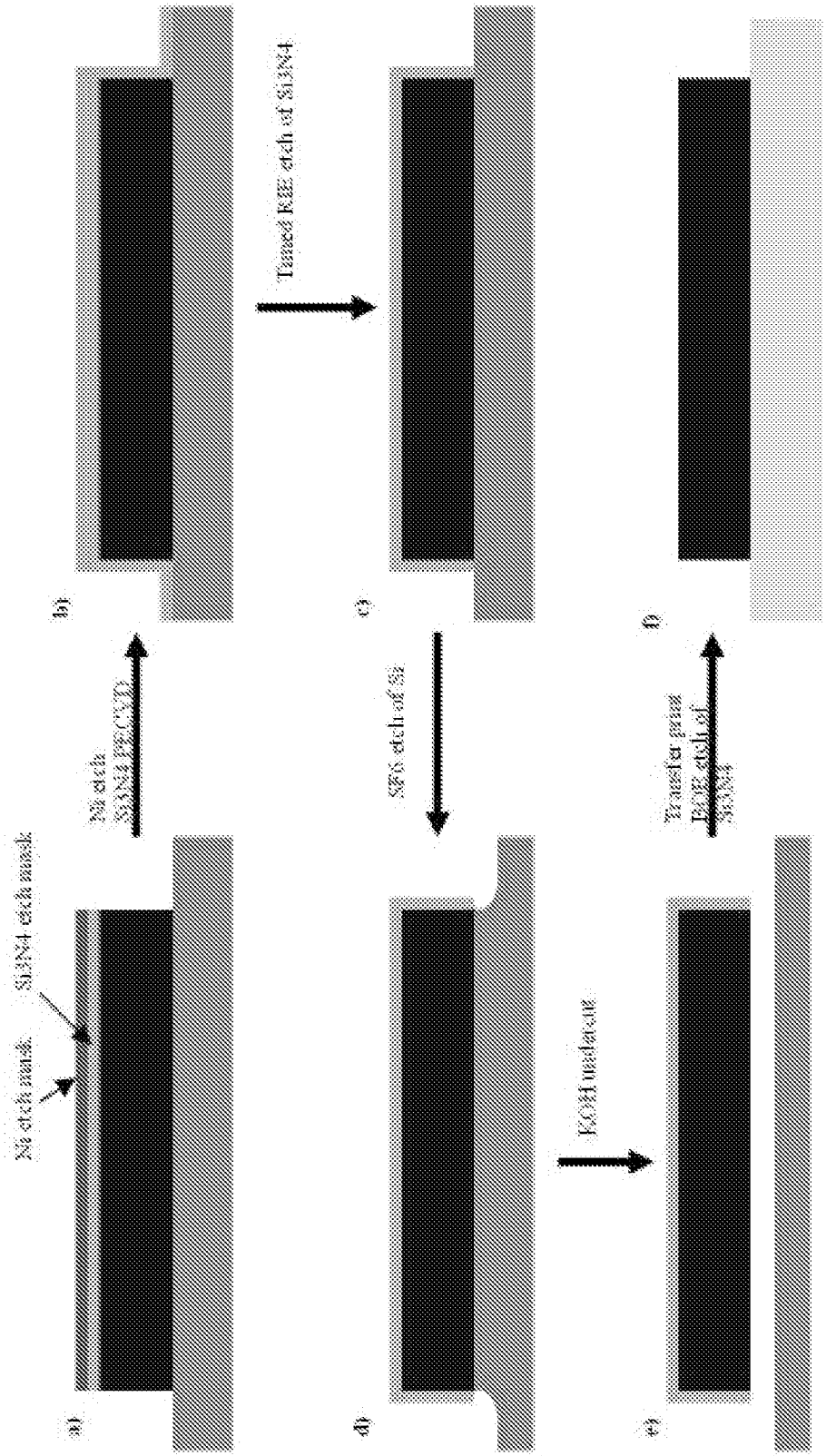

Si etch mask
Si3N4 etch mask
a)
Si etch
Si3N4 RIE/CHF3
b)
Timed RIE etch of Si3N4
c)
SF6 etch of Si
d)
KOH undercut
e)
Transfer print
RIE etch of
Si3N4
f)

Figure 39

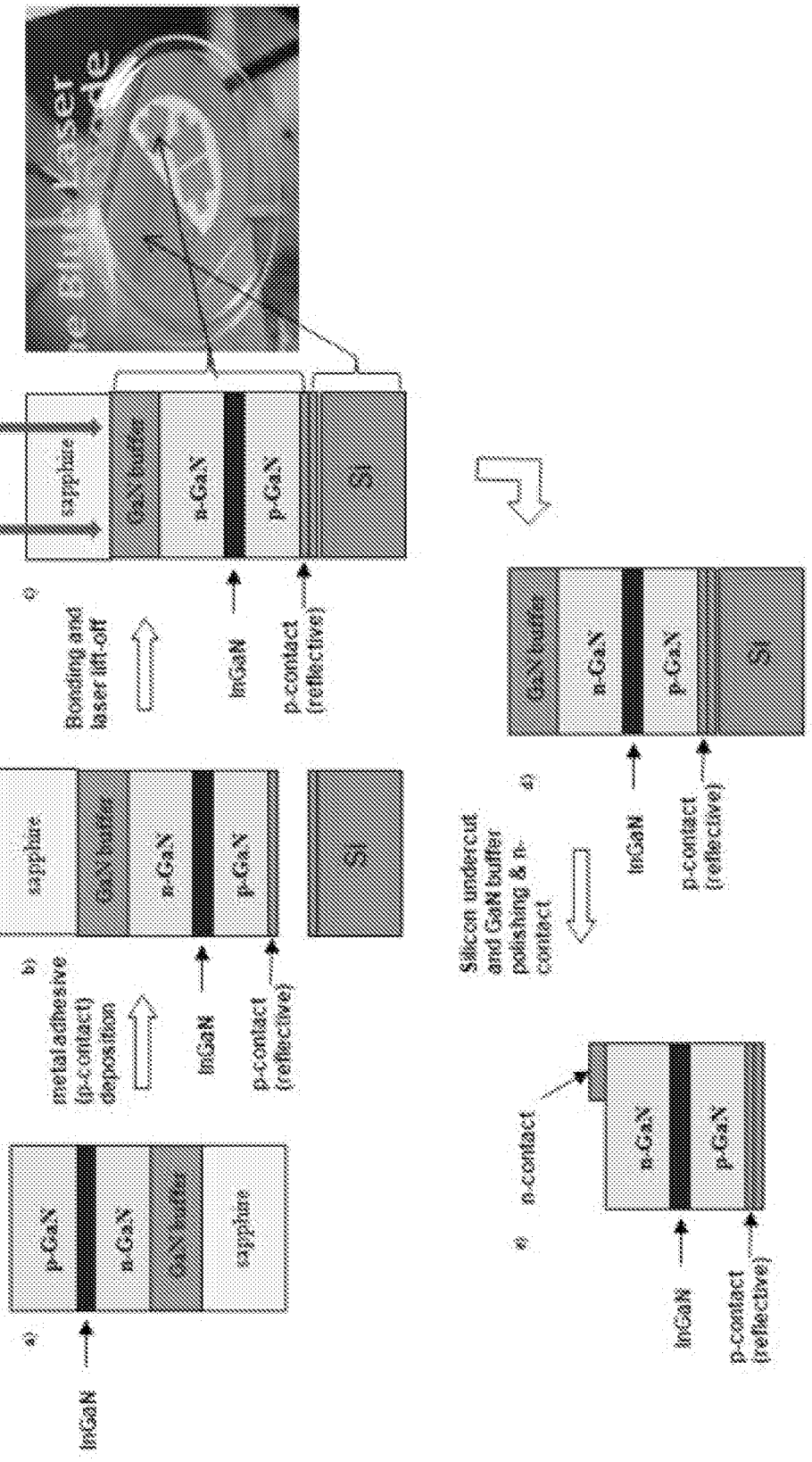

a)
InGaN
p-GaN
n-GaN
GaN buffer
sapphire
b)
metal adhesive (p-contact) deposition
InGaN
p-contact (reflective)
Si
c)
Laser
sapphire
Bonding and laser lift-off
InGaN
p-contact (reflective)
Silicon undercut and GaN buffer polishing & n-contact
d)
GaN buffer
n-GaN
p-GaN
Si
InGaN
p-contact (reflective)
e)
n-contact
n-GaN
p-GaN
InGaN
p-contact (reflective)

Figure 40

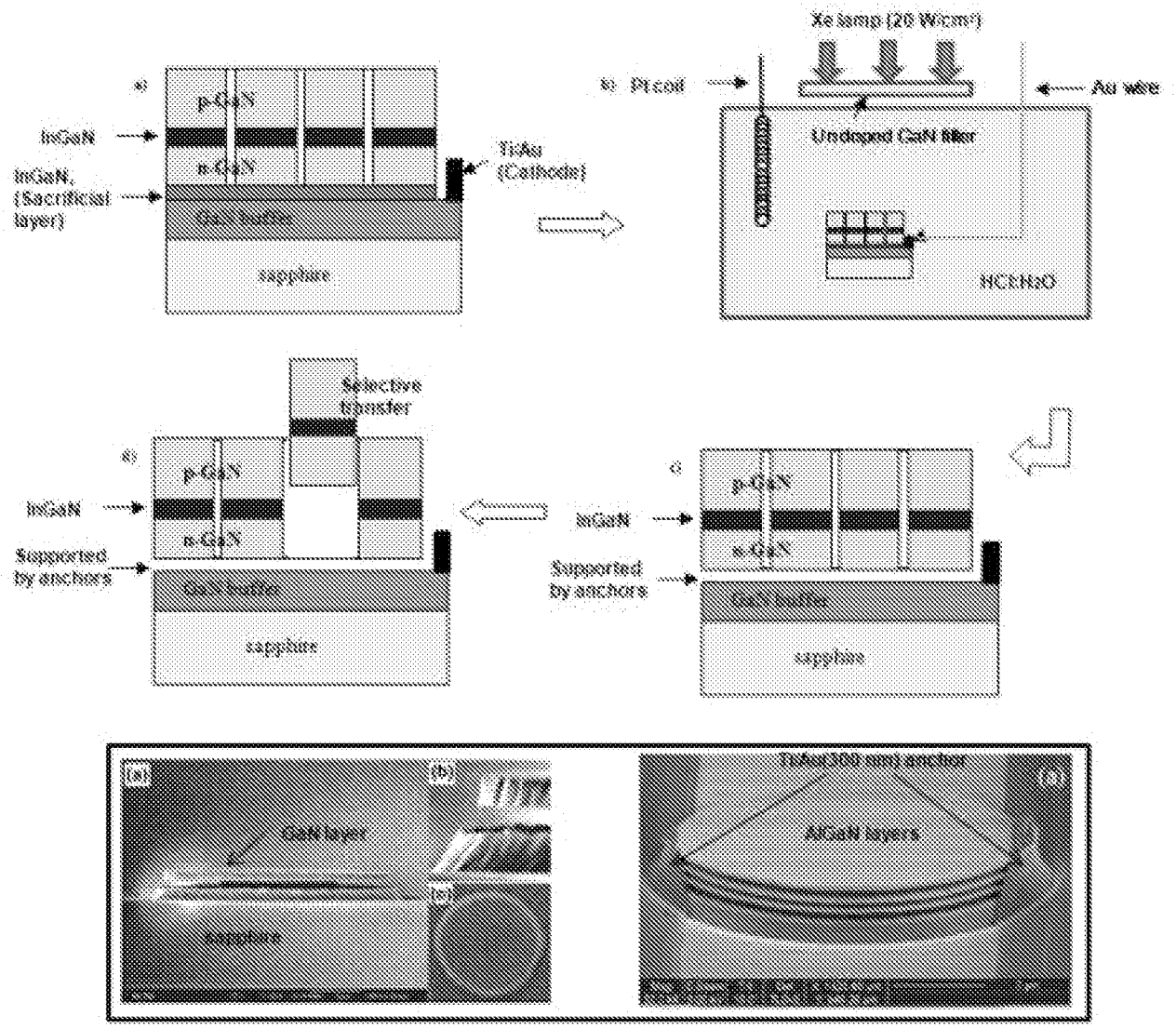

Xe lamp (20 W/cm²)
Pt coil
Au wire
Undoped GaN filler
HCl:H2O
p-GaN
InGaN
n-GaN
InGaN, (Sacrificial layer)
Ti/Au (Cathode)
GaN buffer
sapphire
Selective transfer
Supported by anchors
GaN layer
Ti/Au(300 nm) anchor
AlGaN layers

Figure 41

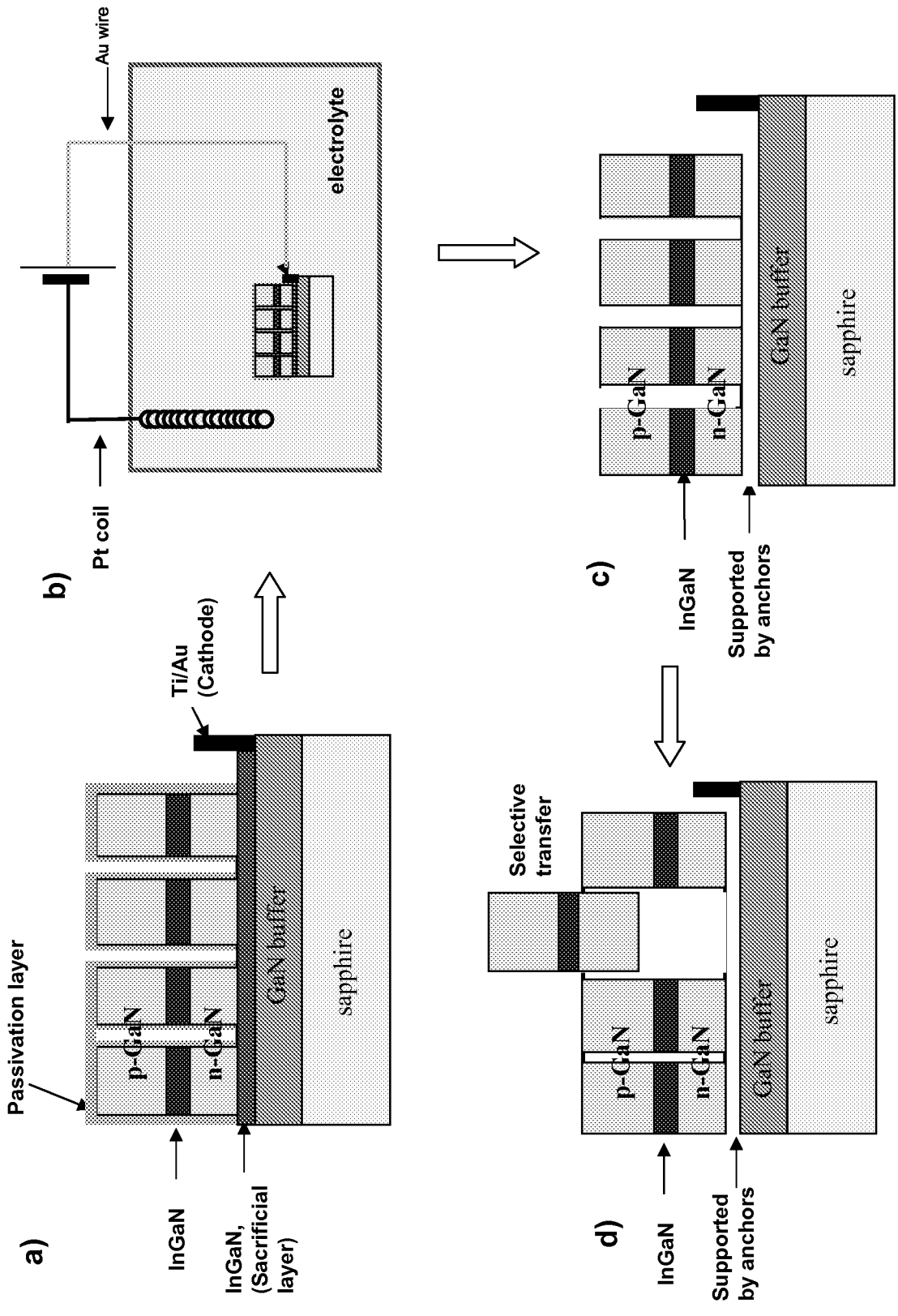

a)
Passivation layer
p-GaN
n-GaN
GaN buffer
sapphire
InGaN
InGaN, (Sacrificial layer)
Ti/Au (Cathode)
b)
Au wire
electrolyte
Pt coil
c)
p-GaN
n-GaN
GaN buffer
sapphire
InGaN
Supported by anchors
d)
Selective transfer
p-GaN
n-GaN
GaN buffer
sapphire
InGaN
Supported by anchors

Figure 42

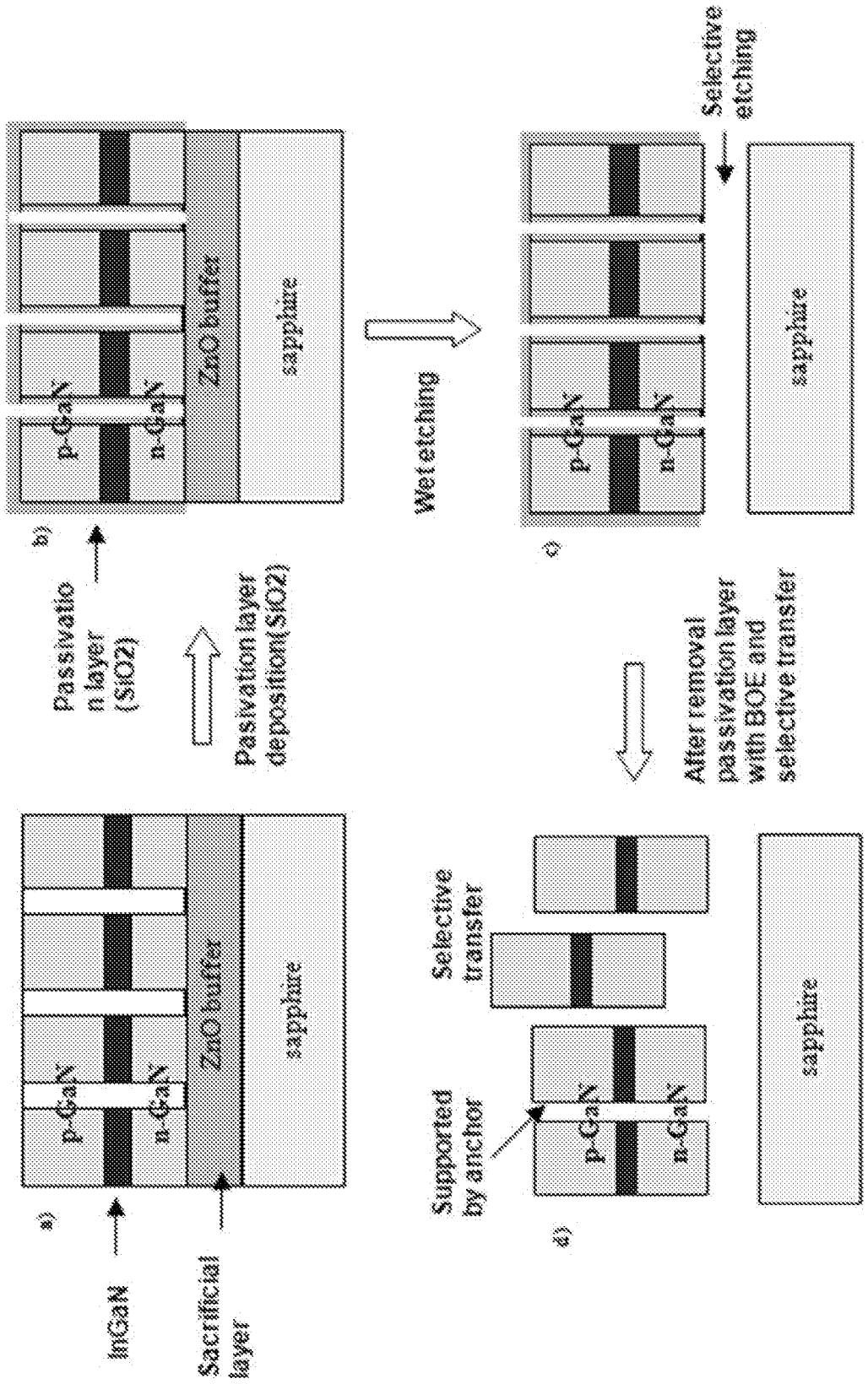

a)
InGaN
Sacrificial layer
p-GaN
n-GaN
ZnO buffer
sapphire
Passivation layer deposition(SiO2)
b)
Passivation layer (SiO2)
Wet etching
c)
Selective etching
After removal passivation layer with BOE and selective transfer
d)
Supported by anchor
Selective transfer

Figure 43

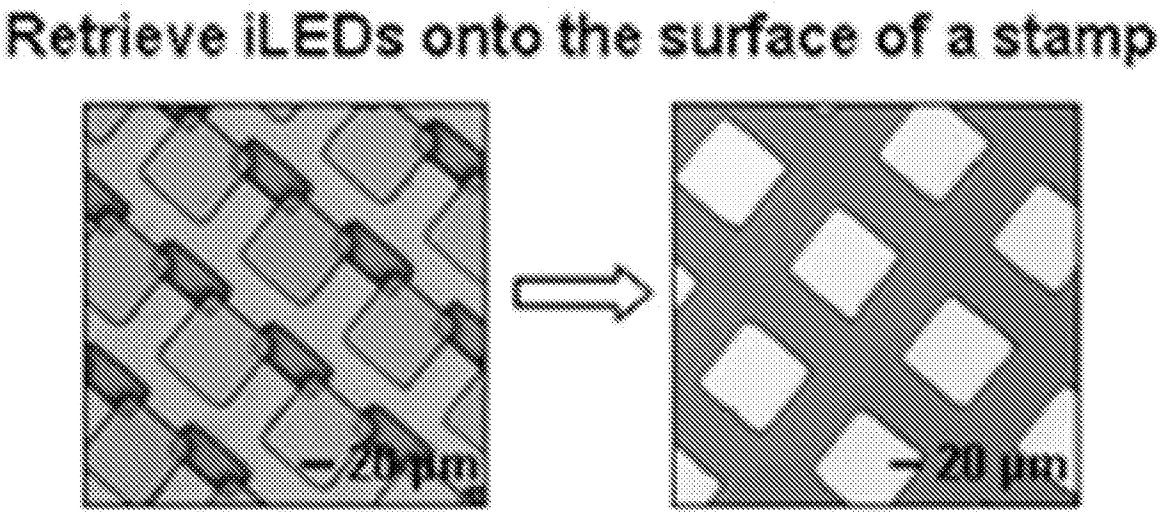


Figure 44

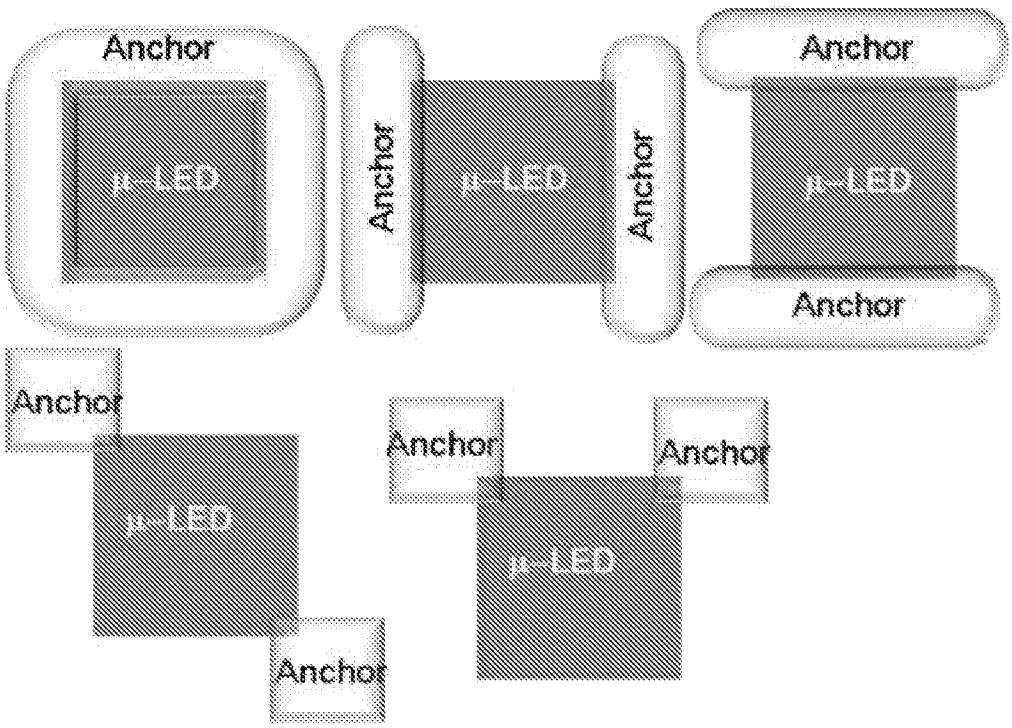


Figure 45

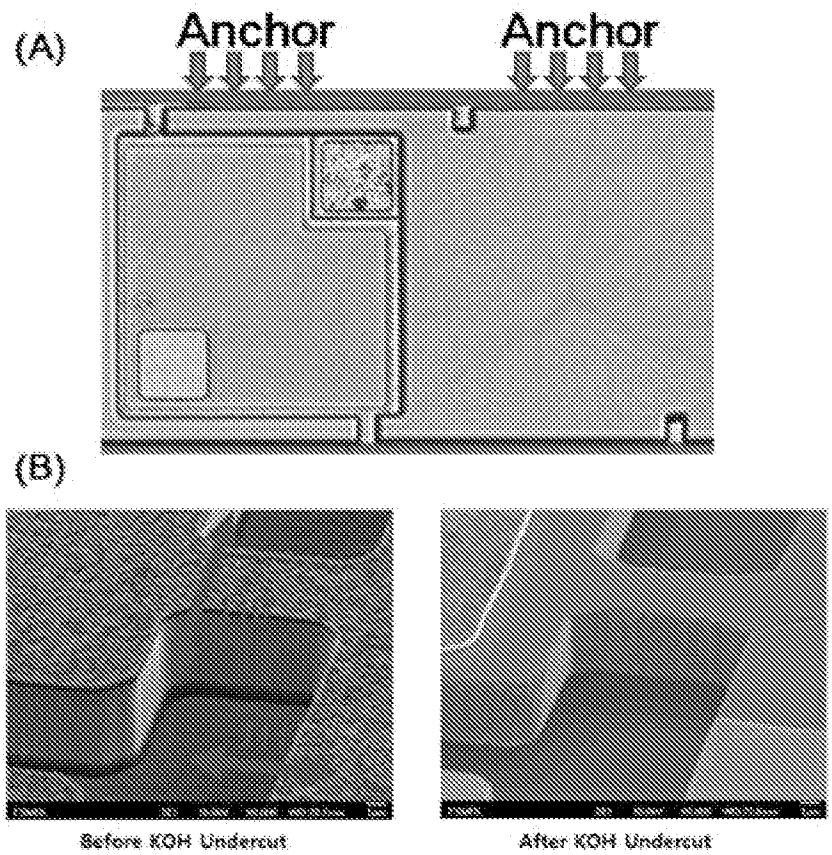


Figure 46

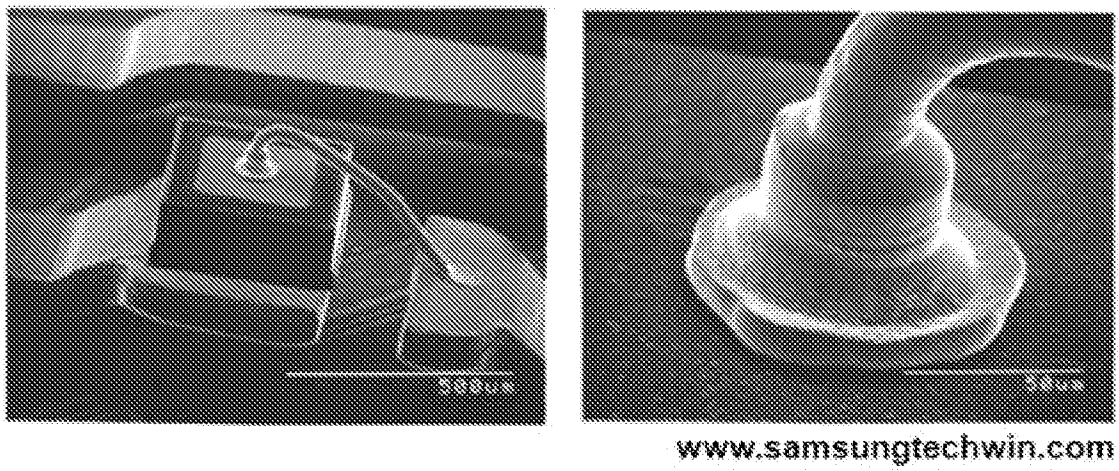


Figure 47

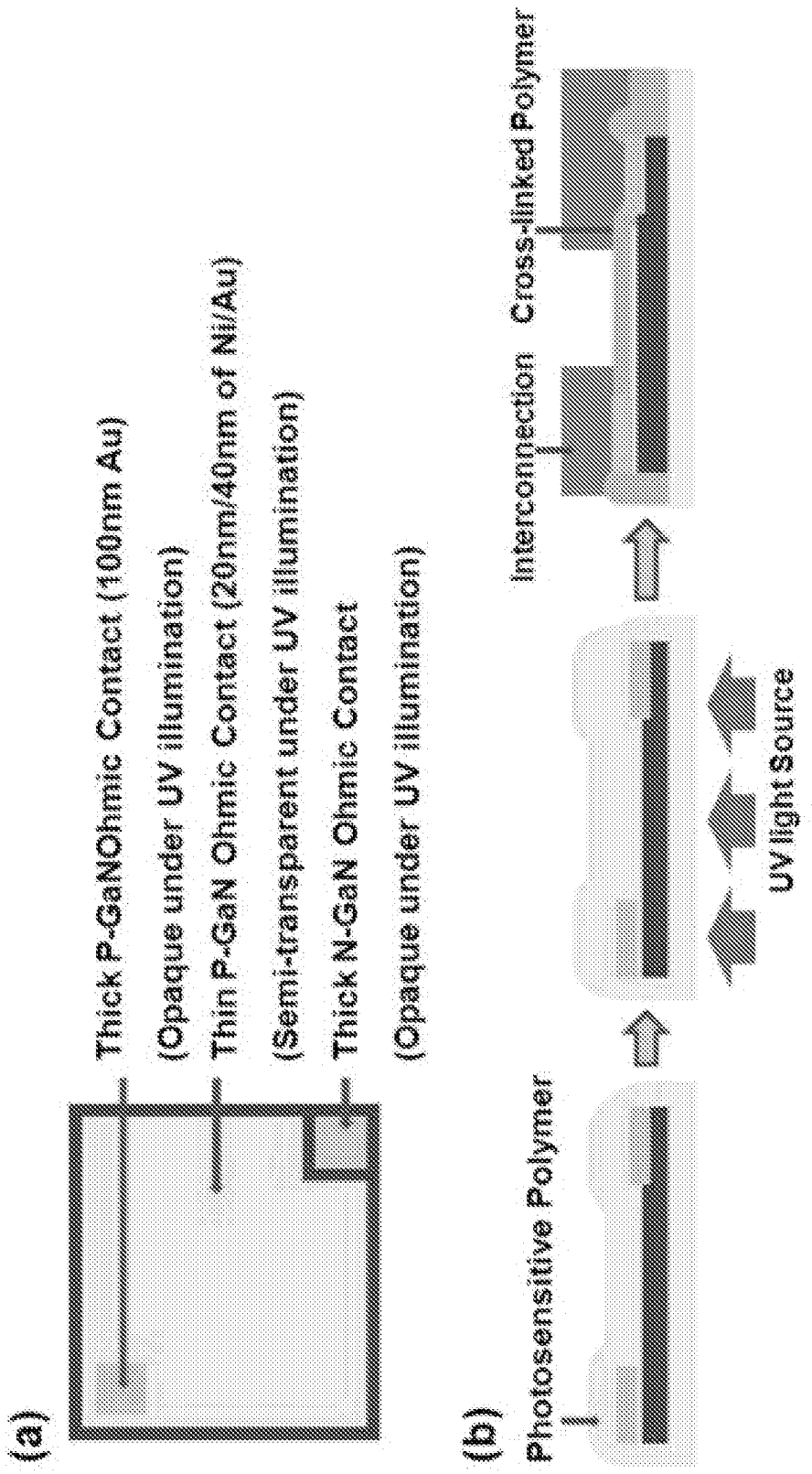

(a)
Thick P-GaNOhmic Contact (100nm Au)
(Opaque under UV illumination)
Thin P-GaN Ohmic Contact (20nm/40nm of Ni/Au)
(Semi-transparent under UV illumination)
Thick N-GaN Ohmic Contact
(Opaque under UV illumination)
(b)
Photosensitive Polymer
Interconnection
Cross-linked Polymer
UV light Source

Figure 48

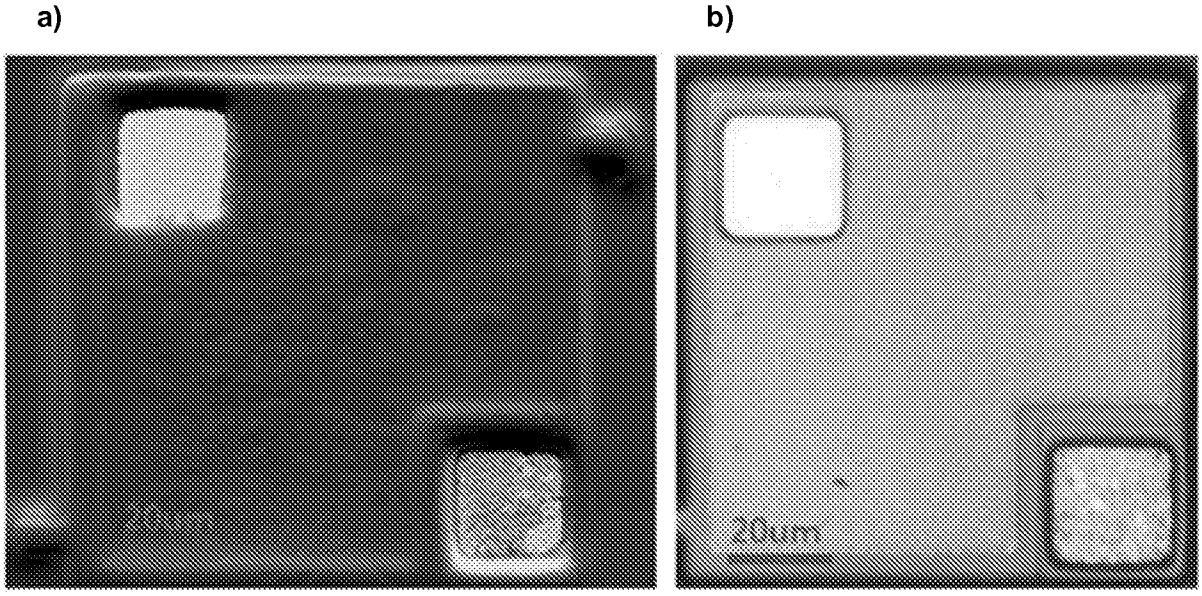


Figure 49

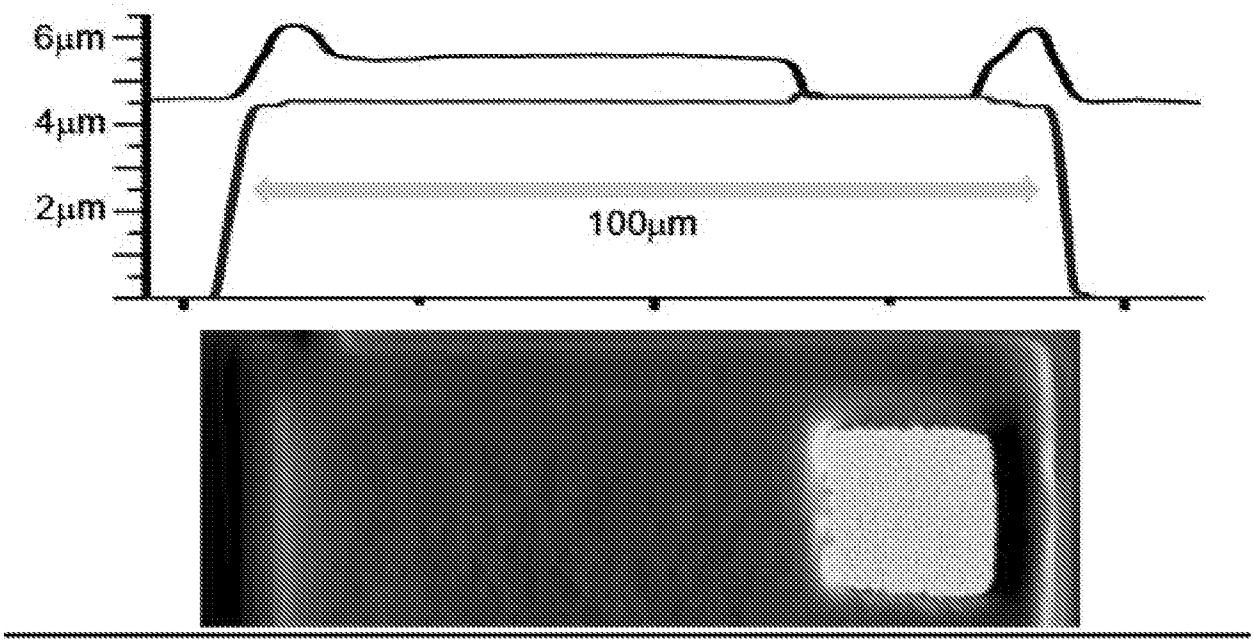


Figure 50

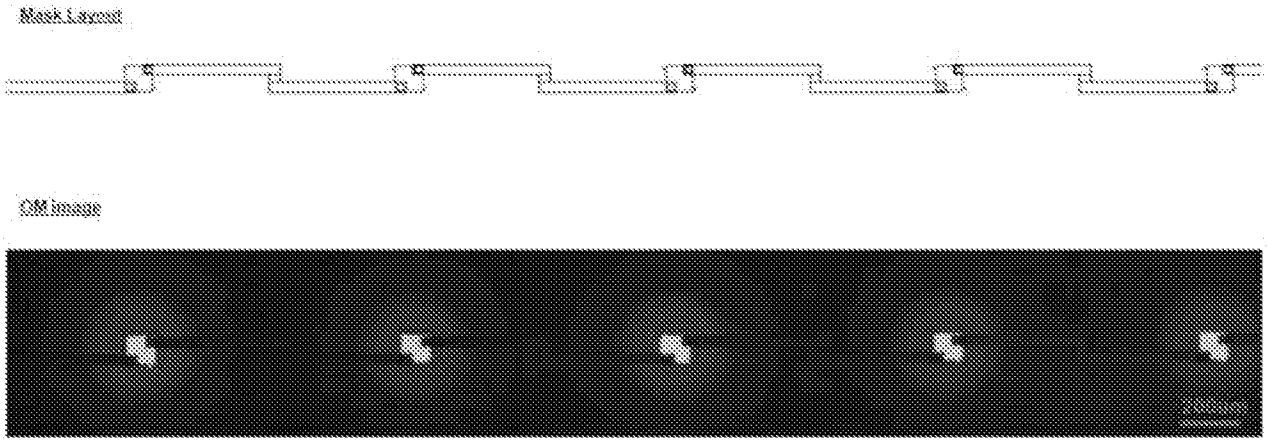


Figure 51

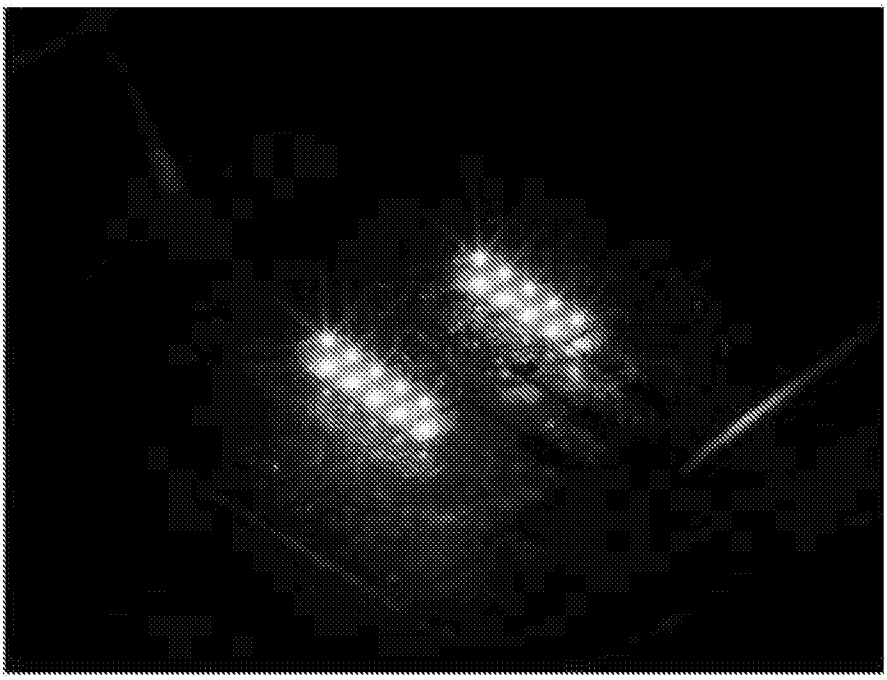


Figure 52

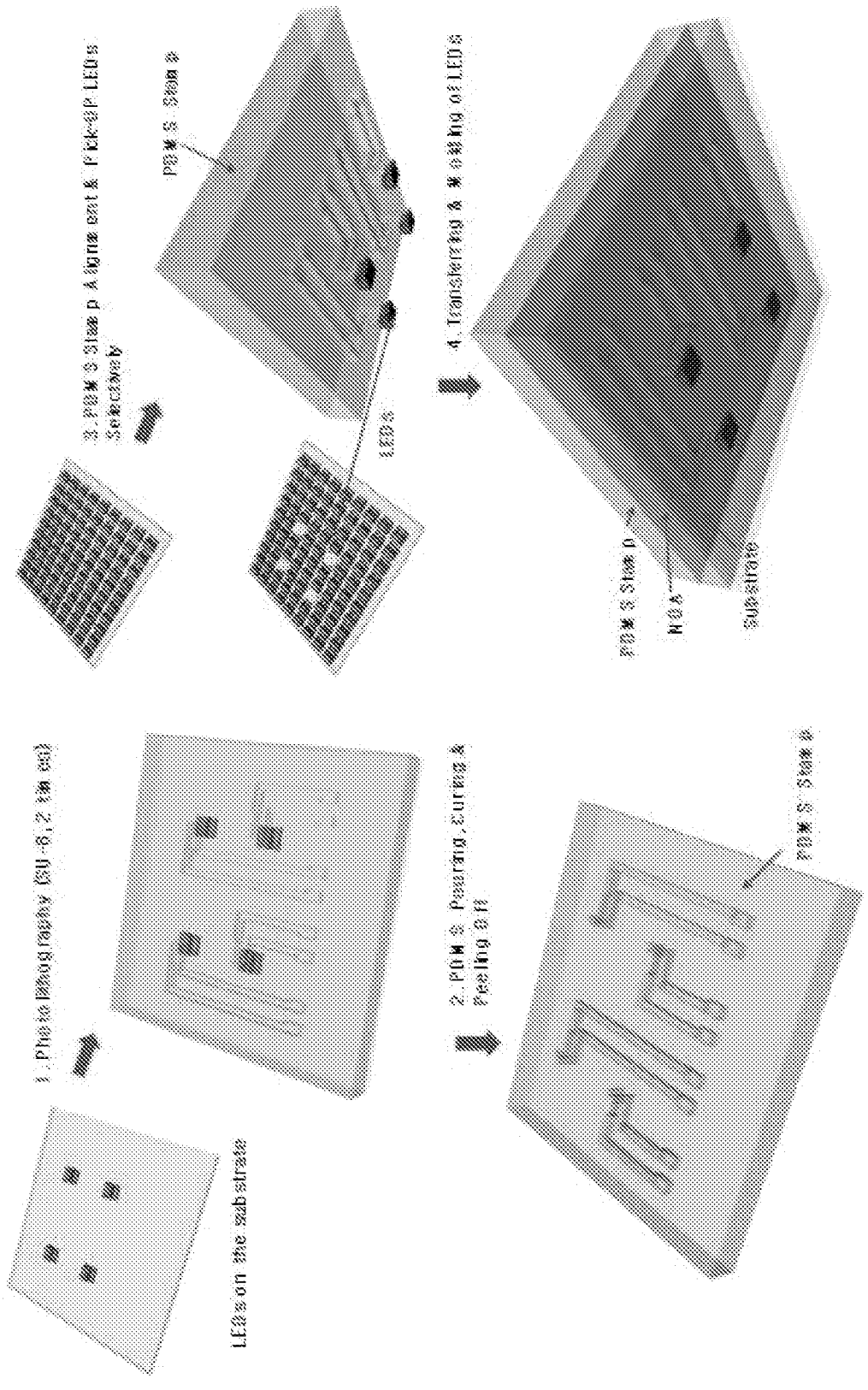

LEDs on the substrate
1. Photolithography (GU-8, 2 layers)
2. PDMS Peeling, Curving & Peeling Off
PDMS Stamp
3. PDMS Stamp Alignment & Pick-up LEDs Selectively
LEDs
4. Transferring & Printing of LEDs
PDMS Stamp
NOA
Substrate
PDMS Stamp

Figure 53

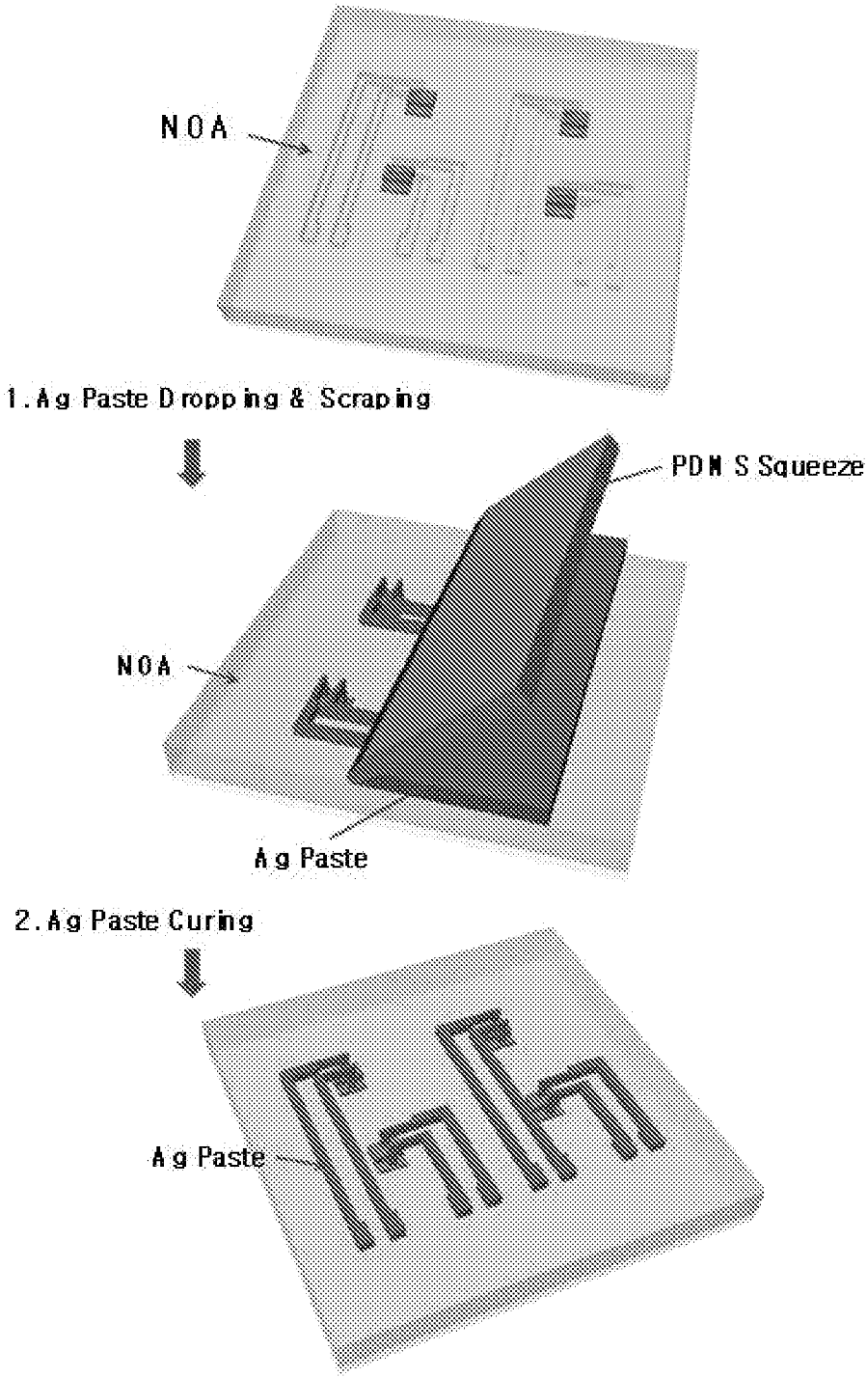

NOA
1. Ag Paste Dropping & Scraping
PDMS Squeeze
NOA
Ag Paste
2. Ag Paste Curing
Ag Paste

Figure 54

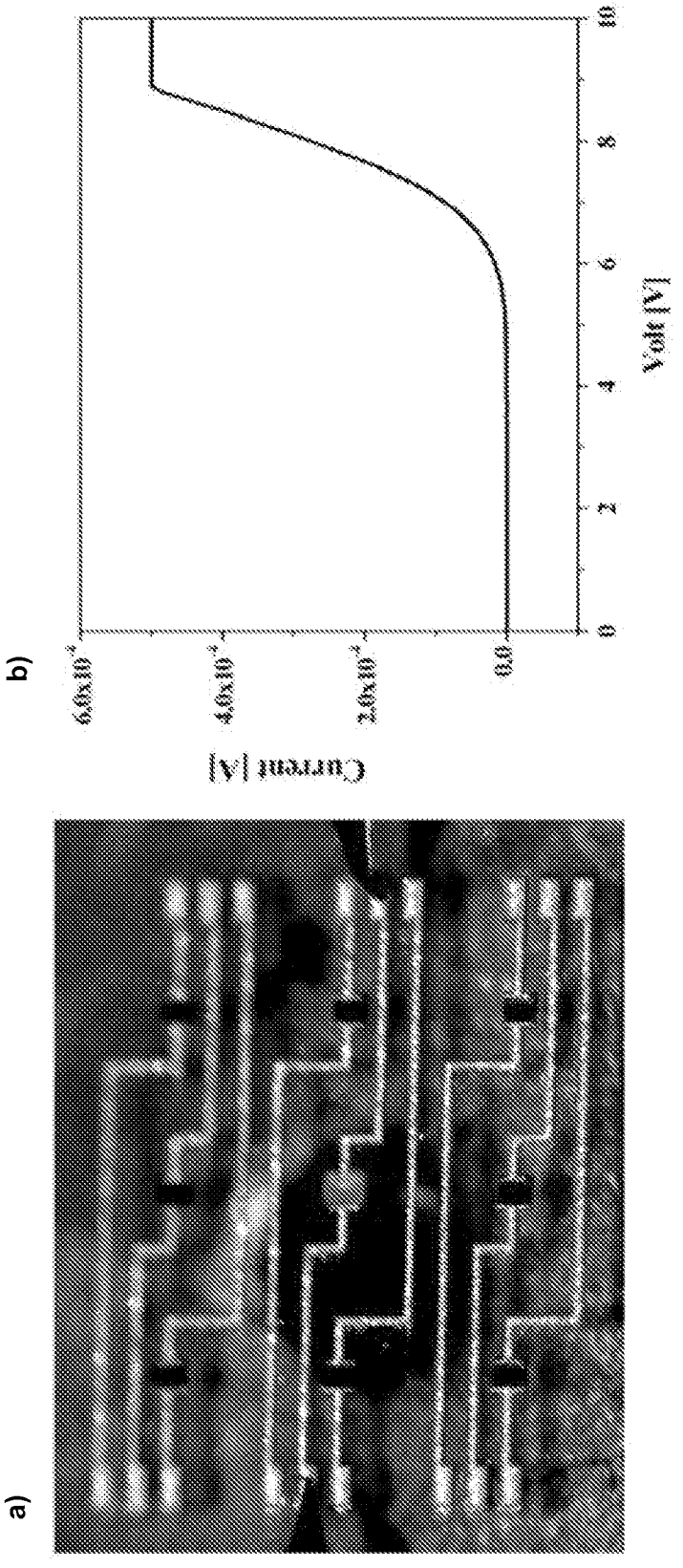


Figure 55

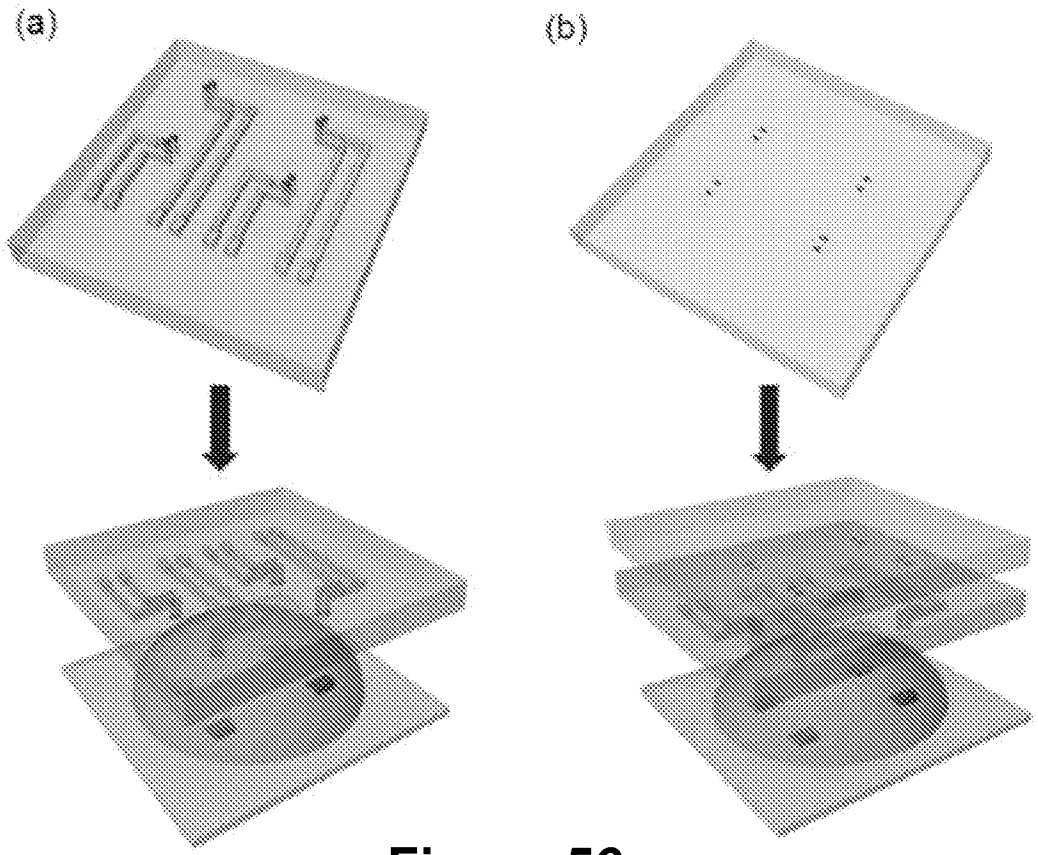


Figure 56

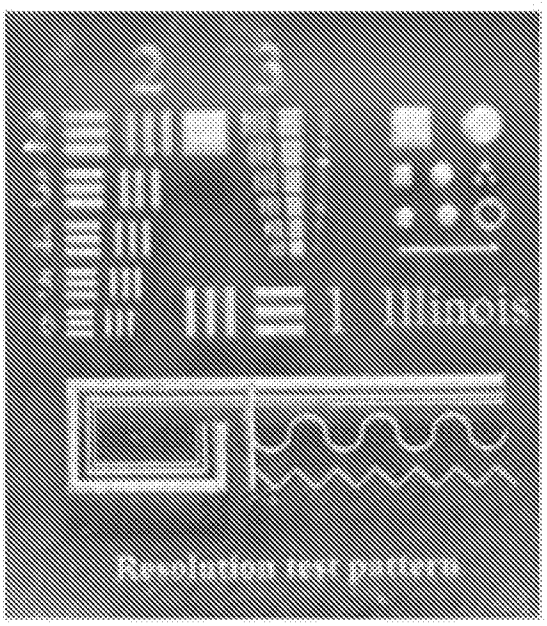
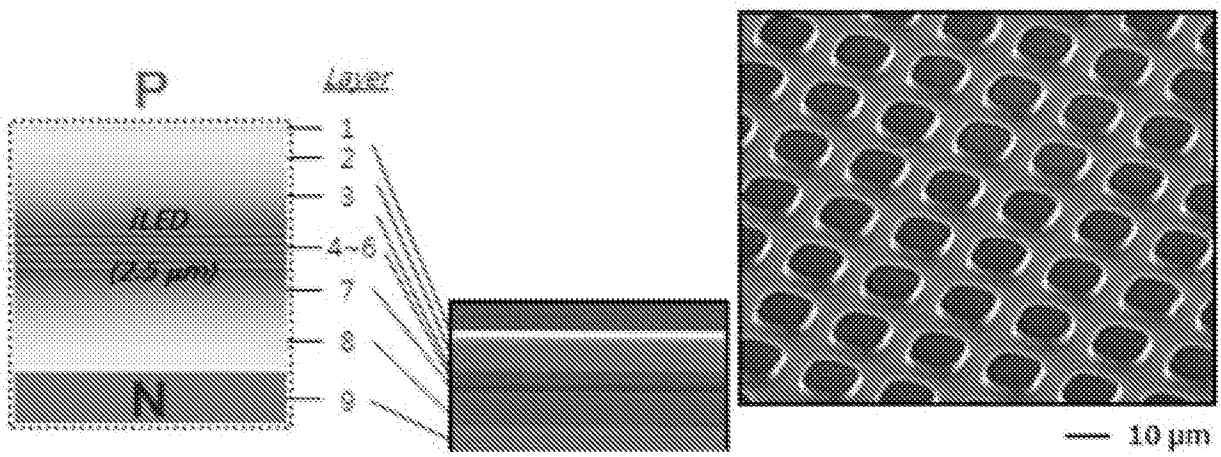


Figure 57



Layer	Layer Name	Material	Thickness (nm)	Type	Dopant	Concentration (cm^{-3})
1	Contact	GaAs	5	P	C	1.00E+19
2	Spreader	$Al_{0.45}Ga_{0.55}As$	800	P	C	1.00E+18
3	Clad	$In_{0.5}Al_{0.5}P$	200	P	Zn	3E17 to 6E17
4	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
5	Well	$In_{0.56}Ga_{0.44}P$	6	-	-	<1E16
6	Barrier	$Al_{0.25}Ga_{0.25}In_{0.5}P$	6	-	-	<1E16
7	Clad	$In_{0.5}Al_{0.5}P$	200	N	Si	1.00E+18
8	Spreader	$Al_{0.45}Ga_{0.55}As$	800	N	Si	1.00E+18
9	Contact	GaAs	500	N	Si	4.00E+18

Figure 58

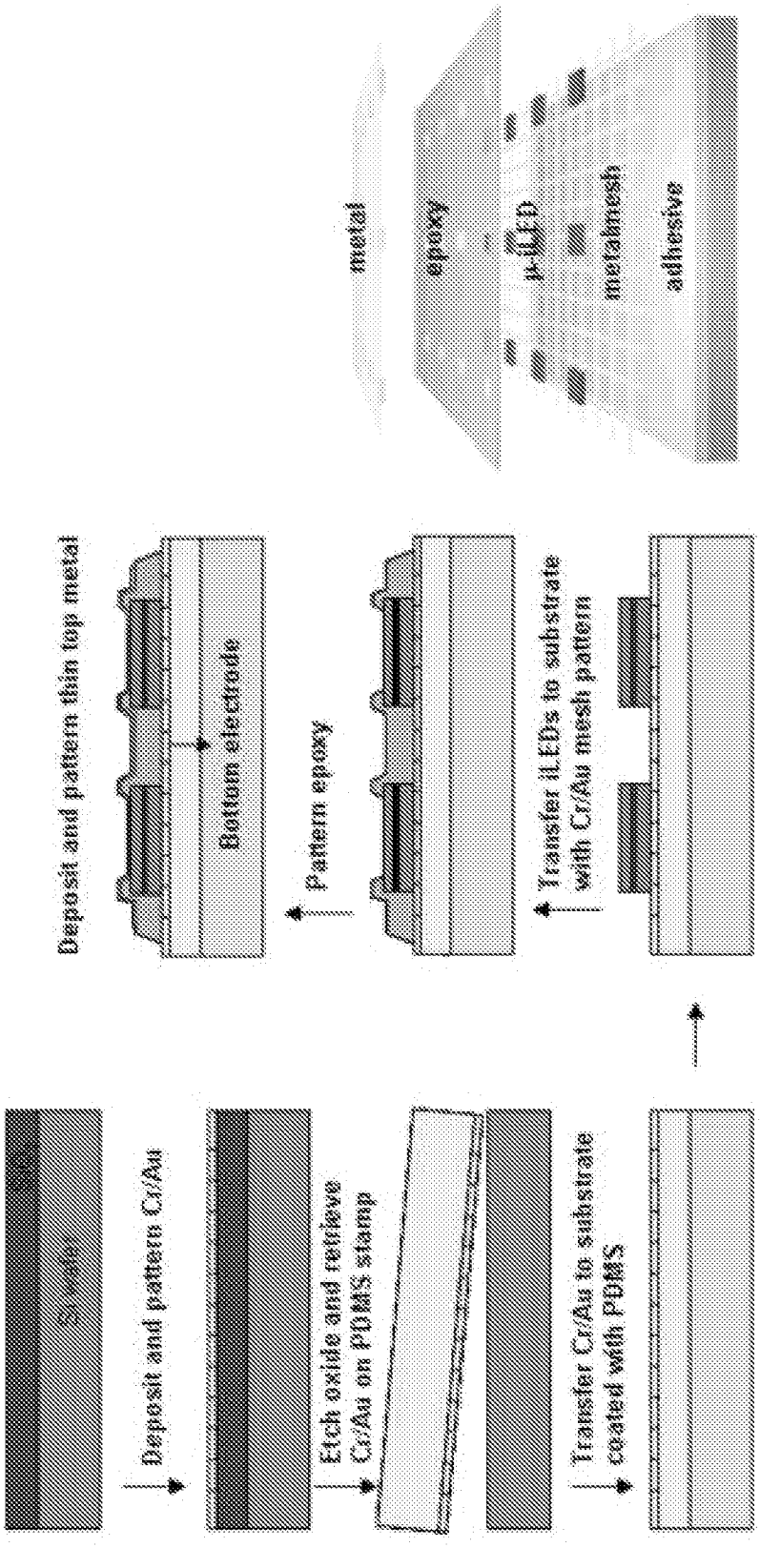

Deposit and pattern Cr/Au
Etch oxide and retrieve Cr/Au on PDMS stamp
Transfer Cr/Au to substrate coated with PDMS
Deposit and pattern thin top metal
Bottom electrode
Pattern epoxy
Transfer iLEDs to substrate with Cr/Au mesh pattern
metal
epoxy
μ-LED
metalmesh
adhesive

Figure 59

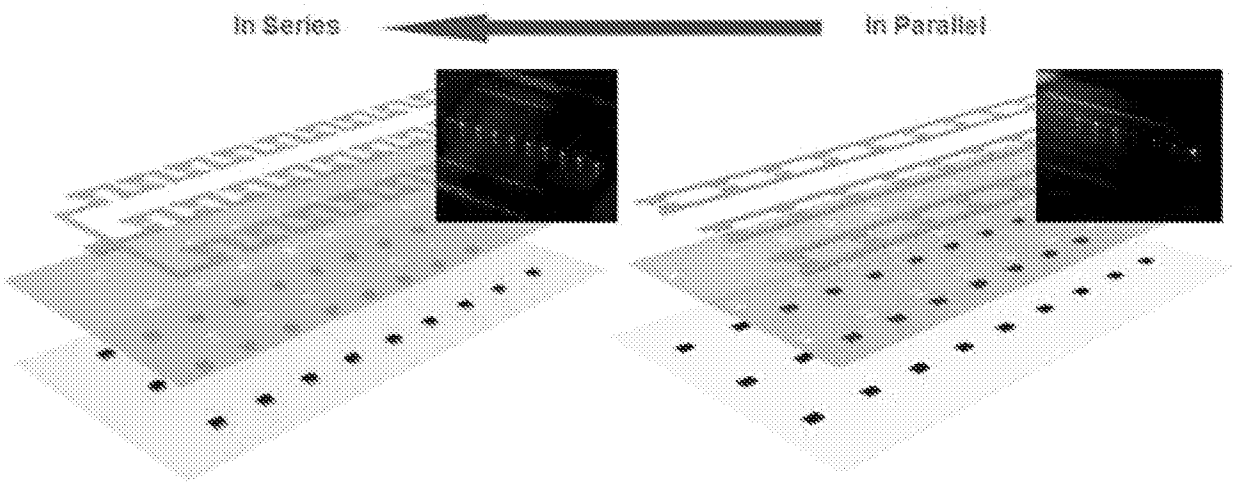


Figure 60

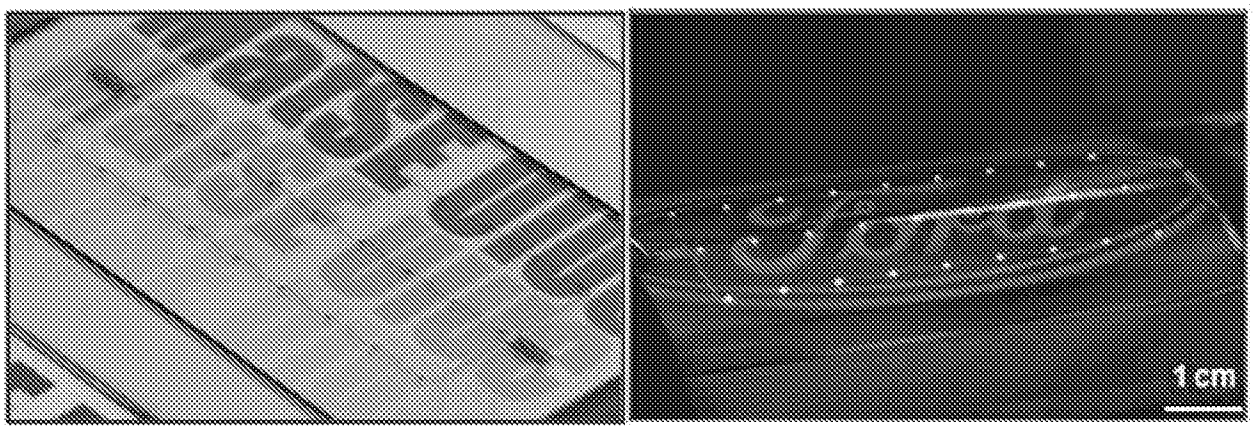


Figure 61

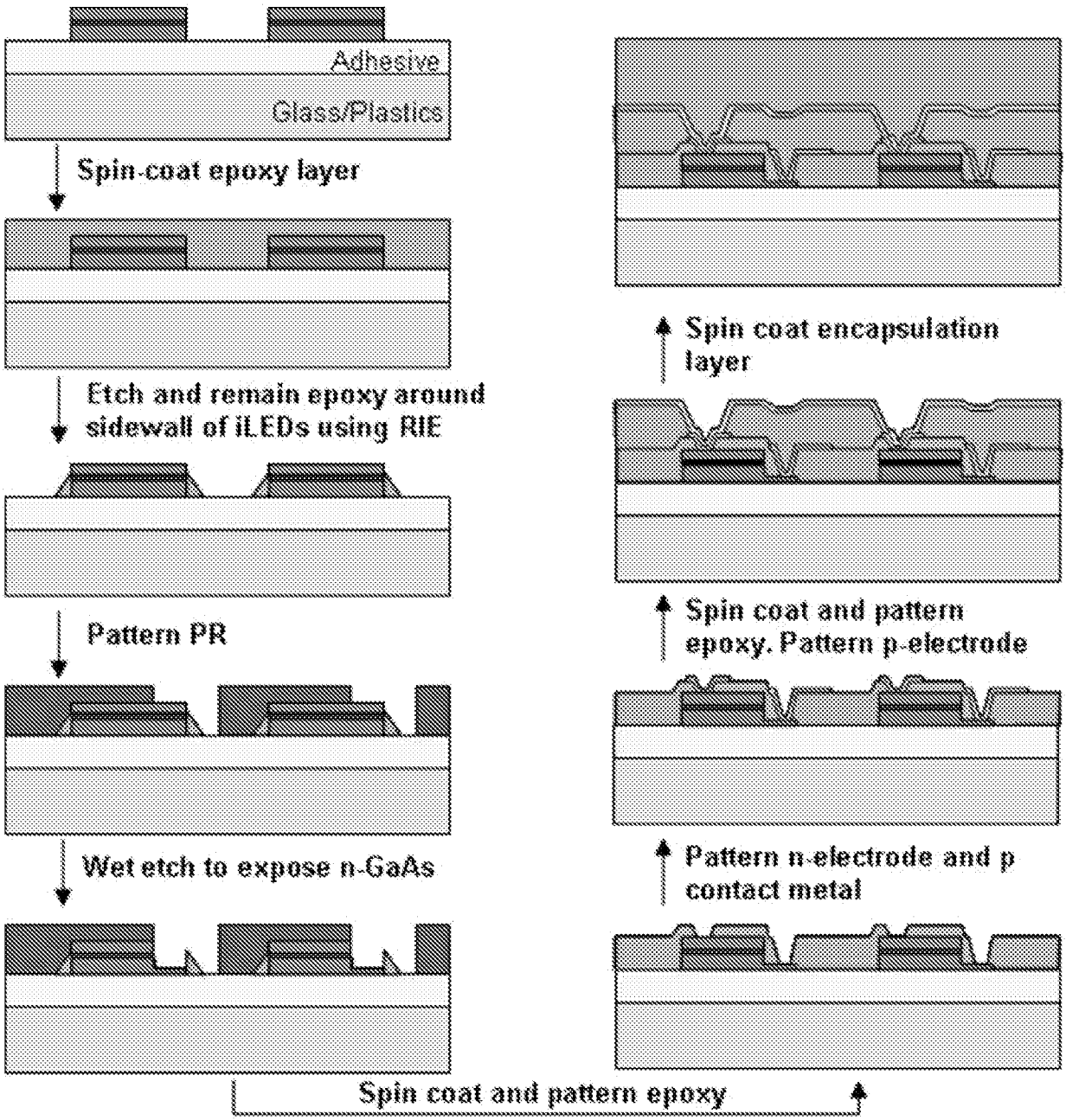

Adhesive
Glass/Plastics
Spin-coat epoxy layer
Etch and remain epoxy around sidewall of iLEDs using RIE
Pattern PR
Wet etch to expose n-GaAs
Spin coat and pattern epoxy
Pattern n-electrode and p contact metal
Spin coat and pattern epoxy. Pattern p-electrode
Spin coat encapsulation layer

Figure 62

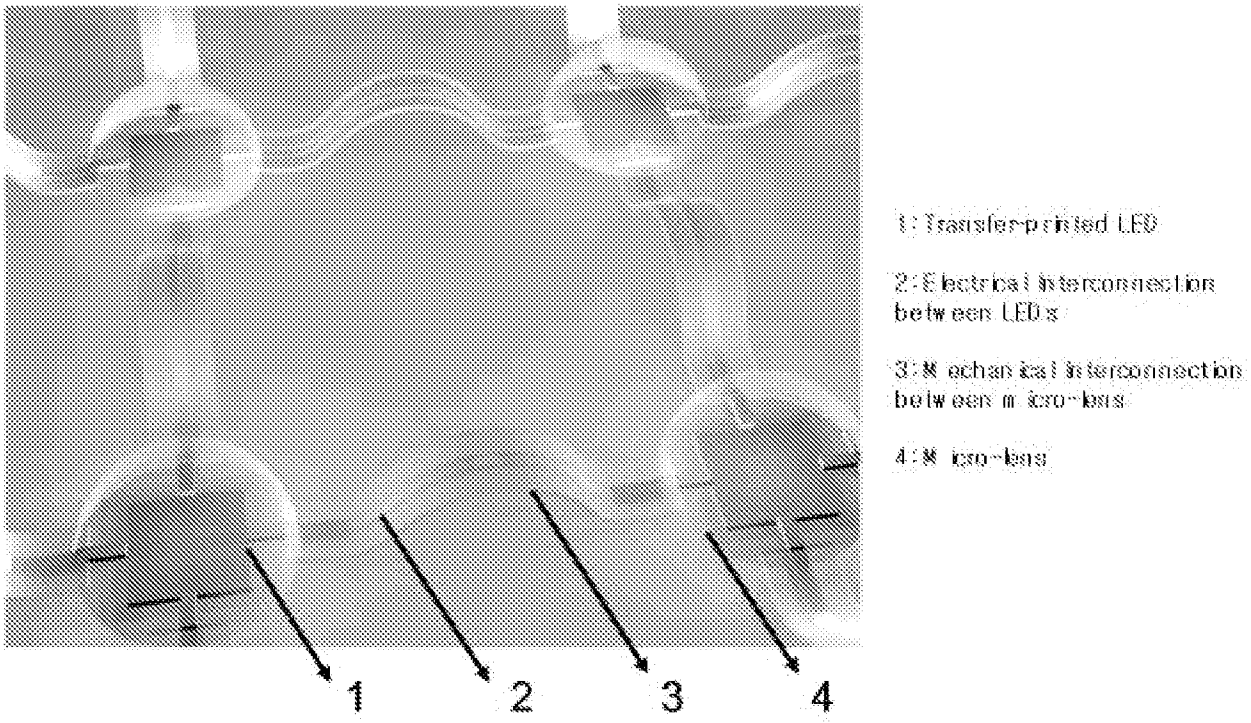


Figure 63

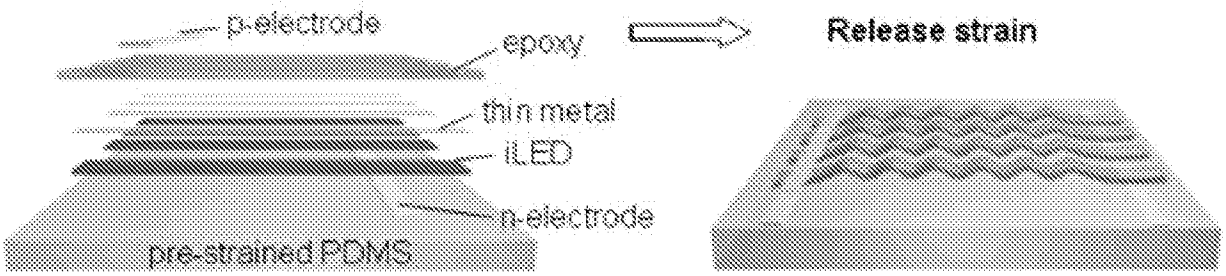


Figure 64

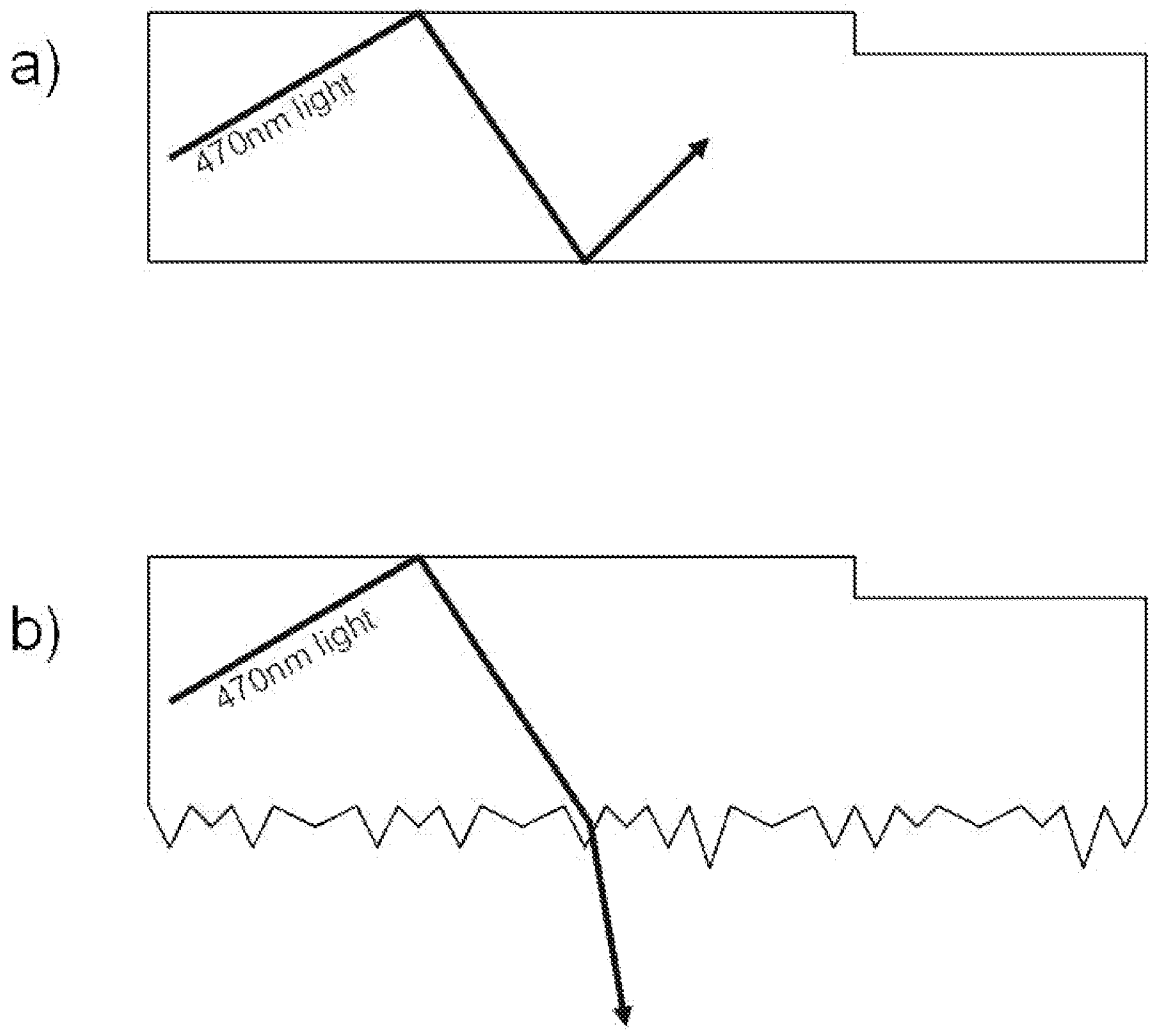


Figure 65

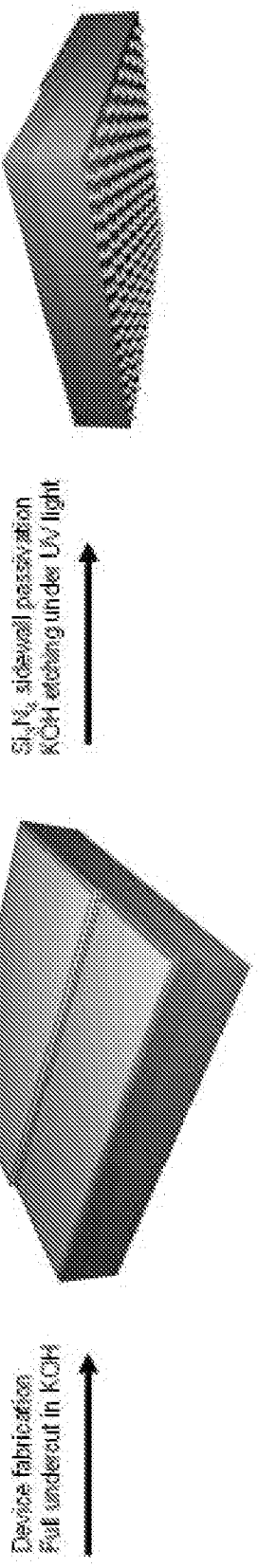

Device fabrication
Full undercut in KOH
Si3N4 sidewall passivation
KOH etching under UV light

Figure 66

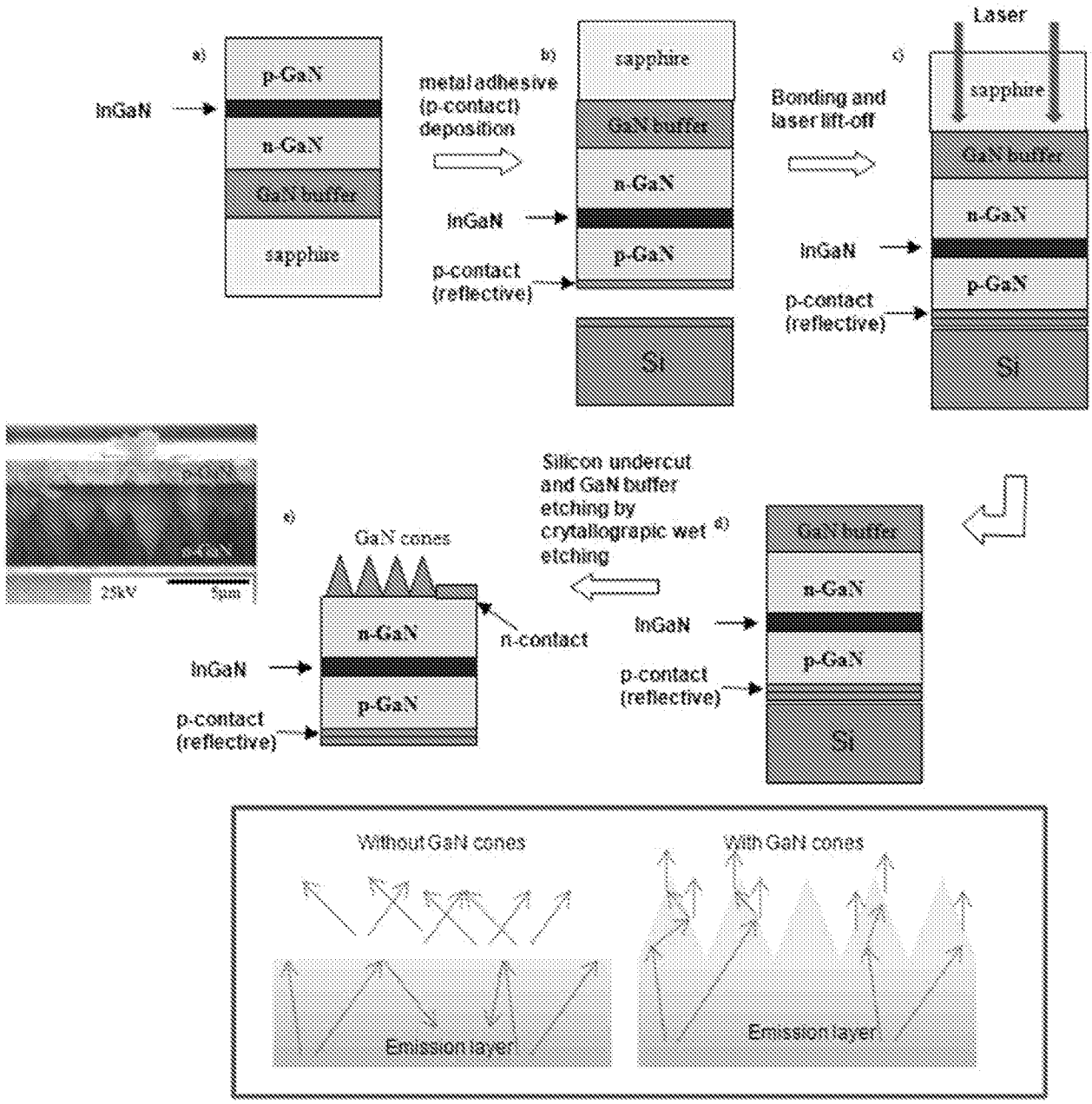

a)
InGaN
p-GaN
n-GaN
GaN buffer
sapphire
b)
metal adhesive
(p-contact)
deposition
sapphire
GaN buffer
n-GaN
InGaN
p-GaN
p-contact
(reflective)
Si
c)
Laser
Bonding and
laser lift-off
sapphire
GaN buffer
n-GaN
InGaN
p-GaN
p-contact
(reflective)
Si
e)
GaN cones
n-GaN
InGaN
p-GaN
p-contact
(reflective)
n-contact
Silicon undercut
and GaN buffer
etching by
crytallograpic wet
etching
d)
GaN buffer
n-GaN
InGaN
p-GaN
p-contact
(reflective)
Si
Without GaN cones
Emission layer
With GaN cones
Emission layer

Figure 67

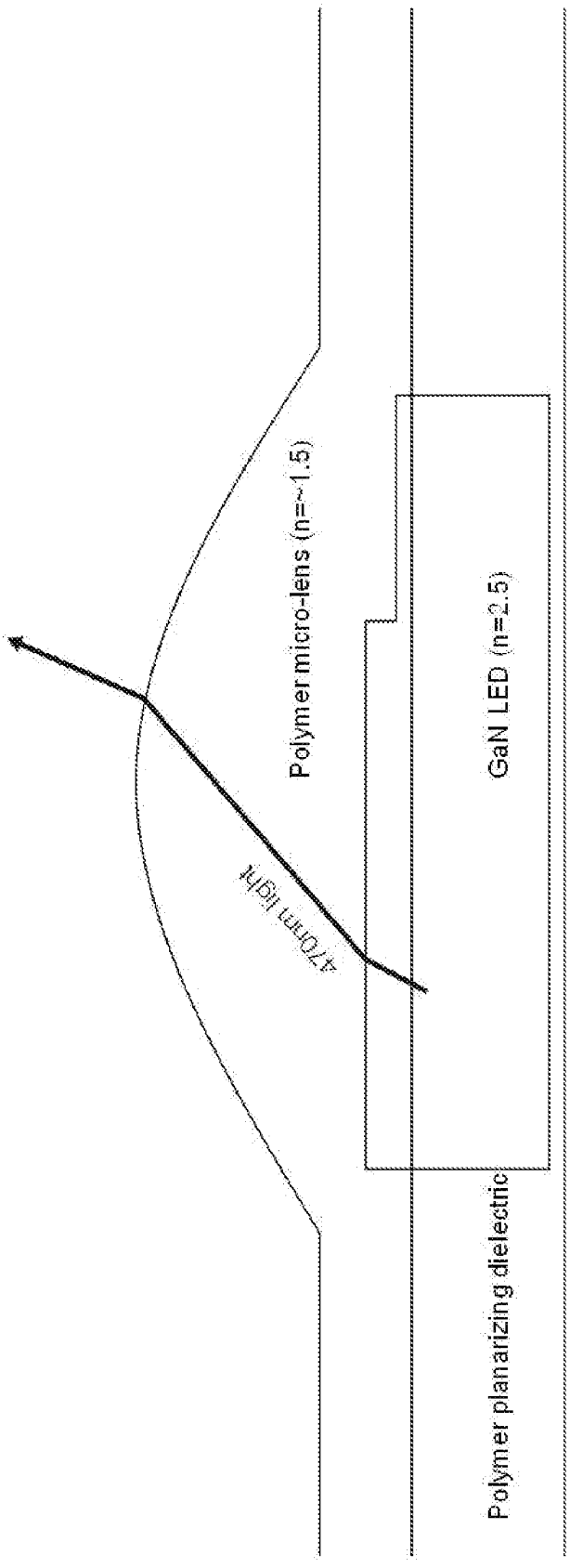

Polymer micro-lens (n=~1.5)
GaN LED (n=2.5)
Polymer planarizing dielectric
470nm light

Figure 68

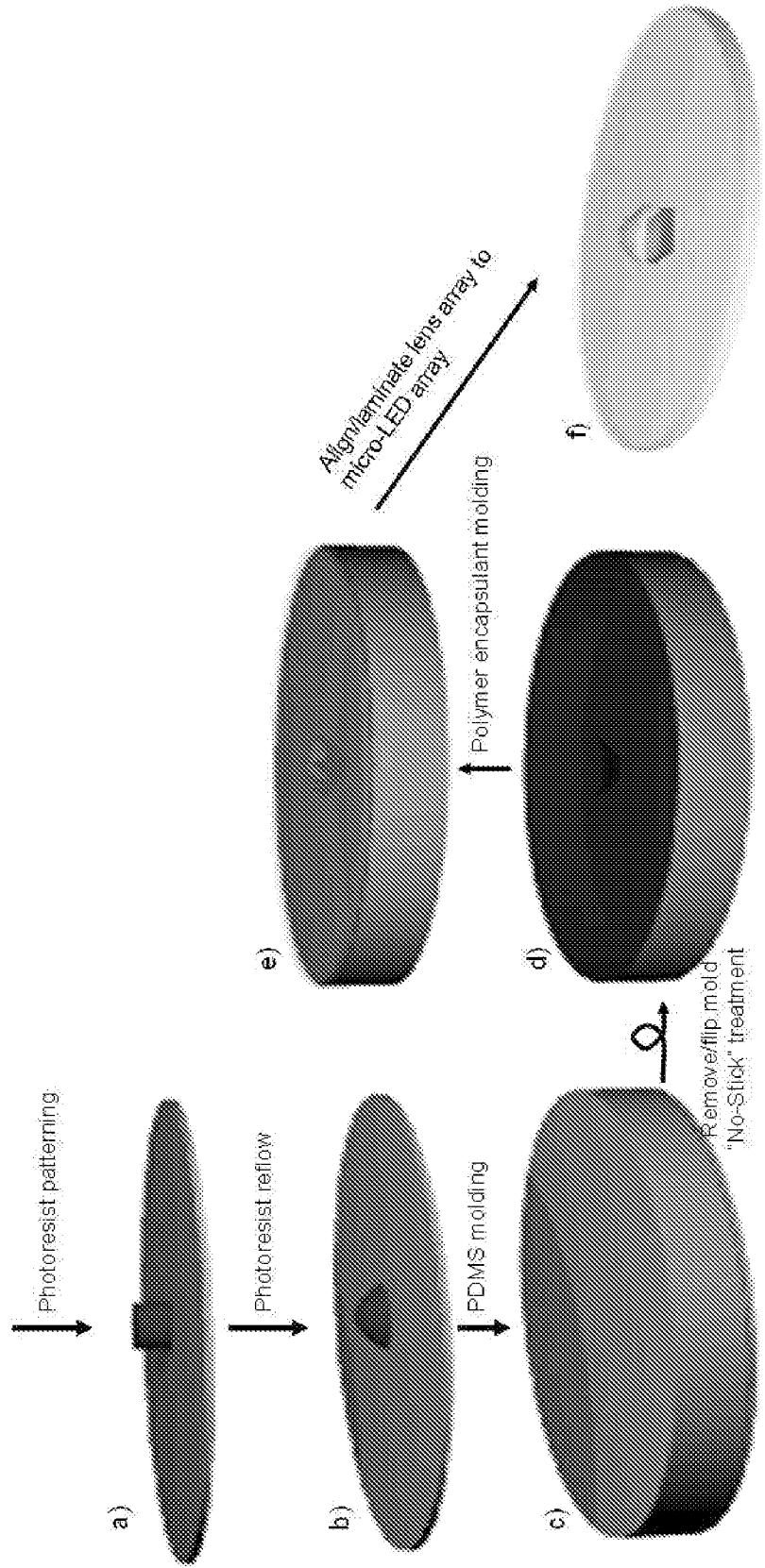

Photoresist patterning
Photoresist reflow
PDMS molding
Remove/flip mold
"No-Stick" treatment
Polymer encapsulant molding
Align/laminate lens array to micro-LED array
a)
b)
c)
d)
e)
f)

Figure 69

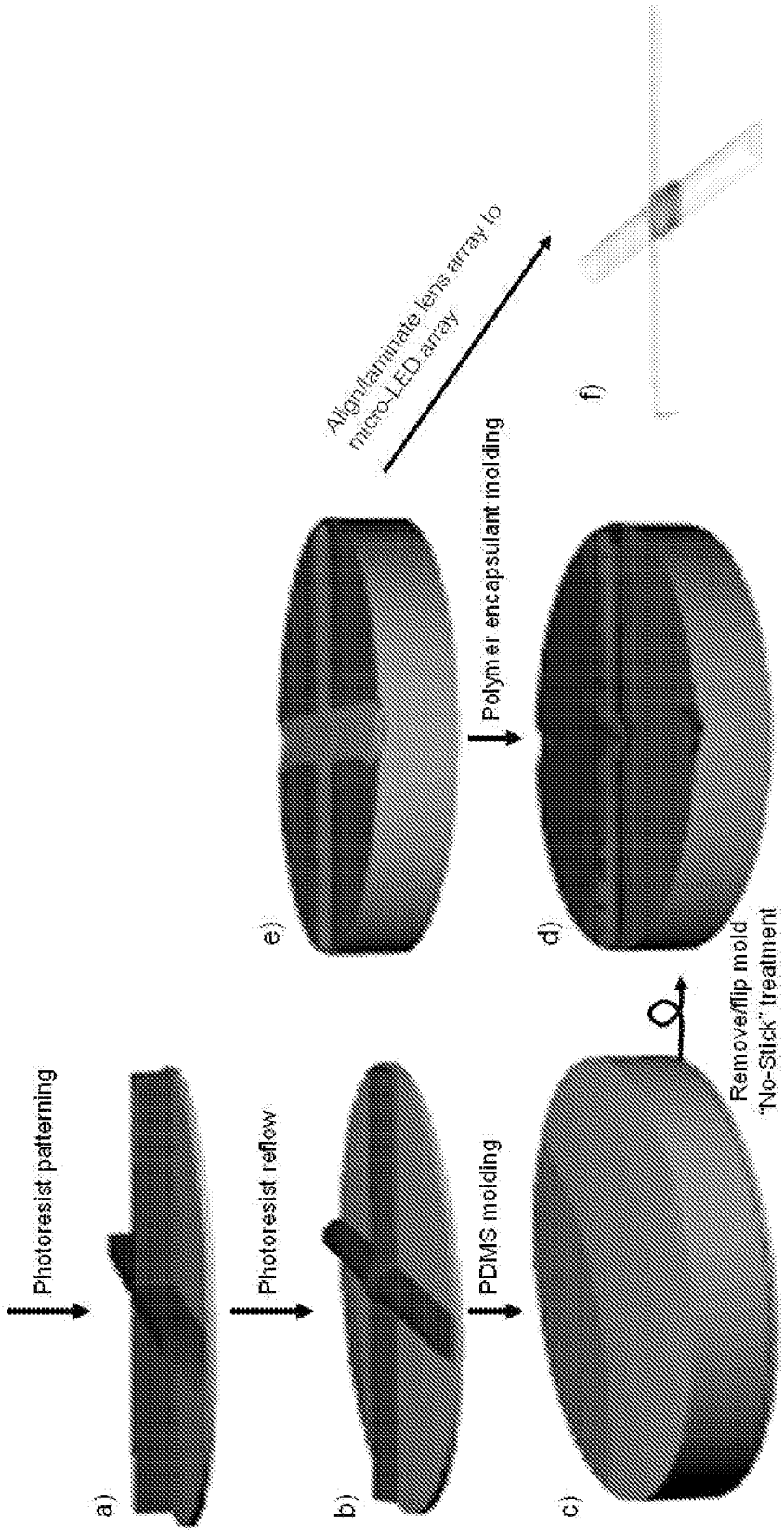

Photoresist patterning
Photoresist reflow
PDMS molding
Remove/flip mold
"No-Stick" treatment
Polymer encapsulant molding
Align/laminate lens array to micro-LED array
a)
b)
c)
d)
e)
f)

Figure 70

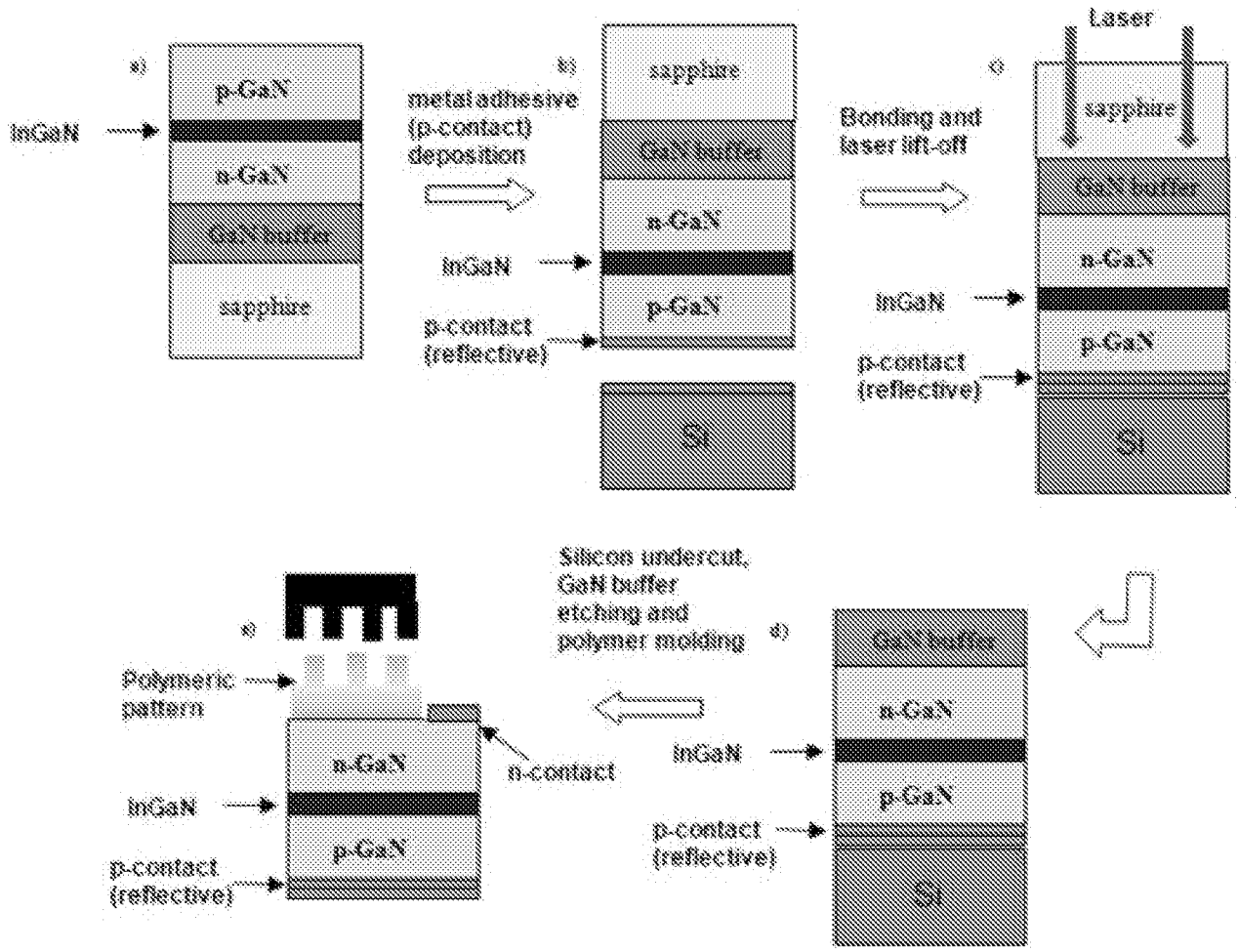

a)
InGaN
p-GaN
n-GaN
GaN buffer
sapphire
b)
metal adhesive
(p-contact)
deposition
sapphire
GaN buffer
n-GaN
InGaN
p-GaN
p-contact
(reflective)
Si
c)
Bonding and
laser lift-off
Laser
sapphire
GaN buffer
n-GaN
InGaN
p-GaN
p-contact
(reflective)
Si
d)
Polymeric
pattern
n-GaN
InGaN
p-GaN
p-contact
(reflective)
n-contact
Silicon undercut,
GaN buffer
etching and
polymer molding
e)
GaN buffer
n-GaN
InGaN
p-GaN
p-contact
(reflective)
Si

Figure 71

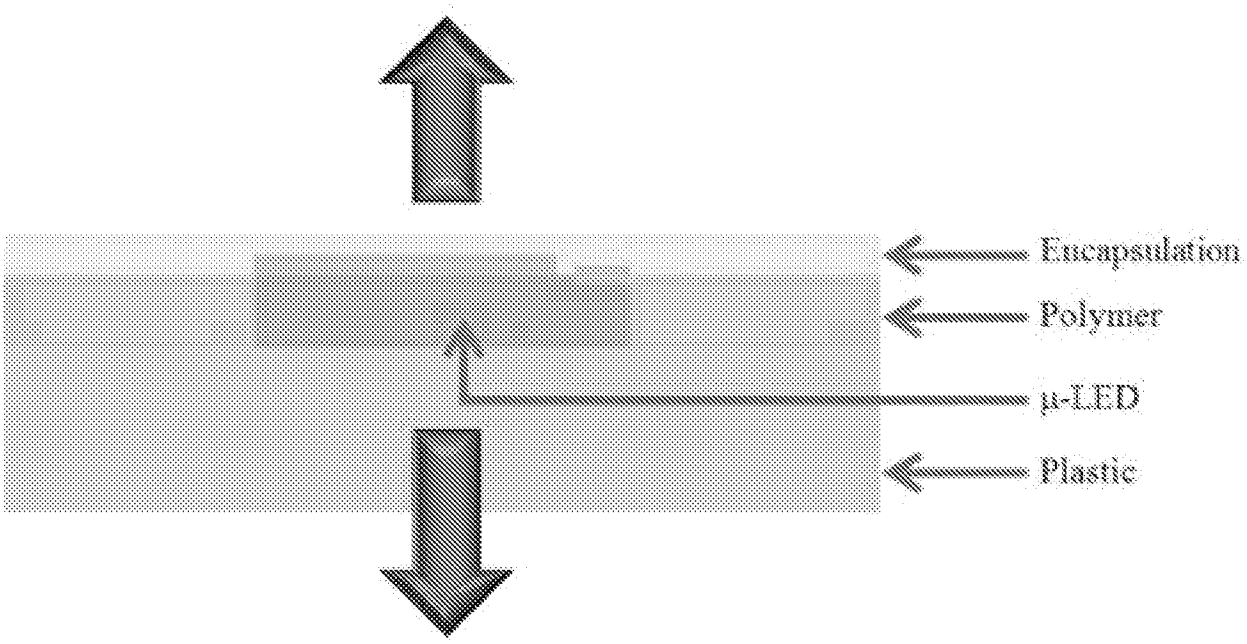


Figure 72

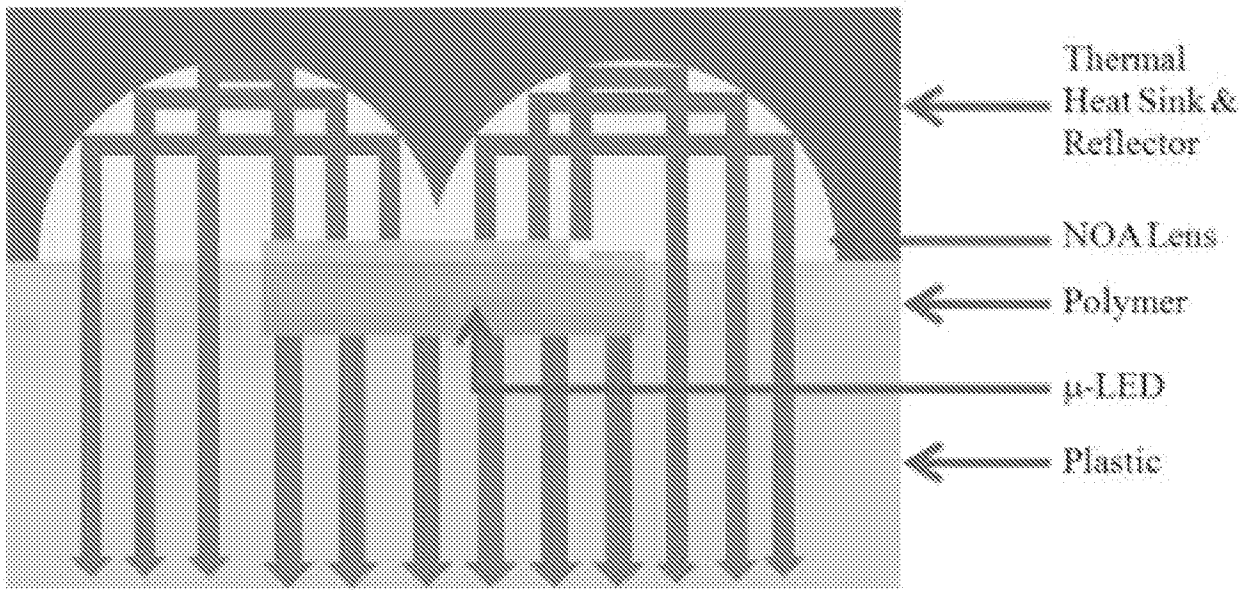


Figure 73

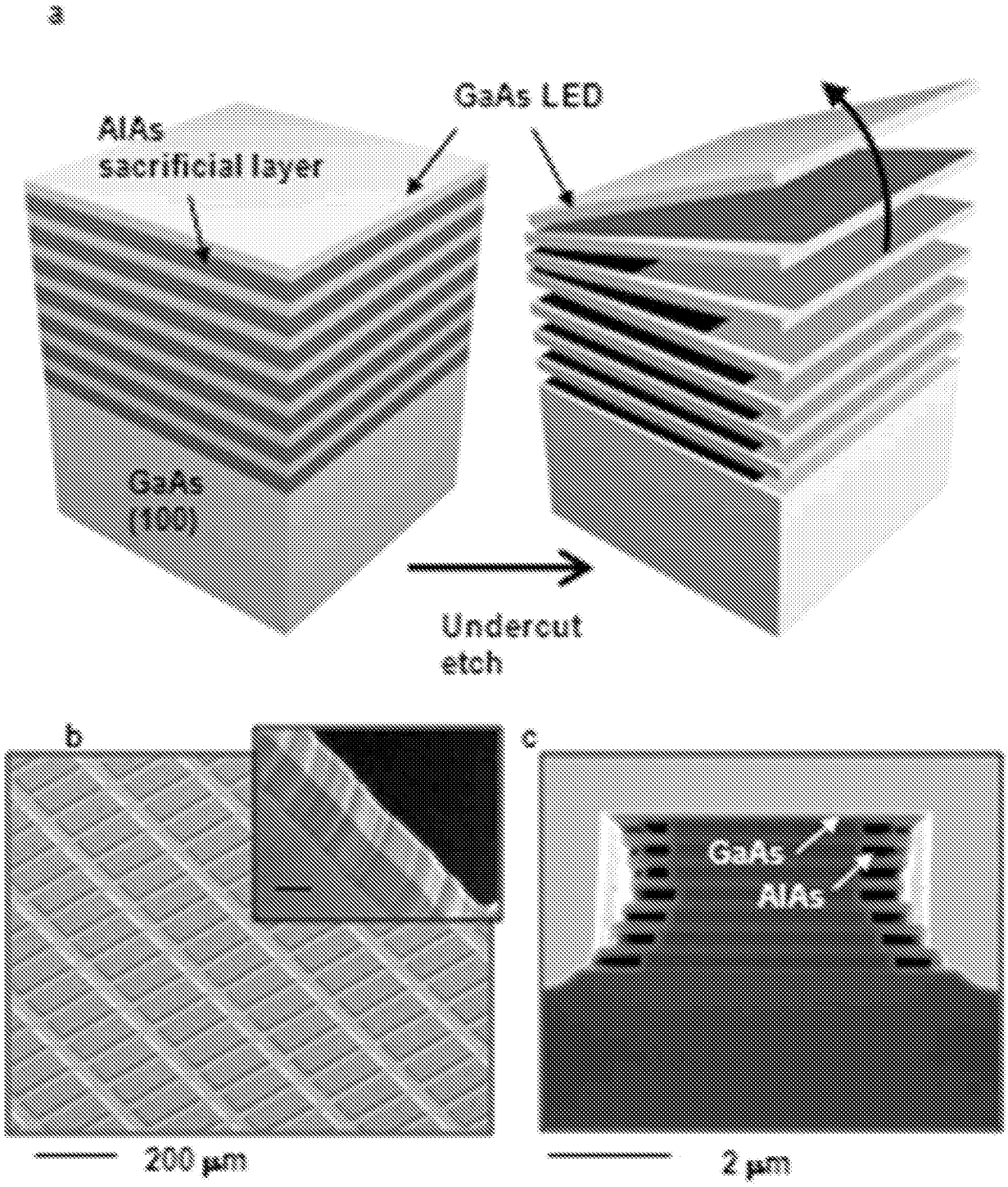

a
GaAs LED
AlAs
sacrificial layer
GaAs
(100)
Undercut
etch
b
200 μm
c
GaAs
AlAs
2 μm

Figure 74

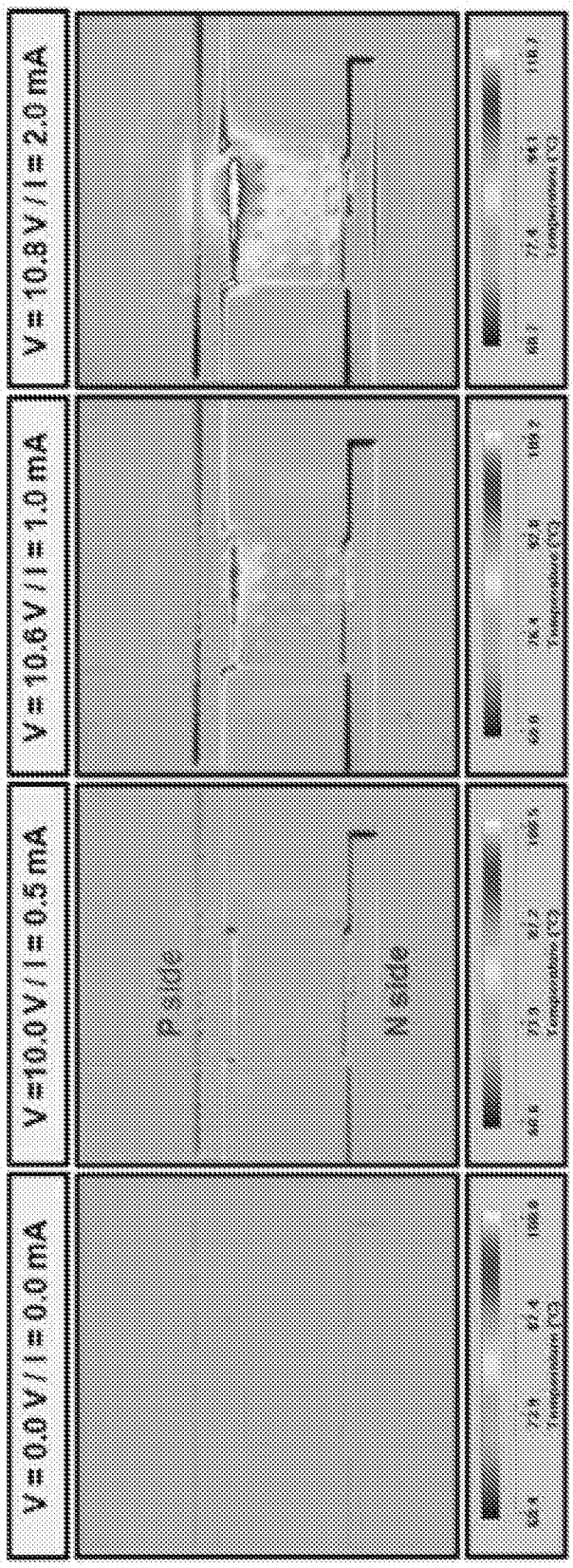


Figure 75

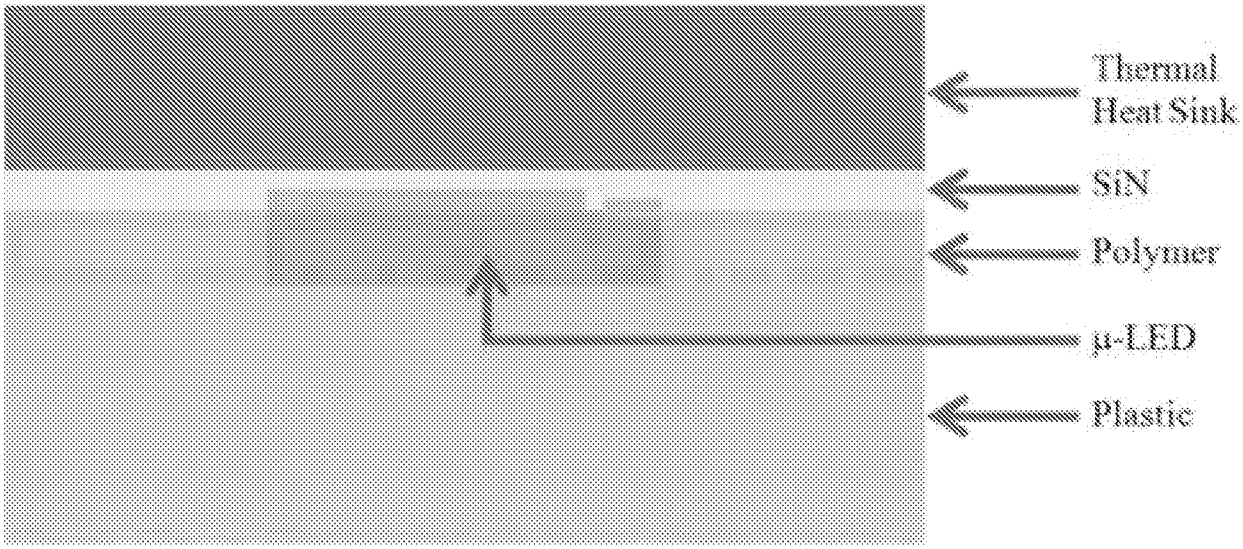


Figure 76

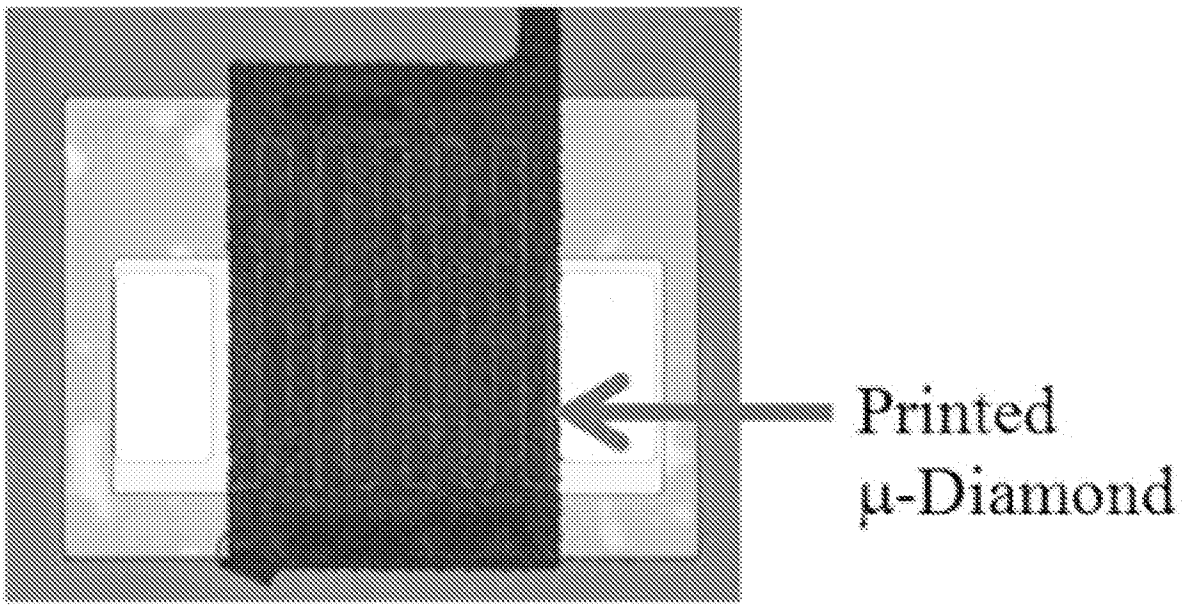


Figure 77

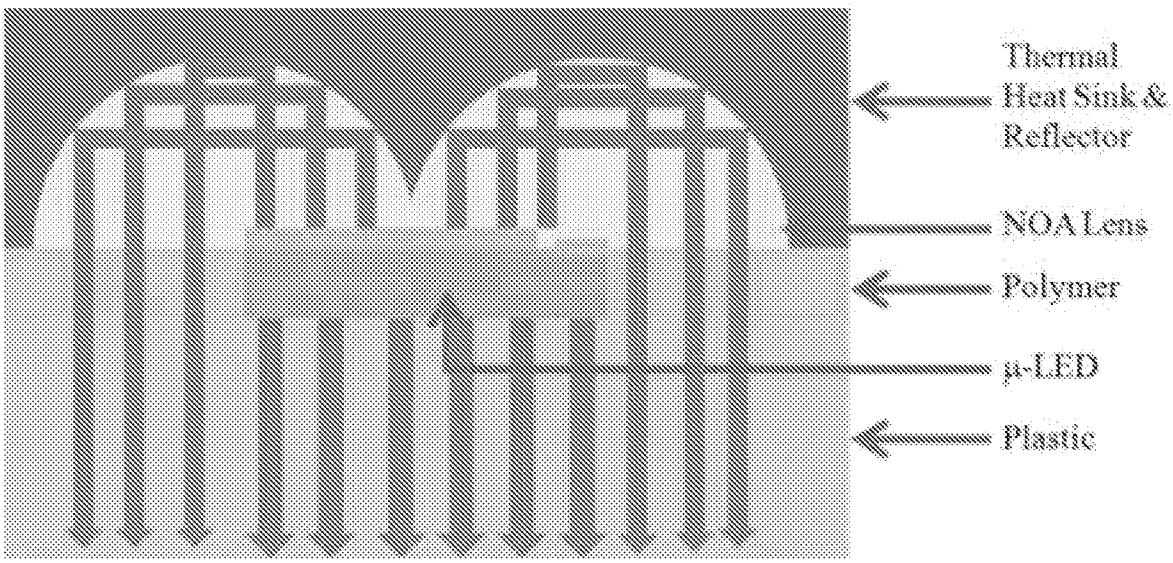


Figure 78

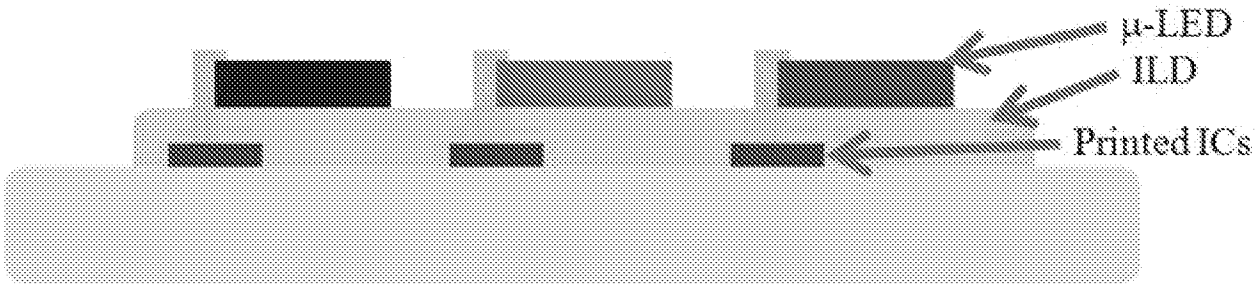


Figure 79

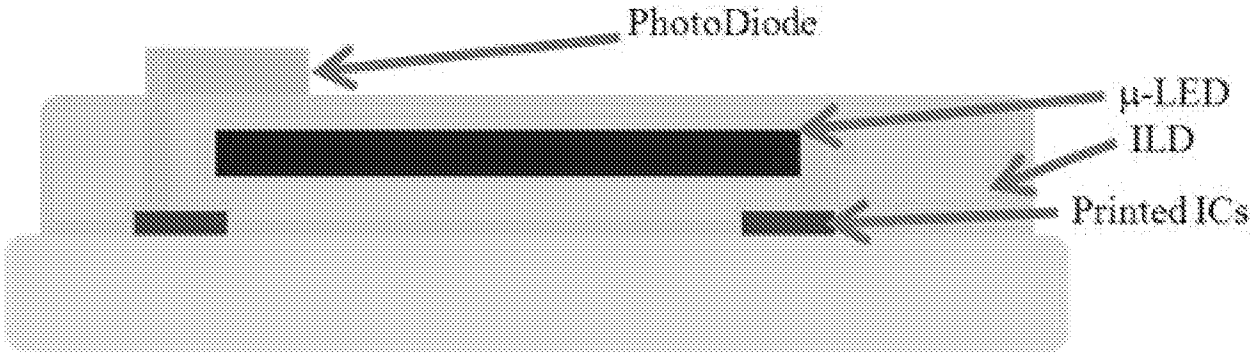


Figure 80

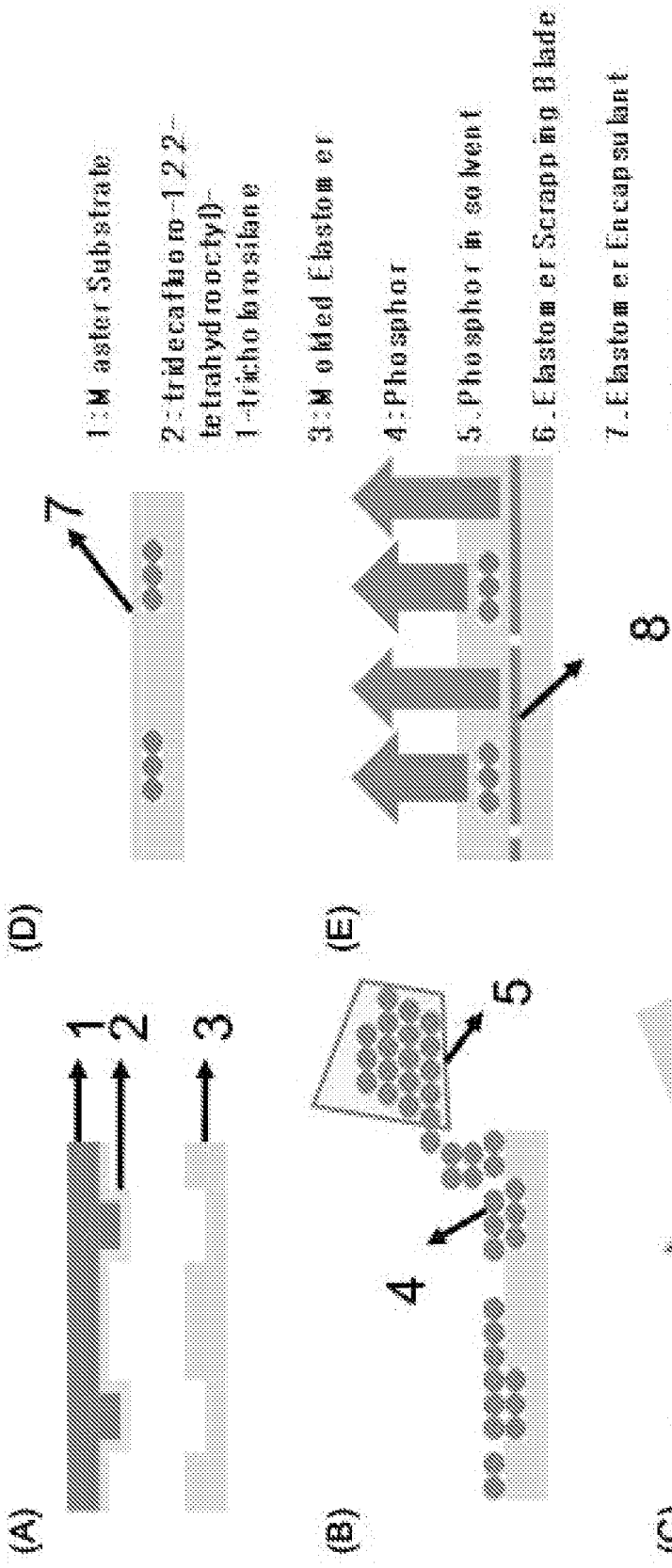

(A)
1
2
3
(B)
4
5
(C)
6
(D)
7
1: Master Substrate
2: tridecafluoro-1,2,2-tetrahydrooctyl)-1-trichlorosilane
3: Molded Elastomer
(E)
4: Phosphor
5: Phosphor in solvent
6: Elastomer Scrapping Blade
7: Elastomer Encapsulant
8
8: GaN LEDs

Figure 81

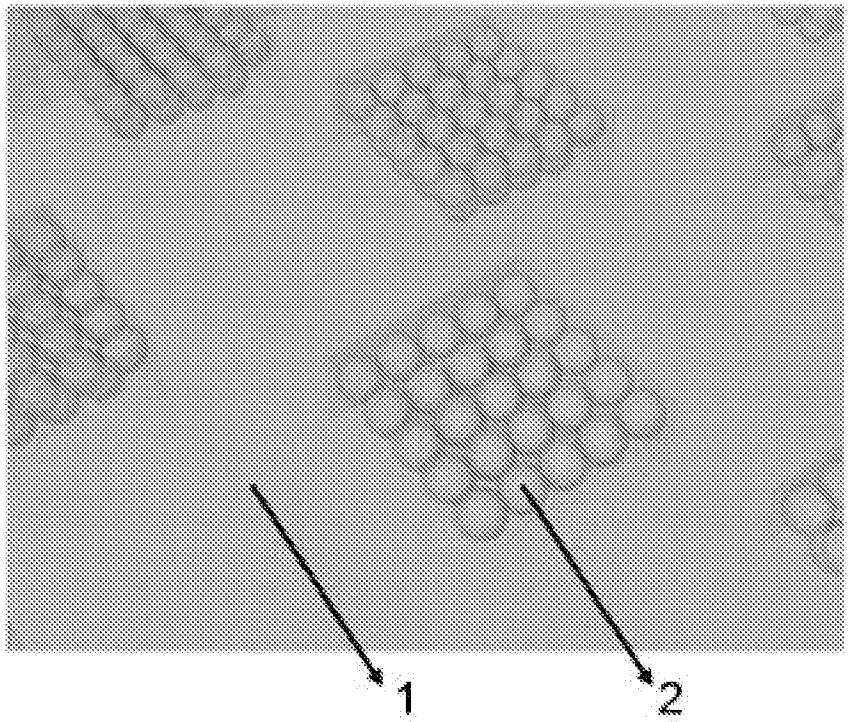


Figure 82

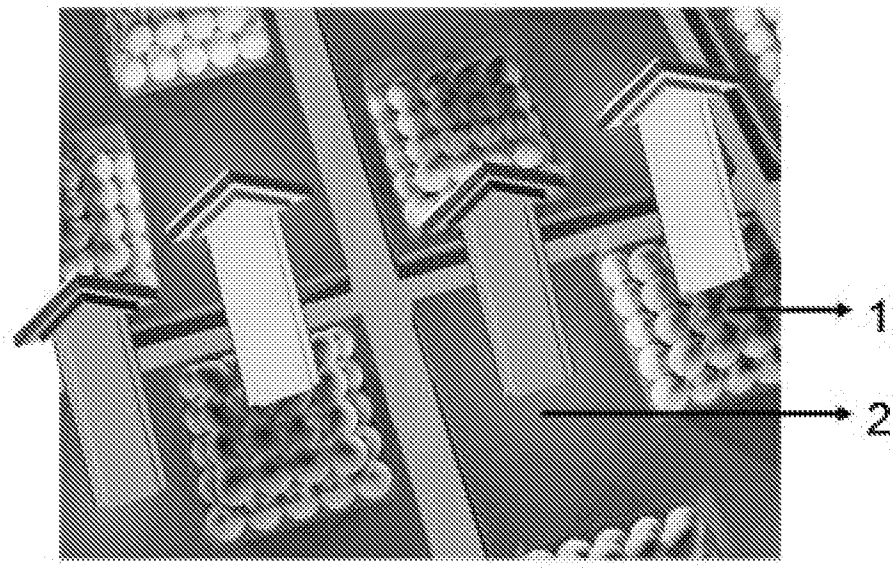


Figure 83

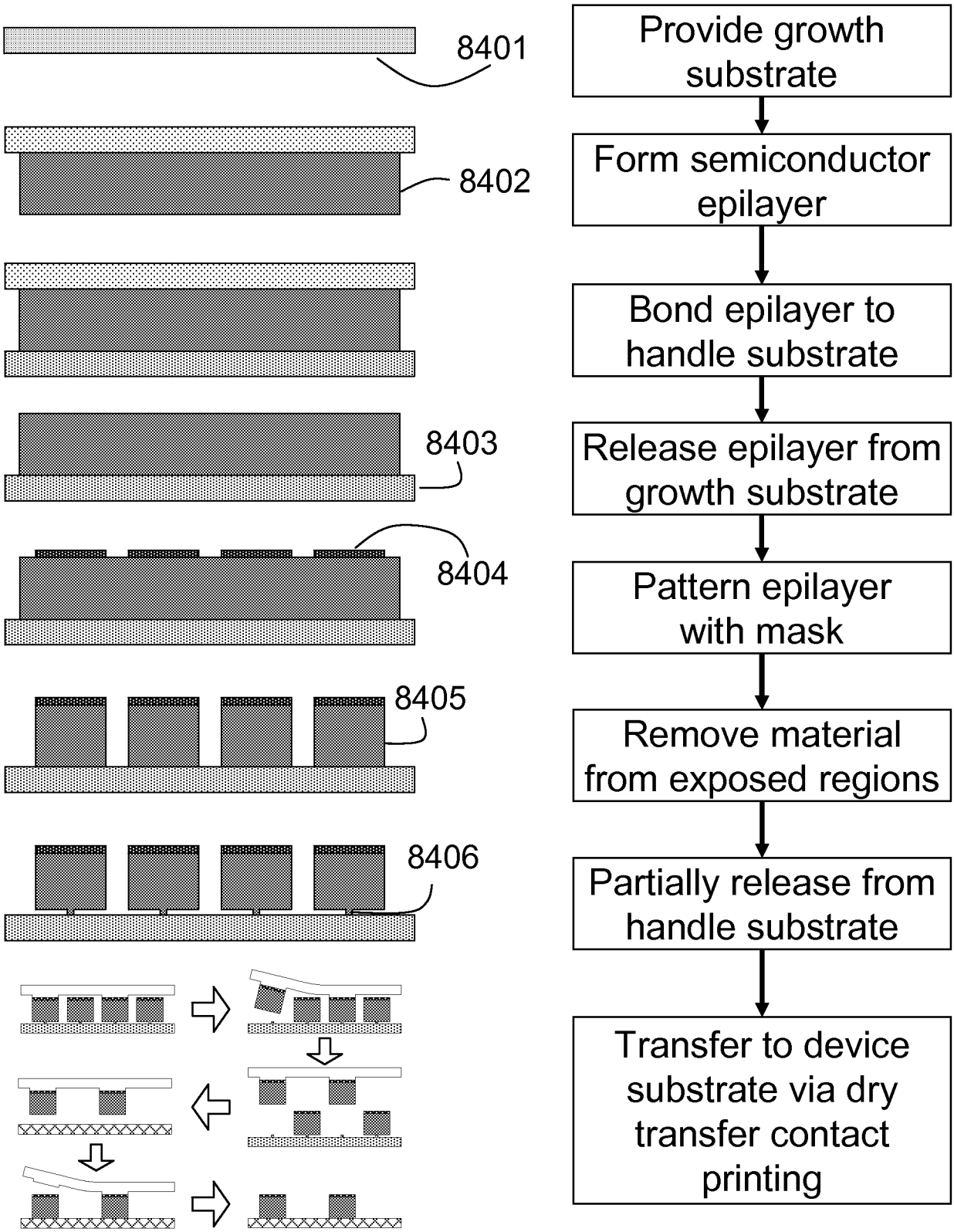

8401
8402
8403
8404
8405
8406
Provide growth substrate
Form semiconductor epilayer
Bond epilayer to handle substrate
Release epilayer from growth substrate
Pattern epilayer with mask
Remove material from exposed regions
Partially release from handle substrate
Transfer to device substrate via dry transfer contact printing

Figure 84

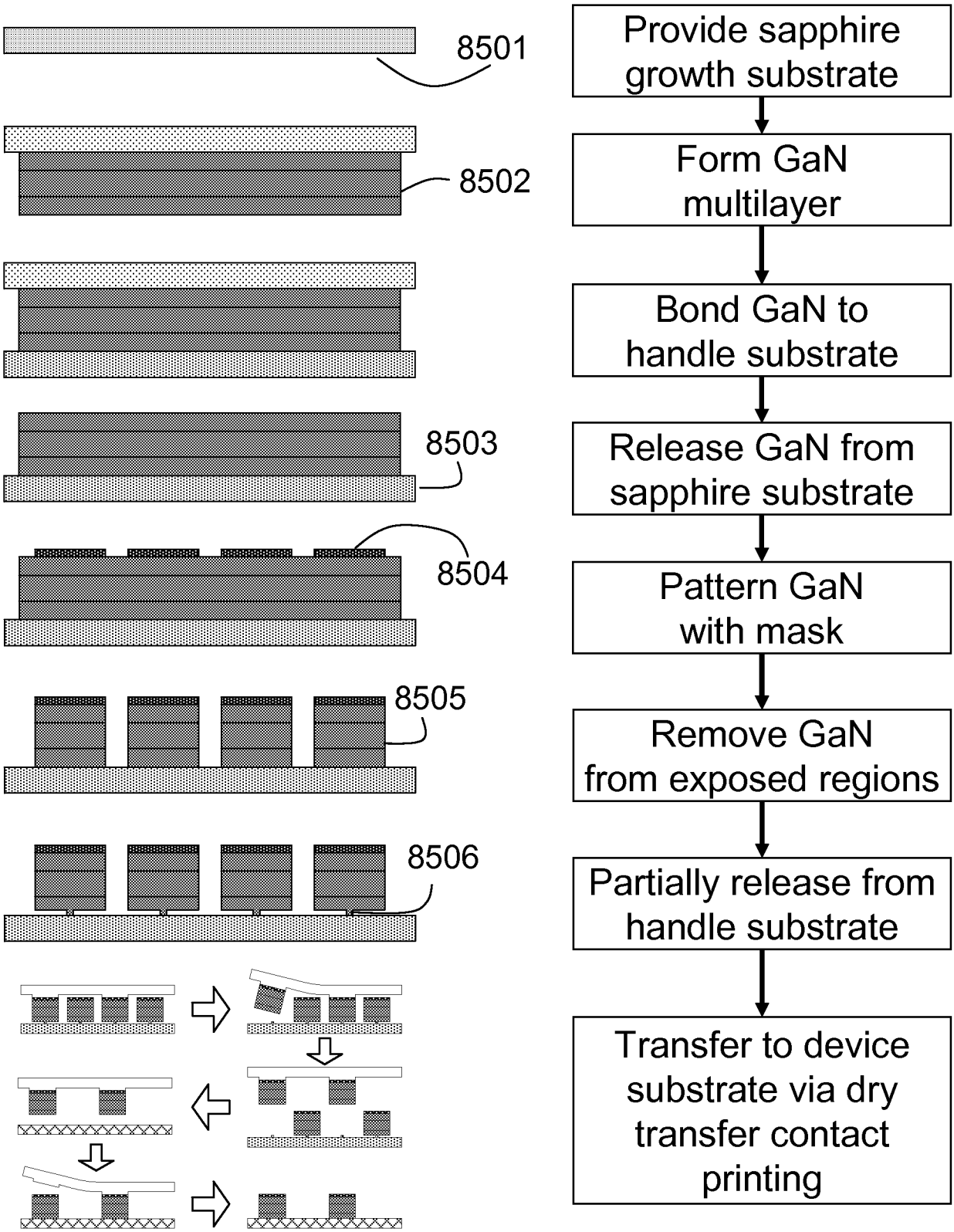

8501
8502
8503
8504
8505
8506
Provide sapphire growth substrate
Form GaN multilayer
Bond GaN to handle substrate
Release GaN from sapphire substrate
Pattern GaN with mask
Remove GaN from exposed regions
Partially release from handle substrate
Transfer to device substrate via dry transfer contact printing

Figure 85

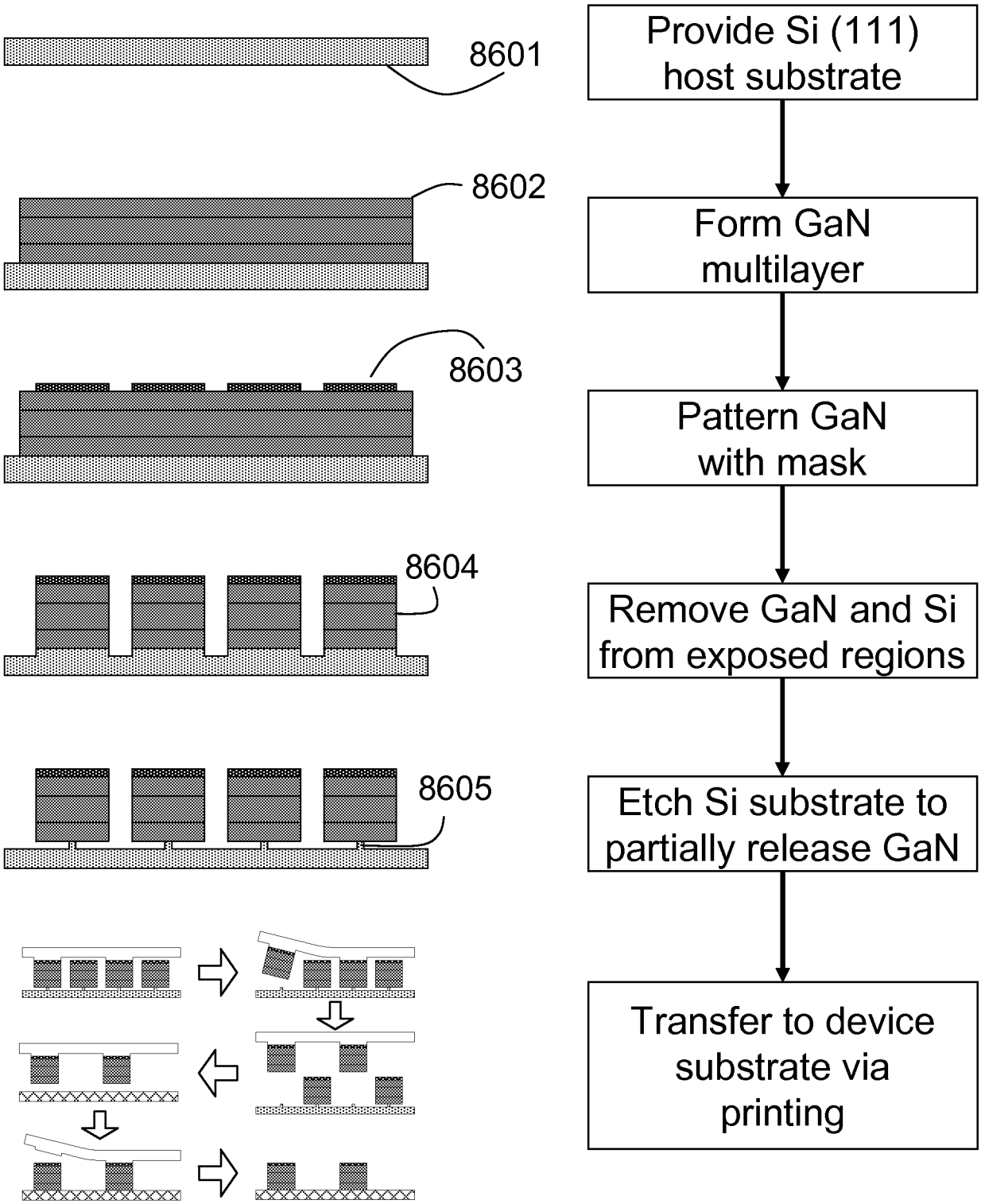

8601
8602
8603
8604
8605
Provide Si (111) host substrate
Form GaN multilayer
Pattern GaN with mask
Remove GaN and Si from exposed regions
Etch Si substrate to partially release GaN
Transfer to device substrate via printing

Figure 86

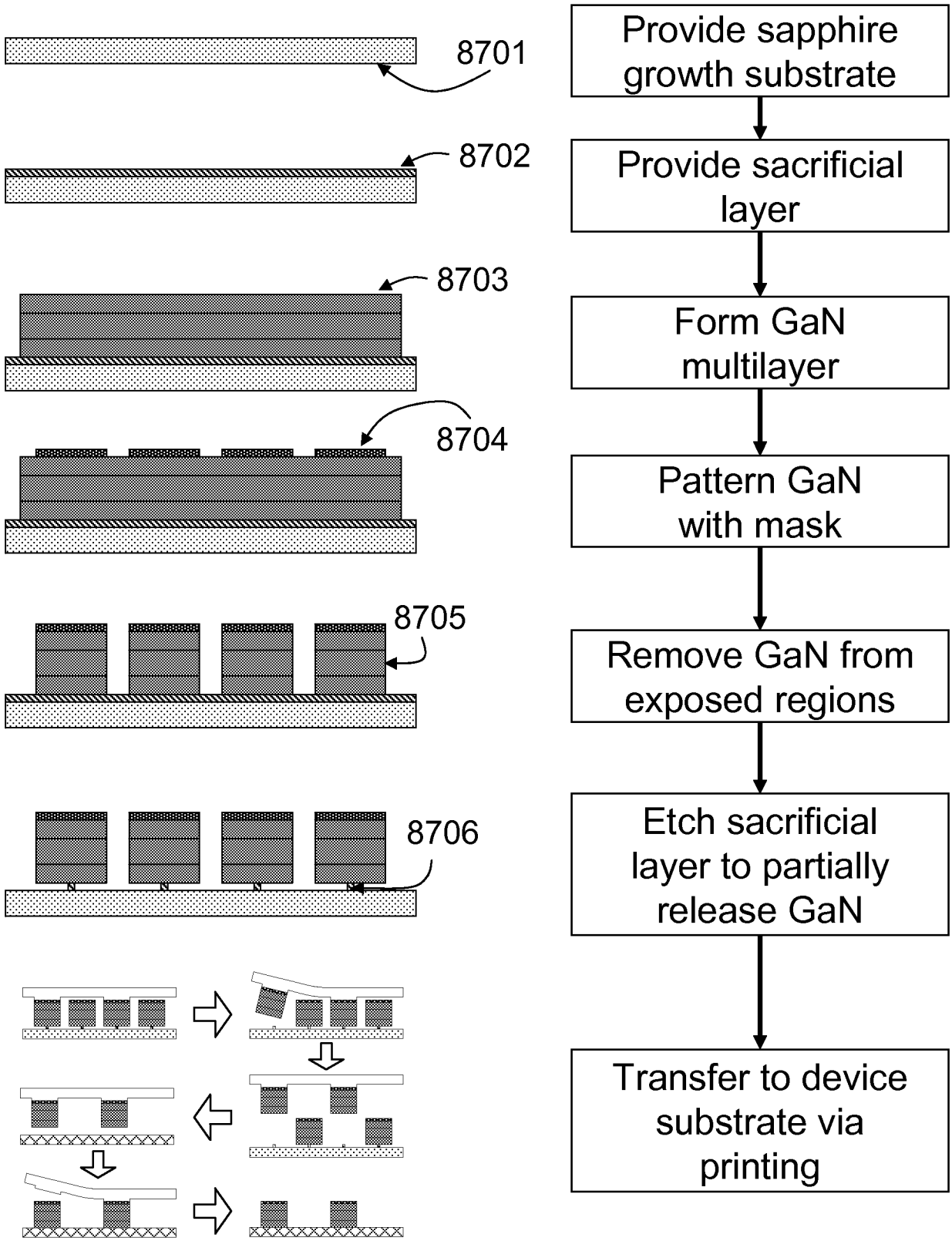

8701
8702
8703
8704
8705
8706
Provide sapphire growth substrate
Provide sacrificial layer
Form GaN multilayer
Pattern GaN with mask
Remove GaN from exposed regions
Etch sacrificial layer to partially release GaN
Transfer to device substrate via printing

Figure 87

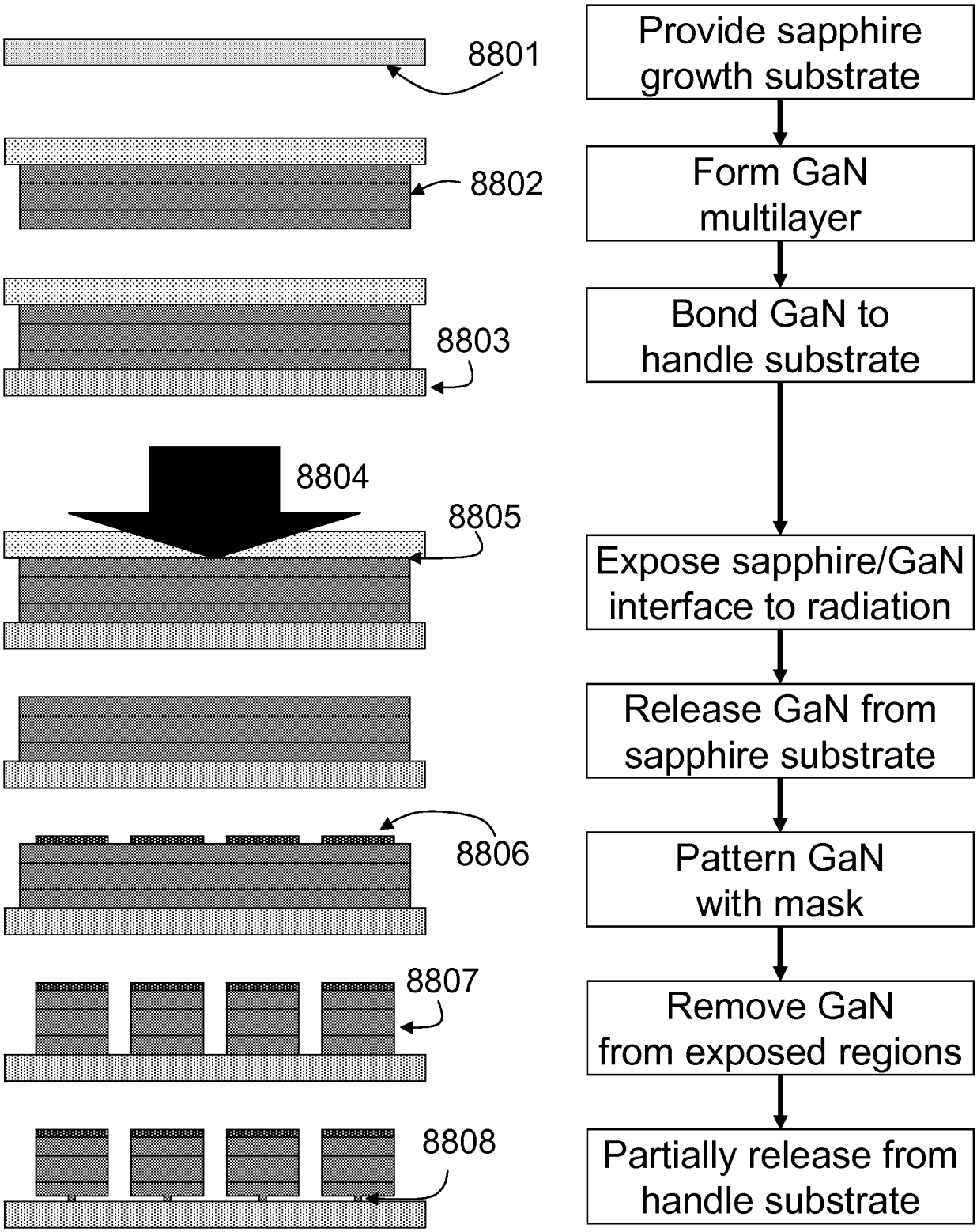

8801
8802
8803
8804
8805
8806
8807
8808
Provide sapphire growth substrate
Form GaN multilayer
Bond GaN to handle substrate
Expose sapphire/GaN interface to radiation
Release GaN from sapphire substrate
Pattern GaN with mask
Remove GaN from exposed regions
Partially release from handle substrate

Figure 88

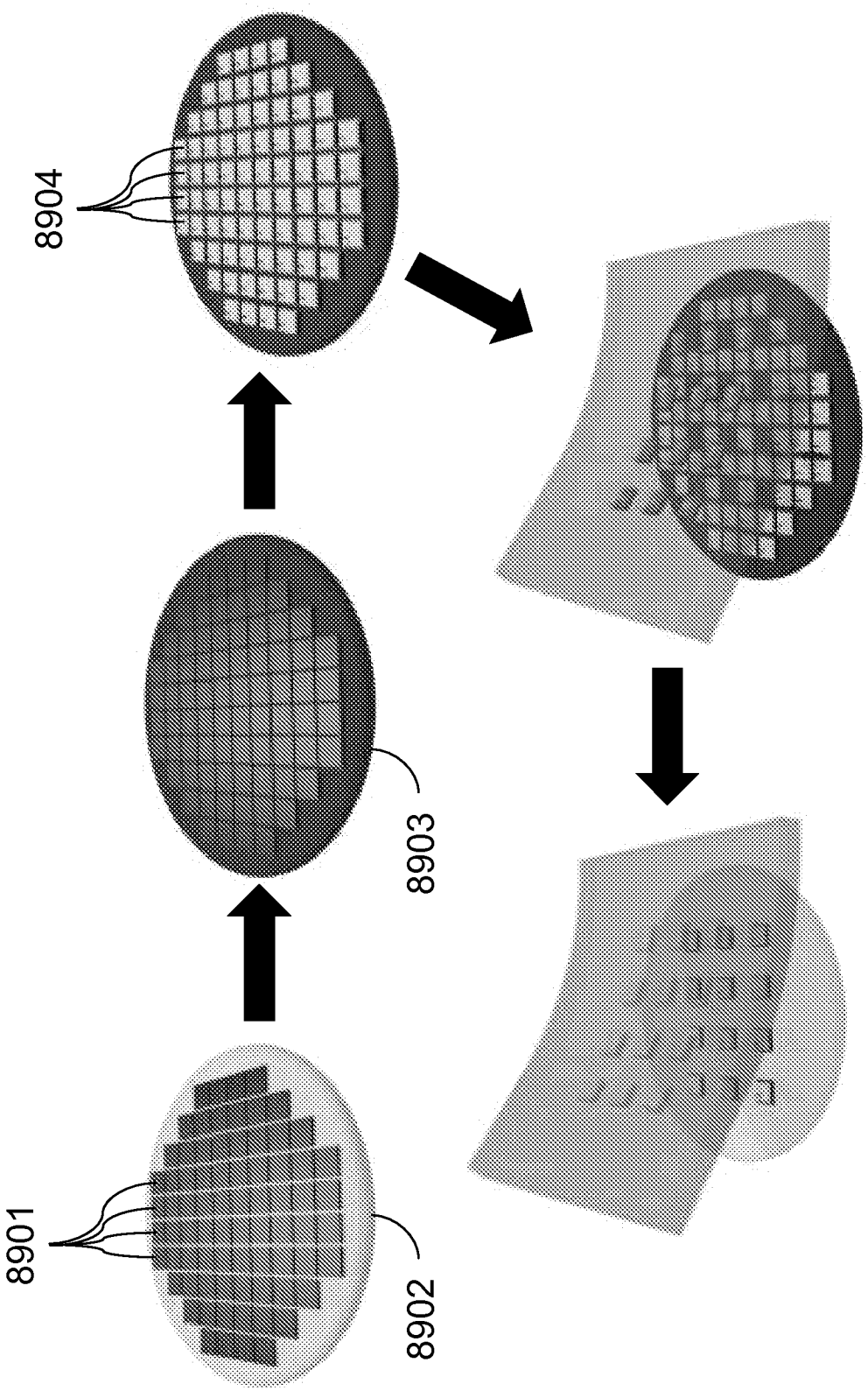


Figure 89

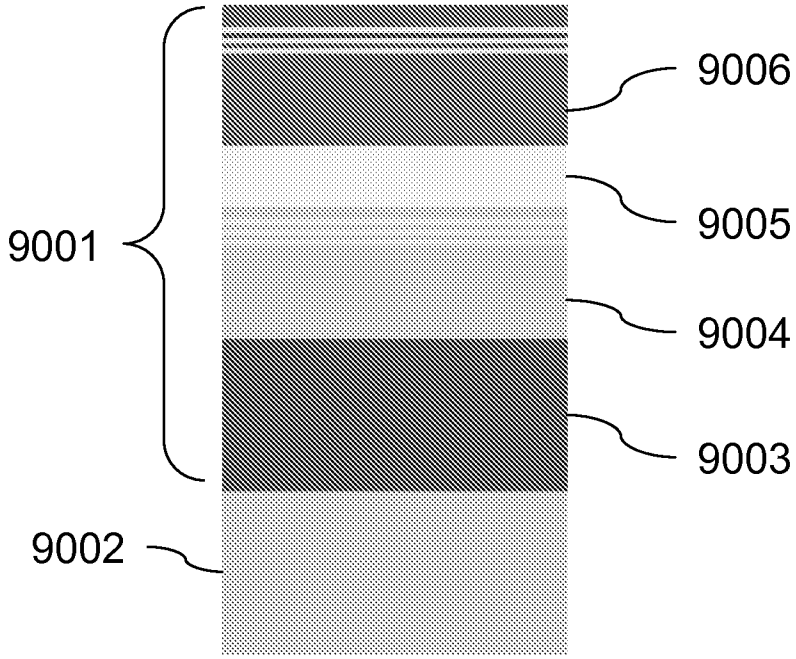


Figure 90A

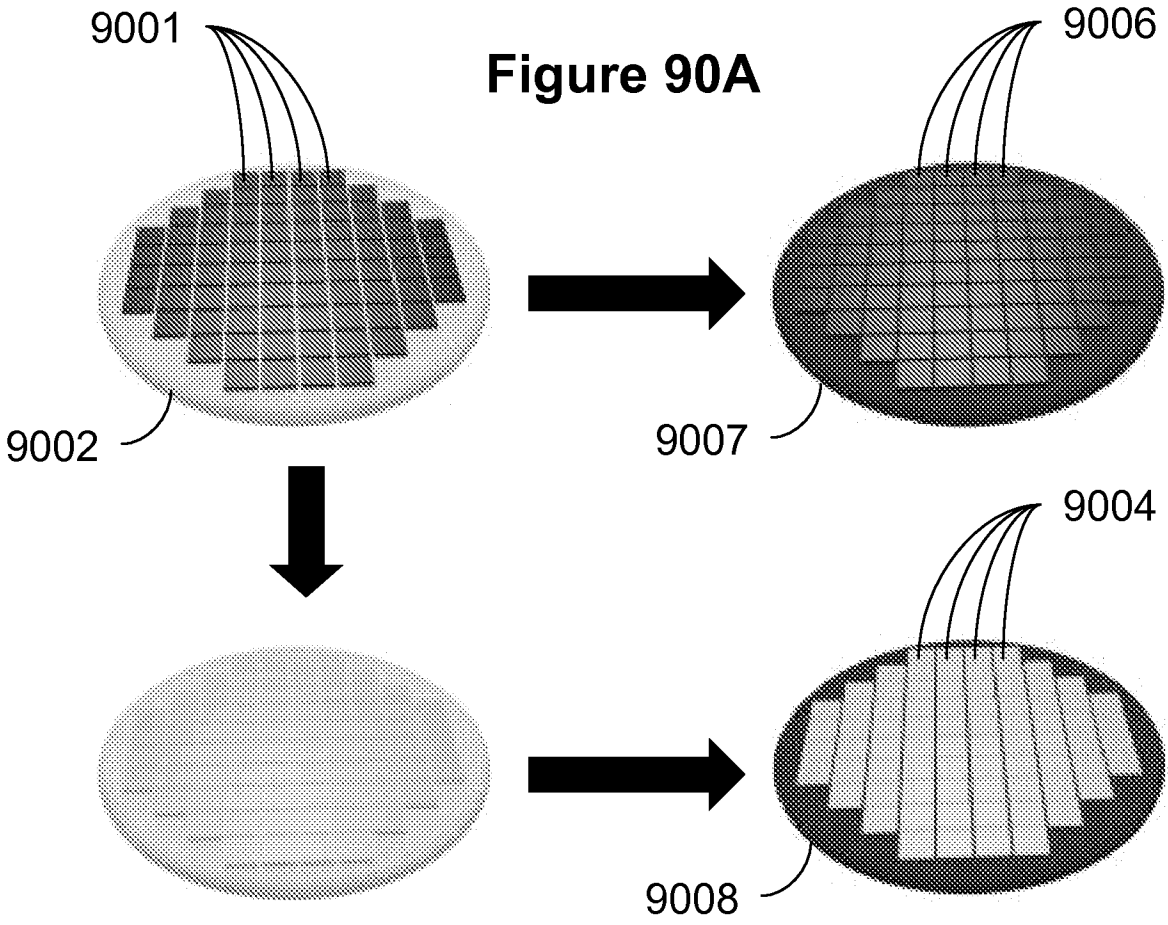


Figure 90B

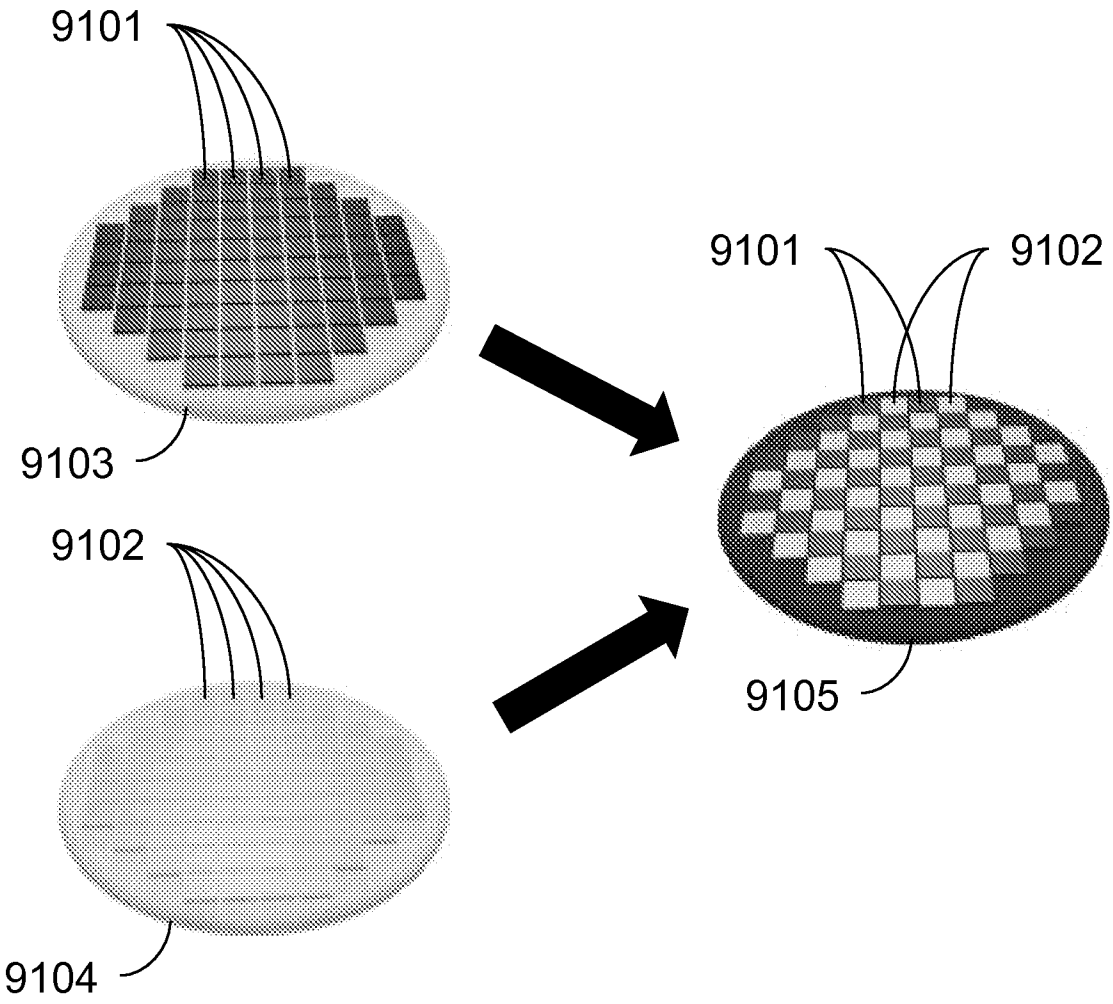


Figure 91

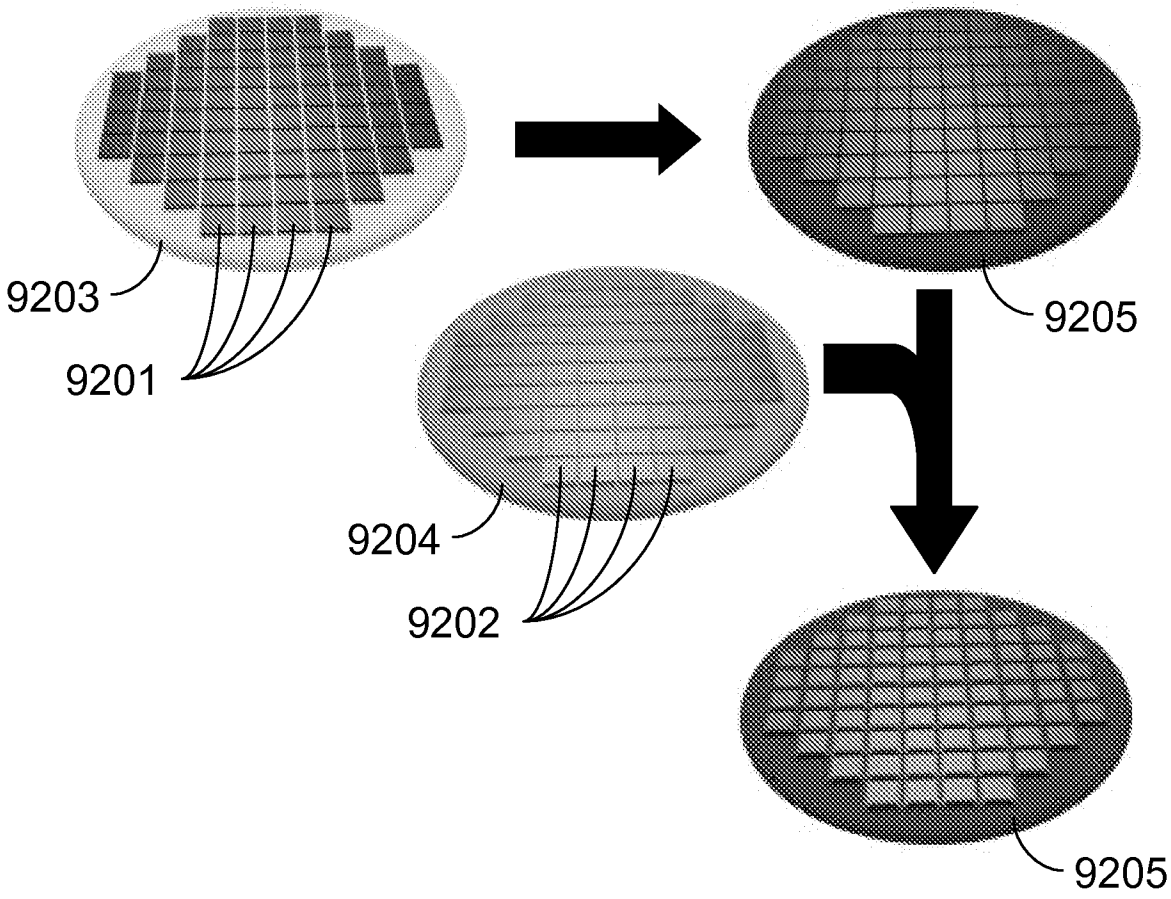


Figure 92A

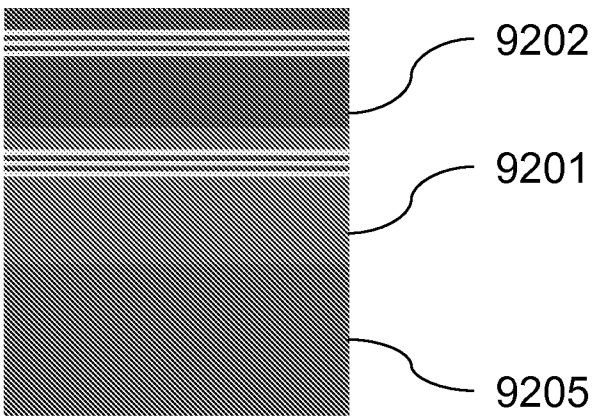


Figure 92B

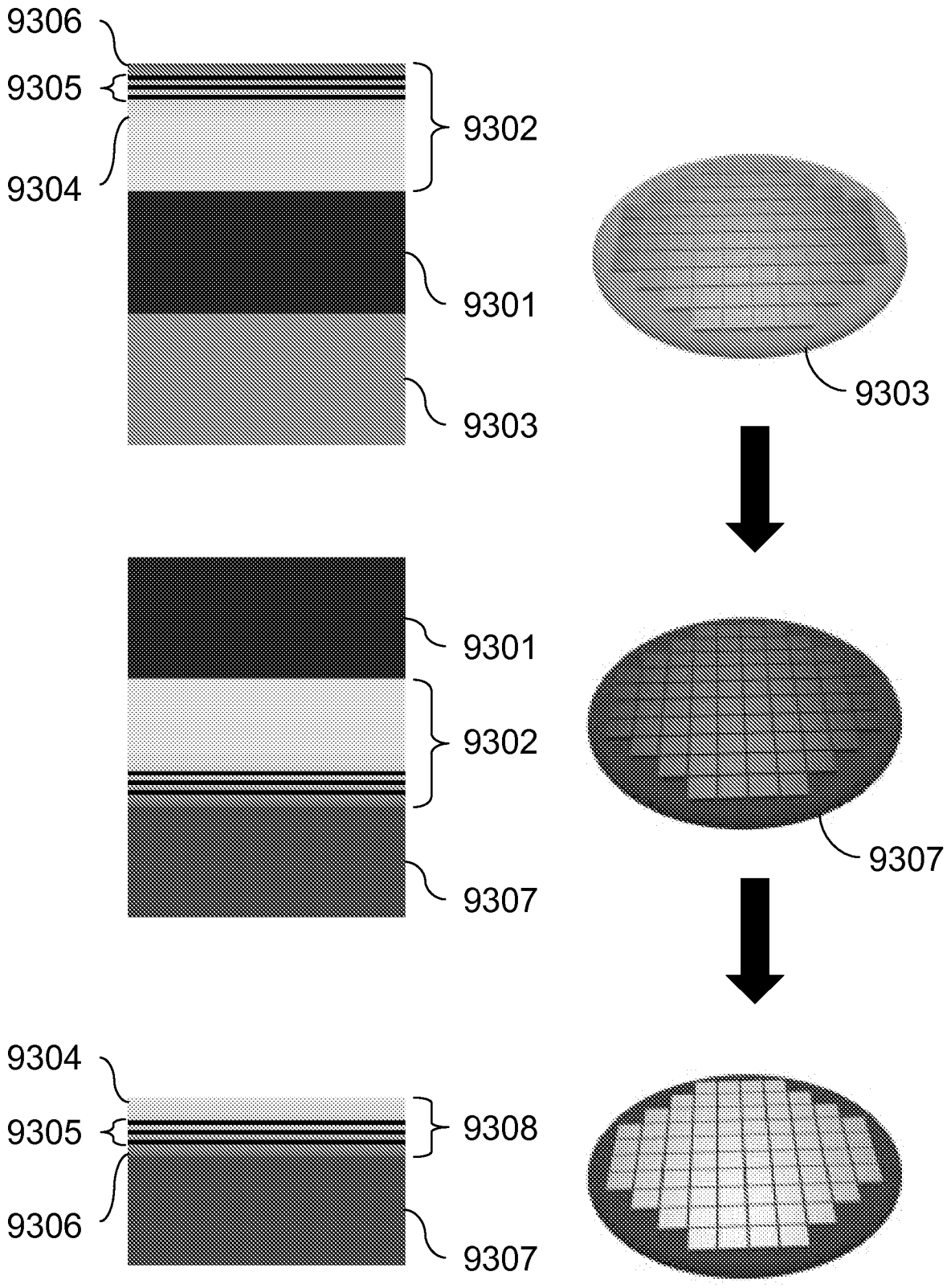

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Figure 93

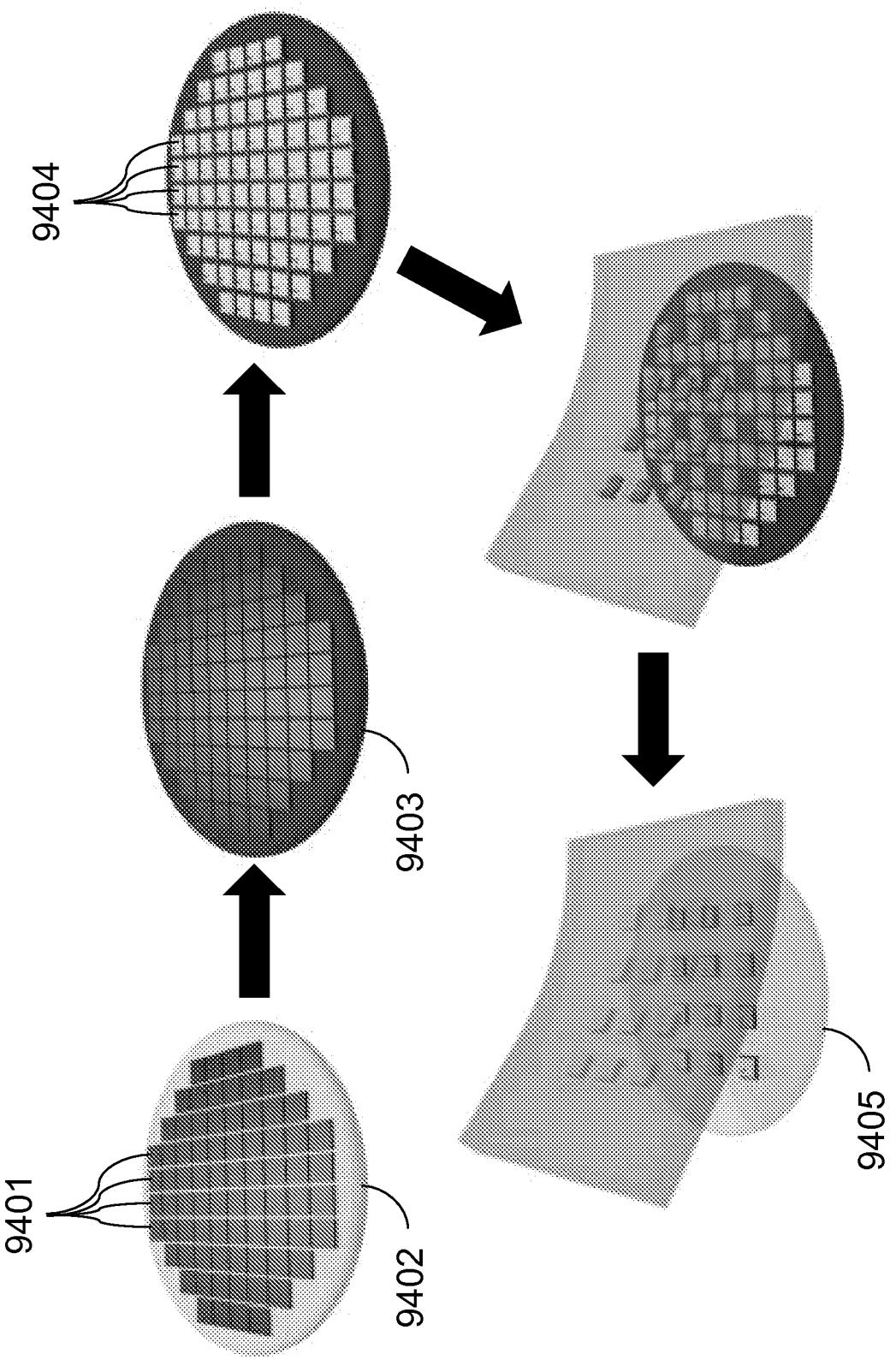


Figure 94

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/034520

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/30 (2010.01)
USPC - 438/455
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 21/30, 21/46, 21/467, 31/18, 33/00 (2010.01)
USPC - 438/455, 458, 459; 257/E21.001, E21.002, E21.017, E21.023, E21.025, E21.034, E33.001

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/0255341 A1 (PINNINGTON et al) 16 November 2006 (16.11.2006) entire document	1-97
Y	US 2008/0108171 A1 (ROGERS et al) 08 May 2008 (08.05.2008) entire document	1-97
A	US 7,195,733 B2 (ROGERS et al) 27 March 2007 (27.03.2007), column 13, lines 7-11; column 33, line 65 to col. 35, line 17; figures 16-18.	1-97
A	US 6,433,401 B1 (CLARK et al) 13 August 2002 (13.08.2002) entire document	1-97

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
31 August 2010	24 SEP 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/034520

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 119
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
See extra sheet.

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-97

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/034520

Continuation of Box III.

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claims 1-97, drawn to a method for forming a semiconductor device by forming an epilayer on a receiving device; bonding the epilayer surface to a handle layer; releasing the epilayer from the growth substrate; patterning and etching the epilayer; and transferring the semiconductor structures to a device substrate via dry transfer contact printing.
Group II, claims 98-114, drawn to a method of making a semiconductor device by providing a transparent substrate; assembling a semiconductor device on a surface of the transparent substrate by dry transfer contact printing, providing and coating metalllic contacts and device with a photosensive layer; exposing portions of the substrate to electromagnetic radiation, where the metallic contacts serve as self-aligned mask elements.
Group III, claims 115-120, drawn to a method for making an array of phosphors comprising molding an elastomer region with an array of recessed regions; providing phosphor particles over the elastomer layer, where the phosphors fill in the recessed regions; providing an encapsulation layer over the elastomer layer to encapsulate the array of phosphors.
Group IV, claims 121-154, drawn to a method of making an electronic device, comprising providing one or more electronic device components; transferring the device components to a conformable transfer and molding device, contacting a prepolymer layer disposed over a host substrate with the conformal transfer and molding device; thereby embedding the electronic device components into the prepolymer layer; patterning the prepolymer layer with one or more recesssed features; curing the prepolymer layer; and filling the recessed features with a filling material selected from the group of: a conductive material, an optical material, a heat transfer material, and any combination of these.

The inventions listed as Groups I, II, III or IV do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the special technical feature of the Group I invention: bonding an epilayer surface to a handle layer; releasing the epilayer from the growth substrate; patterning and etching the epilayer; and transferring the semiconductor structures to a device substrate via dry transfer contact printing as claimed therein is not present in the invention of Groups II, III or IV. The special technical feature of the Group II invention: where the metallic contacts serve as self-aligned mask elements as claimed therein is not present in the invention of Groups I, III or IV. The special technical feature of the Group III invention: providing phosphor particles over the elastomer layer, where the phosphors fill in the recessed regions; providing an encapsulation layer over the elastomer layer to encapsulate the array of phosphors as claimed therein is not present in the invention of Groups I, II or IV. The special technical feature of the Group IV invention: transferring the device components to a conformable transfer and molding device, contacting a prepolymer layer disposed over a host substrate with the conformal transfer and molding device; thereby embedding the electronic device components into the prepolymer layer; patterning the prepolymer layer with one or more recesssed features; curing the prepolymer layer; and filling the recessed features with a filling material selected from the group of: a conductive material; and optical material; a heat transfer material and any combination of these as claimed therein is not present in the invention of Groups I, II or III.

Groups II, II, III and IV lack unity of invention because even though the inventions of these groups require the technical feature of semiconductor package processing, including masking, patterning, etching, dicing and filling recessed areas with conductive material and using dry contact transfer printing, this technical feature is not a special technical feature as it does not make a contribution over the prior art in view of US 7,195,733 B2 (ROGERS et al) 27 March 2007 (27.03.2007), column 13, lines 7-11; column 33, line 65 to col. 35, line 17; figures 16-18.

Since none of the special technical features of the Group I, II, III or IV inventions are found in more than one of the inventions, unity of invention is lacking.