An integrated circuit die including a tight pitch interconnect structure and a method of fabricating a tight pitch interconnect structure is disclosed. The integrated circuit die includes a device layer and an interconnect structure. The interconnect structure includes a via to electrically couple with the device layer to a conductive layer. The interconnect structure includes a plurality of first features having a repeating pattern of feature sizes. The plurality of first features are disposed between a respective one of a plurality of second features. Each of the plurality of first features has a narrower width than the plurality of second features.
Published:

— with international search report (Art. 21(3))
TIGHT PITCH BY ITERATIVE SPACER FORMATION

Background

[0001] Integrated circuits (IC) use interconnect structures to electrically couple devices (e.g., transistors, light-emitting diodes, passive components, etc.) of an integrated circuit or to send and receive signals to the devices of the IC. Conductive materials such as copper or copper alloys may be used for interconnection lines or traces to electrically couple devices to other devices of the IC.

Brief Description of the Drawings

[0002] The present disclosure described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, features illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some features may be exaggerated relative to other features for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0003] **Figure 1** illustrates a fabrication process including first operations for a interconnect structure by iterative spacer formation, according to implementations.

[0004] **Figure 2** illustrates a fabrication process including second operations for a interconnect structure by iterative spacer formation, according to implementations.

[0005] **Figure 3** illustrates a fabrication process including third operations for a interconnect structure by iterative spacer formation, according to implementations.

[0006] **Figure 4** illustrates a fabrication process including fourth operations for a interconnect structure by iterative spacer formation, according to implementations.

[0007] **Figure 5** illustrates a fabrication process including fifth operations for a interconnect structure by iterative spacer formation, according to implementations.

[0008] **Figure 6** illustrates a fabrication process including sixth operations for a interconnect structure by iterative spacer formation, according to implementations.

[0009] **Figure 7** illustrates a fabrication process including seventh operations for a interconnect structure by iterative spacer formation, according to implementations.

[0010] **Figure 8** illustrates a fabrication process including eighth operations for a interconnect structure by iterative spacer formation, according to implementations.

[0011] **Figure 9** illustrates a fabrication process including ninth operations for a interconnect structure by iterative spacer formation, according to implementations.
[0012] **Figure 10** is a flow diagram of a fabrication process for an interconnect structure, according to implementations.

[0013] **Figure 11** illustrates an interposer, according to implementations.

[0014] **Figure 12** is a computing device built in accordance with implementation of the present disclosure.

**Detailed Description**

[0015] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0016] The feature size of integrated circuits (IC) has continued to shrink as performance and cost demands have pushed designers to design integrated circuits with an increasing number of devices per unit area. Semiconductor manufacturing processes are continually developed and employed to enable the manufacture of smaller and smaller features on an IC. A feature may be an element or physical structure of an integrated circuit, such as a transistor channel, via, plug, etc., where the feature size of the element or physical structure is controllable within a tolerance. Feature size may be a physical measurement (e.g., width, length, etc.) of a feature. In implementations, a manufacturing process, such as a semiconductor manufacturing process, may control feature size.

[0017] As the feature size of integrated circuits falls below the sub-micron range, many lithography techniques used for larger feature sizes are not available to effectively produce sub-micron features (e.g. below 50 nanometers (nm)). An additional challenge of manufacturing sub-micron features is to properly align and connect the thousands to billions of features on multiple levels of an IC given manufacturing variation across processes and across a single process.

[0018] For example, as the features size shrinks, pitch also shrinks. Pitch may refer to the sum of the feature size of a feature and the distance between the feature and another adjacent feature. Manufacturing interconnect structures (e.g., including interconnect lines, vias, plugs,
etc.) with smaller pitches presents manufacturing challenges as edge placement margins become smaller. As pitch shrink, misalignment of features such as vias of an interconnect structure, become a greater concern. If a via is misaligned and contacts a wrong metal feature, performance of the IC may be degraded or the IC may fail.

[0019] The present disclosure addresses the above-mentioned and other deficiencies by forming an interconnect structure by iteratively depositing spacers with at least three different materials. The at least three different materials may be alternatingly deposited in a repeating pattern. The different materials may have different etch properties. The different etch properties of the materials allows for greater edge placement margin by allowing a spacer of a particular material to be selectively removed without removing adjacent spacers of different materials. In some implementations, the area created by the removal of the spacer may be used to form a feature, such as a via, plug, or other feature of an interconnect structure.

[0020] It may be noted that for purposes of illustration, rather than limitation, that aspects of the present disclosure describe processes and features of an interconnect structure. It may be noted that aspects of the present disclosure may be applied to features, components, layers, etc. of an IC other than an interconnect structure. For example, processes described herein may be applied for form transistor features (e.g., gate, source, drain, or fin) of a transistor (e.g., bipolar junction transistors (BJT), field effect transistors (FET), such as metal-oxide-semiconductor FET, Fin FET, multiple-gate FET (MuFET) etc.). In other examples, the processes described herein may form features of diodes, light-emitting diodes (LED), or memory cells, among others.

[0021] In implementations, a wafer includes multiple integrated circuit die. In one implementation, an integrated circuit die includes a device layer and an interconnect structure. The interconnect structure includes a via to electrically couple with the device layer to a conductive layer. The interconnect structure includes first features having a repeating pattern of feature sizes. The first features are disposed between a respective one of multiple second features. Each of the first features has a narrower width than the second features.

[0022] In another implementation, the feature size of the repeating pattern of feature sizes has a tolerance of less than or equal to 2 nm. In implementations, the first features have features sizes in a range of 1 nanometer (nm) to 10 nm. In implementations, the second features have feature sizes have features sizes greater than 10 nm.

[0023] In implementations, the IC die includes a conductive layer of the interconnect structure to electrically couple with the device layer through the via. In implementations, the first features includes multiple spacers of a dielectric material. In implementations, the
multiple spacers of the dielectric material have approximately a same feature size having a tolerance of less than or equal to 2 nm.

[0024] In implementations, a wafer includes multiple integrated circuit die. The integrated circuit die includes a device layer and an interconnect structure. The interconnect structure includes a via to electrically couple with the device layer to a conductive layer. The interconnect structure includes first features having a repeating pattern of feature sizes. The first features are disposed between a respective one of multiple second features. Each of the first features has a narrower width than the second features.

[0025] In implementations, a method of fabricating an interconnect structure of an integrated circuit is disclosed. The method includes forming a hardmask layer above a substrate. The method also includes forming multiple spacers above the hardmask layer by iteratively depositing spacers of at least three different materials. At least three different materials are alternately deposited in a repeating pattern. The method includes forming a via of the interconnect structure in an area formed by a selective etch of a spacer of multiple spacers.

[0026] In implementations, the method includes etching the spacer having one of the at least three different materials selectively to form the area for the via without removing adjacent spacers having a material different from the etched spacer. In implementations, the multiple spacers have a repeating pattern including a first spacer of a first material, a second spacer of a second material adjacent the first spacer, a third spacer of a third material adjacent the second spacer, and a fourth spacer of the second material adjacent the third spacer.

[0027] In implementations, forming the via of the interconnect structure includes etching the third spacer of the multiple spacers. The third spacer is selectively etched without removing the first spacer, the second spacer, or the fourth spacer based on different etch properties of the first material, the second material, and the third material. The method also includes forming the via of the interconnect structure in the area formed by the etch of the third spacer of the multiple spacers.

[0028] In implementations, the method includes forming a first backbone structure and a second backbone structure. The multiple spacers are formed between the first backbone structure and the second backbone structure.

[0029] In implementations, the method includes subsequent to forming the multiple spacers, removing the first backbone structure and the second backbone structure. The method also includes forming additional spacers of the plurality of spacers in an area formed by removal of the first backbone structure and the second backbone structure.
[0030] In implementations, the method of forming a plurality of spacers above the hardmask layer includes depositing the plurality of spacers using atomic layer deposition (ALD). In implementations, the method of forming a plurality of spacers above the hardmask layer includes depositing a first material between a first backbone structure and a second backbone structure. The method includes etching the first material to form a first spacer and depositing a second material adjacent the first spacer. The method includes etching the second material to form a second spacer adjacent the first spacer and depositing a third material adjacent the second spacer. The method includes etching the third material to form a third spacer and depositing the second material adjacent the third spacer. The method includes etching the second material adjacent the third spacer to form a fourth spacer.

[0031] In implementations, at least three different materials are dielectric materials with different etch properties. In implementations, the plurality of spacers have feature sizes in a range of 1 nanometer (nm) to 10 nm.

[0032] Figures 1-9 illustrate a fabrication process for a interconnect structure by iterative spacer formation, according to implementations. Fabrication processes 100 through 900 include interconnect structure 110 at various stages of the fabrication process, according to one exemplary implementation. It may be noted that fabrication processes 100-900 are shown for purposes of illustration, rather than limitation. Fabrication processes 100-900 may be performed in any order, include any number of processes, and include additional, the same, or fewer processes. It may also be noted that for purposes of illustration, rather than limitation, materials are described for the various layers or structures illustrated in fabrication processes 100-900. Other materials, other than or in addition to the materials described with respect to Figures 1-9, may also be used in other implementations. It may be noted that for purposes of illustration, rather than limitation, interconnect structure 110 may be part of an integrated circuit die diced from a wafer or be part of a wafer. It may also be noted that the orientation of interconnect structure 110 relative other layers is shown for purposes of illustration, rather than limitation. For example, interconnect structure 110 may be below device layer 118. It may also be noted that a layer (e.g., transfer layer 112, hardmask layer 114, etc.), described herein, may include one or more layers. In implementations, each layer may include the same or different materials as other layers.

[0033] In Figure 1, process 100 shows interconnect structure 110 above device layer 118, according to implementations. Device layer 118 may include one or more devices (D1-D4). As noted above, devices D1-D4 may be any component, active or passive, such as transistors, diodes, LEDs, capacitors, etc. Devices D1-D4 may be part of a substrate or above a substrate
In implementations, the substrate may be a variety of materials, including, but not limited to, Silicon, Gallium Nitride (GaN), Germanium, Sapphire, or Silicon Carbide such as 3C-Silicon Carbide (3C-SiC). In implementations, the substrate may be silicon on insulator (SOI). In implementations, the crystallographic orientation of a substantially monocrystalline substrate may be any of (100), (111), or (110). Other crystallographic orientations are also possible. In implementations, the crystallographic orientations of the substrate may be offcut.

In one implementation, the substrate is (100) silicon with crystalline substrate surface region having cubic crystallinity. In another implementation, for a (100) silicon substrate, the semiconductor surface may be miscut, or offcut, for example 2-10° toward [110]. In another implementation, substrate is (111) silicon with crystalline substrate surface region having hexagonal crystallinity.

[0034] Interconnect structure 110 of process 100 includes transfer layer 112, hardmask layer 114, and backbone 116. It may be noted that interconnect structure 110 may include the same, more, or fewer features or layers or levels in other implementations. It may be noted that backbone 116 may refer to backbone 116A and/or backbone 116B, while reference to backbone 116A may refer only backbone 116A, unless otherwise specified.

[0035] Transfer layer 112 may be deposited or grown above a substrate or device layer 118. Transfer layer 112 may be used to electrically separate an interconnect layer above from a device or interconnect layer below. Transfer layer 112 may be referred to as inter layer dielectric or ILD. Transfer layer materials may include one or more of Silicon Dioxide or Cadmium Oxide (CdO), among others.

[0036] Hardmask layer 114 (also referred to as a "hard mask" or "protective layer" herein) may be formed, deposited, or grown above transfer layer 112. In one exemplary implementation, hardmask layer 114 may be Silicon Nitride (Si$_3$N$_4$). A hard mask layer, such as hardmask layer 114, may be a variety of materials including one or more of Silicon Oxide (SiO$_2$) or Silicon Nitride (Si$_3$N$_4$).

[0037] In one implementation, hardmask layer 114 is a dielectric material. Representative dielectric materials may include, but are not limited to, various Oxides, Nitrides and Carbides, for example, Silicon Oxide, Titanium Oxide, Hafnium Oxide, Aluminum Oxide, Oxynitride, Zirconium Oxide, Hafnium Silicate, Lanthanum Oxide, Silicon Nitride, Boron Nitride, Amorphous Carbon, Silicon Carbide, Amorphous Silicon, or other similar dielectric materials. In one implementation, hardmask layer 114 is deposited, for example, by a plasma deposition process, to a thickness to serve as a mask to transfer layer 112 (e.g., to protect from undesired modification of the underlying layer from energy used in a subsequent process, such as
subsequent mask registration). In one embodiment, a representative thickness of hardmask layer 114 is on the order of 30 angstroms (Å) ± 20 Å. In another embodiment, a representative thickness of hardmask layer 114 is on the order of two to five nanometers (nm). In some implementations, the thickness of hardmask layer 114 may be 5 nm to 15 nm.

[0038] Process 100 illustrates the formation of backbone 116A and backbone 116B above hardmask layer 114. Backbone 116 may also be referred to as "backbone structure" or "mandrel" or "mandrel structure," herein. In implementations, a backbone material may be deposited or grown above the hardmask layer 114 as a conformal layer. Backbone materials include, but are not limited to Polysilicon, Amorphous Silicon, Amorphous Carbon, Silicon Nitride and Germanium. Backbone 116 may offer structural support or scaffolding to create multiple spacers of different material, as described below.

[0039] In implementations, a layer of backbone material may be deposited above hardmask layer 114. A photoresist material may be patterned to define one or more trenches (e.g., trench 120) within the layer of backbone material. The photoresist material may form a pattern over the layer of backbone material that may in turn, be used to form a pattern within the backbone material for the opening of trenches to form backbone 116A and backbone 116B, as illustrated in Figure 1. In implementations, the backbones 116 may be formed using lithography (e.g., 193 nanometer (nm) or extreme ultraviolet lithography (EUV)). Removal of remaining resist or an anti-reflection layer may be performed using ash or wet cleans, for example. The height of backbone 116 may be related to the number of spacers that are to be created using the backbone 116 as a template feature. For instance, for each spacer formed adjacent (to at least one side), an etch process used to form the spacer may remove some portion of backbone 116. With formation of each subsequent spacer, the height of backbone 116 may decrease. A backbone used as a template feature for hundreds of spacers may be taller (at least after formation) than a backbone used as a template feature for tens of spacers (assuming the spacers in both cases are the same relative width). In one implementation, the backbone 116 may be greater than 50 nm in height after formation.

[0040] In Figure 2, process 200 shows the formation of spacers 220A on backbones 116, according to implementations. Spacers 220A are formed using the same spacer material illustrated as material A. The spacer material may be any material. In one implementation, the spacer material may be a dielectric material. Examples of dielectric materials are described at least with respect to hardmask layer 114, above. In other implementations, the spacer material may be a metal, or oxide or nitride of a metal. For example, Titanium Oxide or Titanium Nitride may be used as a spacer material. In other implementations, the spacer material may
be Zirconium Oxide (ZrN), Zirconium Nitride (ZrN), Hafnium Oxide (HfO), Hafnium Nitride (HfN), or Aluminum Oxide (AlOx).

[0041] In some implementations, the spacers 220A may be formed by atomic layer depositions (ALD). ALD may be used to control the deposit of materials at the atomic level by depositing a single layer of atoms at a time. ALD may deposit spacers 220A with a feature size (e.g., width 221) in the range of 1 nm to 10 nm with a tolerance of less than or equal to 2 nm. It may be noted that spacers wider than 10 nm may be formed using ALD or other processing technique. Subsequent to depositing the spacer material using ALD, the hardmask layer 114 may be etched (e.g., anisotropic etch) to remove any superfluous spacer material from hardmask layer 114 and prepare hardmask layer 114 for subsequent spacer formation. It may be appreciated that other or additional techniques may be implemented to form spacers, such as spacers 220A. In one implementation, spacers 220A may be formed using selective growth techniques or directed self-assembly (DSA), for example.

[0042] In Figure 3, process 300 illustrates the iterative deposition of spacers using at least three different materials, according to an implementation. In an implementation, the spacer material of each of spacers 220A, 320B, and 320C, may be one or more of the materials described with respect to Figure 2. It may be noted that the use of a letter with spacer numbers (e.g., spacers 220A, 320B, and 320C) is provided to help identify the different spacer material associated with each spacer. For example, spacers 220A use material A, spacers 320B use material B, and spacers 320C use material C. In an implementation, material A, B, and C are different materials from one another having different etch properties. It may be noted that forming spacers using different three materials is provided for purposes of illustration, rather than limitation. In other implementations, any number of spacer materials may be used. For example, forming spacers with four or more spacer materials may be implemented.

[0043] In implementations, the different spacer materials may have different etch properties. Etch properties may refer to a property (e.g., etch rate) or response of a material to a particular etch process. In one example, different etch properties may refer to the etch rate of the target material compared to the etch rate of other materials exposed to an etch process having a high ratio (e.g., high etch selectivity). In some implementations, etch selectivity may from 3 to 1 rates, to 1000 to 1 rates. In implementations, spacers with different etch properties may be exposed to an etch process to remove a spacer with one etch property without removing spacers having different etch properties (at least not enough to materially affect the remaining spacers).
In implementations, using spacers of different materials with different etch properties allows for the removal of a particular spacer without removing neighboring spacers with different etch properties. In implementations having features with tight pitch (e.g., 40 nm or below), the additional margin for error granted by the use of spacers of different materials allows for the manufacture of an IC with smaller features sizes and greater reliability.

In implementations, spacers 220A, 320B, and 320C having different materials are alternately deposited using repeating patterns. For example, the pattern may include the repetition of the following group of spacers: material A of spacer may be deposited, followed by material B of spacers 320B, followed by material C of spacers 320C, followed by material B of spacers 320B. It may be noted that any pattern using three or more materials may be implemented.

As illustrated by process 300, multiple spacers are formed on both sides of backbone 116. In an implementation, the spacers having different materials may be formed using multiple processes. For example, spacers 220A are formed on both sides of backbone 116, followed by the formation of spacers 320B on both sides of backbone 116, and so forth. In an implementation, one or more of spacers 220A, 320B, and 320C may have a feature size in the range of 1 nm to 10 nm with a tolerance of less than or equal to 2 nm. In implementations, all the spacers 220A may have the same features size (e.g. width) within a tolerance (e.g., 1 nm), all the spacers 320B may have the same features sizes within a tolerance, and all the spacers 320C have the same feature sizes within a tolerance. In implementations, the spacers 230A, 320B, and 320C may have the same or different feature sizes.

In Figure 4, process 400 illustrates the iterative deposition of additional spacers using at least three different materials, according to an implementation. As noted above, the pattern of spacers with different material is repeated. In implementations, the number of spacers between backbone 116 may be from 6 to hundreds, depending on the application. It may be noted (and as illustrated) that with each successive etch of a spacer, the height of the backbone 116 is reduce and a subsequently deposited spacer is shorter than previously deposited spacers.

In Figure 5, process 500 illustrates the removal of backbone 116, according to an implementation. In one implementation, the removal of backbone 116 facilitates additional area for feature generation. In an implementation, backbone 116 may be selectively etched leaving spacers 220A, 320B, and 320C. In another implementation, backbone 116 not be removed. In an implementation, backbone 116 uses a backbone material with different etch properties than spacers 220A, 320B, and 320C.
In Figure 6, process 600 illustrates forming additional spacers in an area created by the removal of backbone 116. In implementation, the area formed by the removal of backbone 116 may be used to form spacers with narrower feature sizes (e.g., Inm-10nm width) or spacers with larger feature sizes, respectively (e.g., greater than 10 nm shown by width 621). As illustrated, the spacers with narrower features sizes are buffered by spacers with larger feature sizes, respectively. The additional spacers may be formed similarly as described above.

In Figure 7, process 700 illustrates a planarization process to smooth the surface of the interconnect structure 110. The planarization process may include any planarization process, such as chemical-mechanical planarization (CMP).

In Figure 8, process 800 illustrates formation of vias 822 and other features by the selective removal of spacers of a particular type of material, according to an implementation. A via, such as via 822, may be made of a conductive material and connect components on one plane to components on a different plane. In one implementation, spacers 220A of material A may be selectively removed without removing spacers 320B and 320C made from a different material than spacers 220A. The area created by the removal of the spacers 220A may be filled with any material, such as a conductive material (e.g., material D). Conductive material may be any material capable of conduction including metals, such as Copper, Aluminum, Tungsten, or metal alloys. As illustrated, via 822 made of a conductive material may be made to a plane below (or above) interconnect structure 110. In some implementations, the areas formed by the selective removal of spacers 220A may be filled with a conductive material without forming a via (e.g., feature 830). In implementations, feature 830 may be a vertical interconnect line of interconnect structure 110 to connect interconnect structure 110 to layers above (e.g., other interconnect layers of interconnect structure 110). For example, feature 830 may be used to connect to a conductive layer (not shown) (e.g., metal layer) above interconnect structure 110. In some implementations, feature 830 may be used to connect layers above interconnect structure 110 to a conductive layer (not shown) embedding in interconnect structure 110. In some implementations, subsequent to filling the areas with conductive material, a hardmask material (e.g., dielectric material as described above) (e.g., material E) may be used to cap the conductive material (e.g., material D). In some implementations, a dielectric material (e.g., material E) of hardmask 821 may be selected to be different than the adjacent material of spacers 320B and 320C (e.g., and have different etch properties) to facilitate connecting a via or other feature from a layer above interconnect structure 110 with greater edge placement margin, as described above. In other
implementations, material E of hardmask 821 may be the same material as spacers 320B (e.g., material B) or spacers 320C (e.g., material C).

[0052] In Figure 9, process 900 illustrates an integrated circuit including a device layer 118 and an interconnect structure 110. In implementations, interconnect structure 110 may connect device layer 118 to a conductive layer (e.g., horizontal metal layer including interconnect lines) (not shown) located above interconnect structure 110 or to additional layers (not shown) of interconnect structure 110.

[0053] In implementation, spacers 320C of material C are selectively removed without removing spacers 320B and hardmask 821 made from different materials than spacers 320C. The area created by the removal of the spacers 320C may be filled with any material, such as a conductive material (e.g., material F). In implementations, material F may be the same conductive material as material D. In other implementations, material F may be a different conductive material than material D. As illustrated, vias 922 made of a conductive material (material F) may be made to a plane below the interconnect structure 110 to connect to devices of device layer 118.

[0054] In some implementations, the areas formed by the selective removal of spacers 320C may be filled with a conductive material (material F) without forming a via (e.g., feature 950). In some implementations, subsequent to filling the areas formed by the removal of spacers 320C with conductive material (material F), a hardmask material (material G) for hardmask 921 may be used to cap the conductive material (e.g., material F). In some implementations, a dielectric material (material G) of hardmask 821 may be selected to be different than the adjacent material of spacers 320B and hardmask 821 (material E) (e.g., and have different etch properties) to facilitate connecting a via or other feature to a layer above with greater edge placement margin, as described above. In other implementations, material F of hardmask 921 may be the same material as spacers 320B (e.g., material B) or hardmask 821 (e.g., material E).

[0055] In implementations, areas formed by the removal of spacers 320C (or spacers 220A) may be filled with different materials from one another. In one example, a non-conductive (or low-conducting) material may be used to form a plug, such as plugs 923. An example of non-conductive materials includes Silicon Nitride or Silicon Dioxide, among others. Pitch 924 illustrates example of a tight pitch, in accordance with implementations. In some implementations, the pitch 924 may be in the range of 1 nm to 20 nm with a tolerance of +/-2 nm. Tolerance herein may refer to plus or minus (+) a given value, unless otherwise described.
[0056] It may be noted that narrower features, such as feature 945, may be positioned between wider features, illustrated by feature 943 and 944. In some examples, the narrower features such feature 945, may be 1-10 nm wide. Wider features, such as feature 943 and 944, may be greater than 10nm wide.

[0057] Figure 10 is a flow diagram of a fabrication process for forming a interconnect structure, according to an implementation. It may be noted that elements of Figures 1-9 may be described below to help illustrate method 1000. Method 1000 may be performed as one or more operations. It may be noted that method 1000 may be performed in any order and may include the same, more, or fewer operations. It may be noted that method 1000 may be performed by one or more pieces of semiconductor fabrication equipment or fabrication tools.

[0058] Method 1000 begins at operation 1005 by forming a hardmask layer above a substrate. At operation 1010, a first backbone structure and a second backbone structure are formed. At operation 1015, multiple spacers are formed above the hardmask layer by iteratively depositing spacers of at least three different materials. At least three different materials are alternatingly deposited in a repeating pattern to form the spacers. At operation 1020, subsequent to forming the plurality of spacers, the first backbone structure and the second backbone structure are removed. At operation 1025, additional spacers are formed in an area formed by removal of the first backbone structure and the second backbone structure. At operation 1030, a spacer having one of the at least three different materials is selectively etched to form the area for the via without removing adjacent spacers having a material different than the etched spacer. At operation 1035, a via of the interconnect structure is formed in an area formed by a selective etch of a spacer of the plurality of spacers.

[0059] Figure 11 illustrates an interposer, according to implementations. The interposer 1100 may be an intervening substrate used to bridge a first substrate 1102 to a second substrate 1104. The first substrate 1102 may be, for instance, an integrated circuit die, including interconnect structure 110. The second substrate 1104 may be, for instance, a memory module, a computer motherboard, backplane, or another integrated circuit die. In one implementation, first substrate 1102 may be an integrated circuit die described with respect to Figure 1-9. Generally, the purpose of an interposer 1100 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1100 may couple an integrated circuit die to a ball grid array (BGA) 1106 that can subsequently be coupled to the second substrate 1104. In some implementations, the first and second substrates 1102/1104 are attached to opposing sides of the interposer 1100. In other implementations, the first and second substrates 1102/1104 are attached to the same side of
the interposer 1100. In further implementations, three or more substrates are interconnected by way of the interposer 1100.

[0060] The interposer 1100 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0061] The interposer may include metal interconnects 1108 and vias 1110, including but not limited to through-silicon vias (TSVs) 1112. The interposer 1100 may further include embedded devices 1114, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1100. In accordance with one or more implementations, apparatuases or processes disclosed herein may be used in the fabrication of interposer 1100.

[0062] Figure 12 is a computing device built in accordance with implementations of the present disclosure. The computing device 1200 may include a number of components. In one implementation, the components are attached to one or more motherboards. In an alternate implementation, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die, such as an SoC used for mobile devices. In implementations, the components in the computing device 1200 include, but are not limited to, an integrated circuit die 1202 and at least one communications logic unit 1208. In some implementations the communications logic unit 1208 is fabricated within the integrated circuit die 1202 while in other implementations the communications logic unit 1208 is fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the integrated circuit die 1202. The integrated circuit die 1202 may include a CPU 1204 as well as on-die memory 1206, often used as cache memory that can be provided by technologies such as embedded DRAM (eDRAM), SRAM, or spin-transfer torque memory (STT-MRAM). It may be noted that in implementations integrated circuit die 1202 may include fewer elements (e.g., without processor 1204 and/or on-die memory 1206) or additional elements other than processor 1204 and on-die memory 1206. In one example, integrated circuit die 1202 may include in interconnect structure 110 as described herein. In
another example, integrated circuit die 1202 may include some or all the elements described herein, as well as include additional elements.

[0063] Computing device 1200 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1210 (e.g., DRAM), non-volatile memory 1212 (e.g., ROM or flash memory), a graphics processing unit 1214 (GPU), a digital signal processor 1216, a crypto processor 1242 (e.g., a specialized processor that executes cryptographic algorithms within hardware), a chipset 1220, at least one antenna 1222 (in some implementations two or more antenna may be used), a display or a touchscreen display 1224 (e.g., that may include integrated circuit die 1202), a touchscreen controller 1226, a battery 1228 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 1227, a compass (not shown), a motion coprocessor or sensors 1232 (that may include an accelerometer, a gyroscope, and a compass), a microphone (not shown), a speaker 1234, a camera 1236, user input devices 1238 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1240 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). The computing device 1200 may incorporate further transmission, telecommunication, or radio functionality not already described herein. In some implementations, the computing device 1200 includes a radio that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space. In further implementations, the computing device 1200 includes a transmitter and a receiver (or a transceiver) that is used to communicate over a distance by modulating and radiating electromagnetic waves in air or space.

[0064] The communications logic unit 1208 enables wireless communications for the transfer of data to and from the computing device 1200. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some implementations they might not. The communications logic unit 1208 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Infrared (IR), Near Field Communication (NFC), Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G,
and beyond. The computing device 1200 may include a plurality of communications logic units 1208. For instance, a first communications logic unit 1208 may be dedicated to shorter range wireless communications such as Wi-Fi, NFC, and Bluetooth and a second communications logic unit 1208 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1204 (also referred to "processing device" herein) of the computing device 1200 includes one or more devices, such as transistors, RF filters, or LEDs, that are formed in accordance with implementations of the present disclosure. The term "processor" or "processing device" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. Processor 1204 represents one or more general-purpose processing devices such as a microprocessor, a central processing unit, or the like. More particularly, the processor 1204 may be complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, or processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 1204 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like.

The communications logic unit 1208 may also include one or more devices, such as transistors, RF filters, or LEDs, that are formed in accordance with implementations of the present disclosure.

In further implementations, another component housed within the computing device 1200 may contain one or more devices, such as transistors, RF filters, or LEDs, that are formed in accordance with implementations of the present disclosure.

In various implementations, the computing device 1200 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a dumbphone, a tablet, a tablet/laptop hybrid, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1200 may be any other electronic device that processes data.

The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the
precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0070] Various operations are described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0071] The terms "over," "above" "under," "between," and "on" as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed above or over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0072] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to Germanium, Indium Antimonide, Lead Telluride, Indium Arsenide, Indium Phosphide, Gallium Arsenide, Indium Gallium Arsenide, Gallium Antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0073] A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein
may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

[0074] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO$_2$) and/or a high-k dielectric material. The high-k dielectric material may include elements such as Hafnium, Silicon, Oxygen, Titanium, Tantalum, Lanthanum, Aluminum, Zirconium, Barium, Strontium, Yttrium, Lead, Scandium, Niobium, and Zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, Hafnium Oxide, Hafnium Silicon Oxide, Lanthanum Oxide, Lanthanum Aluminum Oxide, Zirconium Oxide, Zirconium Silicon Oxide, Tantalum Oxide, Titanium Oxide, Barium Strontium Titanate Oxide, Barium Titanate Oxide, Strontium Titanate Oxide, Yttrium Oxide, Aluminum Oxide, Lead Scandium Tantalum Oxide, and Lead Zinc Niobate. In some implementations, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0075] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0076] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, Ruthenium, Palladium, Platinum, Cobalt, Nickel, and conductive metal oxides, e.g., Ruthenium Oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, Hafnium, Zirconium, Titanium, Tantalum, Aluminum, alloys of these metals, and carbides of these metals such as Hafnium Carbide, Zirconium Carbide, Titanium Carbide, Tantalum Carbide, and Aluminum Carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0077] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two
sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0078] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as Silicon Nitride, Silicon Oxide, Silicon Carbide, Silicon Nitride doped with Carbon, and Silicon Oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process operations. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0079] In implementations, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions may be formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as Boron, Aluminum, Antimony, Phosphorus, or Arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a Silicon alloy such as Silicon Germanium or Silicon Carbide. In some implementations, the epitaxially deposited silicon alloy may be doped in situ with dopants such as Boron, Arsenic, or Phosphorus. In further implementations, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. In further implementations, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0080] In other implementations, one or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their
applicability in integrated circuit structures, such as low-k dielectric materials. Examples of
dielectric materials that may be used include, but are not limited to, Silicon Dioxide (SiO$_2$). Carbon doped oxide (CDO), Silicon Nitride, organic polymers such as Perfluorocyclobutane or Polytetrafluoroethylene, Fluorosilicate glass (FSG), and organosilicates such as Silsesquioxane, Siloxane, or Organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0081] The words "example" or "exemplary" are used herein to mean serving as an example, instance, or illustration. Any aspect or design described herein as "example" or "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects or designs. Rather, use of the words "example" or "exemplary" is intended to present concepts in a concrete fashion. As used in this application, the term "or" is intended to mean an inclusive "or" rather than an exclusive "or." That is, unless specified otherwise, or clear from context, "X includes A or B" is intended to mean any of the natural inclusive permutations. That is, if X includes A; X includes B; or X includes both A and B, then "X includes A or B" is satisfied under any of the foregoing instances. In addition, the articles "a" and "an" as used in this application and the appended claims may generally be construed to mean "one or more" unless specified otherwise or clear from context to be directed to a singular form. Moreover, use of the term "an implementation" or "one implementation" or "an implementation" or "one implementation" throughout is not intended to mean the same implementation or implementation unless described as such. The terms "first," "second," "third," "fourth," etc. as used herein are meant as labels to distinguish among different elements and may not necessarily have an ordinal meaning according to their numerical designation.
What is claimed is:

1. An integrated circuit die comprising:
   a device layer; and
   an interconnect structure comprising a via to electrically couple with the device layer to a conductive layer, wherein the interconnect structure comprises a plurality of first features having a repeating pattern of feature sizes, and wherein the plurality of first features are located between a respective one of a plurality of second features, wherein each of the plurality of first features has a narrower width than the plurality of second features.

2. The integrated circuit die of claim 1, wherein a feature size of the repeating pattern of feature sizes has a tolerance of less than 2 nanometers.

3. The integrated circuit die of claim 1, wherein the plurality of first features have feature sizes in a range of 1 nanometer (nm) to 10 nm.

4. The integrated circuit die of claim 1, wherein the plurality of second features have feature sizes greater than 10 nm.

5. The integrated circuit die of claim 1, comprising:
   a conductive layer of the interconnect structure to electrically couple with the device layer through the via.

6. The integrated circuit die of claim 1, wherein the plurality of first features comprises a plurality of spacers of a dielectric material.

7. The integrated circuit die of claim 6, wherein the plurality of spacers of the dielectric material have approximately a same feature size having a tolerance of less than 2 nm.

8. A computing device comprising:
   a device layer; and
   an interconnect structure comprising a via to electrically couple with the device layer to a conductive layer, wherein the interconnect structure comprises a plurality of first features having
a repeating pattern of feature sizes, and wherein the plurality of first features are located between a respective one of a plurality of second features, wherein each of the plurality of first features has a narrower width than the plurality of second features.

9. The computing device of claim 8, wherein the plurality of first features have feature sizes in a range of 1 nanometer (nm) to 10 nm.

10. The computing device of claim 8, wherein the plurality of second features have feature sizes greater than 10 nm.

11. A method of fabricating an interconnect structure of an integrated circuit comprising:
    forming a hardmask layer above a substrate;
    forming a plurality of spacers above the hardmask layer by iteratively depositing spacers of at least three different materials, wherein the at least three different materials are alternatingly deposited in a repeating pattern; and
    forming a via of the interconnect structure in an area formed by a selective etch of a spacer of the plurality of spacers.

12. The method of claim 11, further comprising
    etching the spacer having one of the at least three different materials selectively to form the area for the via without removing adjacent spacers having a material different from the etched spacer.

13. The method of claim 11, wherein the plurality of spacers have a repeating pattern comprising a first spacer of a first material, a second spacer of a second material adjacent the first spacer, a third spacer of a third material adjacent the second spacer, and a fourth spacer of the second material adjacent the third spacer.

14. The method of claim 13, wherein forming the via of the interconnect structure comprises:
    etching the third spacer of the plurality of spacers, wherein the third spacer is selectively etched without removing the first spacer, the second spacer, or the fourth spacer based on different etch properties of the first material, the second material, and the third material; and
    forming the via of the interconnect structure in the area formed by the etch of the third spacer of the plurality of spacers.
15. The method of claim 11, further comprising:
   forming a first backbone structure and a second backbone structure, wherein the plurality of spacers are formed between the first backbone structure and the second backbone structure.

16. The method of claim 15, further comprising:
   subsequent to forming the plurality of spacers, removing the first backbone structure and the second backbone structure; and
   forming additional spacers of the plurality of spacers in an area formed by removal of the first backbone structure and the second backbone structure.

17. The method of claim 11, wherein forming a plurality of spacers above the hardmask layer comprises:
   depositing the plurality of spacers using atomic layer deposition (ALD).

18. The method of claim 11, wherein forming a plurality of spacers above the hardmask layer comprises:
   depositing a first material between a first backbone structure and a second backbone structure;
   etching the first material to form a first spacer;
   depositing a second material adjacent the first spacer;
   etching the second material to form a second spacer adjacent the first spacer;
   depositing a third material adjacent the second spacer;
   etching the third material to form a third spacer;
   depositing the second material adjacent the third spacer; and
   etching the second material adjacent the third spacer to form a fourth spacer.

19. The method of claim 11, wherein the at least three different materials are dielectric materials with different etch properties.

20. The method of claim 11, wherein the plurality of spacers have feature sizes in a range of 1 nanometer (nm) to 10 nm.
START

Form a hardmask layer above a substrate 1005

Form a first backbone structure and a second backbone structure 1010

Form a plurality of spacers above the hardmask layer by iteratively depositing spacers of at least three different materials 1015

Remove the first backbone structure and the second backbone structure 1020

Form additional spacers of the plurality of spacers in an area formed by removal of the first backbone structure and the second backbone structure 1025

Etch the spacer having one of the at least three different materials selectively to form the area for the via without removing adjacent spacers having a material different than the etched spacer 1030

Form a via of the interconnect structure in an area formed by a selective etch of a spacer of the plurality of spacers 1035

END

FIG. 10
A. CLASSIFICATION OF SUBJECT MATTER

HOIL 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

HOIL 21/768; HOIL 21/308; HOIL 21/28; HOIL 23/48; HOIL 21/033; H01L 29/772; H01L 29/06; H01L 23/522

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS (KIPO internal) & Keywords: interconnect, via, feature, pattern

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>US 2015-0194341 Al (MICRON TECHNOLOGY, INC.) 09 July 2015 See paragraphs [0025]-[0063] and figures 1A-6B.</td>
<td>1-20</td>
</tr>
<tr>
<td>A</td>
<td>US 2015-0371852 Al (APPLIED MATERIALS, INC.) 24 December 2015 See paragraphs [0020]-[0049] and figures 1A-4.</td>
<td>1-20</td>
</tr>
<tr>
<td>A</td>
<td>US 2016-0329280 Al (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 10 November 2016 See paragraphs [0009]-[0020] and figures 1-8.</td>
<td>1-20</td>
</tr>
<tr>
<td>A</td>
<td>US 2013-0134486 Al (NICHOLAS V. LICAUSI) 30 May 2013 See paragraphs [0019H0027] and figures 2A-2J.</td>
<td>1-20</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C.

See patent family annex.

Date of the actual completion of the international search
27 September 2017 (27.09.2017)

Date of mailing of the international search report
28 September 2017 (28.09.2017)

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheonja-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
CHOI, Sang Won
Telephone No. +82-42-481-8291

Form PCT/ISA/210 (second sheet) (January 2015)
<table>
<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>kr 10-2009-0126588 A</td>
<td>09/12/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 2009-0305495 Al</td>
<td>10/12/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 7968447 B2</td>
<td>28/06/2011</td>
</tr>
<tr>
<td>US 2015-0194341 Al</td>
<td>09/07/2015</td>
<td>cn 101772832 A</td>
<td>07/07/2010</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cn 101772832 B</td>
<td>08/04/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>jp 2010-536176 A</td>
<td>25/11/2010</td>
</tr>
<tr>
<td></td>
<td></td>
<td>kr 10-2010-0049085 A</td>
<td>11/05/2010</td>
</tr>
<tr>
<td></td>
<td></td>
<td>kr 10-2012-0081253 A</td>
<td>18/07/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>sg 183671 Al</td>
<td>27/09/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>tw 200926262 A</td>
<td>16/06/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>tw 1471905 B</td>
<td>01/02/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>tw 1503863 B</td>
<td>11/10/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 2009-0032963 Al</td>
<td>05/02/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 2011-0285029 Al</td>
<td>24/11/2011</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 2014-0246784 Al</td>
<td>04/09/2014</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 8481417 B2</td>
<td>09/07/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 8723326 B2</td>
<td>13/05/2014</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 8994189 B2</td>
<td>31/03/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 9437480 B2</td>
<td>06/09/2016</td>
</tr>
<tr>
<td></td>
<td></td>
<td>wo 2009-020773 A2</td>
<td>12/02/2009</td>
</tr>
<tr>
<td></td>
<td></td>
<td>wo 2009-020773 A3</td>
<td>23/04/2009</td>
</tr>
<tr>
<td>US 2015-0371852 Al</td>
<td>24/12/2015</td>
<td>us 2017-0092494 Al</td>
<td>30/03/2017</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 9548201 B2</td>
<td>17/01/2017</td>
</tr>
<tr>
<td>US 2016-0329280 Al</td>
<td>10/11/2016</td>
<td>cn 102810474 A</td>
<td>05/12/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cn 102810474 B</td>
<td>18/02/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 2012-0306023 Al</td>
<td>06/12/2012</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 2014-0042557 Al</td>
<td>13/02/2014</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 8569129 B2</td>
<td>29/10/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 9406607 B2</td>
<td>02/08/2016</td>
</tr>
<tr>
<td>US 2013-0134486 Al</td>
<td>30/05/2013</td>
<td>cn 103137459 A</td>
<td>05/06/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cn 103137459 B</td>
<td>23/09/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>de 10201221620 Al</td>
<td>29/05/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>kr 10-2013-0059275 A</td>
<td>05/06/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>sg 190521 Al</td>
<td>28/06/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>tw 201331996 A</td>
<td>01/08/2013</td>
</tr>
<tr>
<td></td>
<td></td>
<td>tw 1509669 B</td>
<td>21/11/2015</td>
</tr>
<tr>
<td></td>
<td></td>
<td>us 8557675 B2</td>
<td>15/10/2013</td>
</tr>
</tbody>
</table>