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(54) Title: RRAM BASED COMPLIMENTARY SWITCH FOR CROSSPOINT MEMORY APPLICATIONS

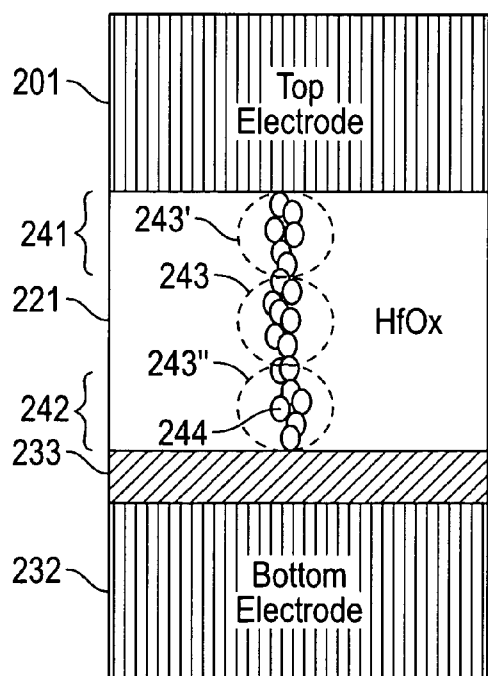


FIG. 2A

(57) Abstract: An embodiment includes a resistive random access memory (RRAM) system comprising: a bi-polar complementary resistive switch (CRS) comprising a top electrode, a bottom electrode, and an oxide layer between the top and bottom electrodes; wherein (a) a first plurality of oxygen vacancies are within the oxide layer and are adjacent the top electrode at a first concentration, (b) a second plurality of oxygen vacancies are within the oxide layer and are adjacent the bottom electrode at a second concentration, and (c) a third plurality of oxygen vacancies are within the oxide layer at a third concentration and between the first and second pluralities of oxygen vacancies. Other embodiments are described herein.



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RRAM Based Complimentary Switch for Crosspoint Memory Applications

[0001] Embodiments of the invention are in the field of semiconductor devices and, in particular, non-volatile memory.

Background

[0002] Resistive random access memory (RRAM or ReRAM) relies on a class of materials that switch in a one-time event from a virgin insulating state to a low resistive state by way of a “forming” event. In the forming event, the device goes through “soft breakdown” in which a localized filament forms in a dielectric layer located between two electrodes. This filament shunts current through the filament to form a low resistance state. The RRAM switches from a low to a high resistive state (by disbanding the filament) and from a high to a low resistive state (by reforming the filament) by applying voltages of different polarities to the electrodes to switch the state. Thus, conventional RRAM can serve as a memory.

Brief Description of the Drawings

[0003] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

Figure 1(a) includes a conventional RRAM stack and Figure 1(b) includes corresponding I-V characteristics;

Figure 2(a) includes a RRAM stack and Figure 2(b) includes corresponding I-V characteristics in an embodiment of the invention;

Figures 3a-3e include a method of forming a RRAM stack in an embodiment of the invention;

Figure 4 is a memory array in an embodiment; and

Figures 5 and 6 include systems that each include an embodiment of the RRAM stack.

Detailed Description

[0004] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of semiconductor/circuit structures. Thus, the actual appearance of the fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. For example, not every layer of a semiconductor device is necessarily shown. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

[0005] RRAM can sometimes include a complimentary switch, which consists of two anti-serially connected bipolar resistive switches. As noted in "Complementary Resistive Switches", by Eike Cyrus Linn, ([***.publications.rwth-aachen.de/record/210058/files/4365.pdf](http://www.publications.rwth-aachen.de/record/210058/files/4365.pdf)), such switches may be included in a crossbar (also referred to as "crosspoint") array, which is a matrix consisting of n word lines, m bit lines and n·m memory cells, which can be accessed individually or row by row. The array may be active or passive. For the active implementation, each matrix element has its own activatable select transistor (1T), while for the passive implementation, only two terminal selector devices, like diodes, are used. For resistive random access memory (ReRAM), a resistive switch (1R) and a

transistor (1T) are used (1T1R configuration). Every resistive switching cell, either unipolar or bipolar, can be used in this approach. In contrast to active arrays, no transistors are used in passive crossbar arrays. Passive crossbar arrays consist only of bit and word lines and a storing element at each junction, resulting in a minimum feature size of $4F^2$.

[0006] Figure 1(a) includes a RRAM based complementary switch 100. Switch 100 includes top electrode 101, oxygen exchange layer (OEL) 111 (e.g., Hf, Ti, and the like), oxide 121 (e.g., HfOx), and middle metal layer 131. Oxygen vacancies 144 have a higher concentration in region 141 and a relatively lower concentration in region 142. The vacancies collectively form a filament that serves as a memory. As addressed above, a “soft breakdown” occurs whereby, for example, an anneal takes place such that oxygen is scavenged by OEL 111 thereby producing vacancies 144. The vacancies cluster near the OEL/oxide interface (interface between layers 111 and 121) because that is where the scavenging takes place. Stack 100 further includes bottom electrode 101', OEL 111' (e.g., Hf, Ti, and the like), and oxide 121' (e.g., HfOx). Oxygen vacancies 144' have a higher concentration in region 141' and a relatively lower concentration in region 142'. Oxygen is scavenged by OEL 111' thereby producing vacancies 144'. The vacancies cluster near the OEL/oxide interface (interface between layers 111' and 121').

[0007] Biasing electrodes 101, 101' with one polarity may purposely remove vacancies in areas 143, 143' to disband or disrupt the filament and create a high resistance state (a “0” memory state). Reversing the bias to electrodes 101, 101' with an opposite polarity may reform vacancies in areas 143, 143' to reform the filament and create a low resistance state (a “1” memory state). Figure 1(b) shows I-V characteristic of an example of stack 100. As voltage rises past a first threshold both RRAM1 and RRAM2 are in low resistance (point 1—set), then when a second threshold is exceeded one of the devices (RRAM1) resets to high resistance (point 2—reset) resulting in a “high resistive state” or HRS or memory state “0”. Then both devices enter into low resistance as voltage falls past another threshold (point 3—set), and finally another of the devices (RRAM2) resets to high resistance (point 4—reset) placing the device into a “low resistive state” or LRS or memory state “1”.

[0008] Applicant has identified shortcomings with complementary switch 100. For example, switch 100 requires 2 RRAM switches, which leads to process complexity and layout penalties (e.g., relatively large area needed for switches). To address the shortcomings, Applicant provides an embodiment with a complementary switch (e.g., a bi-polar complementary resistive switch, sometimes referred to herein as a “CRS”) using only one RRAM stack instead of two such stacks. Embodiments with such a complementary switch that uses one RRAM stack have several advantages over conventional complementary RRAM switches. First, a complimentary switch that is made from a single RRAM stack simplifies processing and reduces layout penalties (e.g., saves space vs. two switch conventional device). Second, an embodiment limits switching current (e.g., switching current $\ll 1$ mA) based on an oxide resistor (described below), which increases reliability for memory using the device (i.e., protects against damage to device due to excessive current). Third, an embodiment provides an RRAM stack that is symmetric (because no OEL is present), which reduces processing complexity. Fourth, an embodiment that includes a filament RESET/SET that occurs at two positions (e.g., see areas 243' and 243” in Figure 2(a)) in the vacancy filament (removing need for a second RRAM switch).

[0009] Figure 2(a) includes RRAM stack 200 including top electrode 201, oxide 221 (e.g., HfOx), and bottom electrode 232. Oxygen vacancies 244 are distributed (when in a low resistance state) among regions 241, 242, 243. The vacancies collectively form a filament that serves as a memory. As addressed above, a “soft breakdown” occurs to produce vacancies 144. The vacancies cluster near the electrode/oxide interfaces (interface between layers 201/221 and 232/221). Figure 2(b) is analogous to the I-V characteristic plot of Figure 1(b), showing stack 200 operates with HRS (memory state “1” when V_{th2} is exceeded) and LRS (memory state “0” when V_{th4} is exceeded) states despite having no OEL.

[0010] Returning to Figure 2(a), a first plurality of oxygen vacancies 241 is adjacent electrode 201 at a first concentration, a second plurality of oxygen vacancies 242 is adjacent (not necessarily directly adjacent) electrode 232 at a second concentration, and a third plurality of oxygen vacancies 245 is between pluralities 241, 242 and at a third concentration. “Adjacent” or “immediately adjacent”, as used herein, are

relative terms. Thus, vacancies 242 are adjacent layer 232 but not layer 201 and vacancies 241 are adjacent layer 201 but not layer 232.

[0011] In an embodiment, there is no OEL between electrodes 201, 232 or separate and apart from electrodes 201, 232.

[0012] In an embodiment the oxide layer 221 includes at least one of HfO_2 , SiO_2 , Al_2O_3 , TiO_2 , SrTiO_3 , Cr-SrTiO_3 , NiO , CuOx , ZrO_2 , Nb_2O_5 , MgO , Fe_2O_3 , Ta_2O_5 , ZnO , CoO , CuMnOx , CuMoOx , InZnO , Cr-SrZrO_3 , PrCaMnO_3 , SrLaTiO_3 , LaSrFeO_3 , $(\text{Pr,Ca})\text{MnO}_3$, Nb-SrTiO_3 , and LaSrCoO_3 . In an embodiment top electrode 201 includes at least one of Hf, Ti, Ta, Pd, W, Mo, and Pt (e.g., TiN) and bottom electrode 231 includes at least one of Hf, Ti, Ta, Pd, W, Mo, and Pt (e.g., TiN). Additionally, electrodes 201, 231 may include multiple layers of materials with differing properties.

[0013] An embodiment includes a resistor 233 adjacent one of the electrodes, such as electrode 232 (but adjacent electrode 201 in other embodiments). In some embodiments resistors are adjacent both electrodes. Resistor 233 may be an oxide or a nitride such as, for example, TiON . Such a resistor may be formed by, for example, exposing an electrode surface (e.g., upper surface of electrode 232 at Figure 3(b)) to oxygen (or general atmospheric gases) during manufacture of device 200.

[0014] In an embodiment the oxide layer 221 directly contacts electrodes 201, 232 (e.g., in an embodiment where no resistor 233 is present). In another embodiment oxide layer 221 directly contacts resistor 233 and electrode 201.

[0015] RRAM stack 200 is a functioning nonvolatile memory in that in a first state (when energy is applied to the top electrode at a first polarity and satisfying a first threshold voltage) the first, second, and third pluralities of oxygen vacancies form a first filament having a first electrical resistance; and in a second state (when energy is applied to the top electrode at the first polarity and satisfying a second threshold voltage) the first, second, and third pluralities of oxygen vacancies form a second filament configuration or discontinuity thereby causing the higher resistivity.

[0016] For example, in Figure 2(b) the first state may occur at V_{th1} and the second state may occur at V_{th2} . In the first state there may be continuous vacancies at 243, 243', 243" thereby forming a filament that is relatively low resistance. In the second state there may be non-continuous vacancies. For example, there may be a lower concentration (or even a discontinuity) at 243', thereby forming a discontinuous filament that is relatively high resistance (a "0" memory state).

[0017] In RRAM stack 200 in a third state (when energy is applied to the top electrode at a second polarity, opposite the first polarity, and satisfying a third threshold voltage) the first, second, and third pluralities of oxygen vacancies form a third filament having a relatively lower electrical resistance; and in a fourth state (when energy is applied to the top electrode at the second polarity and satisfying a fourth threshold voltage) the first, second, and third pluralities of oxygen vacancies form a fourth filament configuration or discontinuity thereby causing the higher resistivity.

[0018] For example, in Figure 2(b) the third state may occur at V_{th3} and the fourth state may occur at V_{th4} . In the third state there may be continuous vacancies at 243, 243', 243" thereby forming a filament that is relatively low resistance. In the fourth state there may be non-continuous vacancies. For example, there may be a lower concentration (or even a discontinuity) at 243", thereby forming a discontinuous filament that is relatively high resistance (a "1" memory state).

[0019] Figures 3(a)-3(e) include a method of forming a RRAM stack in an embodiment of the invention. In Figure 3(a) the bottom electrode 331 is formed. In Figure 3(b) the oxide resistor 351 is deposited on the bottom electrode. Next oxide 321 is formed (Figure 3(c)) followed by top electrode 301 (Figure 3(d)). Finally, patterning and etching occur to form the RRAM cell and an anneal is performed to produce filament 245 composed of oxygen vacancies (Figure 3(e)).

[0020] Various embodiments disclosed herein have addressed RRAM stacks. As seen in Figure 4, any such RRAM stack 200 may be used in a memory cell (and memory array) by coupling one portion or node of the stack (e.g., top electrode of

Figure 2(a)) to a column decoder and another node of the stack (e.g., bottom electrode of Figure 2(a)) to a row decoder in a crossbar/crosspoint array.

[0021] Embodiments provide smaller and more power efficient memory cells that can be scaled below, for example, 22 nm CD.

[0022] Referring now to Figure 5, shown is a block diagram of an example system with which embodiments can be used. As seen, system 900 may be a smartphone or other wireless communicator or any other internet of things (IoT) device. A baseband processor 905 is configured to perform various signal processing with regard to communication signals to be transmitted from or received by the system. In turn, baseband processor 905 is coupled to an application processor 910, which may be a main CPU of the system to execute an OS and other system software, in addition to user applications such as many well-known social media and multimedia apps. Application processor 910 may further be configured to perform a variety of other computing operations for the device.

[0023] In turn, application processor 910 can couple to a user interface/display 920 (e.g., touch screen display). In addition, application processor 910 may couple to a memory system including a non-volatile memory, namely a flash memory 930 and a system memory, namely a DRAM 935. In some embodiments, flash memory 930 may include a secure portion 932 in which secrets and other sensitive information may be stored. As further seen, application processor 910 also couples to a capture device 945 such as one or more image capture devices that can record video and/or still images.

[0024] A universal integrated circuit card (UICC) 940 comprises a subscriber identity module, which in some embodiments includes a secure storage 942 to store secure user information. System 900 may further include a security processor 950 (e.g., Trusted Platform Module (TPM)) that may couple to application processor 910. A plurality of sensors 925, including one or more multi-axis accelerometers may couple to application processor 910 to enable input of a variety of sensed information such as motion and other environmental information. In addition, one or more

authentication devices 995 may be used to receive, for example, user biometric input for use in authentication operations.

[0025] As further illustrated, a near field communication (NFC) contactless interface 960 is provided that communicates in a NFC near field via an NFC antenna 965. While separate antennae are shown, understand that in some implementations one antenna or a different set of antennae may be provided to enable various wireless functionalities.

[0026] A power management integrated circuit (PMIC) 915 couples to application processor 910 to perform platform level power management. To this end, PMIC 915 may issue power management requests to application processor 910 to enter certain low power states as desired. Furthermore, based on platform constraints, PMIC 915 may also control the power level of other components of system 900.

[0027] To enable communications to be transmitted and received such as in one or more IoT networks, various circuitries may be coupled between baseband processor 905 and an antenna 990. Specifically, a radio frequency (RF) transceiver 970 and a wireless local area network (WLAN) transceiver 975 may be present. In general, RF transceiver 970 may be used to receive and transmit wireless data and calls according to a given wireless communication protocol such as 3G or 4G wireless communication protocol such as in accordance with a code division multiple access (CDMA), global system for mobile communication (GSM), long term evolution (LTE) or other protocol. In addition a GPS sensor 980 may be present, with location information being provided to security processor 950 for use as described herein when context information is to be used in a pairing process. Other wireless communications such as receipt or transmission of radio signals (e.g., AM/FM) and other signals may also be provided. In addition, via WLAN transceiver 975, local wireless communications, such as according to a Bluetooth™ or IEEE 802.11 standard can also be realized.

[0028] System 900 may include hundreds or thousands of the above described memory cells/stacks (e.g., stack 200 of Figure 2(a)) and be critical to memory functions in system 900. Memory 935, 932, 930, 942, 950 and other non-labeled

memories may include memory stacks and/or arrays (see Figure 4) described herein.

[0029] Embodiments may be used in environments where IoT devices may include wearable devices or other small form factor IoT devices. Referring now to Figure 6, shown is a block diagram of a wearable module 1300 in accordance with another embodiment. In one particular implementation, module 1300 may be an Intel® Curie™ module that includes multiple components adapted within a single small module that can be implemented as all or part of a wearable device. As seen, module 1300 includes a core 1310 (of course in other embodiments more than one core may be present). Such core may be a relatively low complexity in-order core, such as based on an Intel Architecture® Quark™ design. In some embodiments, core 1310 may implement a TEE as described herein. Core 1310 couples to various components including a sensor hub 1320, which may be configured to interact with a plurality of sensors 1380, such as one or more biometric, motion environmental or other sensors. A power delivery circuit 1330 is present, along with a non-volatile storage 1340 (which includes embodiments of the RRAM stack 200 and/or other embodiments described herein). In an embodiment, this circuit may include a rechargeable battery and a recharging circuit, which may in one embodiment receive charging power wirelessly. One or more input/output (IO) interfaces 1350, such as one or more interfaces compatible with one or more of USB/SPI/I2C/GPIO protocols, may be present. In addition, a wireless transceiver 1390, which may be a Bluetooth™ low energy or other short-range wireless transceiver is present to enable wireless communications as described herein. Understand that in different implementations a wearable module can take many other forms. Wearable and/or IoT devices have, in comparison with a typical general purpose CPU or a GPU, a small form factor, low power requirements, limited instruction sets, relatively slow computation throughput, or any of the above.

[0030] The following examples pertain to further embodiments.

[0031] Example 1 includes a resistive random access memory (RRAM) system comprising: a bi-polar complimentary resistive switch (CRS) comprising a top electrode, a bottom electrode, and an oxide layer between the top and bottom

electrodes; wherein (a) a first plurality of oxygen vacancies are within the oxide layer and are adjacent the top electrode at a first concentration, (b) a second plurality of oxygen vacancies are within the oxide layer and are adjacent the bottom electrode at a second concentration, (c) a third plurality of oxygen vacancies are within the oxide layer at a third concentration and between the first and second pluralities of oxygen vacancies, and (d) the CRS does not include an oxygen exchange layer (OEL) between the top and bottom electrodes.

[0032] “Top” and “bottom” are relative terms and may change based on the orientation of the stack. OEL is a term of art known to those of ordinary skill in the art. The OEL may also be referred to as a “metal cap layer”. The OEL may include a metal such that, when the OEL is adjacent or contacting an oxygen source (e.g., oxide layer), the OEL facilitates “oxygen exchange” with the oxygen source. Example 1 has no such metal layer between the top and bottom electrodes.

[0033] The “first concentration” (as well as other aforementioned concentrations) may be extremely low (little to no vacancies) or extremely high depending on the state of CRS.

[0034] Another version of Example 1 includes a resistive random access memory (RRAM) system comprising: a bi-polar complimentary resistive switch (CRS) comprising a top electrode, a bottom electrode, and an oxide layer between the top and bottom electrodes; wherein (a) a first plurality of oxygen vacancies are within the oxide layer and are adjacent the top electrode at a first concentration, (b) a second plurality of oxygen vacancies are within the oxide layer and are adjacent the bottom electrode at a second concentration, and (c) a third plurality of oxygen vacancies are within the oxide layer at a third concentration and between the first and second pluralities of oxygen vacancies.

[0035] In example 2 the subject matter of Example 1 can optionally include wherein the oxide layer is monolithic and directly contacts both of the top and bottom electrodes.

[0036] The direct contact may preclude barrier layers and the like.

[0037] In example 3 the subject matter of the Examples 1-2 can optionally include a resistor having an additional oxide layer, wherein the additional oxide layer directly contacts both the bottom electrode and the oxide layer.

[0038] In example 4 the subject matter of the Examples 1-3 can optionally include wherein (a) the CRS includes no metal layer between the additional oxide layer and the top electrode, (b) the oxide layer directly contacts the upper electrode, and (c) the oxide layer is monolithic.

[0039] In example 5 the subject matter of the Examples 1-4 can optionally include wherein: in a first state when energy is applied to the top electrode at a first polarity and satisfies a first threshold voltage, the first, second, and third pluralities of oxygen vacancies form a first filament having a first electrical resistance; and in a second state when energy is applied to the top electrode at the first polarity and satisfies a second threshold voltage, the first, second, and third pluralities of oxygen vacancies form a second filament having a second electrical resistance that is greater than the first electrical resistance.

[0040] The second electrical resistance may be very high when the path is incomplete due to an absence of vacancies at area 243'. Thus, a second filament can constitute a broken or incomplete filament. There may be some vacancies at area 243' but so few that resistance is high.

[0041] In example 6 the subject matter of the Examples 1-5 can optionally include wherein in the second state the first plurality of oxygen vacancies is at the first concentration and in the first state the first plurality of oxygen vacancies is at an additional concentration that is greater than the first concentration.

[0042] In example 7 the subject matter of the Examples 1-6 can optionally include wherein in the second state the first plurality of oxygen vacancies is at the first concentration and the second plurality of oxygen vacancies is at the second concentration, and the second concentration is greater than the first concentration.

[0043] In example 8 the subject matter of the Examples 1-7 can optionally include wherein the first and second threshold voltages are both positive and the second threshold voltage is greater than the first threshold voltage.

[0044] By “greater”, V_{th2} is greater than V_{th1} and V_{th4} is greater than V_{th3} .

[0045] In example 9 the subject matter of the Examples 1-8 can optionally include wherein: in a third state when energy is applied to the top electrode at a second polarity, opposite the first polarity, and satisfies a third threshold voltage, the first, second, and third pluralities of oxygen vacancies form a third filament having a third electrical resistance; and in a fourth state when energy is applied to the top electrode at the second polarity and satisfies a fourth threshold voltage, the first, second, and third pluralities of oxygen vacancies form a fourth filament having a fourth electrical resistance that is greater than the third electrical resistance.

[0046] A resistance that is “greater” than another resistance is to be considered “more resistive” than the other resistance.

[0047] In example 10 the subject matter of the Examples 1-9 can optionally include wherein in the fourth state the first plurality of oxygen vacancies is at the first concentration and the second plurality of oxygen vacancies is at the second concentration and the second concentration is less than the first concentration.

[0048] In example 11 the subject matter of the Examples 1-10 can optionally include wherein the third and fourth threshold voltages are both negative and the fourth threshold voltage is greater than the third threshold voltage.

[0049] By “greater”, V_{th2} is greater than V_{th1} and V_{th4} is greater than V_{th3} .

[0050] In example 12 the subject matter of the Examples 1-11 can optionally include wherein in an initial forming state when energy is applied to the top electrode at the first polarity the first, second, and third pluralities of oxygen vacancies form the first filament; wherein the initial forming state precedes the first and second states.

[0051] In example 13 the subject matter of the Examples 1-12 can optionally include wherein the oxide layer includes at least one member selected from the group comprising HfOx, SiOx, Al₂Ox, TiOx, TaOx, GdOx, ErOx, NbOx, WOx, ZnOx, and InGaZnOx.

[0052] Another version of claim 13 provides the CRS does not include an oxygen exchange layer (OEL) between the top and bottom electrodes.

[0053] In example 14 the subject matter of the Examples 1-13 can optionally include wherein the top electrode includes at least one member selected from the group comprising TiN, TaN, W, Ru, Ir, Pd, Pt, Mo, TiAlN, and TaAlN and the bottom electrode also includes the at least one member.

[0054] In example 15 the subject matter of the Examples 1-14 can optionally include a memory array including a column decoder and a row decoder that couple to each other via the CRS.

[0055] Example 16 includes A resistive random access memory (RRAM) system comprising: a bi-polar complimentary resistive switch (CRS) comprising a top electrode, a bottom electrode, and an oxide layer between the top and bottom electrodes; wherein in a first state when energy is applied to the top electrode at a first polarity and which satisfies a first voltage threshold, first, second, and third pluralities of oxygen vacancies in the oxide layer form a first path having a first electrical resistance; wherein in a second state when energy is applied to the top electrode at the first polarity and which satisfies a second voltage threshold, the first, second, and third pluralities of oxygen vacancies form a second path between the top and bottom electrodes having a second electrical resistance that is greater than the first electrical resistance; wherein in the second state: (a) the first oxygen vacancies are within an upper third of the oxide layer at a first concentration, (b) the second oxygen vacancies are within a lower third of the oxide layer at a second concentration that is greater than the first concentration, and (c) the third oxygen vacancies are within a middle third of the oxide layer at a third concentration.

[0056] The first concentration may have few to no vacancies.

[0057] In example 17 the subject matter of the Example 16 can optionally include wherein the CRS does not include an oxygen exchange layer (OEL) between the top and bottom electrodes.

[0058] In example 18 the subject matter of the Examples 16-17 can optionally include comprising a resistor having an additional oxide layer, wherein the additional oxide layer directly contacts both the bottom electrode and the oxide layer.

[0059] In example 19 the subject matter of the Examples 16-18 can optionally include wherein the additional oxide layer includes TiON.

[0060] Example 20 includes a method comprising: forming a bottom electrode; forming an oxide resistor on the bottom electrode; forming an oxide layer on the oxide resistor; forming a top electrode on the oxide layer; patterning the oxide resistor, the top and bottom electrodes, and the oxide layer to form a resistive random access memory (RRAM) cell comprising a complimentary resistive switch (CRS); and annealing the RRAM cell to produce a filament, composed of oxygen vacancies, in the oxide layer.

[0061] In example 21 the subject matter of the Example 20 can optionally include coupling the RRAM cell to a row decoder and a column decoder of a memory array.

[0062] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and still fall within the meaning of the term "top." The term "on" as used herein (including in the claims) does not indicate that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is

therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

- 1 1. A resistive random access memory (RRAM) system comprising:
2 a bi-polar complimentary resistive switch (CRS) comprising a top electrode, a
3 bottom electrode, and an oxide layer between the top and bottom electrodes;
4 wherein (a) a first plurality of oxygen vacancies are within the oxide layer and
5 are adjacent the top electrode at a first concentration, (b) a second plurality of
6 oxygen vacancies are within the oxide layer and are adjacent the bottom electrode at
7 a second concentration, and (c) a third plurality of oxygen vacancies are within the
8 oxide layer at a third concentration and between the first and second pluralities of
9 oxygen vacancies.
- 1 2. The system of claim 1, wherein the oxide layer is monolithic and directly
2 contacts both of the top and bottom electrodes.
- 1 3. The system of claim 1 comprising a resistor having an additional oxide layer,
2 wherein the additional oxide layer directly contacts both the bottom electrode and the
3 oxide layer.
- 1 4. The system of claim 3, wherein (a) the CRS includes no metal layer between
2 the additional oxide layer and the top electrode, (b) the oxide layer directly contacts
3 the upper electrode, and (c) the oxide layer is monolithic.
- 1 5. The system of claim 1, wherein:
2 in a first state when energy is applied to the top electrode at a first polarity and
3 satisfies a first threshold voltage, the first, second, and third pluralities of oxygen
4 vacancies form a first filament having a first electrical resistance; and
5 in a second state when energy is applied to the top electrode at the first
6 polarity and satisfies a second threshold voltage, the first, second, and third
7 pluralities of oxygen vacancies form a second filament having a second electrical
8 resistance that is greater than the first electrical resistance.

1 6. The system of claim 5, wherein in the second state the first plurality of oxygen
2 vacancies is at the first concentration and in the first state the first plurality of oxygen
3 vacancies is at an additional concentration that is greater than the first concentration.

1 7. The system of claim 5, wherein in the second state the first plurality of oxygen
2 vacancies is at the first concentration and the second plurality of oxygen vacancies is
3 at the second concentration, and the second concentration is greater than the first
4 concentration.

1 8. The system of claim 7, wherein the first and second threshold voltages are
2 both positive and the second threshold voltage is greater than the first threshold
3 voltage.

1 9. The system of claim 5, wherein:
2 in a third state when energy is applied to the top electrode at a second
3 polarity, opposite the first polarity, and satisfies a third threshold voltage, the first,
4 second, and third pluralities of oxygen vacancies form a third filament having a third
5 electrical resistance; and
6 in a fourth state when energy is applied to the top electrode at the second
7 polarity and satisfies a fourth threshold voltage, the first, second, and third pluralities
8 of oxygen vacancies form a fourth filament having a fourth electrical resistance that
9 is greater than the third electrical resistance.

1 10. The system of claim 9, wherein in the fourth state the first plurality of oxygen
2 vacancies is at the first concentration and the second plurality of oxygen vacancies is
3 at the second concentration and the second concentration is less than the first
4 concentration.

1 11. The system of claim 10, wherein the third and fourth threshold voltages are
2 both negative and the fourth threshold voltage is greater than the third threshold
3 voltage.

1 12. The system of claim 5, wherein in an initial forming state when energy is
2 applied to the top electrode at the first polarity the first, second, and third pluralities
3 of oxygen vacancies form the first filament; wherein the initial forming state precedes
4 the first and second states.

1 13. The system of claim 5, wherein the CRS does not include an oxygen
2 exchange layer (OEL) between the top and bottom electrodes.

1 14. The system of claim 1, wherein the oxide layer includes at least one member
2 selected from the group comprising HfOx, SiOx, Al₂Ox, TiOx, TaOx, GdOx, ErOx,
3 NbOx, WOx, ZnOx, and InGaZnOx.

1 15. The system of claim 14, wherein the top electrode includes at least one
2 member selected from the group comprising TiN, TaN, W, Ru, Ir, Pd, Pt, Mo, TiAlN,
3 and TaAlN and the bottom electrode also includes the at least one member.

1 16. The system of claim 1 comprising a memory array including a column decoder
2 and a row decoder that couple to each other via the CRS.

1 17. A resistive random access memory (RRAM) system comprising:
2 a bi-polar complimentary resistive switch (CRS) comprising a top electrode, a
3 bottom electrode, and an oxide layer between the top and bottom electrodes;
4 wherein in a first state when energy is applied to the top electrode, at a first
5 polarity, and which satisfies a first voltage threshold, first, second, and third
6 pluralities of oxygen vacancies in the oxide layer form a first path having a first
7 electrical resistance;
8 wherein in a second state when energy is applied to the top electrode, at the
9 first polarity, and which satisfies a second voltage threshold, the first, second, and
10 third pluralities of oxygen vacancies form a second path between the top and bottom
11 electrodes having a second electrical resistance that is greater than the first
12 electrical resistance;

13 wherein in the second state: (a) the first oxygen vacancies are within an upper
14 third of the oxide layer at a first concentration, (b) the second oxygen vacancies are
15 within a lower third of the oxide layer at a second concentration that is greater than
16 the first concentration, and (c) the third oxygen vacancies are within a middle third of
17 the oxide layer at a third concentration.

1 18. The system of claim 17, wherein the CRS does not include an oxygen
2 exchange layer (OEL) between the top and bottom electrodes.

1 19. The system of claim 17 comprising a resistor having an additional oxide layer,
2 wherein the additional oxide layer directly contacts both the bottom electrode and the
3 oxide layer.

1 20. The system of claim 19, wherein the additional oxide layer includes TiON.

1 21. A method comprising:
2 forming a bottom electrode;
3 forming an oxide resistor on the bottom electrode;
4 forming an oxide layer on the oxide resistor;
5 forming a top electrode on the oxide layer;
6 patterning the oxide resistor, the top and bottom electrodes, and the oxide
7 layer to form a resistive random access memory (RRAM) cell comprising a
8 complimentary resistive switch (CRS); and
9 annealing the RRAM cell to produce a filament, composed of oxygen
10 vacancies, in the oxide layer.

1 22. The method of claim 21 comprising coupling the RRAM cell to a row decoder
2 and a column decoder of a memory array.

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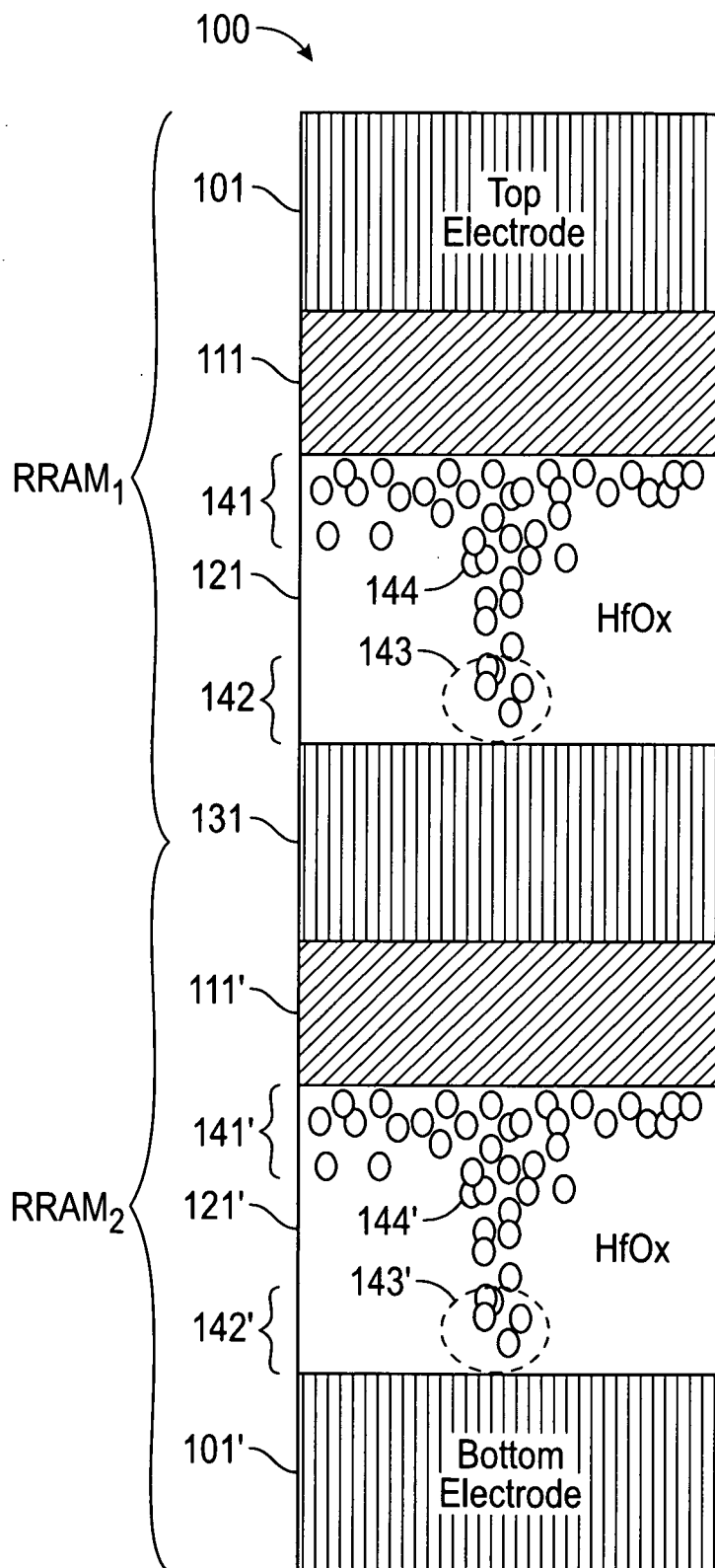


FIG. 1A
(Prior Art)

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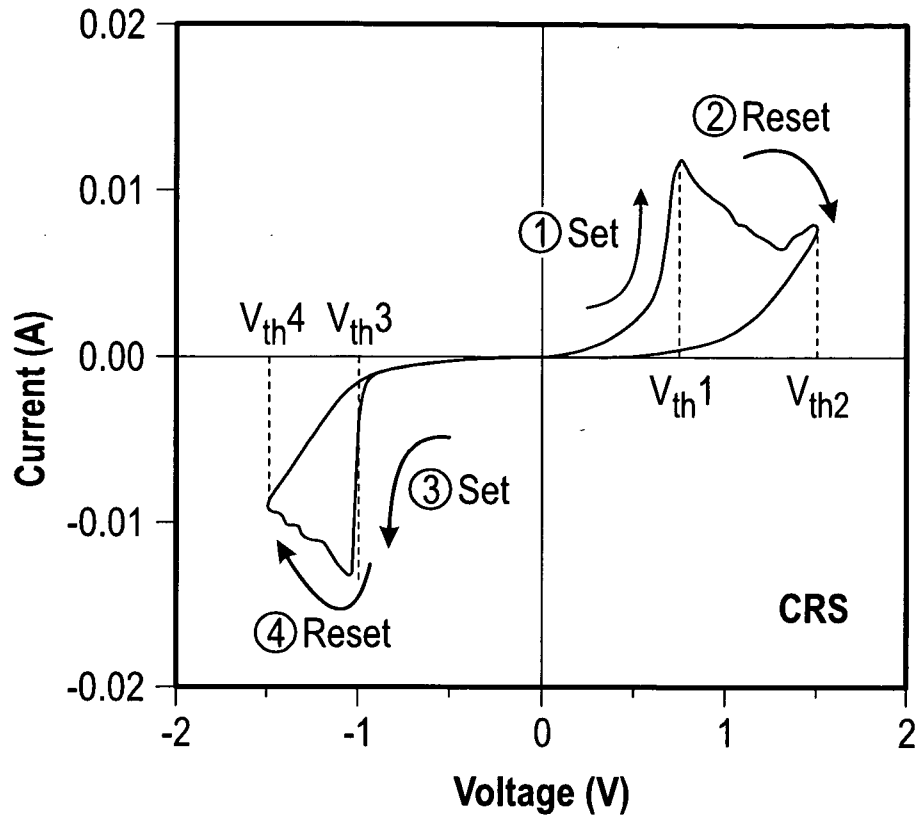


FIG. 1B
(Prior Art)

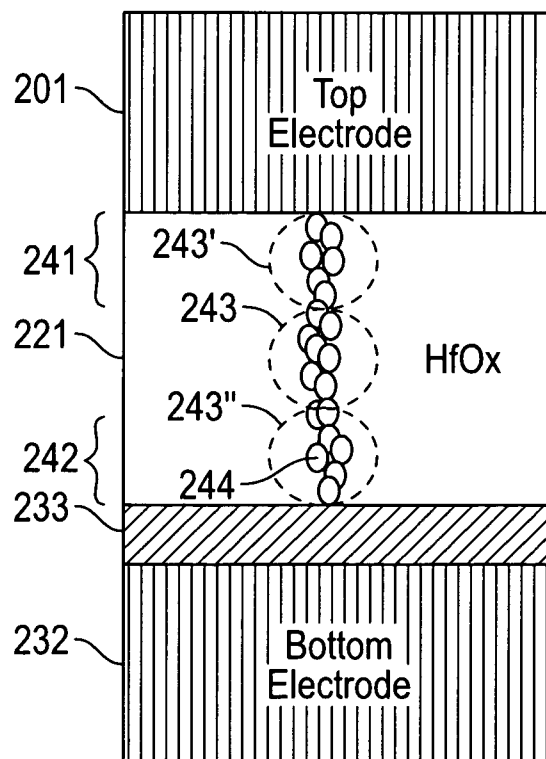


FIG. 2A

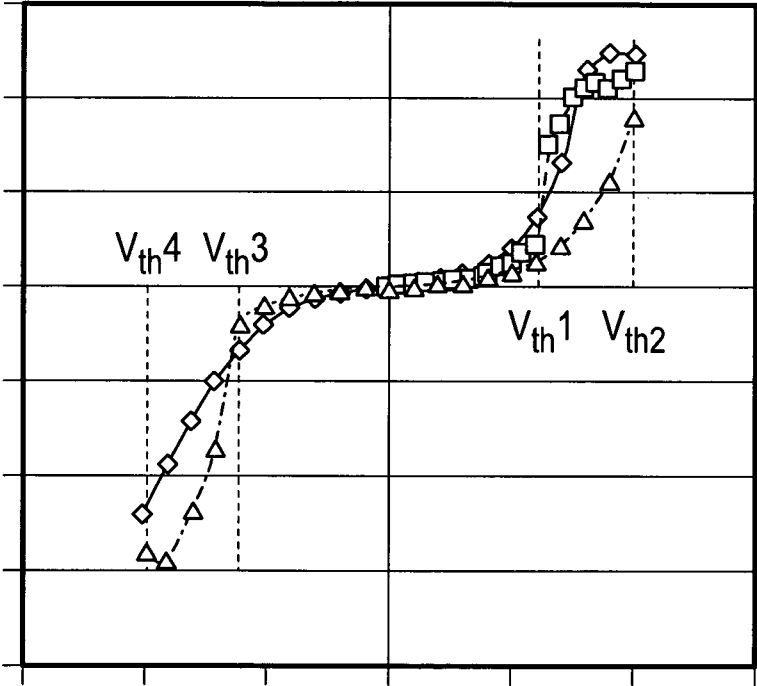
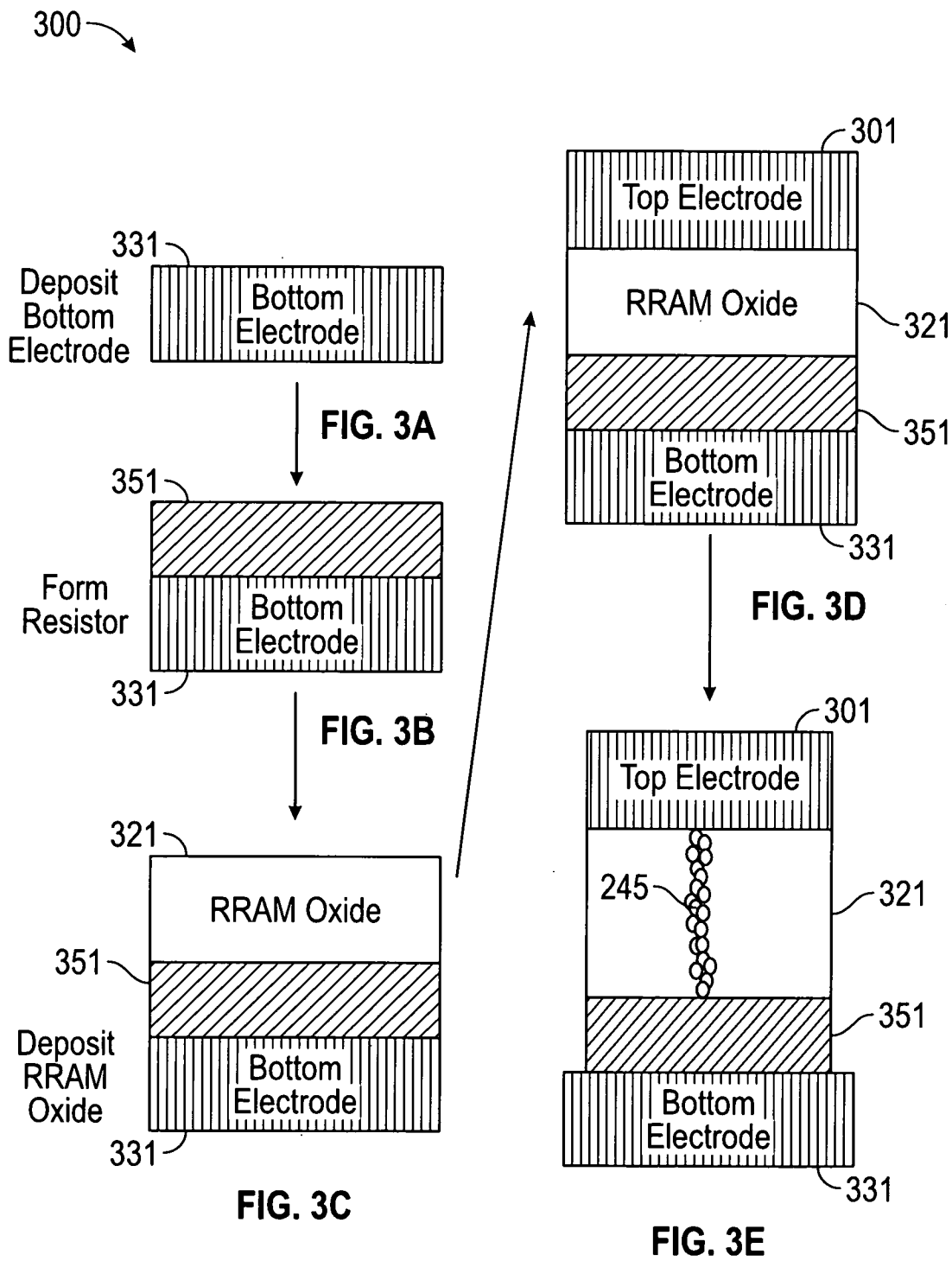


FIG. 2B

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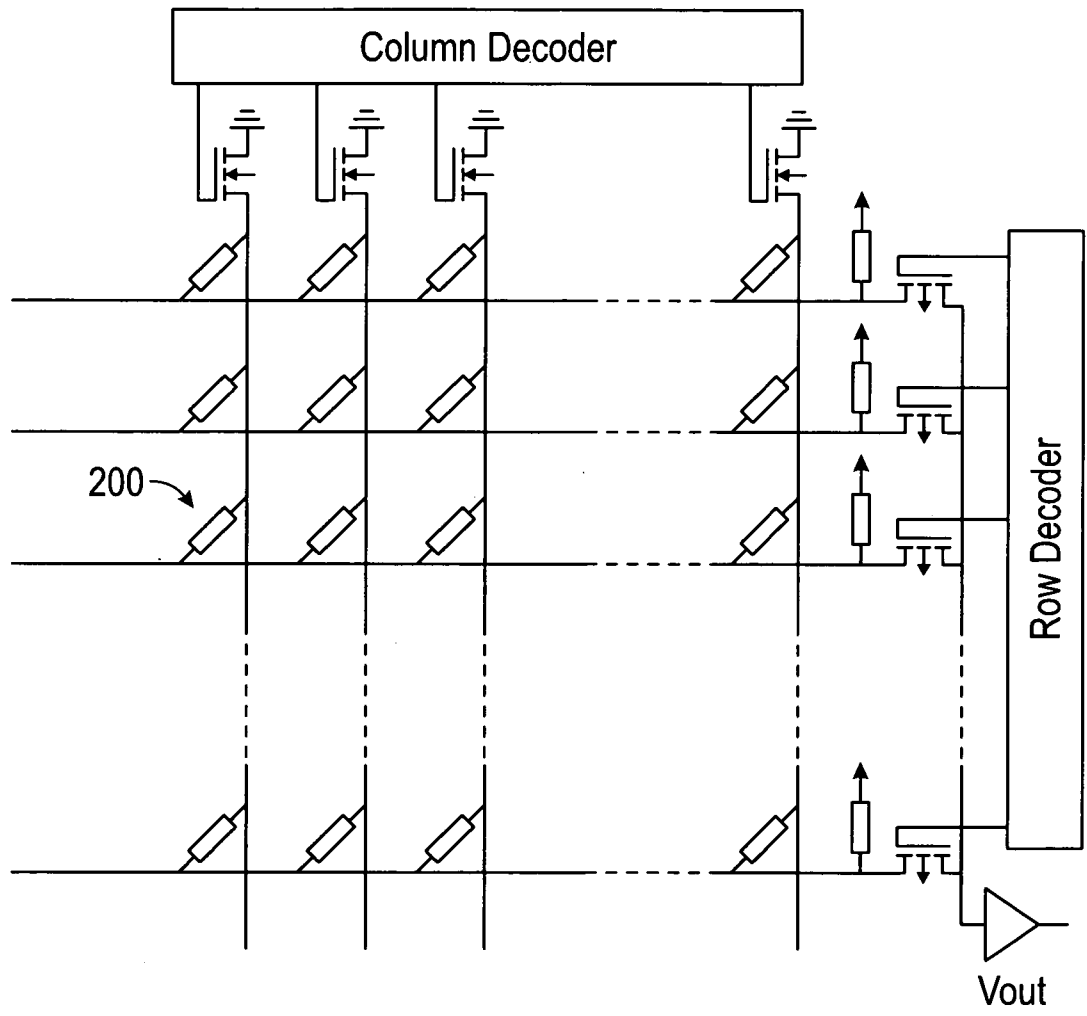


FIG. 4

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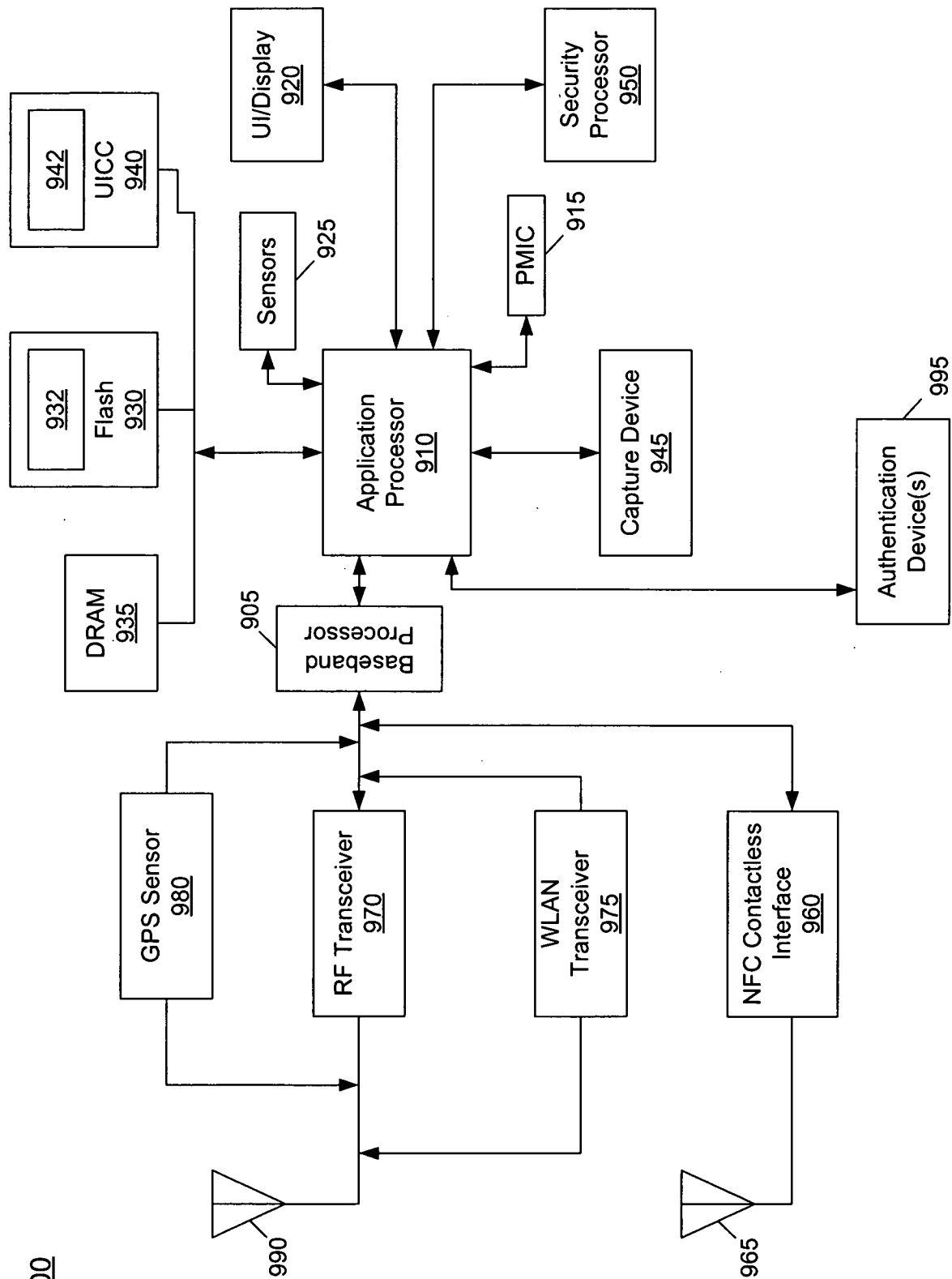


FIG. 5

1300 →

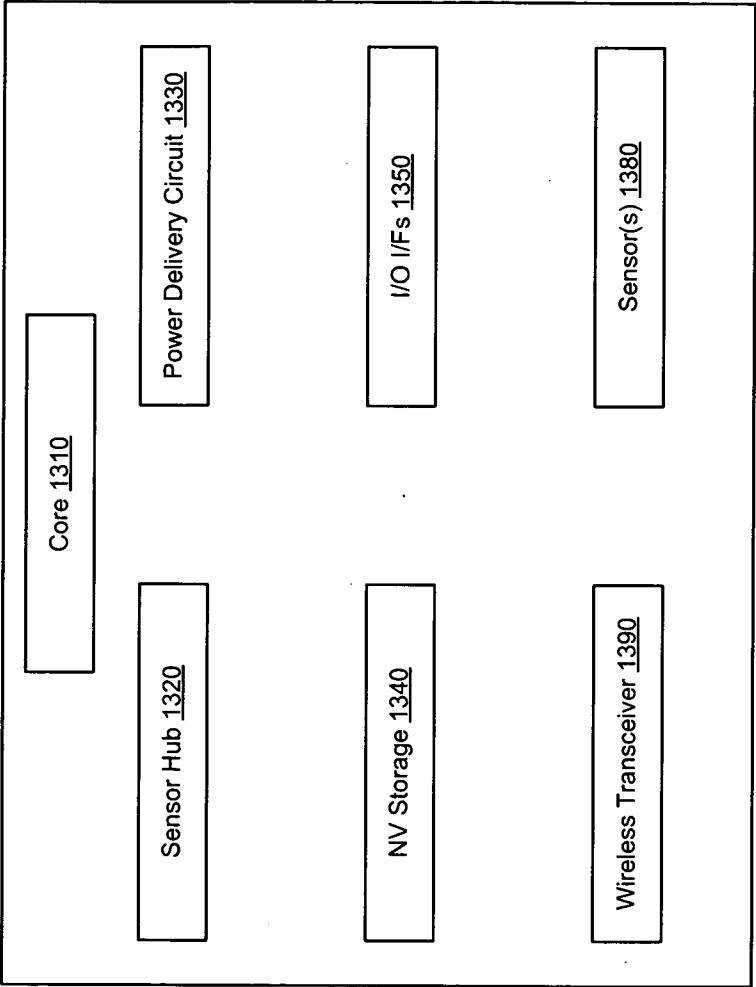


FIG. 6

A. CLASSIFICATION OF SUBJECT MATTER**H01L 45/00(2006.01)i, H01L 45/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 45/00; H01L 27/115; G11C 11/56; H01L 21/8247; H01L 27/24; H01L 45/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: Complementary Resistive Switch, Resistive Random Access Memory, oxygen vacancy, concentration, resistance state

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013-0334486 A1 (CHUN-YANG TSAI et al.) 19 December 2013 See paragraphs [0002], [0016]-[0040], [0067], claim 1 and figures 1, 2.	1-5, 9, 12-16, 21, 22
A		6-8, 10, 11, 17-20
Y	US 2015-0034898 A1 (INTERMOLECULAR INC. et al.) 05 February 2015 See paragraphs [0021], [0041]-[0047], [0065], [0089], claim 1 and figures 1A, 1B, 5B-5D.	1-5, 9, 12-16, 21, 22
A	US 2015-0003144 A1 (INTERNATIONAL BUSINESS MACHINES CORP.) 01 January 2015 See paragraphs [0066]-[0081], claim 1 and figure 4.	1-22
A	US 2015-0255509 A1 (INFINEON TECHNOLOGIES AG) 10 September 2015 See paragraphs [0017]-[0031], claim 1 and figure 2.	1-22
A	KR 10-2013-0077514 A (SK HYNIX INC.) 09 July 2013 See paragraphs [0018]-[0025], claim 1 and figure 1.	1-22



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 September 2016 (26.09.2016)

Date of mailing of the international search report

26 September 2016 (26.09.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000368

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