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(54) Title: OMEGA SHAPED NANOWIRE FIELD EFFECT TRANSISTORS

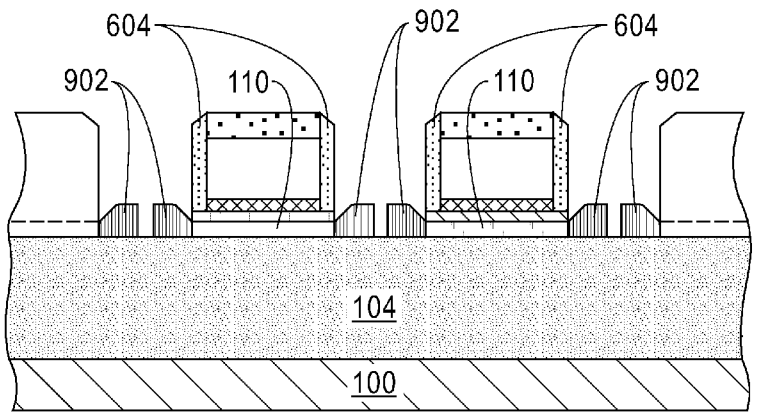

FIG. 8B

(57) Abstract: A method for forming a nanowire field effect transistor (FET) device includes forming a nanowire (110) on a semiconductor substrate, (100) forming a first gate structure on a first portion of the nanowire, forming a first protective spacer (604) adjacent to sidewalls of the first gate structure and over portions of the nanowire extending from the first gate structure, removing exposed portions of the nanowire left unprotected by the first spacer, and epitaxially growing a doped semiconductor material (902) on exposed cross sections of the nanowire to form a first source region and a first drain region.

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OMEGA SHAPED NANOWIRE FIELD EFFECT TRANSISTORS

FIELD OF INVENTION

The present invention relates to semiconductor nanowire field effect transistors.

DESCRIPTION OF RELATED ART

A nanowire field effect transistor (FET) includes doped portions of nanowire that contact the channel region and serve as source and drain regions of the device. Previous fabrication methods that used ion-implantation to dope the small diameter nanowire may result in undesirable amorphization of the nanowire or an undesirable junction doping profile.

BRIEF SUMMARY

In one aspect of the present invention, a method for forming a nanowire field effect transistor (FET) device includes forming a nanowire on a semiconductor substrate, forming a first gate structure on a first portion of the nanowire, forming a first protective spacer adjacent to sidewalls of the first gate structure and over portions of the nanowire extending from the first gate structure, removing exposed portions of the nanowire left unprotected by the first spacer, and epitaxially growing a doped semiconductor material on exposed cross sections of the nanowire to form a first source region and a first drain region

In another aspect of the present invention, A method for a nanowire field effect transistor (FET) device includes forming a nanowire on a semiconductor substrate, forming a gate structure on a portion of the nanowire, forming a protective spacer adjacent to sidewalls of the gate structure and over portions of the nanowire extending from the gate structure, removing exposed portions of the nanowire to form a cavity defined by the nanowire surrounded by the gate structure, the semiconductor substrate, and the spacer, and epitaxially growing a doped semiconductor material in the cavity from exposed cross sections of the nanowire.

In yet another aspect of the present invention, a nanowire field effect transistor (FET) device includes a channel region including a silicon portion disposed on a semiconductor substrate having a first distal end extending from the channel region and a second distal end extending from the channel region, the silicon portion is partially surrounded by a gate structure disposed circumferentially on the silicon portion, a source region including a first doped epi-silicon nanowire extension contacting the first distal end of the silicon portion, and a drain region including a second doped epi-silicon nanowire extension contacting the second distal end of the silicon portion.

In yet another aspect of the present invention, a nanowire field effect transistor (FET) device includes a channel region disposed on a semiconductor substrate including a silicon portion having a first distal end and a second distal end, the silicon portion is surrounded by a gate structure disposed circumferentially on the silicon portion, a first cavity defined by the first distal end of the silicon portion, the semiconductor substrate, and an inner diameter of the gate structure, a second cavity defined by the second distal end of the silicon portion, the semiconductor substrate, and an inner diameter of the gate structure, a source region including a first doped epi-silicon nanowire extension epitaxially extending from the first distal end of the silicon portion in the first cavity, and a drain region including a second doped epi-silicon nanowire extension epitaxially extending from the second distal end of the silicon portion in the second cavity.

Additional features and advantages are realized through the techniques of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention. For a better understanding of the invention with the advantages and the features, refer to the description and to the drawings.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The subject matter which is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The forgoing and other features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIGS. 1-12B illustrate an exemplary method for forming field effect transistor (FET) devices.

FIGS. 13A-14B illustrate an alternate exemplary method for forming field effect transistor (FET) devices.

DETAILED DESCRIPTION

With reference now to FIG. 1, a silicon on insulator (SOI) portion 102 is defined on a buried oxide (BOX) layer 104 that is disposed on a silicon substrate 100. The SOI portion 102 includes a SOI pad region 106, a SOI pad region 108, and nanowire portions 109. The SOI portion 102 may be patterned by the use of lithography followed by an etching process such as, for example, reactive ion etching (RIE).

FIG. 2 illustrates the nanowires 110 disposed on the BOX layer 104 following an oxidation process that reduces the diameter of the nanowires 110. The reduction of the diameter of the nanowires 110 may be performed by, for example, an oxidation of the nanowires 110 followed by the etching of the grown oxide. The oxidation and etching process may be repeated to achieve a desired nanowire 110 diameter. Once the diameters of the nanowires 110 have been reduced, gates are formed over the channel regions of the nanowires 110 (described below).

FIG. 3A illustrates gates 402 that are formed on the nanowires 110, as described in further detail below, and capped with a polysilicon layer (capping layer) 404. A hardmask layer 406, such as, for example silicon nitride (Si_3N_4) is deposited over the polysilicon layer 404. The polysilicon layer 404 and the hardmask layer 406 may be formed by depositing polysilicon material over the BOX layer 104 and the SOI portion 102, depositing the hardmask material over the polysilicon material, and etching by RIE to form the polysilicon layer 406 and the hardmask layer 404 illustrated in FIG. 3A. The etching of the gate 402 may be performed by directional etching that results in straight sidewalls of the gate 402.

FIG. 3B illustrates a perspective view of an exemplary alternate arrangement that includes a plurality of gates 402 that are formed on the nanowires 110 between SOI pad regions 106

and 108. The fabrication of the arrangement shown in FIG. 3B may be performed using similar methods as described above for the fabrication of a single row of gates 402 line, and illustrates how the methods described herein may be used to form any number of devices on a nanowire between SOI pad regions 106 and 108.

FIG. 4 illustrates a cross sectional view of a gate 402 along the line A-A (of FIG. 3A). The gate 402 is formed by depositing a first gate dielectric layer 502, such as silicon dioxide (SiO_2) on a channel portion of the nanowire 110. A second gate dielectric layer 504 such as, for example, hafnium oxide (HfO_2) is formed on the first gate dielectric layer 502. A metal layer 506 such as, for example, tantalum nitride (TaN) is formed on the second gate dielectric layer 504. The metal layer 506 is surrounded by polysilicon layer 404 (of FIG. 3A). Doping the polysilicon layer 404 with impurities such as boron (p-type), or phosphorus (n-type) makes the polysilicon layer 404 conductive.

FIGS. 5A and 5B illustrate the spacer portions 604 formed along opposing sides of the polysilicon layer 404. The spacers are formed by depositing a blanket dielectric film such as silicon nitride and etching the dielectric film from all horizontal surfaces by RIE. The spacer walls 604 are formed around portions of the nanowire 110 that extend from the polysilicon layer 404 and surround portions of the nanowires 110. FIGS. 5A and 5B include spacer portions 602 that are formed under the nanowires 110, and in the undercut regions 202 (of FIG. 2).

FIG. 6A illustrates a cross-sectional view (of FIG. 5A). FIG. 6B illustrates a similar cross-sectional view of the exemplary alternate arrangement of FIG. 5B.

FIGS. 7A and 7B illustrate cross-sectional views of the resultant structures following a selective RIE process, that removes exposed portions of the nanowires 110 and the SOI pad regions 106 and 108 (shown in FIG. 6A). An example of a selective RIE process includes a RIE based on HBr chemistry that etches silicon while being selective to reduce the etching of dielectrics such as silicon oxide and silicon nitride. The portions of the nanowire 110 that are surrounded by the spacer walls 604 are not etched, and have exposed cross sections defined by the spacer walls 604.

FIGS. 8A and 8B illustrate cross-sectional views of the resultant structures following a selective epi-silicon growth to form epi-nanowire extensions 902 (nanowire extensions). The nanowire extensions 902 are epitaxially grown from the exposed cross-sectional portions of the nanowire 110 that are surrounded by the spacer walls 604. The nanowire extensions 902 are formed by epitaxially growing, for example, in-situ doped silicon (Si) or a silicon germanium (SiGe) that may be either n-type or p-type doped. The in-situ doped epi process forms the source region and the drain region of the nanowire FET. As an example, a chemical vapor deposition (CVD) reactor may be used to perform the epitaxial growth. Precursors for silicon epitaxy include $SiCl_4$, SiH_4 combined with HCL. The use of chlorine allows selective deposition of silicon only on exposed silicon surfaces. A precursor for SiGe may be GeH_4, which may obtain deposition selectivity without HCL. Precursors for dopants may include PH_3 or AsH_3 for n-type doping and B_2H_6 for p-type doping. Deposition temperatures may range from 550°C to 1000°C for pure silicon deposition, and as low as 300°C for pure Ge deposition.

FIGS. 9A-10B illustrate an exemplary method for fabricating complementary metal-oxide-semiconductors (CMOS) having both N-FETs and P-FETs fabricated on the same chip. Since N-FETs and P-FETs have nanowire extensions with different types of dopants, the N-FET device and P-FET device nanowire extensions are grown in separately. Referring to FIG. 9A, a P-FET and N-FET device is shown. The N-FET is covered with an epi blocking mask 1001 that blocks the growth from the exposed cross-sectional portions of the nanowire 110. The epi blocking mask 1001 may be, for example, a deposited oxide film that is patterned to cover the N-FET devices. The P-FET cross-sectional portions of the nanowire 110 are exposed allowing the formation of the p+ doped nanowire extensions 902P using a selective epitaxially grown silicon deposition process similar to the process described above. FIG. 9B illustrates a similar process as described in FIG. 9A for a plurality of N-FET and P-FET devices.

Referring to FIGS. 10A and 10B, following the growth of the p+ doped nanowire extensions 902P (in FIGS. 9A and 9B), the epi blocking masks 1001 are removed, and a second epi blocking mask 1101 is deposited and patterned to cover the P-FET and the p+ doped nanowire extensions 902P. Selective epitaxy with n-type in-situ doping is used to form the

n+ doped nanowire extensions 902N. Once the n+ doped nanowire extensions 902N are formed, the second epi blocking mask 1101 may be removed. The order by which the P-FET and N-FET nanowire extensions 902 are formed may be chosen to minimize diffusion of dopants in the first grown extension during the growth of the second nanowire extension. Thus, the epitaxy of the n+ doped nanowire extensions 902N may be formed prior to forming the p+ doped nanowire extensions 902P. Since the formation of the nanowire extensions 902 may be carried out in separate processing steps, the extensions composition may be different. For example, SiGe nanowire extensions may be formed for the P-FET devices while pure silicon nanowire extensions may be formed for the N-FET devices.

FIGS. 11A and 11B illustrate an example of the resultant structures following a thermal process (performed after the growth of the nanowire extensions 902 described above) that diffuses the doped ions from the nanowire extensions 902 into the regions 1202 of the nanowires 110 that are surrounded by the spacer walls 604 and the gates 404 to overlap the device. The nanowire extensions 902 are uniformly doped when grown; resulting in a uniform doping profile in the regions 1202 of the nanowires 110 following diffusion of the ions from the nanowire extension 902 into the regions 1202. For the CMOS devices (described above in FIGS. 9A-10B), a similar thermal process may be performed. When the n-type and p-type dopant diffusion properties are similar, similar doped regions of the nanowires 110 for both PFET and NFET devices will result. When the n-type and p-type dopant diffusion properties are dissimilar, the penetration of the n-type and p-type dopants may result in dissimilar regions 1202 in the nanowires 110. The thermal process may be performed in a rapid thermal annealing (RTA) chamber. The thermal process may be performed, for example, at annealing temperatures between 900°C to 1100°C for 0-10 seconds in an ambient N_2 gas. The annealing temperature rate may range, for example, between 50°C/second to 300°C/second.

FIGS. 12A and 12B illustrate a resultant structure following silicidation where a silicide 1302 is formed on the nanowires extensions 902, and over the polysilicon layer 404. Examples of silicide forming metals include Ni, Pt, Co, and alloys such as NiPt. When Ni is used the NiSi phase is formed due to its low resistivity. For example, formation temperatures

include 400-600°C. Once the silicidation process is performed, capping layers and vias for connectivity (not shown) may be formed.

FIGS. 13A-14B illustrate an alternate exemplary method for forming a nanowire FET. The alternate exemplary method is similar to the method described above in FIGS. 1-12B. However, when the nanowires 110 are etched to remove the exposed portions of the nanowires 110, the etching process removes a portion of the nanowires 110 that are surrounded by the spacer walls 604 and the gates 402 to recess the nanowires 110 into the gates 402, and form cavities 1402 defined by the gates 402, the nanowires 110 and the spacer walls 604. FIGS. 13A and 13B illustrate a cross-sectional view of the resultant structure.

The lateral etching process that forms cavities 1402 may be time based. Width variation in spacer 604 may lead to variations in the position of the edges of the recessed nanowires 110. The etching rate in the cavity 1402 depends on the size of the cavity, with narrower orifice corresponding to slower etch rates. Variations in the nanowire size will therefore lead to variations in the depth of cavity 1402.

The variations described above may be reduced by bombarding the exposed ends of nanowire 110 with ions (e.g. silicon ions, germanium ions, and even dopants such as boron which do not amorphize) prior to the formation of the spacer 604 (in FIGS. 5A and 5B). The etching rate of the bombarded portions of nanowires 110 is several times faster than that of the un-exposed portion of nanowire 110 protected by gate material 402. As a result, the cavity 1402 becomes self-aligned with the sidewalls of gate 402 when etched.

If the deposition of spacer 604 is performed at an elevated temperature, the deposition process may anneal the exposed nanowire 110 portions (that have been bombarded with ions) and increase the etching resistance of the exposed nanowire 110 portion. For silicon nanowires 110, the spacer 604 may be formed at a low temperature, for example, less than 500°C to avoid annealing the bombarded portions of the nanowires 110. If other materials are used to form the nanowires 110 are used, the formation temperature of the spacer 604 may be higher. An alternative that accommodates high temperature deposition of spacer 604

includes performing an ion implantation at an oblique angle to the substrate 100 after the deposition of the spacer 604 with an ion energy that damages the portions of the nanowires 110 that are encapsulated by spacer 604.

Referring to FIGS. 14A and 14B, a cross-sectional view of the resultant structure having nanowire extensions 1502 that are formed from an in-situ doped epi-silicon growth process similar to the process described above in FIGS. 8A and 8B. The epi silicon growth began in the cavity 1402 (of FIGS. 13A and 13B) from the exposed nanowire 110 in the gate 402 to form the nanowire extensions 1502. Once nanowire extensions 1502 are formed, the doping may be activated by, for example, a laser or flash anneal process. The laser or flash annealing may reduce diffusion of ions into the channel region 1501 of the gate 402, and result in a high uniform concentration of doping in the nanowire extensions 1502 with an abrupt junction in the nanowires 110. Once the ions have been activated, silicidation similar to the process described in FIGS. 12A and 12B above may be performed and capping layers and vias for connectivity (not shown) may be formed.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one ore more other features, integers, steps, operations, element components, and/or groups thereof.

The corresponding structures, materials, acts, and equivalents of all means or step plus function elements in the claims below are intended to include any structure, material, or act for performing the function in combination with other claimed elements as specifically claimed. The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment

was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated

The diagrams depicted herein are just one example. There may be many variations to this diagram or the steps (or operations) described therein without departing from the invention. For instance, the steps may be performed in a differing order or steps may be added, deleted or modified. All of these variations are considered a part of the claimed invention.

While the preferred embodiment to the invention had been described, it will be understood that those skilled in the art, both now and in the future, may make various improvements and enhancements which fall within the scope of the claims which follow. These claims should be construed to maintain the proper protection for the invention first described.

CLAIMS

1. A method for forming a nanowire field effect transistor (FET) device, the method comprising:

forming a nanowire on a semiconductor substrate;

forming a first gate structure on a first portion of the nanowire;

forming a first protective spacer adjacent to sidewalls of the first gate structure and over portions of the nanowire extending from the first gate structure;

removing exposed portions of the nanowire left unprotected by the first spacer; and

epitaxially growing a doped semiconductor material on exposed cross sections of the nanowire to form a first source region and a first drain region.

2. The method of claim 1, wherein the method further includes:

forming a second gate structure on a second portion of the nanowire;

forming a second protective spacer adjacent to sidewalls of the second gate structure and over portions of the nanowire extending from the second gate structure;

removing exposed portions of the nanowire left unprotected by the second spacer;

depositing a first protective mask over the second gate structure and the second protective spacer prior to epitaxially growing a doped semiconductor material on exposed cross sections of the nanowire to form the first source region and the first drain region;

removing the first protective mask;

depositing a second protective mask over the first gate structure, the first protective spacer, the first source region, and the first drain region; and

epitaxially growing a doped semiconductor material on exposed cross sections of the nanowire of the second gate structure to form a second source region and a second drain region.

3. The method of claim 2, wherein the epitaxially grown doped semiconductor material of the first source region and the first drain region is a p-type doped material.

4. The method of claim 2, wherein the epitaxially grown doped semiconductor material of the second source region and the second drain region is an n-type doped material.

5. The method of claim 1, wherein the first gate structure includes a silicon oxide layer disposed on a channel portion of the nanowire, a dielectric layer disposed on the silicon oxide layer, and a metal layer disposed on the dielectric layer.

6. The method of claim 1, wherein the first gate structure is formed in circumferential layers over the gate portion of the nanowire.

7. The method of claim 1, wherein the first protective spacer includes a nitride material.

8. The method of claim 1, wherein the method further comprises heating the device to diffuse dopants from the doped semiconductor material into portions of the nanowire.

9. A method for a nanowire field effect transistor (FET) device, the method comprising:

forming a nanowire on a semiconductor substrate;

forming a gate structure on a portion of the nanowire;

forming a protective spacer adjacent to sidewalls of the gate structure and over portions of the nanowire extending from the gate structure;

removing exposed portions of the nanowire to form a cavity defined by the nanowire surrounded by the gate structure, the semiconductor substrate, and the spacer; and

epitaxially growing a doped semiconductor material in the cavity from exposed cross sections of the nanowire.

10. The method of claim 9, wherein the method further includes implanting exposed portions of the nanowire with ions prior to forming a protective spacer adjacent to sidewalls of the gate and over portions of nanowire extending from the gate.

11. The method of claim 9, wherein the method further includes implanting exposed portions of the nanowire with ions to increase the etching rate properties of the exposed portions of the nanowire prior to forming a protective spacer adjacent to sidewalls of the gate and over portions of nanowire extending from the gate.

12. The method of claim 9, wherein the protective spacer adjacent to sidewalls of the gate and over portions of nanowire extending from the gate is formed at a temperature less than 500 degrees Celsius.

13. The method of claim 9 or claim 1, wherein the epitaxially grown doped semiconductor material is an n-type doped material.

14. The method of claim 9 or claim 1, wherein the epitaxially grown doped semiconductor material is a p-type doped material.

15. The method of claim 9 or claim 1, wherein the epitaxially grown doped semiconductor material is silicon.

16. The method of claim 9 or claim 1, wherein the epitaxially grown doped semiconductor material is a SiGe alloy.

17. The method of claim 9, wherein the gate structure includes a silicon oxide layer disposed on a channel portion of the nanowire, a dielectric layer disposed on the silicon oxide layer, and a metal layer disposed on the dielectric layer.

18. The method of claim 9, wherein the gate structure is formed in circumferential layers on the gate portion of the nanowire.

19. The method of claim 9, wherein the protective spacer includes a nitride material.

20. The method of claim 9 or claim 1, wherein the epitaxially grown doped semiconductor material is an in-situ doped material.

21. The method of claim 9 or claim 1, wherein the epitaxially grown doped semiconductor material is uniformly doped.

22. A nanowire field effect transistor (FET) device, comprising:

a channel region including a silicon portion disposed on a semiconductor substrate having a first distal end extending from the channel region and a second distal end extending from the channel region, the silicon portion is partially surrounded by a gate structure disposed circumferentially on the silicon portion;

a source region including a first doped epi-silicon nanowire extension contacting the first distal end of the silicon portion; and

a drain region including a second doped epi-silicon nanowire extension contacting the second distal end of the silicon portion.

23. The device of claim 22, wherein the first and second epi-silicon nanowire extensions are uniformly doped with ions.

24. The device of claim 22, wherein a portion of the first distal end of the silicon portion is doped with ions diffused from the first epi-silicon nanowire extension and a portion of the second distal end of the silicon portion is doped with ions diffused from the second epi-silicon nanowire extension.

25. The device of claim 22, wherein the silicon portion is elliptically shaped.

26. The device of claim 22, wherein the silicon portion is cylindrically shaped.

27. A nanowire field effect transistor (FET) device, comprising:

a channel region disposed on a semiconductor substrate including a silicon portion having a first distal end and a second distal end, the silicon portion is surrounded by a gate structure disposed circumferentially on the silicon portion;

a first cavity defined by the first distal end of the silicon portion, the semiconductor substrate, and an inner diameter of the gate structure;

a second cavity defined by the second distal end of the silicon portion, the semiconductor substrate, and an inner diameter of the gate structure;

a source region including a first doped epi-silicon nanowire extension epitaxially extending from the first distal end of the silicon portion in the first cavity; and

a drain region including a second doped epi-silicon nanowire extension epitaxially extending from the second distal end of the silicon portion in the second cavity.

28. The device of claim 27, wherein the first epi-silicon nanowire extension fills the first cavity and second epi-silicon nanowire extension fills the second cavity.

29. The device of claim 27, wherein the first and second epi-silicon nanowires are uniformly doped.

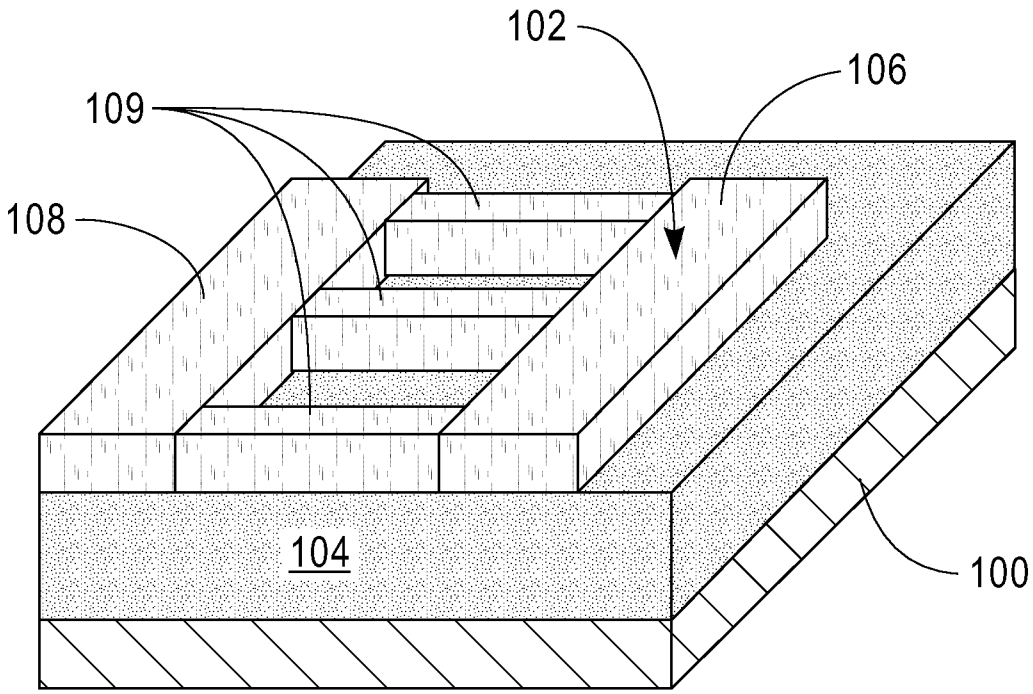

FIG. 1

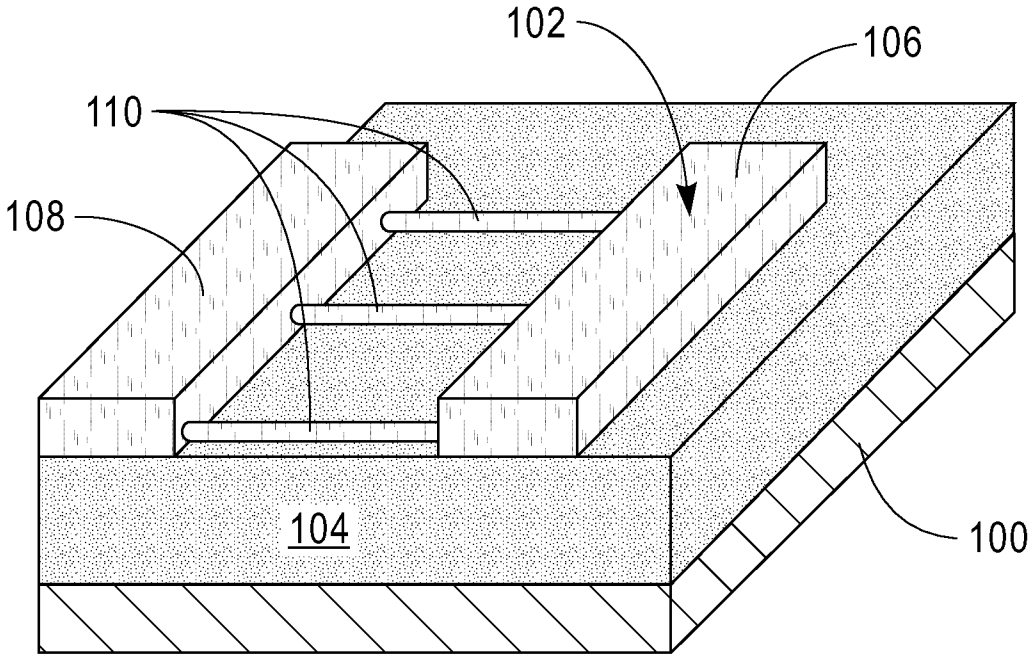
102
106
110
108
104
100

FIG. 2

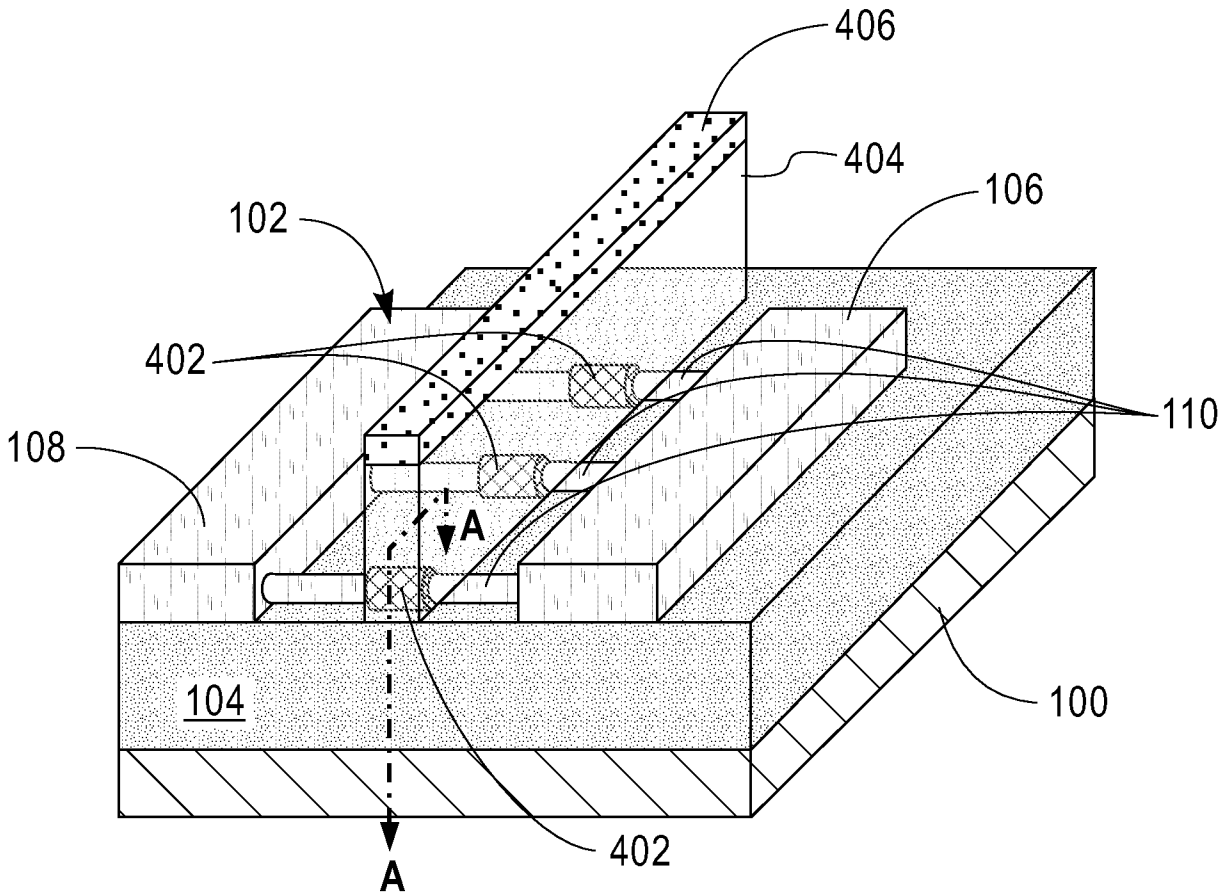
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FIG. 3A

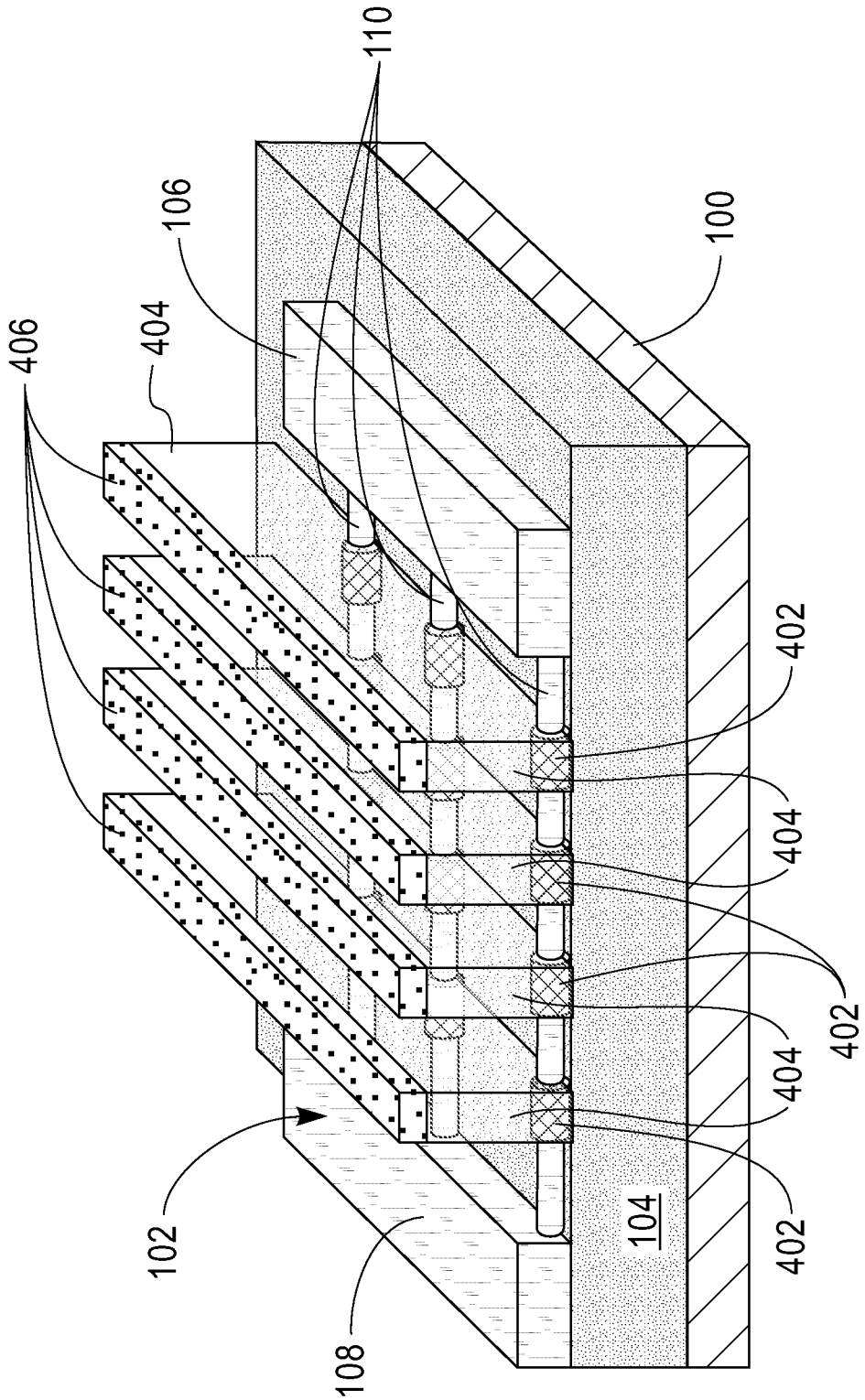

FIG. 3B

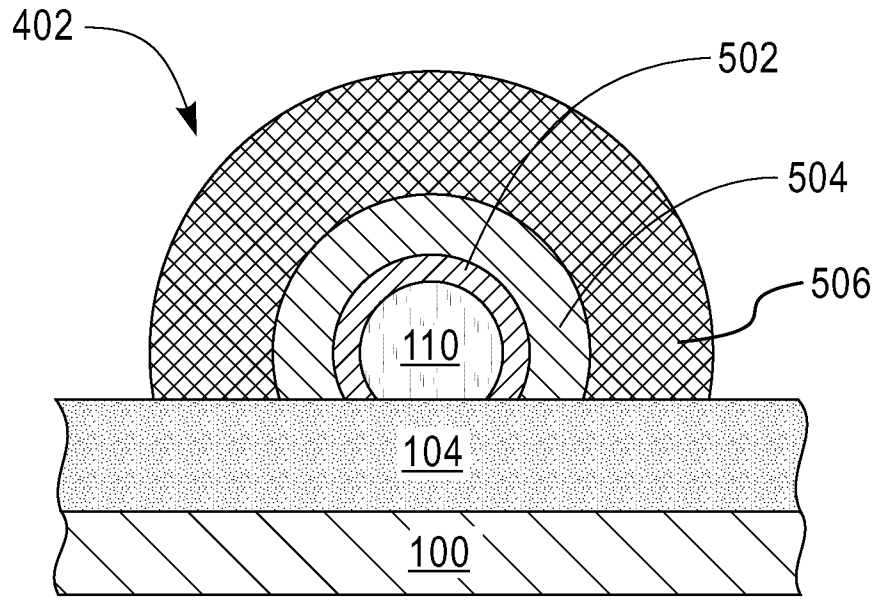

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FIG. 4

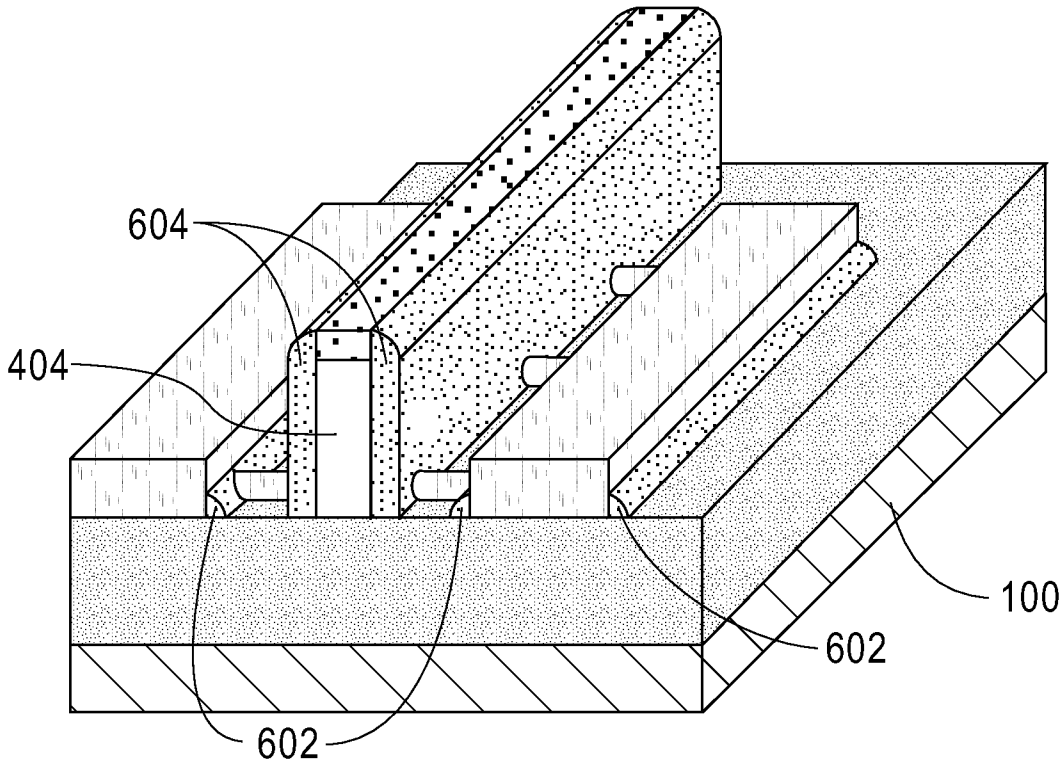
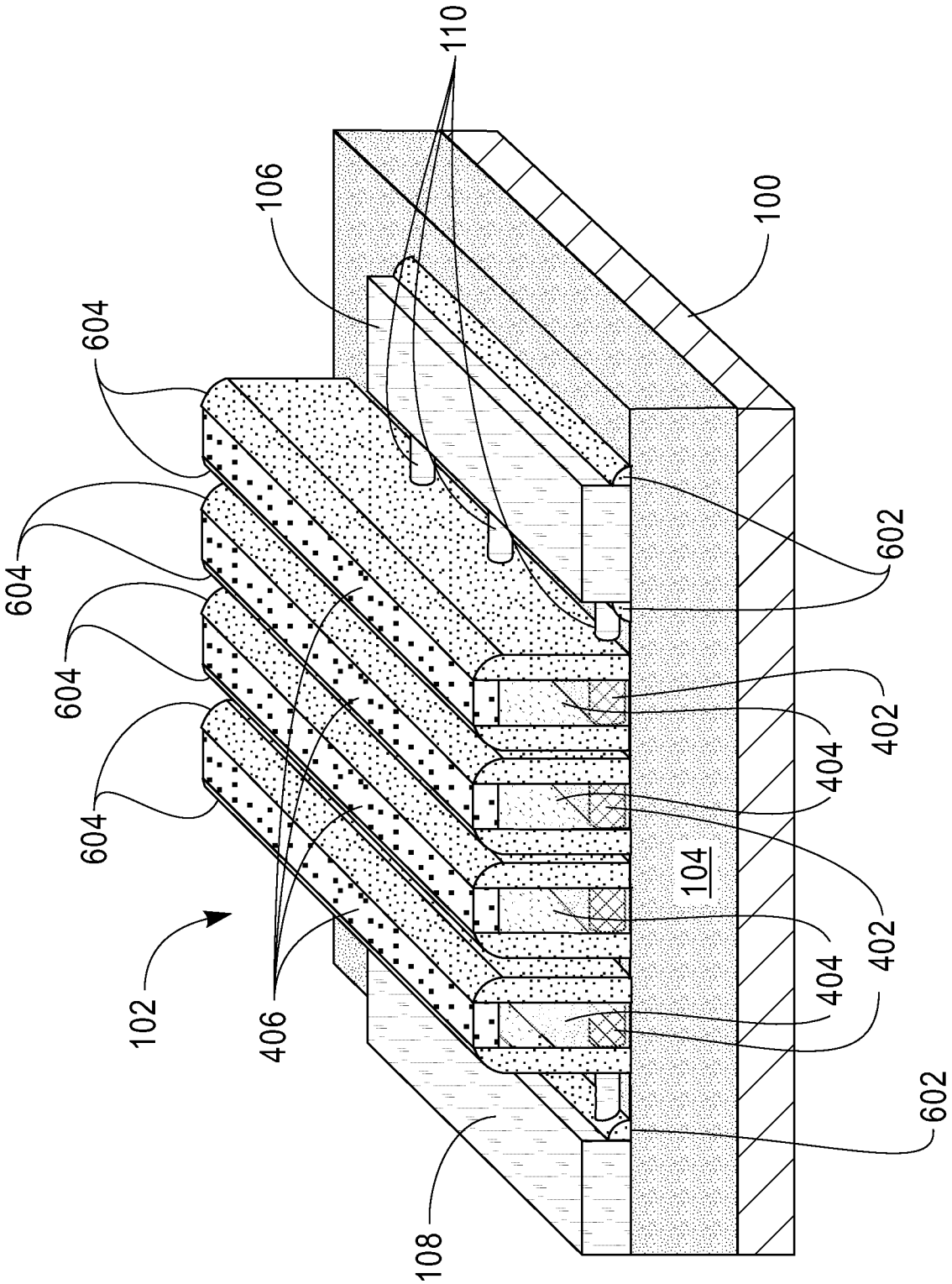


FIG. 5A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402
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602
104
102
406
108

FIG. 5B

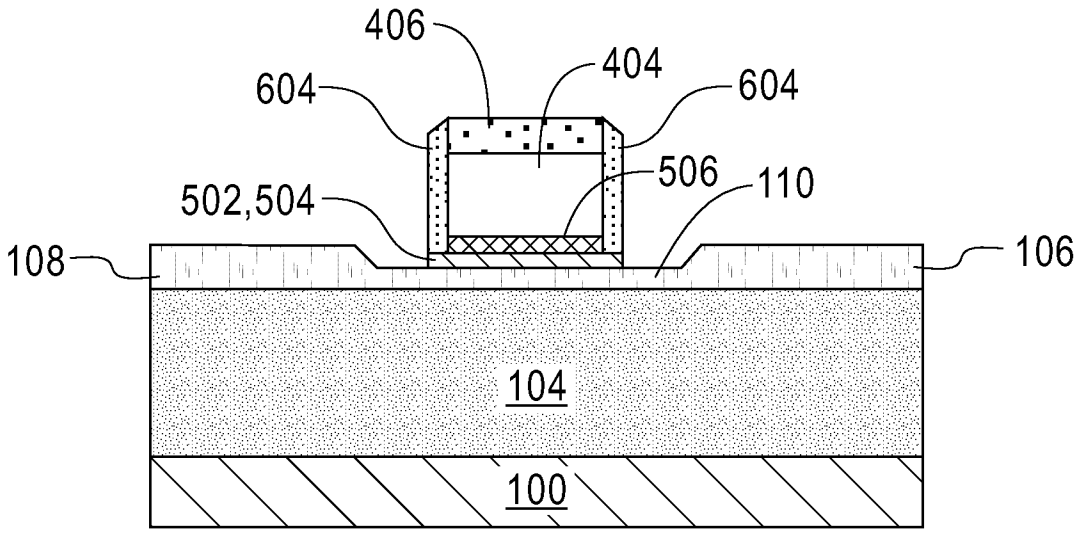
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FIG. 6A

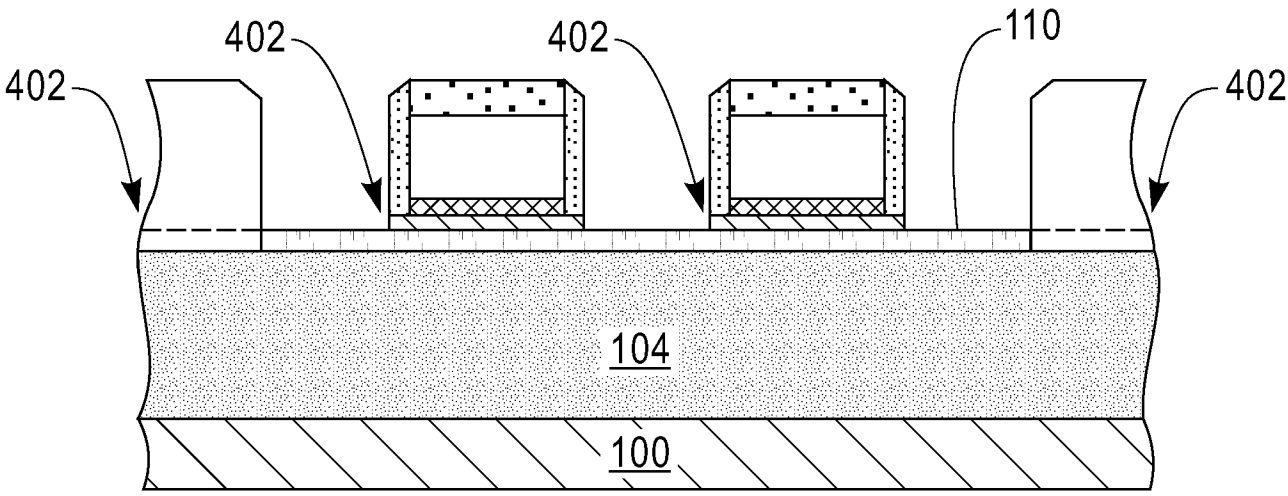
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FIG. 6B

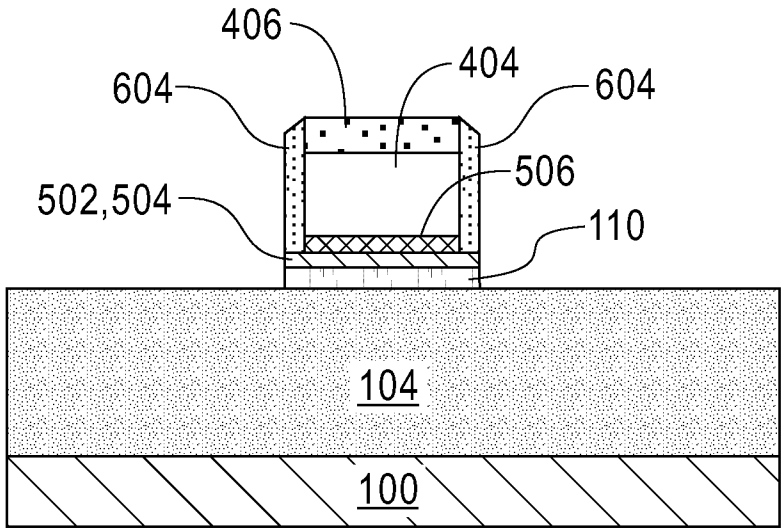

FIG. 7A

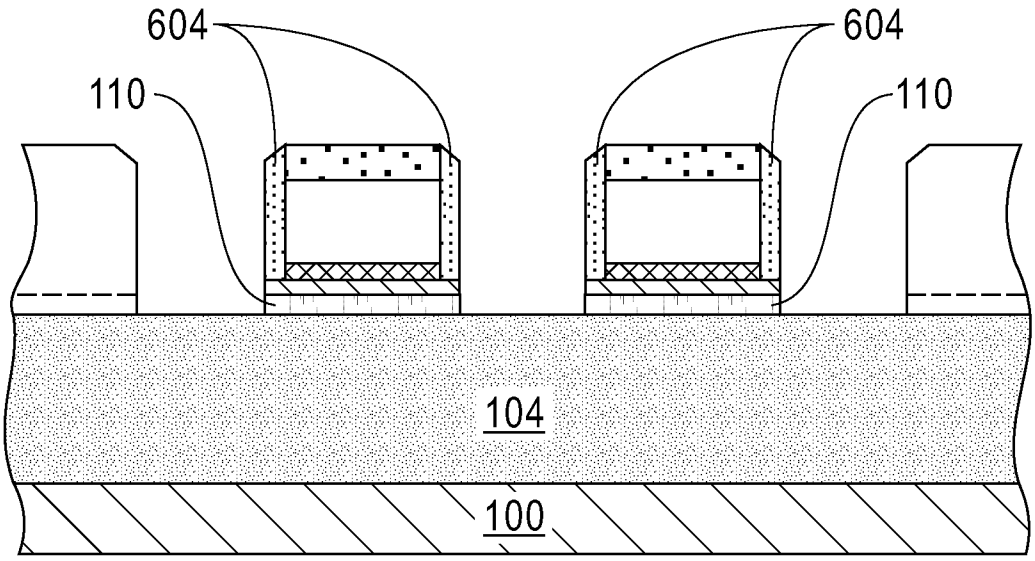

FIG. 7B

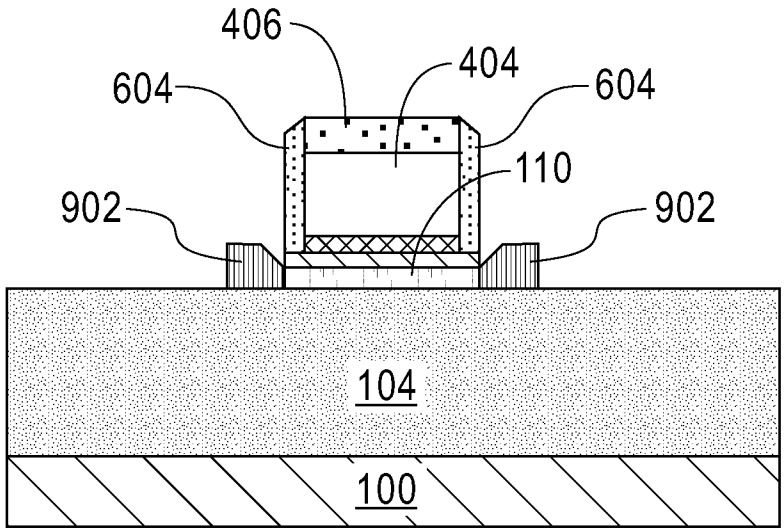
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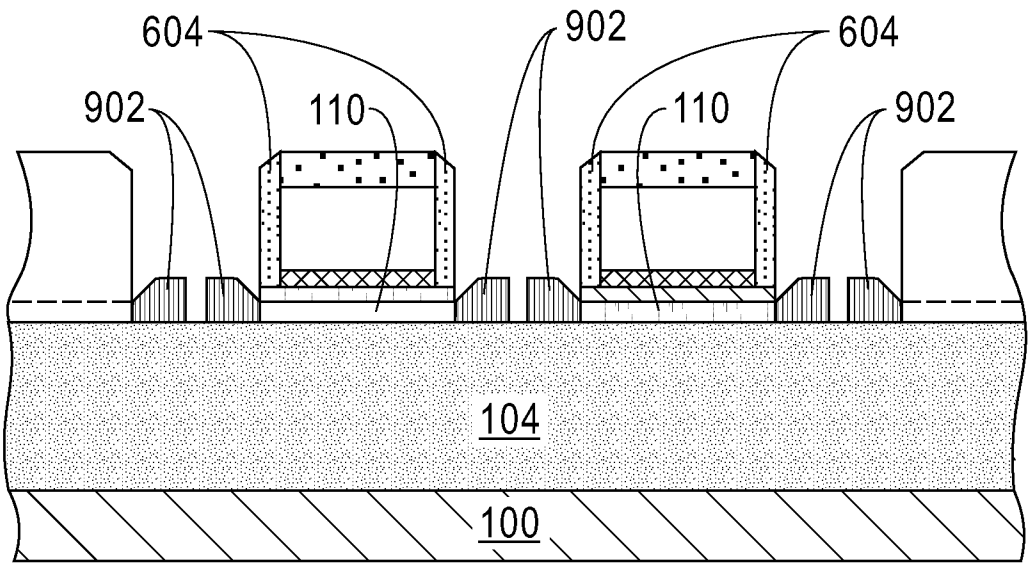
FIG. 8A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902
604
902
110
110
902
104
100

FIG. 8B

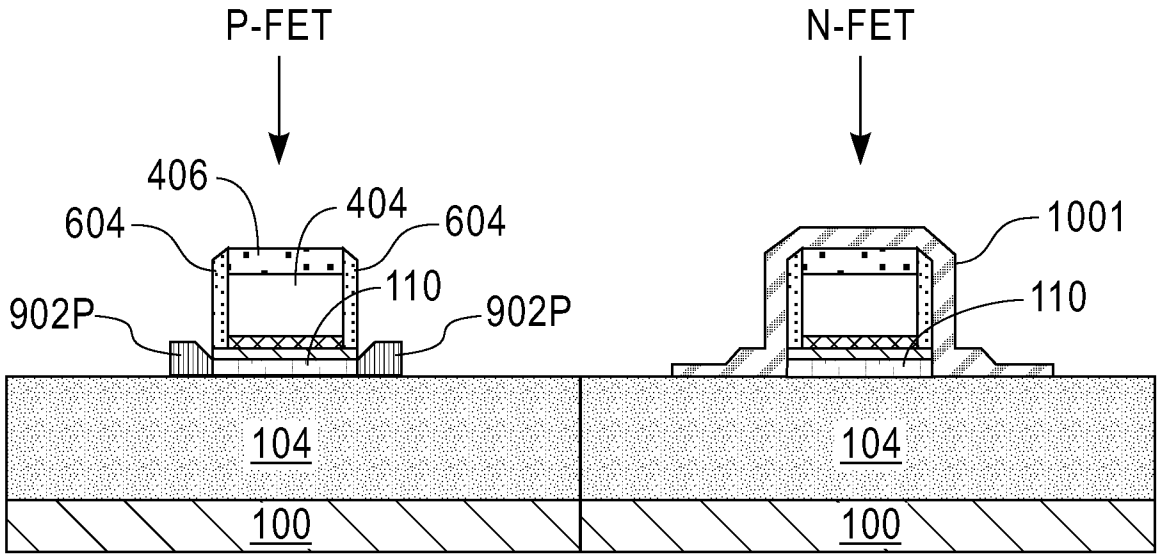
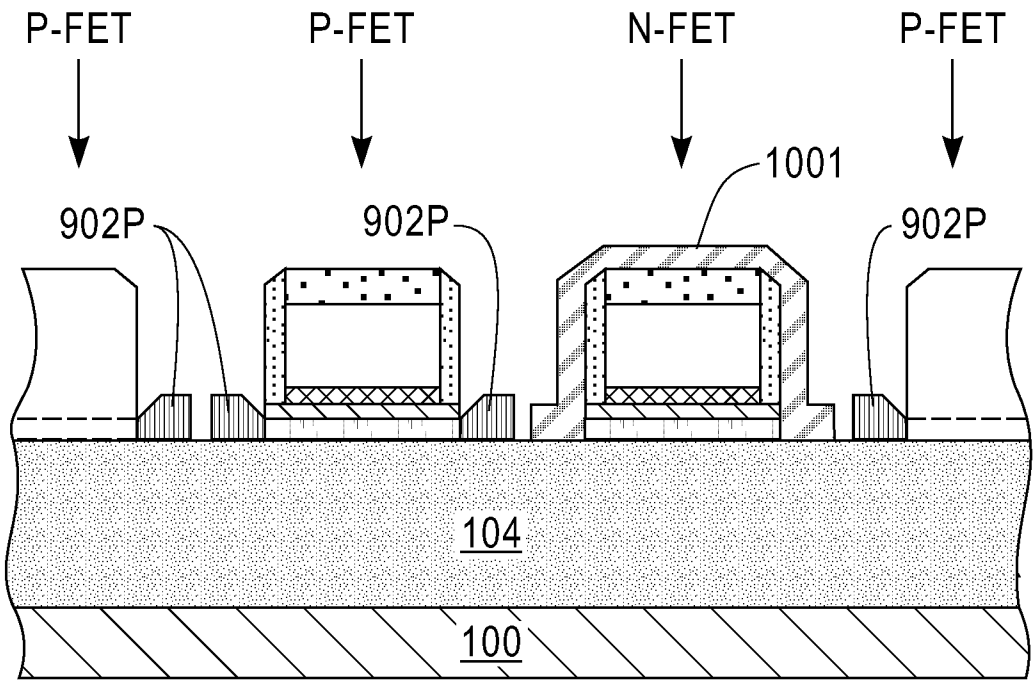

P-FET
N-FET
406
404
604
604
110
902P
902P
1001
110
104
104
100
100

FIG. 9A


P-FET
P-FET
N-FET
P-FET
1001
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902P
902P
104
100

FIG. 9B

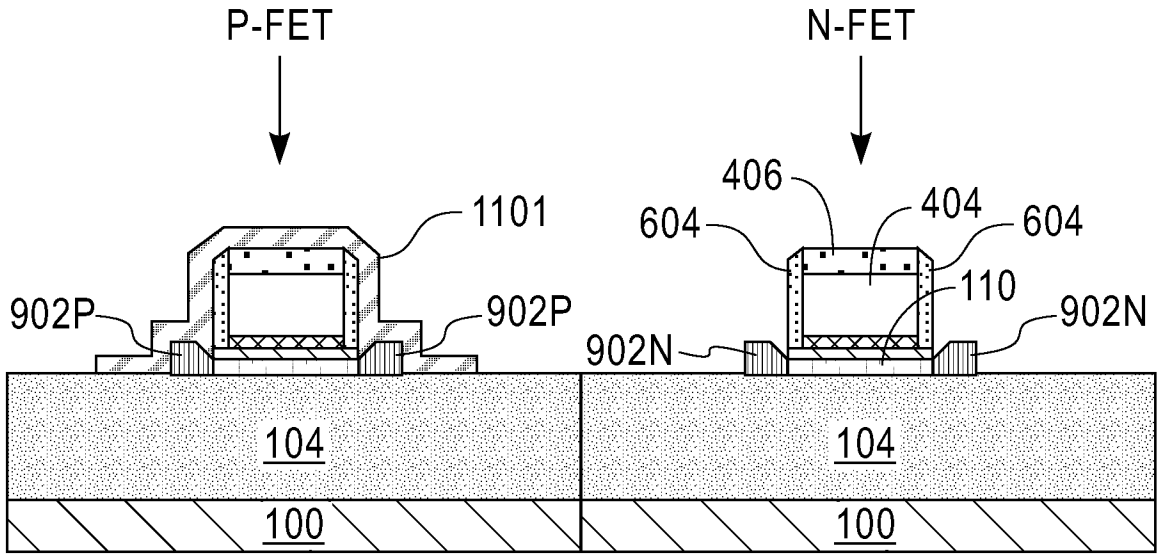

FIG. 10A

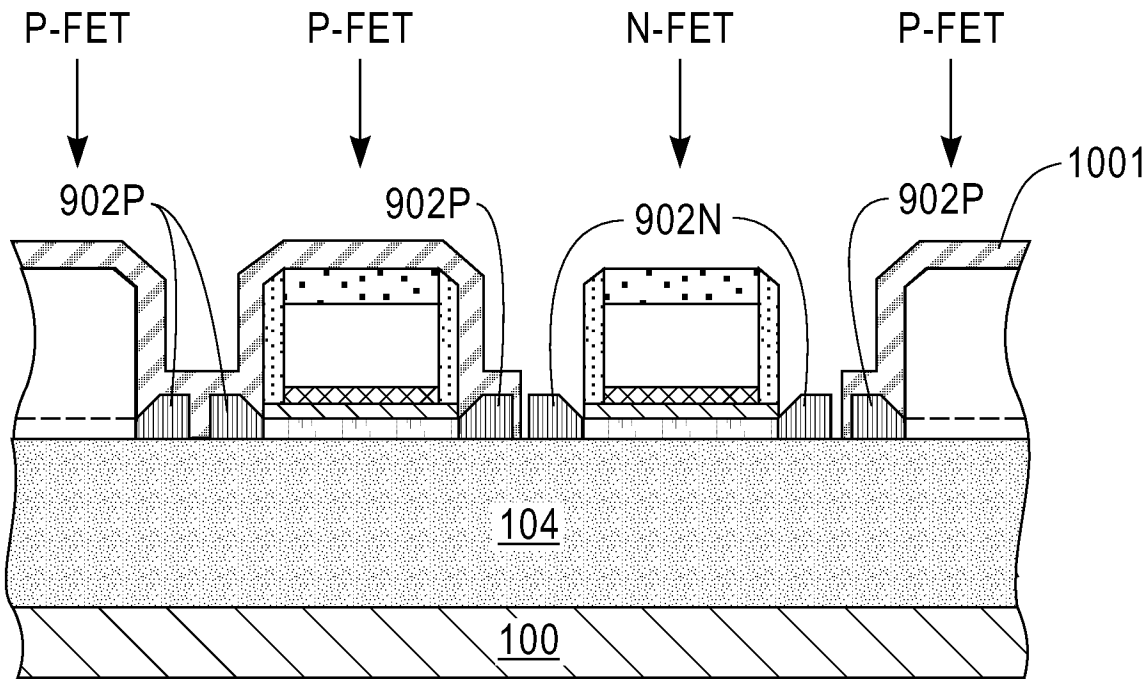

FIG. 10B

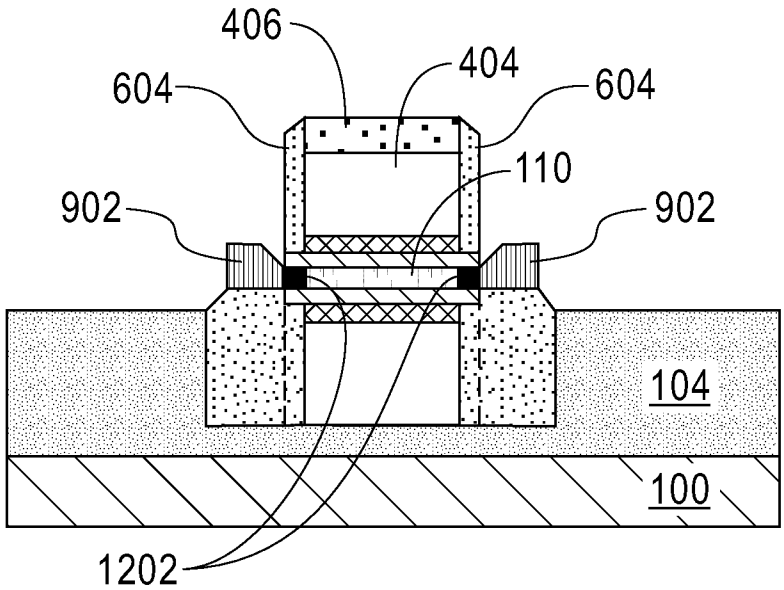

FIG. 11A

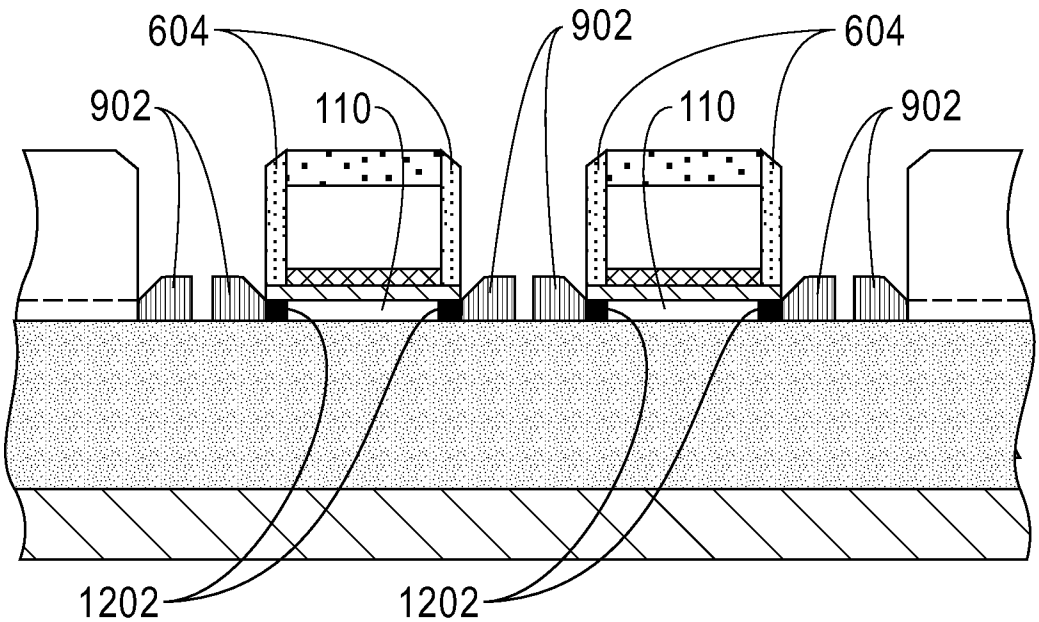

FIG. 11B

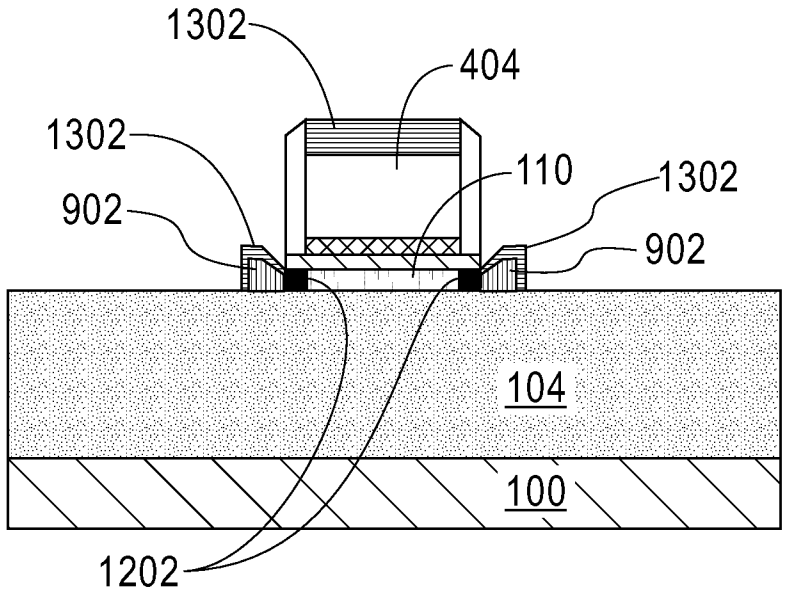

FIG. 12A

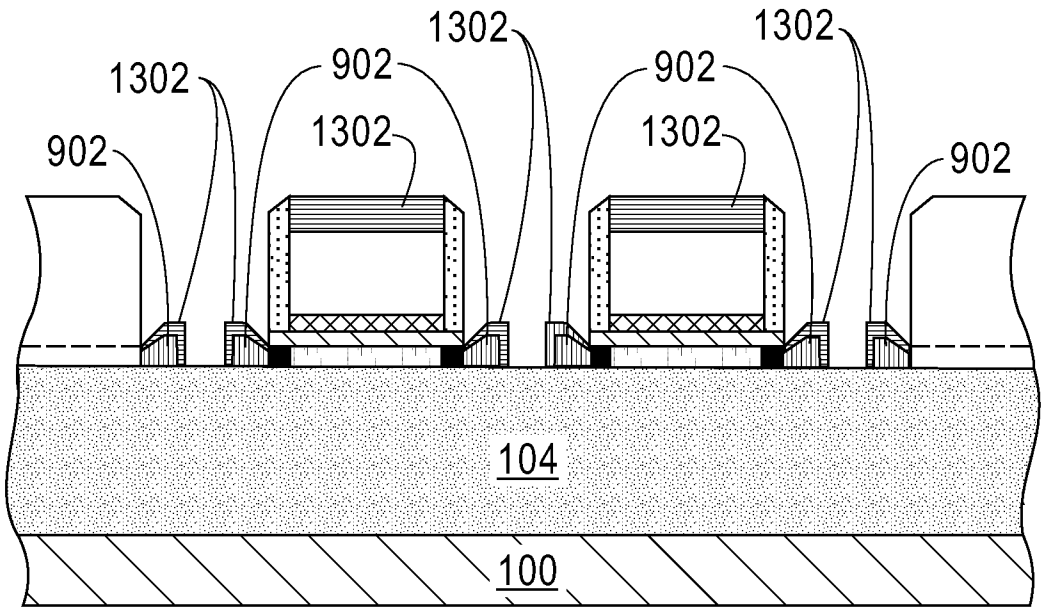

FIG. 12B

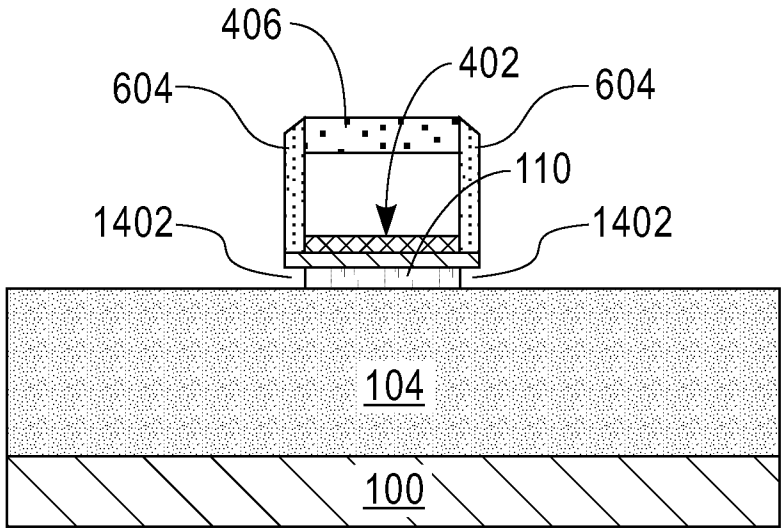

FIG. 13A

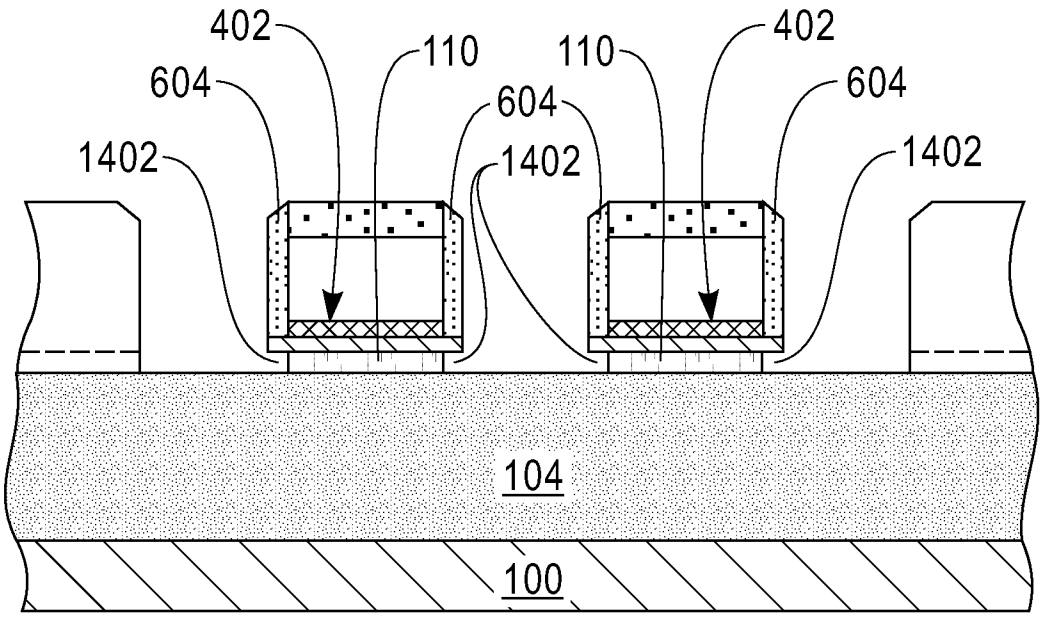

FIG. 13B

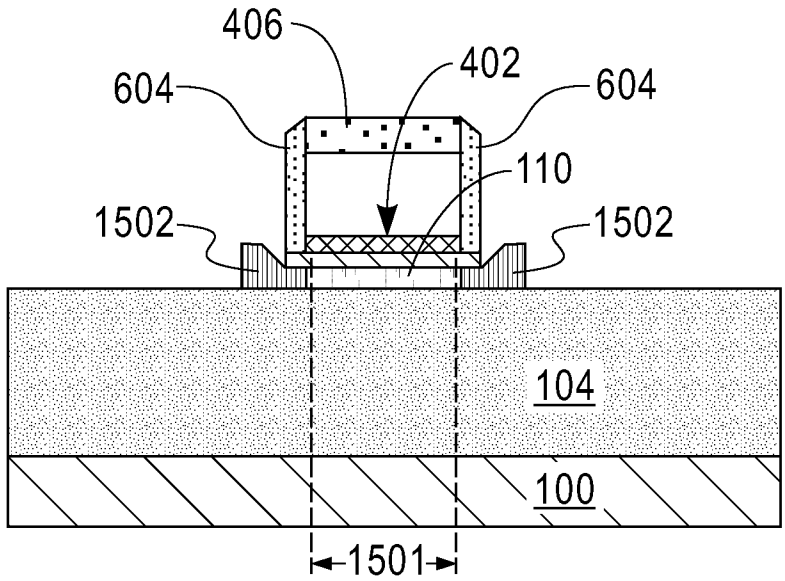

FIG. 14A

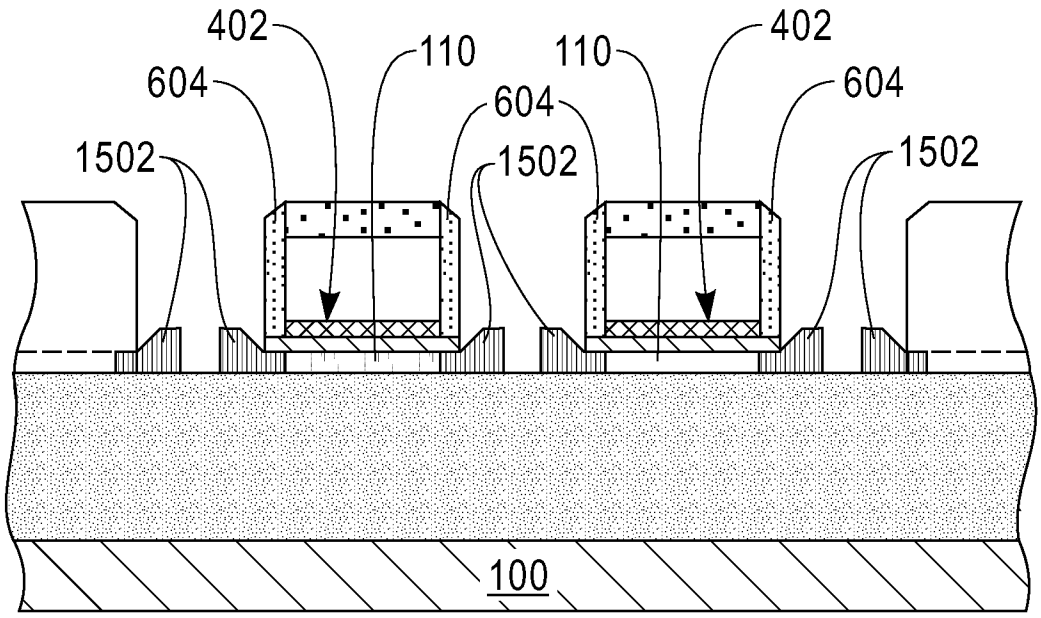

FIG. 14B

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/066961

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/335 H01L29/775
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/284613 A1 (CHUI CHI ON [US] ET AL) 13 December 2007 (2007-12-13) figure 7 and associated text paragraph [0024]	1-29

X	US 2008/061284 A1 (CHU JACK O [US] ET AL) 13 March 2008 (2008-03-13)	22-26
A	figures 5-9 and associated text	7,19

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Date of the actual completion of the international search	Date of mailing of the international search report
17 January 2011	10/02/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Moehl, Sebastian

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2010/066961

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	NEUDECK G W ED - INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "An overview of double-gate MOSFETs", PROCEEDINGS OF THE 15TH. BIENNIAL UNIVERSITY/GOVERNMENT/INDUSTRY MICROELECTRONICS. UGIM 2003. BOISE, ID, JUNE 30 - JULY 2, 2003, NEW YORK, NY : IEEE, US, 30 June 2003 (2003-06-30), pages 214-217, XP010655063, DOI: DOI:10.1109/UGIM.2003.1225728 ISBN: 978-0-7803-7972-5	22-26
A	figure 11 and associated text	1-21, 27-29

A	US 2008/179752 A1 (YAMAUCHI TAKASHI [JP] ET AL) 31 July 2008 (2008-07-31) figures 30-37	2,7,10, 11,16,19

A	PAVANELLO ET AL: "Evaluation of triple-gate FinFETs with SiO2-HfO2-TiN gate stack under analog operation", SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 51, no. 2, 7 March 2007 (2007-03-07), pages 285-291, XP005912674, ISSN: 0038-1101, DOI: DOI:10.1016/J.SSE.2007.01.012 page 289 paragraph "Conclusions"	5,17

A	US 2004/166642 A1 (CHEN HAO-YU [TW] ET AL) 26 August 2004 (2004-08-26) figures 3A, 7B, 7D	25,26

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Information on patent family members

International application No
PCT/EP2010/066961

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