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(54) **Title:** HIGH PERFORMANCE SURFACE MOUNT ELECTRICAL INTERCONNECT

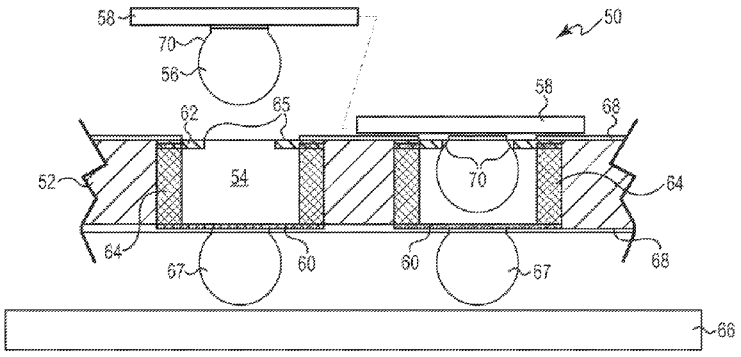

Fig. 1B

(57) **Abstract:** A surface mount electrical interconnect adapted to provide an interface between solder balls on a BGA device and a PCB. The electrical interconnect includes a socket substrate with a first surface, a second surface, and a plurality of openings sized and configured to receive the solder balls on the BGA device. A plurality of electrically conductive contact tabs are bonded to the first surface of the socket substrate so that contact tips on the contact tabs extend into the openings. The contact tips electrically couple with the BGA device when the solder balls are positioned in the openings. Vias are located in the openings that electrically couple the contact tabs to contact pads located proximate the second surface of the socket substrate. Solder balls are bonded to the contact pad that are adapted to electrically and mechanically couple the electrical interconnect to the PCB.

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HIGH PERFORMANCE SURFACE MOUNT ELECTRICAL INTERCONNECT

Technical Field

[0001]The present disclosure relates to a high performance electrical interconnect between an integrated circuit device and a printed circuit board. The present disclosure also discloses the use of unique fabrication techniques that merge processes used in the printed circuit and semiconductor packaging industries with the flexibility of additive printing technology to make the present surface mount electrical interconnect.

Background of the Invention

[0002] Traditional IC sockets are generally constructed of an injection molded plastic insulator housing that includes stamped and formed copper alloy contact members stitched or inserted into recesses. The assembled IC socket is then generally processed through a reflow oven to attach solder balls to the contact members. During final assembly the contact pads on the printed circuit board ("PCB") are printed with solder paste or flux and the solder balls on the IC socket are placed in registration with the contact pads. The assembly is then reflowed and the solder balls essentially weld the IC socket to the PCB.

[0003] During use IC socket receives an IC device, such as a packaged integrated circuits. The contact members electrically couple the terminals on the IC device with the corresponding terminal on the PCB. The terminals on the IC device are typically held against the contact members by applying a load, which is expected to maintain intimate contact and reliable circuit connection throughout the life of the system without a permanent connection. As a result, the IC device can be removed or replaced without the need for reflowing solder connections.

[0004] These types of IC sockets and interconnects have been produced in high volume for many years. As IC devices advance to next generation architectures traditional IC sockets have reached mechanical and electrical limitations that require alternate methods. For example, increased terminal count, reduction in the distance between the contacts known as terminal pitch, and signal integrity have been the main drivers that impact the IC socket design. As terminal counts go up, the IC package essentially gets larger due to the additional space needed for the terminals.

As the package grows larger, costs go up and the relative flatness of the package and corresponding PCB require compliance between the contact members in the IC socket and the terminal pad to accommodate the topography differences and maintain reliable connection.

[0005]As the terminal pitch is decreased the thickness of the insulating walls in the IC socket housing is also decreased. The length of the contact members is frequently increased to optimize the spring properties. Longer contact members also tend to reduce signal integrity and increase contact resistance due to self-heating of power delivering contacts. The thinner insulating walls increase the difficulty of molding and increase latent stresses in the IC socket housing, increasing the risk of warpage during solder reflow. The thinner insulating walls also increase the risk of cross-talk between adjacent contact members.

[0006] Traditional IC sockets have reached an electrical performance limit. Next generation IC devices will operate above 5 GHz and beyond and the existing IC sockets do not provide acceptable performance levels without significant revision.

Brief Summary of the Invention

[0007] The present disclosure is directed to a high performance electrical interconnect that will enable next generation electrical performance. The present solution mimics the mechanical details of a simple beam structure made of traditional materials, and removes the normal retention features which add parasitic mass and distort or degrade the integrity of the signal as it passes through the contact. This approach provides a reliable connection to BGA devices and creates a platform to add electrical and mechanical enhancements to the socket substrate or assembly to address the challenges of next generation interconnect requirements.

[0008] The present disclosure merges the long-term performance advantages of traditional PCB and semiconductor packaging with the flexibility of additive printing technology. By combining methods used in the PCB fabrication and semiconductor packaging industries, the present disclosure enables fine line high density circuit structures with attractive cost of manufacture.

[0009] The present disclosure includes adding a bulk material to create the vias and other circuit geometry to supplement or replace the traditional circuit production techniques. This approach enables the production of very small low resistance vias to increase density and reduce line and feature pitch of the circuits as well as a host

of electrical enhancements that provide an electrical interconnect that may prove to be superior to the traditional methods.

[0010] The present high performance electrical interconnect can be treated as a system of its own by incorporating electrical devices or other passive and active function, such as for example, ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. In some embodiments, the electrical devices can be formed using printing technology, adding intelligence to the interconnect assembly.

[001 1]The present high performance electrical interconnect can be produced digitally, without tooling or costly artwork. The high performance electrical interconnect can be produced as a "Green" product, with dramatic reductions in environmental issues related to the production of conventional flexible circuits.

[0012] The vias and associated circuit geometry can be printed in a variety of shapes and sizes, depending on the terminal structure on the circuit members. The contact members and vias can be positioned at a variety of locations, heights, or spacing to match the parameters of existing connections.

[0013]The use of additive printing processes permits the material set in a given layer to vary. Traditional PCB and flex circuit fabrication methods take sheets of material and stack them up, laminate, and/or drill. The materials in each layer are limited to the materials in a particular sheet. Additive printing technologies permit a wide variety of materials to be applied on a layer with a registration relative to the features of the previous layer. Selective addition of conductive, non-conductive, or semi-conductive materials at precise locations to create a desired effect has the major advantages in tuning impedance or adding electrical function on a given layer. Tuning performance on a layer by layer basis relative to the previous layer greatly enhances electrical performance.

[0014]The circuit geometry preferably has conductive traces that have substantially rectangular cross-sectional shapes, corresponding to the recesses. The use of additive printing processes permits conductive material, non-conductive material, and semi-conductive material to be located on a single layer.

[0015] In one embodiment, pre-formed conductive trace materials are located in the recesses. The recesses are than plated to form conductive traces with substantially

rectangular cross-sectional shapes. In another embodiment, a conductive foil is pressed into at least a portion of the recesses. The conductive foil is sheared along edges of the recesses. The excess conductive foil not located in the recesses is removed and the recesses are plated to form conductive traces with substantially rectangular cross-sectional shapes.

[0016] At least one electrical device is optionally printed on a dielectric layer and electrically coupled to at least a portion of the circuit geometry. Optical quality materials can be printed or deposited in at least a portion of the recesses to form optical circuit geometries. Alternatively, optical fibers can be located in the recesses.

[0017] The printing process permits the fabrication of functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[0018] One embodiment is directed to a surface mount electrical interconnect adapted to provide an interface between solder balls on a BGA device and a PCB. The electrical interconnect includes a socket substrate with a first surface, a second surface, and a plurality of openings sized and configured to receive the solder balls on the BGA device. A plurality of electrically conductive contact tabs are bonded to the first surface of the socket substrate so that contact tips on the contact tabs extend into the openings. The contact tips electrically couple with the BGA device when the solder balls are positioned in the openings. Vias are located in the openings that electrically couple the contact tabs to contact pads located proximate the second surface of the socket substrate. Solder balls are bonded to the contact pads that are adapted to electrically and mechanically couple the electrical interconnect to the PCB.

[0019] The electrical interconnect optionally includes at least one dielectric layer printed or laminated on the first surface of the socket substrate to mechanically support the contact tabs. In one embodiment, the dielectric layer extends into the openings to mechanically engage with the solder balls on the BGA device. In

another embodiment, the dielectric layer is configured to bias the solder balls on the BGA device toward the contact tips.

[0020] In one embodiment, each opening includes a plurality of conductive contact tabs electrically and mechanically coupled to the vias that extend into the openings in a spaced configuration. The plurality of conductive tabs are preferably arranged to simultaneously engage a top portion, a center diameter, and a lower portion of the solder balls on the BGA device. In one embodiment, the contact tabs are a planar structure that is folded to fit in the openings and to form the plurality of conductive tabs. In another embodiment, the contact tabs include a pair of opposing spring arms adapted to flex outward during insertion of the solder balls on the BGA device into the openings.

[0021]The electrical interconnect also permits at least one dielectric layer to be printed on one of the first or second surfaces of the socket substrate. The dielectric layer is printed to include a plurality recesses. A conductive material is deposited in at least a portion of the recesses to create a circuit geometry that electrically couples at least two of the contact tabs. The conductive material can be one of sintered conductive particles or a conductive ink. In another embodiment, optical quality material is located in the recesses.

[0022] In one embodiment, the dielectric layer is an additional circuitry plane selected from one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, or a flexible circuit. At least one electrical device is optionally printed on the socket substrate and electrically coupled to at least a one of the contact tabs. The electrical device can be selected from one of shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded IC devices, RF antennae, and the like.

[0023] The present disclosure is also directed to an electrical assembly including a housing retaining the present electrical interconnect. Solder balls on a BGA device are located in the openings in the socket substrate and electrically coupled to the contact tips of the contact tabs. A PCB is soldered to the contact pads located at the second surface of the socket substrate.

[0024] The present disclosure is also directed to a method of making a surface mount electrical interconnect adapted to provide an interface between solder balls on a BGA device and a PCB. The method comprising the steps of forming a socket

substrate with a first surface, a second surface, and a plurality of openings sized and configured to receive the solder balls on the BGA device. A plurality of electrically conductive contact tabs are bonded to the first surface of the socket substrate so that contact tips on the contact tabs extend into the openings. The contact tips are electrically coupled with the BGA device when the solder balls are positioned in the openings. Vias are formed in the openings that electrically couple the contact tabs to contact pads located proximate the second surface of the socket substrate. Solder balls are attached to the contact pad to electrically and mechanically couple the electrical interconnect to the PCB.

Brief Description of the Several Views of the Drawing

[0025] Figures 1A and 1B illustrate a surface mount electrical interconnect in accordance with an embodiment of the present disclosure.

[0026] Figures 2B and 2B illustrate an alternate surface mount electrical interconnect with supported contact tabs in accordance with an embodiment of the present disclosure.

[0027] Figures 3A and 3B illustrate an alternate surface mount electrical interconnect with polymeric retention tabs in accordance with an embodiment of the present disclosure.

[0028] Figures 4A and 4B illustrate a surface mount electrical interconnect with a lateral biasing structure in accordance with an embodiment of the present disclosure.

[0029] Figures 5A and 5B illustrate a surface mount electrical interconnect with multiple layers of connection in accordance with an embodiment of the present disclosure.

[0030] Figures 6A and 6B illustrate an alternate surface mount electrical interconnect with multiple layers of connection in accordance with an embodiment of the present disclosure.

[0031] Figures 7A and 7B illustrate alternate contact structures in accordance with an embodiment of the present disclosure.

[0032] Figure 8 illustrates an electrical interconnect with on-board electrical devices in accordance with an embodiment of the present disclosure.

[0033] Figure 9 illustrates an alternate electrical interconnect with on-board electrical devices in accordance with an embodiment of the present disclosure.

[0034] Figure 10 illustrates an electrical interconnect with capacitive coupling in accordance with an embodiment of the present disclosure.

[0035] Figure 11 is a cross-sectional view of a method of making high performance electrical interconnects in accordance with an embodiment of the present disclosure.

[0036] Figure 12 illustrates via formation on the high performance electrical interconnect of Figure 11.

[0037] Figure 13 illustrates application to a second circuitry layer to the high performance electrical interconnect of Figure 11.

[0038] Figure 14 illustrates an alternate method of making an electrical interconnect in accordance with an embodiment of the present disclosure.

[0039] Figure 15 illustrates application of a second circuitry layer to the electrical interconnect of Figure 14.

[0040] Figure 16 illustrates another method of making an electrical interconnect in accordance with an embodiment of the present disclosure.

[0041] Figure 17 illustrates via formation on the electrical interconnect of Figure 16.

[0042] Figure 18 illustrates an electrical interconnect with bulk metal deposited in recesses to form the vias in accordance with an embodiment of the present disclosure.

[0043] Figure 19 illustrates an electrical interconnect with recesses filed with conductive particles as the vias in accordance with an embodiment of the present disclosure.

[0044] Figure 20 is a side sectional view of an electrical interconnect in accordance with an embodiment of the present disclosure.

[0045] Figure 21 is a side sectional view of an alternate electrical interconnect with printed compliant material in accordance with an embodiment of the present disclosure.

[0046] Figure 22 illustrates an electrical interconnect with optical features in accordance with an embodiment of the present disclosure.

[0047] Figure 23 illustrates an alternate high performance electrical interconnect with optical features in accordance with an embodiment of the present disclosure.

[0048] Figure 24 illustrates an alternate high performance electrical interconnect with printed vias in accordance with an embodiment of the present disclosure.

[0049] Figure 25 illustrates an alternate high performance electrical interconnect with printed electrical devices in accordance with an embodiment of the present disclosure.

[0050] Figure 26 illustrates an alternate high performance electrical interconnect with printed compliant electrical pads to plug into another connector in accordance with an embodiment of the present disclosure.

Detailed Description of the Invention

[0051] A high performance electrical interconnect according to the present disclosure may permit fine contact-to-contact spacing (pitch) on the order of less than 1.0 mm pitch, and more preferably a pitch of less than about 0.7 millimeter, and most preferably a pitch of less than about 0.4 millimeter. Such fine pitch high performance electrical interconnects are especially useful for communications, wireless, and memory devices.

[0052] The present high performance electrical interconnect can be configured as a low cost, high signal performance interconnect assembly, which has a low profile that is particularly useful for desktop and mobile PC applications. IC devices can be installed and uninstalled without the need to reflow solder. The solder-free electrical connection of the IC devices is environmentally friendly.

[0053] Figures 1A and 1B are top and cross-sectional views of a surface mount electrical interconnect 50 in accordance with an embodiment of the present disclosure. Socket substrate 52 includes openings 54 sized to receive solder balls 56 on integrated circuit device 58. Copper contact pads 60 are located at the base of the socket substrate 52. The contact pads 60 typically include solder balls 67 that can be reflowed to electrically and mechanically couples the electrical interconnect 50 to PCB 66.

[0054] Contact tabs 62 are located on the top surface of the socket substrate 52 and vias 64 electrically connecting the contact pads 60 to the contact tabs 62. The contact tabs 62 are preferably an etched or stamped foil of copper or copper alloy that is transferred to the socket substrate 52 using known techniques.

[0055] The contact tabs 62 include contact tips 65 that extend into the recess 54 and mimic points around the solder balls 56 spherical circumferences. Solder mask 68 is applied to the top and bottom of the socket substrate 52 so the contact tips 65 are exposed. The solder mask 68 also helps secure the contact tabs 62 to the substrate 52.

[0056] After insertion of BGA device 58, the contact tips 65 engage with solder balls 56 near the upper radius 70 proximate the interface to the BGA device 58. The resulting electrical interconnect 50 creates a very short physical height with good

electrical performance and an assembly process that does not require the insertion of individual contacts.

[0057] The electrical interconnect 50 enables users to directly socket the BGA device 58 without reflow to the PCB 66. In many cases, there is a desire to have the BGA device 58 removable and replaceable without the need for rework or reflow of the solder balls 56. The electrical interconnect 50 is soldered to the PCB 66, and the upper contact structures 62 are shaped to accept the solder balls 56 on the BGA device 58 in a manner that retains the device 58, but allows the device to be lifted out.

[0058] One challenge with this type of electrical interconnect 50 is to create an interface between the solder balls 56 on the BGA device 58 and the contact tips 65 such that the BGA device 58 can be inserted with low enough force to enable insertion by hand, while still providing stable contact resistance and reliable connection. Related to this challenge is the extraction force relative to insertion force such that the BGA device 58 can be easily removed by hand or with the aid of a tool without breaking solder joints 67 between the contact pads 60 and the PCB 66, as well as the joint from the BGA device 58 to the solder balls 56 on the package.

[0059] The present designs leverage a technique which treats the socket substrate 52 as if it were a printed circuit board. The core area within a traditional printed circuit board is normally not utilized as circuit area and primarily serves as a mechanical support member for the fashioned circuitry. In the present electrical interconnect 50, however, the dielectric core is processed to provide recesses 54 for the solder ball 56 on a BGA package 58 to reside within after insertion into the electrical interconnect 50.

[0060] In alternate embodiments, a polymer layer with features designed to engage with the solder balls 56 after insertion can be added to assist with device retention, while in other embodiments an external retention mechanism can be used to hold the BGA device 58 into the socket 50 and maintain reliable electrical interconnection.

[0061] **While** the present electrical interconnect 50 permits the BGA device 58 to be removed without solder reflow, in another embodiment, the device solder balls 56 can also be reflowed and welded to the contact tips 65 to provide a permanent connection. For example, the BGA device 58 may be tested prior to reflowing the solder balls 56. Once the testing is successfully completed, the solder balls 56 can be reflowed to permanently attached the BGA device 58.

[0062] Figures 2A and 2B are top and cross-sectional views of a variation of the surface mount electrical interconnect 50 in accordance with an embodiment of the present disclosure. As best illustrated in Figure 2A, top surface mask 68 is replaced with film 82, such as a 1 mil polyimide or LCP film. The film 82 is configured with tabs 84 that extend into the openings 54 to assist with centering the solder balls 56 with the openings 54, as well as aid with retention. In another embodiment, the tabs 84 can be segmented in multiple places to dial in the insertion, retention, and extraction force. The tabs 84 also assist with engaging the solder balls 56 on the BGA device 58 with contact tips 65 and sealing the openings 54 to increase reliability.

[0063] Figures 3A and 3B illustrate an alternate contact structure 100 for use in the electrical interconnect 50 in accordance with an embodiment of the present disclosure. The contact structure 100 is configured as an annular ring with multiple contact points 102. In the illustrated embodiment, the contact structure is reduced to ½ oz copper or copper alloy foil (0.7 mil thick). The top film 104 includes tabs 106 with geometry to support the thin foil of the annular ring 100, yet still provides some relief notches to receive the solder balls 56.

[0064] Figures 4A and 4B illustrate an alternate contact structure 120 for use in the electrical interconnect 50 in accordance with an embodiment of the present disclosure. The contact structure 120 is configured to engage with only a portion of the solder ball 56 near the BGA device 58. The polymer film 122 is modified to include a tab 124 that provides biasing force 128.

[0065] In operation, the solder ball 56 essentially enters the recess 54 with little or no engagement with the contact tips 126. Thereafter, the tab 124 applies a biasing force 128 on the solder ball 56 toward the contact tips 126. In one embodiment, a supplemental biasing force 130 is applied to the BGA device 58 to maintain long term reliability and accommodate coefficient of thermal expansion and temperature cycles.

[0066] The geometry of the opening 132 in the polymer film 122 and the contact structure 120 can be modified in many ways to optimize electrical performance, contact deformation, engagement reliability etc.

[0067] The biasing force 128 optionally eliminates the need for the contact tips 126. For example, the contact tips 126 are eliminated to form an annular ring. The contact structure 120 is enlarged to extend further into the recess 54 so the biasing

force 128 brings the solder balls 56 into engagennent with the annular ring 120 at multiple contact tips 126.

[0068] Figures 5A and 5B illustrate an alternate electrical interconnect 150 with a plurality of contact structure 152A, 152B, 152C ("152") in accordance with an embodiment of the present disclosure. The contact structures 152 are configured to engage with only a portion of the solder ball 56 near the BGA device 58. The polymer film 154 is modified to include a tab 156 that provides biasing force 158, as discussed above.

[0069] In the illustrated embodiment, the contact structures 152B and 152C are embedded in the vias 64. The contact structure 152B is sized to engage the theoretical diameter "D" of the solder balls 56, and the contact structure 152C with the base "B" of the solder ball 56 with a slight interference. In the illustrated embodiment, each contact structure 152 includes five contact points 160 resulting in a total of fifteen contact points 160 engaged with the solder balls 56. In an alternate embodiment, the substrate 52 is a multilayered structure and the contact structures 152B, 152C are sandwiched between the layers as well as embedded in the via 64.

[0070] Figures 6A and 6B illustrate an alternate electrical interconnect 170 with a plurality of contact structure 172A, 172B, 172C ("172") in accordance with an embodiment of the present disclosure. The polymer film 174 is modified to include a tab 176 that provides biasing force 178, as discussed above.

[0071] The contact structure 172A is located at the top of the substrate 180. In the illustrated embodiment, the contact structure 172A includes a pair of opposing spring arms that flex apart as the solder balls 56 are inserted and the compressively engage the solder balls 56 when the BGA device 58 is engaged with the electrical interconnect 170. The contact structures 172B and 172C are embedded in the vias 182. The contact structure 172B is sized to engage the theoretical diameter "D" of the solder balls 56, and the contact structure 172C with the base "B" of the solder ball 56 with a slight interference.

[0072] *Jim can you explain this section? From a signal integrity standpoint, once the base model is completed, it would be possible to create a 3 X 3 grid with the center pin being a signal line, and the outer ground pins tied together at the contact layers. It may be a problem from a capacitive coupling to the package standpoint to have the upper most contact layer tied to ground. Multiple layers can be added to increase the number of contact points as desired through the stack, with annular ring*

type interfaces tied back to a common though via or a staggered via pattern which may ease routing restrictions and distribute capacitive and inductive effects of a common via structure.

[0073] *In addition to the planar contact structures discussed above, the present electrical interconnects can be complemented with more traditional stamped and formed contacts that are inserted discretely into the substrate openings and further processed to create the solder ball attachment structure.*

[0074] Figures 7A and 7B illustrate alternate contact structures 200A, 200B ("200") in accordance with an embodiment of the present disclosure. The illustrated contact structures 200 that can be stamped or etched. Center regions 202 operate as the contact pads 60 illustrated in Figure 1B. Two right-angle bends are formed at fold lines 204, 206 to create a three-dimensional structure that can be inserted into openings 54 in the substrate 52. In the illustrated embodiments, the contact structures 200 are annular rings with cut-outs 208 that permit arms 210 to flex outward during engagement and disengagement with solder balls 56.

[0075] Figure 8 illustrates electrical interconnect 220 with electrical devices 222, such as for example, internal decoupling capacitors, located on substrate 224 in accordance with an embodiment of the present disclosure. Printed conductive traces 226 electrically couple the electrical devices 222 to one or more of the contact pads 228. The electrical devices 222 can be added as discrete components or printed materials, reducing the need for discrete components on the PCB 232 and the integrated circuit device 230. Locating the electrical devices 222 in the semiconductor socket 220 permits integrated circuit manufactures to reduce or eliminate the capacitors currently located on the package 230 and printed circuit board 232. This shift can greatly reduce cost and simplify the package 230 and printed circuit board 232, while improving performance.

[0076] The electrical devices 222 can be a power plane, ground plane, capacitor, resistor, filters, signal or power altering and enhancing device, memory device, embedded IC, RF antennae, and the like. The electrical devices 222 can be located on either surface of the substrate 224, or embedded therein. The electrical devices 222 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like.

[0077] Locating such electrical devices 222 on the electrical interconnect 220 improves performance and enables a reduction in the cost of integrated circuit devices and the PCB 232. Integrated circuit manufactures are limited by the pitch that the PCB 232 can accommodate and still keep the printed circuit board to four layers. The integrated circuit makers can manufacture the integrated circuit device 230 with a smaller pitch, but with the pin counts is so high that the printed circuit board 232 likely requires additional layers in order to route all of the signals. The present electrical interconnect 220 also permits integrated circuit manufactures to reduce the pitch of the contacts on the IC device 230, and perform any required signal routing in the electrical interconnect 220, rather than in the printed circuit board 232 or by adding daughter boards to the system.

[0078] Figure 9 illustrates an alternate electrical interconnect 240 with on-board electrical devices 242 in accordance with an embodiment of the present disclosure. The decoupling capacitance 242 can be a discrete embedded or printed electrical device. Contact member 244 provides the electrical connection to the capacitor located on the semiconductor device 246 and solder ball 248 provides the electrical connection to the capacitor located on printed circuit board 250.

[0079] Figure 10 is a cross-sectional view of electrical interconnect 270 with various capacitive coupling features in accordance with another embodiment of the present disclosure. A capacitive coupling feature 272A is embedded in layer 274 of the substrate 275. A capacitive coupling feature 272B is located on second surface 276 of the layer 274. The capacitive coupling features 272A, 272B are positioned to electrically couple with contact pad 278 on integrated circuit device 280. The capacitive coupling 272C is embedded in layer 288.

[0080] Capacitive coupling feature 282A is embedded in layer 284 of the substrate 275. Capacitive coupling feature 282B is located on first surface 286 of the layer 284. The capacitive coupling feature 282A is positioned to electrically couple with contact pad 290 on the PCB 292. The various capacitive coupling features in the embodiment of Figure 10 are optionally formed using inkjet printing technology, aerosol printing technology, or other printing technology.

[0081] Figure 11 is a side cross-sectional view of a method of making an electrical interconnect 340 using additive processes in accordance with an embodiment of the present disclosure. The process starts similar to a traditional PCB with a first circuitry layer 352 laminated to a stiffening layer or core 350, such as glass-

reinforced epoxy laminate sheets (e.g., FR4). The first circuitry layer 352 can be preformed or can be formed using a fine line imaging step is conducted to etch the copper foil 352 as done with many PCB processes. One or more dielectric layers 354, 356 are printed or placed to the surface 358 such that the first circuitry layer 352 is at least partially encased and isolated. In some embodiments, it may be desirable to use a preformed dielectric film to leave air dielectric gaps between traces. Recesses 360 in the dielectric layer 356 to expose circuitry 352 can be formed by printing, embossing, imprinting, chemical etching with a printed mask, or a variety of other techniques.

[0082] As illustrated in Figure 12, bond points 362, such as for example stud bumps or soldier balls, are added to the exposed circuitry 352 with a traditional bonding machine used in semiconductor packaging applications. Historically, fine gold wire has been used for bonding, with copper seeing increased use in recent years due to the rise in the cost of gold.

[0083] As illustrated in Figure 13, second circuitry layer 364 is applied to the previous construction such that the bond points 362 are deformed to create the interconnecting vias 366 during the lamination operation. The size and shape of the bond points 362 can be tailored to the ideal condition for deformation without piercing the foil 364.

[0084] The second circuitry layer 364 can be pre-etched with the next circuit pattern or can be laminated as a sheet and etched post lamination. In addition, the dielectric material 356 can be left in a tack cure or partial cure state such that a final bond is achieved at final cure. If desired, the bond bumps 362 can be coined planar prior to adding the second circuitry layer 364.

[0085] Figures 14 and 15 illustrate an alternate interconnect 368 with preformed holes or breaks 370 in the first circuitry layer 372 in accordance with an embodiment of the present disclosure. The holes 370 permit the bond points 362 to extend into the openings 370 or reside near the openings 370 so plating solution 374 can enter the mating region to plate the via structure 376 together. The plating 374 is preferably a corrosion resistant metallic material such as nickel, gold, silver, palladium, or multiple layers thereof. One benefit of the present structure is the material set can be varied layer by layer or altered on a given layer to create some desired performance enhancement not possible with conventional construction.

[0086] Figures 16 and 17 illustrate an alternate construction in which bond points 380 are added to the circuitry 382 while it is planar, without upper dielectric layer 384 to provide clearance for the bonding tool to impact the circuitry 382 without encountering or damaging the dielectric 384. The bond points 380 can be coined en masse to planarize them either before or after the dielectric layer 384. In one embodiment, the dielectric layer 384 is added with the bond points 380 in place and then imaged to expose the vias 386 for subsequent application of the next pre-etched circuit layer to be placed and plated together (see e.g., Figures 12 and 14). The dielectric layer 384 can optionally be filled or doped with a near endless list of enhancement materials to lower dielectric constant, provide thermal management properties, create rigid, flexible, or compliant regions etc.

[0087] Figure 18 illustrates an alternate electrical interconnect 388 with solid bulk metal 390, such as copper or solder spheres, or plated copper, located in recesses 392 in dielectric layer 394 in accordance with an embodiment of the present disclosure. The bulk metal 390 electrically couples with the lower circuitry layer 396 and the upper circuitry layer 398 with slight deformation or material displacement. In one embodiment, the bulk metal 390 is plated, such as by flowing a plating solution through openings 400 in the upper circuitry 398. It may be possible to provide sufficient engagement to interconnect reliably without the need for plating since the bulk metal 390 is encased within dielectric 394 and environmentally sealed. In the event the bulk metal 390 is solder, the circuit layers 396, 398 can be interconnected when the solder 390 is reflowed with the dielectric 394 acting as a natural solder wicking barrier.

[0088] Figure 19 illustrates an alternate electrical interconnect 410 with reservoirs 412 between circuitry layers 414, 416 that can be filled with loose conductive particles 418 in accordance with an embodiment of the present disclosure. The conductive particles 418 can optionally be sintered, coined, tightly compacted, plated, mixed with an adhesive binder, etc. to create via 420. The method of Figure 19 can also be used to create the circuitry itself or supplement the etched foil structures. Use of reservoirs containing conductive particles is disclosed in commonly assigned PCT/US2010/36313 entitled Resilient Conductive Electrical Interconnect, filed May 27, 2010, which is hereby incorporated by reference.

[0089] Figure 20 illustrates an alternate electrical interconnect 430 with an insulating layer 432 applied to the circuit geometry 434. The nature of the printing process

allows for selective application of dielectric layer 432 to leave selected portions 436 of the circuit geometry 434 expose if desired. The resulting high performance electrical interconnect 430 can potentially be considered entirely "green" with limited or no chemistry used to produce beyond the direct write materials.

[0090] The dielectric layers of the present disclosure may be constructed of any of a number of dielectric materials that are currently used to make sockets, semiconductor packaging, and printed circuit boards. Examples may include UV stabilized tetrafunctional epoxy resin systems referred to as Flame Retardant 4 (FR-4); bismaleimide-triazine thermoset epoxy resins referred to as BT-Epoxy or BT Resin; and liquid crystal polymers (LCPs), which are polyester polymers that are extremely unreactive, inert and resistant to fire. Other suitable plastics include phenolics, polyesters, and Ryton® available from Phillips Petroleum Company.

[0091] In one embodiment, one or more of the dielectric materials are designed to provide electrostatic dissipation or to reduce cross-talk between the traces of the circuit geometry. An efficient way to prevent electrostatic discharge ("ESD") is to construct one of the layers from materials that are not too conductive but that will slowly conduct static charges away. These materials preferably have resistivity values in the range of 10^5 to 10^{11} Ohm-meters.

[0092] Figure 21 illustrates an alternate high performance electrical interconnect 450 in accordance with an embodiment of the present disclosure. Dielectric layer 452 includes openings 454 into which compliant material 456 is printed before formation of circuit geometry 458. The compliant printed material 456 improves reliability during flexure of the electrical interconnect 450.

[0093] Figure 22 illustrates an alternate high performance electrical interconnect 460 in accordance with an embodiment of the present disclosure. Optical fibers 462 are located between layers 464, 466 of dielectric material. In one embodiment, optical fibers 462 are positioned over printed compliant layer 468, and dielectric layer 470 is printed over and around the optical fibers 462. A compliant layer 472 is preferably printed above the optical fiber 462 as well. The compliant layers 468, 472 support the optical fibers 462 during flexure. In another embodiment, the dielectric layer 470 is formed or printed with recesses into which the optical fibers 462 are deposited.

[0094] In another embodiment, optical quality materials 474 are printed during printing of the high performance electrical interconnect 460. The optical quality material 474 and/or the optical fibers 462 comprise optical circuit geometries. The

printing process allows for deposition of coatings in-situ that enhances the optical transmission or reduces loss. The precision of the printing process reduces misalignment issues when the optical materials 474 are optically coupled with another optical structure.

[0095] Figure 23 illustrates another embodiment of a present high performance electrical interconnect 480 in accordance with an embodiment of the present disclosure. Embedded coaxial RF circuits 482 or printed micro strip RF circuits 484 are located with dielectric/metal layers 486. These RF circuits 482, 484 are preferably created by printing dielectrics and metallization geometry.

[0096] As illustrated in Figure 24, use of additive processes allows the creation of a high performance electrical interconnect 490 with inter-circuit, 3D lattice structures 492 having intricate routing schemes. Vias 494 can be printed with each layer, without drilling.

[0097] The nature of the printing process permit controlled application of dielectric layers 496 creates recesses 498 that control the location, cross section, material content, and aspect ratio of the conductive traces 492 and the vias 494. Maintaining the conductive traces 492 and vias 494 with a cross-section of 1:1 or greater provides greater signal integrity than traditional subtractive trace forming technologies. For example, traditional methods take a sheet of a given thickness and etches the material between the traces away to have a resultant trace that is usually wider than it is thick. The etching process also removes more material at the top surface of the trace than at the bottom, leaving a trace with a trapezoidal cross-sectional shape, degrading signal integrity in some applications. Using the recesses 498 to control the aspect ratio of the conductive traces 492 and the vias 494 results in a more rectangular or square cross-section, with the corresponding improvement in signal integrity.

[0098] In another embodiment, pre-patterned or pre-etched thin conductive foil circuit traces are transferred to the recesses 498. For example, a pressure sensitive adhesive can be used to retain the copper foil circuit traces in the recesses 498. The trapezoidal cross-sections of the pre-formed conductive foil traces are then post-plated. The plating material fills the open spaces in the recesses 498 not occupied by the foil circuit geometry, resulting in a substantially rectangular or square cross-sectional shape corresponding to the shape of the recesses 498.

[0099] In another embodiment, a thin conductive foil is pressed into the recesses 198, and the edges of the recesses 498 acts to cut or shear the conductive foil. The process locates a portion of the conductive foil in the recesses 498, but leaves the negative pattern of the conductive foil not wanted outside and above the recesses 498 for easy removal. Again, the foil in the recesses 498 is preferably post plated to add material to increase the thickness of the conductive traces 492 in the circuit geometry and to fill any voids left between the conductive foil and the recesses 498.

[00100] Figure 25 illustrates a high performance electrical interconnect 500 with printed electrical devices 502. The electrical devices 502 can include passive or active functional elements. Passive structure refers to a structure having a desired electrical, magnetic, or other property, including but not limited to a conductor, resistor, capacitor, inductor, insulator, dielectric, suppressor, filter, varistor, ferromagnet, and the like. In the illustrated embodiment, electrical devices 502 include printed LED indicator 504 and display electronics 506. Geometries can also be printed to provide capacitive coupling 508. Compliant material can be added between circuit geometry, such as discussed above, so the present electrical interconnect can be plugged into a receptacle or socket, supplementing or replacing the need for compliance within the connector.

[00101] The electrical devices 502 are preferably printed during construction of the interconnect assembly 500. The electrical devices 502 can be ground planes, power planes, electrical connections to other circuit members, dielectric layers, conductive traces, transistors, capacitors, resistors, RF antennae, shielding, filters, signal or power altering and enhancing devices, memory devices, embedded IC, and the like. For example, the electrical devices 502 can be formed using printing technology, adding intelligence to the high performance electrical interconnect 500. Features that are typically located on other circuit members can be incorporated into the interconnect 500 in accordance with an embodiment of the present disclosure.

[00102] The availability of printable silicon inks provides the ability to print electrical devices 502, such as disclosed in U.S. Pat. No. 7,485,345 (Renn et al.); 7,382,363 (Albert et al.); 7,148,128 (Jacobson); 6,967,640 (Albert et al.); 6,825,829 (Albert et al.); 6,750,473 (Amundson et al.); 6,652,075 (Jacobson); 6,639,578 (Comiskey et al.); 6,545,291 (Amundson et al.); 6,521,489 (Duthaler et al.); 6,459,418 (Comiskey et al.); 6,422,687 (Jacobson); 6,413,790 (Duthaler et al.); 6,312,971 (Amundson et al.); 6,252,564 (Albert et al.); 6,177,921 (Comiskey et al.); 6,120,588 (Jacobson);

6,1 18,426 (Albert et al.); and U.S. Pat. Publication No. 2008/0008822 (Kowalski et al.), which are hereby incorporated by reference. In particular, U.S. Patent Nos. 6,506,438 (Duthaler et al.) and 6,750,473 (Amundson et al.), which are incorporated by reference, teach using ink-jet printing to make various electrical devices, such as, resistors, capacitors, diodes, inductors (or elements which may be used in radio applications or magnetic or electric field transmission of power or data), semiconductor logic elements, electro-optical elements, transistor (including, light emitting, light sensing or solar cell elements, field effect transistor, top gate structures), and the like.

[00103] The electrical devices 502 can also be created by aerosol printing, such as disclosed in U.S. Patent Nos. 7,674,671 (Renn et al.); 7,658,1 63 (Renn et al.); 7,485,345 (Renn et al.); 7,045,01 5 (Renn et al.); and 6,823,1 24 (Renn et al.), which are hereby incorporated by reference.

[00104] Printing processes are preferably used to fabricate various functional structures, such as conductive paths and electrical devices, without the use of masks or resists. Features down to about 10 microns can be directly written in a wide variety of functional inks, including metals, ceramics, polymers and adhesives, on virtually any substrate - silicon, glass, polymers, metals and ceramics. The substrates can be planar and non-planar surfaces. The printing process is typically followed by a thermal treatment, such as in a furnace or with a laser, to achieve dense functionalized structures.

[00105] Ink jet printing of electronically active inks can be done on a large class of substrates, without the requirements of standard vacuum processing or etching. The inks may incorporate mechanical, electrical or other properties, such as, conducting, insulating, resistive, magnetic, semi conductive, light modulating, piezoelectric, spin, optoelectronic, thermoelectric or radio frequency.

[00106] A plurality of ink drops are dispensed from the print head directly to a substrate or on an intermediate transfer member. The transfer member can be a planar or non-planar structure, such as a drum. The surface of the transfer member can be coated with a non-sticking layer, such as silicone, silicone rubber, or Teflon.

[00107] The ink (also referred to as function inks) can include conductive materials, semi-conductive materials (e.g., p-type and n-type semiconducting materials), metallic material, insulating materials, and/or release materials. The ink pattern can be deposited in precise locations on a substrate to create fine lines

having a width smaller than 10 microns, with precisely controlled spaces between the lines. For example, the ink drops form an ink pattern corresponding to portions of a transistor, such as a source electrode, a drain electrode, a dielectric layer, a semiconductor layer, or a gate electrode.

[00108] The substrate can be an insulating polymer, such as polyethylene terephthalate (PET), polyester, polyethersulphone (PES), polyimide film (e.g. Kapton, available from DuPont located in Wilmington, DE; Upilex available from Ube Corporation located in Japan), or polycarbonate. Alternatively, the substrate can be made of an insulator such as undoped silicon, glass, or a plastic material. The substrate can also be patterned to serve as an electrode. The substrate can further be a metal foil insulated from the gate electrode by a non-conducting material. The substrate can also be a woven material or paper, planarized or otherwise modified on at least one surface by a polymeric or other coating to accept the other structures.

[00109] Electrodes can be printed with metals, such as aluminum or gold, or conductive polymers, such as polythiophene or polyaniline. The electrodes may also include a printed conductor, such as a polymer film comprising metal particles, such as silver or nickel, a printed conductor comprising a polymer film containing graphite or some other conductive carbon material, or a conductive oxide such as tin oxide or indium tin oxide.

[001 10] Dielectric layers can be printed with a silicon dioxide layer, an insulating polymer, such as polyimide and its derivatives, poly-vinyl phenol, polymethylmethacrylate, polyvinyldenedifluoride, an inorganic oxide, such as metal oxide, an inorganic nitride such as silicon nitride, or an inorganic /organic composite material such as an organic-substituted silicon oxide, or a sol-gel organosilicon glass. Dielectric layers can also include a bicylcobutene derivative (BCB) available from Dow Chemical (Midland, Mich.), spin-on glass, or dispersions of dielectric colloid materials in a binder or solvent.

[001 11] Semiconductor layers can be printed with polymeric semiconductors, such as, polythiophene, poly(3-alkyl)thiophenes, alkyl-substituted oligothiophene, polythienylenevinylene, poly(para-phenylenevinylene) and doped versions of these polymers. An example of suitable oligomeric semiconductor is alpha-hexathienylene. Horowitz, Organic Field-Effect Transistors, Adv. Mater., 10, No. 5, p. 365 (1998) describes the use of unsubstituted and alkyl-substituted oligothiophenes in transistors. A field effect transistor made with regioregular poly(3-

hexylthiophene) as the semiconductor layer is described in Bao et al., Soluble and Processable Regioregular Poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility, Appl. Phys. Lett. 69 (26), p. 4108 (December 1996). A field effect transistor made with a-hexathienylene is described in U.S. Pat. No. 5,659,181, which is incorporated herein by reference.

[00112] A protective layer can optionally be printed onto the electrical devices. The protective layer can be an aluminum film, a metal oxide coating, a polymeric film, or a combination thereof.

[00113] Organic semiconductors can be printed using suitable carbon-based compounds, such as, pentacene, phthalocyanine, benzodithiophene, buckminsterfullerene or other fullerene derivatives, tetracyanonaphthoquinone, and tetrakisimethylanimoethylene. The materials provided above for forming the substrate, the dielectric layer, the electrodes, or the semiconductor layers are exemplary only. Other suitable materials known to those skilled in the art having properties similar to those described above can be used in accordance with the present disclosure.

[00114] The ink-jet print head preferably includes a plurality of orifices for dispensing one or more fluids onto a desired media, such as for example, a conducting fluid solution, a semiconducting fluid solution, an insulating fluid solution, and a precursor material to facilitate subsequent deposition. The precursor material can be surface active agents, such as octadecyltrichlorosilane (OTS).

[00115] Alternatively, a separate print head is used for each fluid solution. The print head nozzles can be held at different potentials to aid in atomization and imparting a charge to the droplets, such as disclosed in U.S. Pat. No. 7,148,128 (Jacobson), which is hereby incorporated by reference. Alternate print heads are disclosed in U.S. Pat. No. 6,626,526 (Ueki et al.), and U.S. Pat. Publication Nos. 2006/0044357 (Andersen et al.) and 2009/0061089 (King et al.), which are hereby incorporated by reference.

[00116] The print head preferably uses a pulse-on-demand method, and can employ one of the following methods to dispense the ink drops: piezoelectric, magnetostrictive, electromechanical, electro pneumatic, electrostatic, rapid ink heating, magneto hydrodynamic, or any other technique well known to those skilled in the art. The deposited ink patterns typically undergo a curing step or another processing step before subsequent layers are applied.

[001 17] While ink jet printing is preferred, the term "printing" is intended to include all forms of printing and coating, including: pre-metered coating such as patch die coating, slot or extrusion coating, slide or cascade coating, and curtain coating; roll coating such as knife over roll coating, forward and reverse roll coating; gravure coating; dip coating; spray coating; meniscus coating; spin coating; brush coating; air knife coating; screen printing processes; electrostatic printing processes; thermal printing processes; and other similar techniques.

[001 18] Figure 26 illustrates an alternate high performance electrical interconnect 520 with printed compliant material 522 added between circuit geometries 524, 526 to facilitate insertion of exposed circuit geometries 528, 530 into a receptacle or socket. The compliant material 522 can supplement or replace the compliance in the receptacle or socket. In one embodiment, the compliance is provided by a combination of the compliant material 522 and the exposed circuit geometries 528, 530.

[001 19] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range and any other stated or intervening value in that stated range is encompassed within the embodiments of the disclosure. The upper and lower limits of these smaller ranges which may independently be included in the smaller ranges is also encompassed within the embodiments of the disclosure, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either both of those included limits are also included in the embodiments of the present disclosure.

[00120] Unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the embodiments of the present disclosure belong. Although any methods and materials similar or equivalent to those described herein can also be used in the practice or testing of the embodiments of the present disclosure, the preferred methods and materials are now described. All patents and publications mentioned herein, including those cited in the Background of the application, are hereby incorporated by reference to disclose and described the methods and/or materials in connection with which the publications are cited.

[00121] The publications discussed herein are provided solely for their disclosure prior to the filing date of the present application. Nothing herein is to be construed as an admission that the present disclosure is not entitled to antedate such publication by virtue of prior invention. Further, the dates of publication provided may be different from the actual publication dates which may need to be independently confirmed.

[00122] Other embodiments of the disclosure are possible. Although the description above contains much specificity, these should not be construed as limiting the scope of the disclosure, but as merely providing illustrations of some of the presently preferred embodiments of this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope of the present disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments of the disclosure. Thus, it is intended that the scope of the present disclosure herein disclosed should not be limited by the particular disclosed embodiments described above.

[00123] Thus the scope of this disclosure should be determined by the appended claims and their legal equivalents. Therefore, it will be appreciated that the scope of the present disclosure fully encompasses other embodiments which may become obvious to those skilled in the art, and that the scope of the present disclosure is accordingly to be limited by nothing other than the appended claims, in which reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural, chemical, and functional equivalents to the elements of the above-described preferred embodiment(s) that are known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the present claims. Moreover, it is not necessary for a device or method to address each and every problem sought to be solved by the present disclosure, for it to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims.

What is claimed is:

1. A surface mount electrical interconnect adapted to provide an interface between solder balls on a BGA device and a PCB, the electrical interconnect comprising:

a socket substrate comprising a first surface, a second surface, and a plurality of openings sized and configured to receive the solder balls on the BGA device;

a plurality of electrically conductive contact tabs bonded to the first surface of the socket substrate so that contact tips on the contact tabs extend into the openings, the contact tips electrically coupling with the BGA device when the solder balls are positioned in the openings;

vias located in the openings that electrically couple the contact tabs to contact pads located proximate the second surface of the socket substrate; and

solder balls bonded to the contact pads that are adapted to electrically and mechanically couple the electrical interconnect to the PCB.

2. The electrical interconnect of claim 1 comprising at least one dielectric layer printed on the first surface of the socket substrate mechanically supporting the contact tabs.

3. The electrical interconnect of claim 1 comprising at least one dielectric layer laminated on the first surface of the socket substrate mechanically supporting the contact tabs.

4. The electrical interconnect of claim 1 comprising a dielectric layer on the first surface of the substrate that extends into the openings to mechanically engage with the solder balls on the BGA device.

5. The electrical interconnect of claim 1 comprising a dielectric layer on the first surface of the substrate that extends into a portion of the openings, the dielectric layer adapted to bias the solder balls on the BGA device toward the contact tips.

6. The electrical interconnect of claim 1 comprising a plurality of conductive contact tabs electrically and mechanically coupled to the vias and extending into the openings in a spaced configuration.

7. The electrical interconnect of claim 6 wherein the plurality of conductive tabs are arranged to simultaneously engage a top portion, a center diameter and a lower portion of the solder balls on the BGA device.

8. The electrical interconnect of claim 6 wherein the contact tabs comprise a planar structure folded to fit in the openings and to form the plurality of conductive tabs.

9. The electrical interconnect of claim 1 wherein the contact tabs comprises a pair of opposing spring arms adapted to flex outward during insertion of the solder balls on the BGA device into the openings.

10. The electrical interconnect of claim 1 comprising:

at least one dielectric layer printed on one of the first or second surfaces of the socket substrate, the dielectric layer comprising a plurality recesses; and

a conductive material deposited in at least a portion of the recesses comprising circuit geometry electrically coupling at least two of the contact tabs.

11. The electrical interconnect of claim 10 wherein the conductive material comprises one of sintered conductive particles or a conductive ink.

12. The electrical interconnect of claim 10 wherein dielectric layers comprise at least one additional circuitry plane selected from one of a ground plane, a power plane, an electrical connection to other circuit members, a dielectric layer, or a flexible circuit.

13. The electrical interconnect of claim 1 comprising at least one printed electrical device located on the socket substrate and electrically coupled to at least a one of the contact tabs.

14. The electrical interconnect of claim 13 wherein the electrical device is selected from one of shielding, near device decoupling, capacitors, transistors, resistors, filters, signal or power altering and enhancing devices, memory devices, embedded IC devices, RF antennae, and the like.

15. The electrical interconnect of claim 1 comprising:

at least one dielectric layer printed on one of the first or second surfaces of the socket substrate, the dielectric layer comprising a plurality recesses; and

an optical quality material deposited in recesses.

16. An electrical interconnect assembly comprising:

a housing that retains the electrical interconnect of claim 1;

a BGA device with solder balls located in the openings in the socket substrate and electrically coupled to the contact tips of the contact tabs; and

a PCB soldered to the contact pads located at the second surface of the socket substrate.

17. A method of making a surface mount electrical interconnect adapted to provide an interface between solder balls on a BGA device and a PCB, the method comprising the steps of:

forming a socket substrate with a first surface, a second surface, and a plurality of openings sized and configured to receive the solder balls on the BGA device;

bonding a plurality of electrically conductive contact tabs to the first surface of the socket substrate so that at least one contact tip of the contact tabs extends into the openings, the contact tips electrically coupling with the BGA device when the solder balls are positioned in the openings;

forming vias in the openings that electrically couple the contact tabs to contact pads located proximate the second surface of the socket substrate; and

attaching solder balls to the contact pad that are adapted to electrically and mechanically couple the electrical interconnect to the PCB.

18. The method of claim 17 comprising printing at least one dielectric layer on the first surface of the socket substrate to mechanically support the contact tabs.

19. The method of claim 17 comprising laminating at least one dielectric layer on the first surface of the socket substrate to mechanically support the contact tabs.

20. The method of claim 17 comprising printing a dielectric layer on the first surface of the socket substrate that extends into the openings to mechanically engage with the solder balls on the BGA device.

21. The method of claim 17 comprising printing a dielectric layer on the first surface of the substrate that extends into a portion of the openings, the dielectric layer biasing the solder balls on the BGA device toward the contact tips.

22. The method of claim 17 comprising locating a plurality of conductive contact tabs in the openings that are electrically and mechanically coupled to the vias, and that extend into the openings in a spaced configuration.

23. The method of claim 22 comprising arranging the plurality of conductive tabs to simultaneously engage a top portion, a center diameter and a lower portion of the solder balls on the BGA device.

24. The method of claim 22 comprising the steps of:

forming the contact tabs as a planar structure; and

folding the contact tabs to fit in the openings to form the plurality of conductive tabs.

25. The method of claim 17 comprising the steps of:

forming the contact tabs with a pair of opposing spring arms; and

flexing outward the spring arms during insertion of the solder balls on the BGA device into the openings.

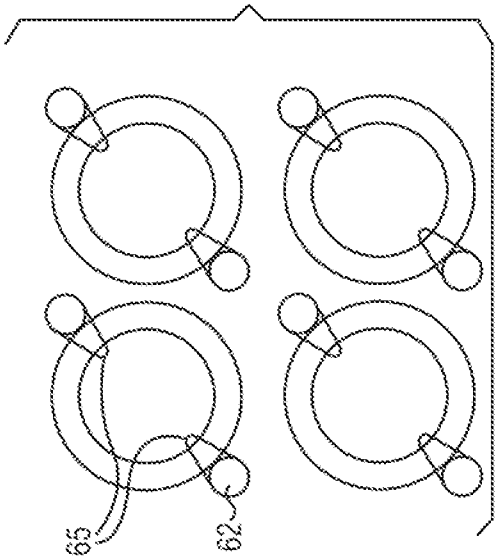
26. The method of claim 17 comprising:

printing at least one dielectric layer on one of the first or second surfaces of the socket substrate, the dielectric layer comprising a plurality recesses; and

printing a conductive material in at least a portion of the recesses comprising circuit geometry electrically coupling at least two of the contact tabs.

27. The method of claim 26 wherein the conductive material comprises one of sintered conductive particles or a conductive ink.

Fig. 1A



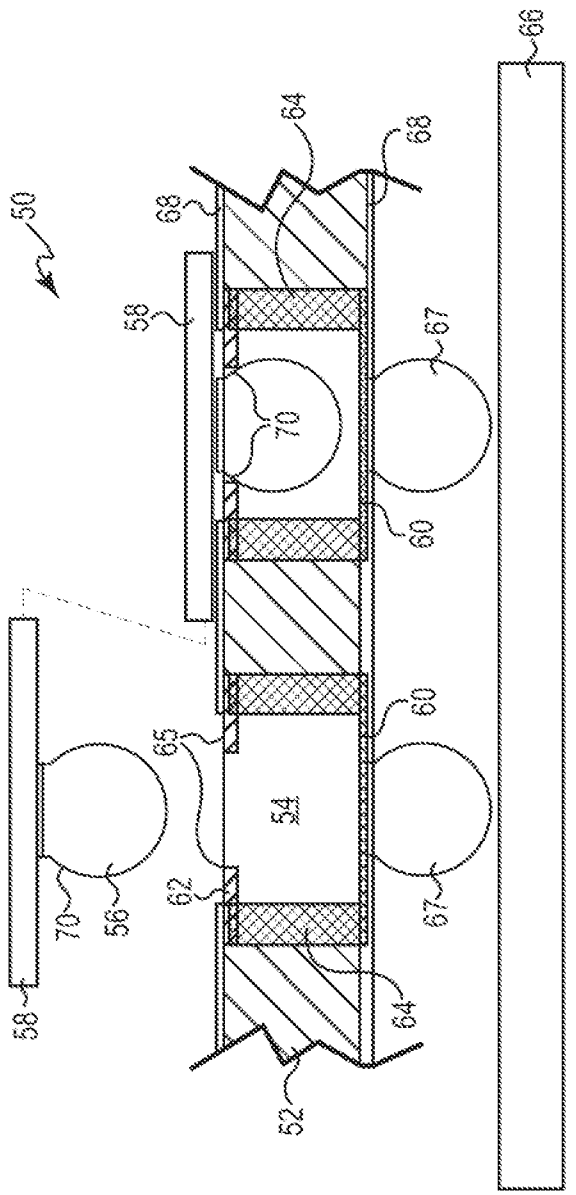
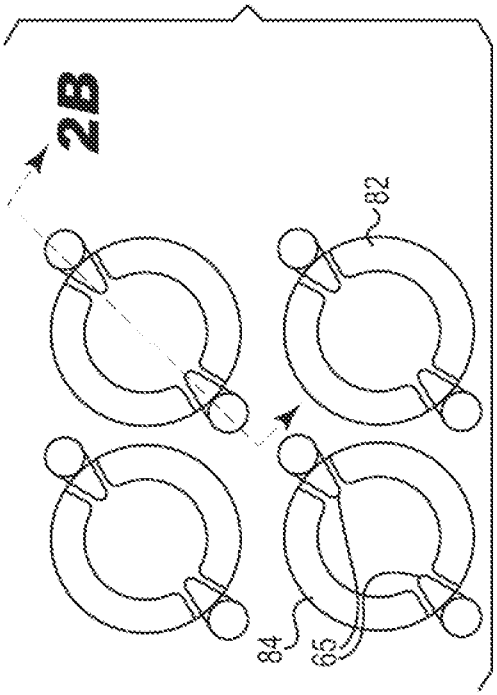


Fig. 1B

Fig. 2A



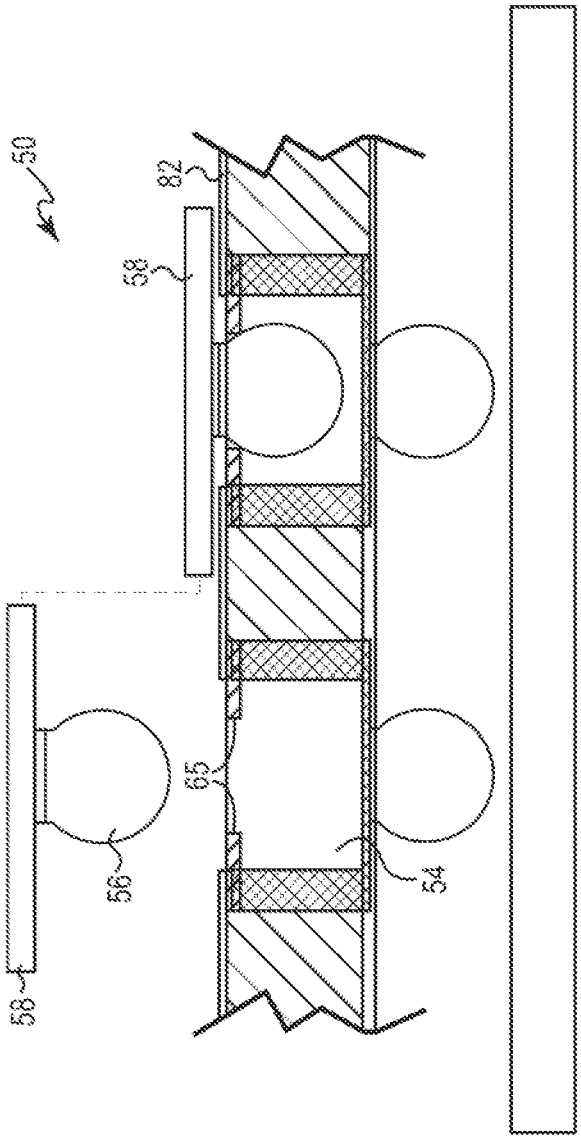
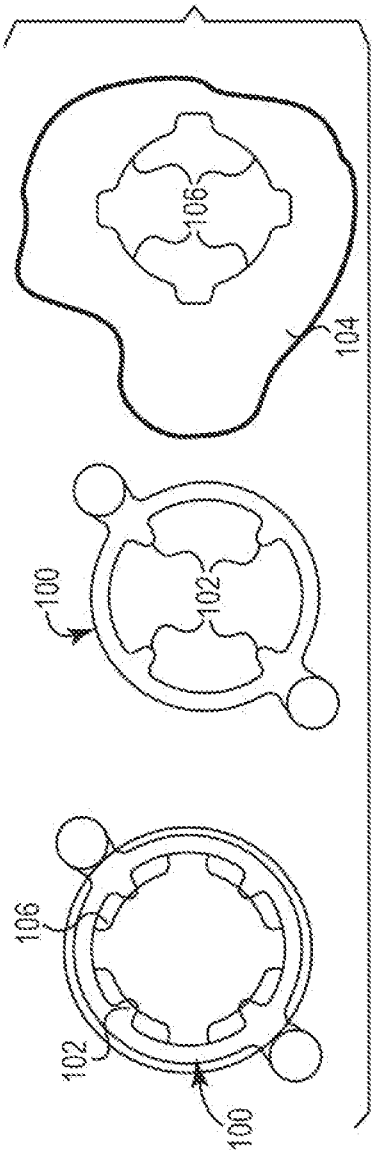


Fig. 2B

Fig. 3A



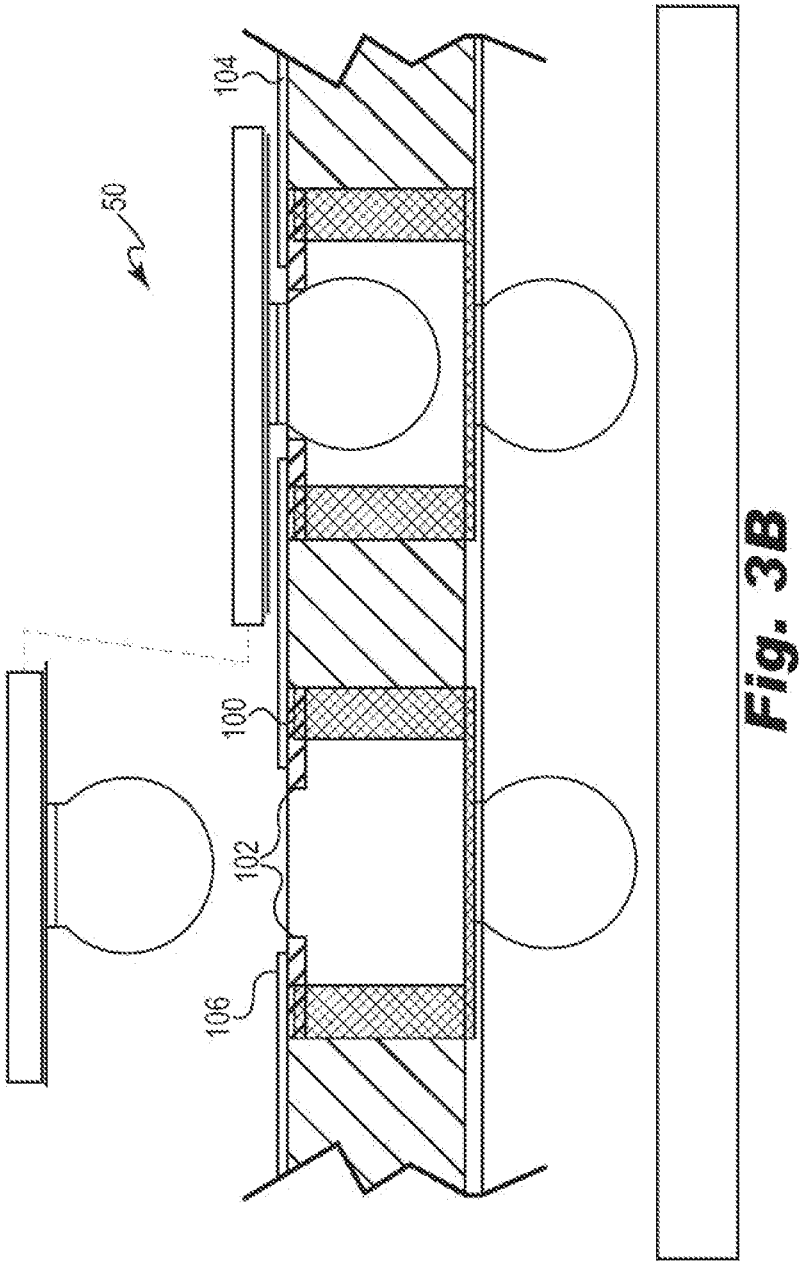


Fig. 3B

Fig. 4A

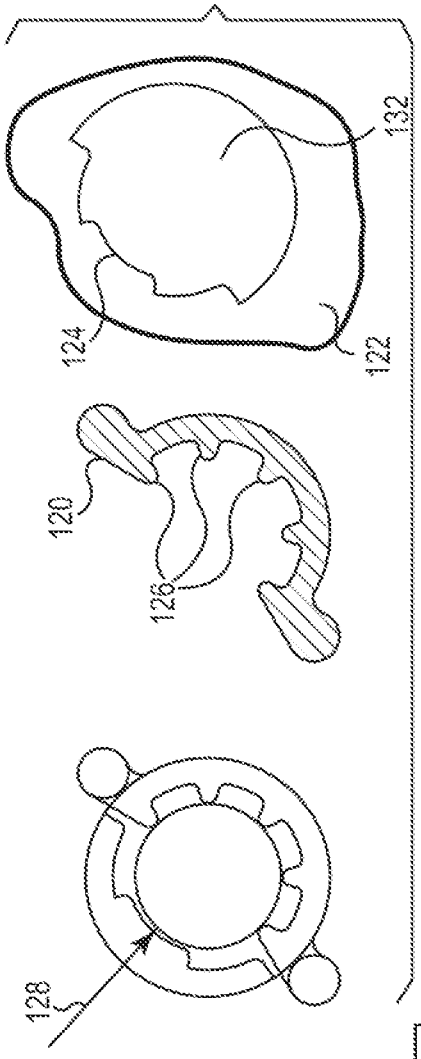
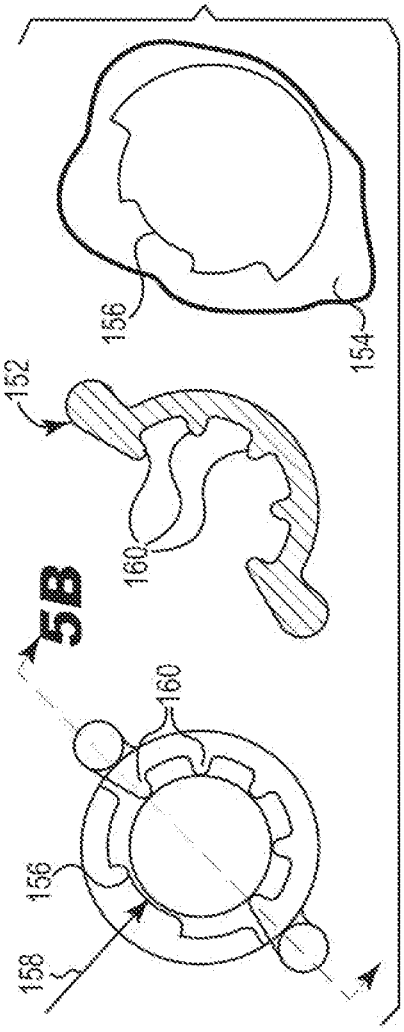


Fig. 4B

Fig. 5A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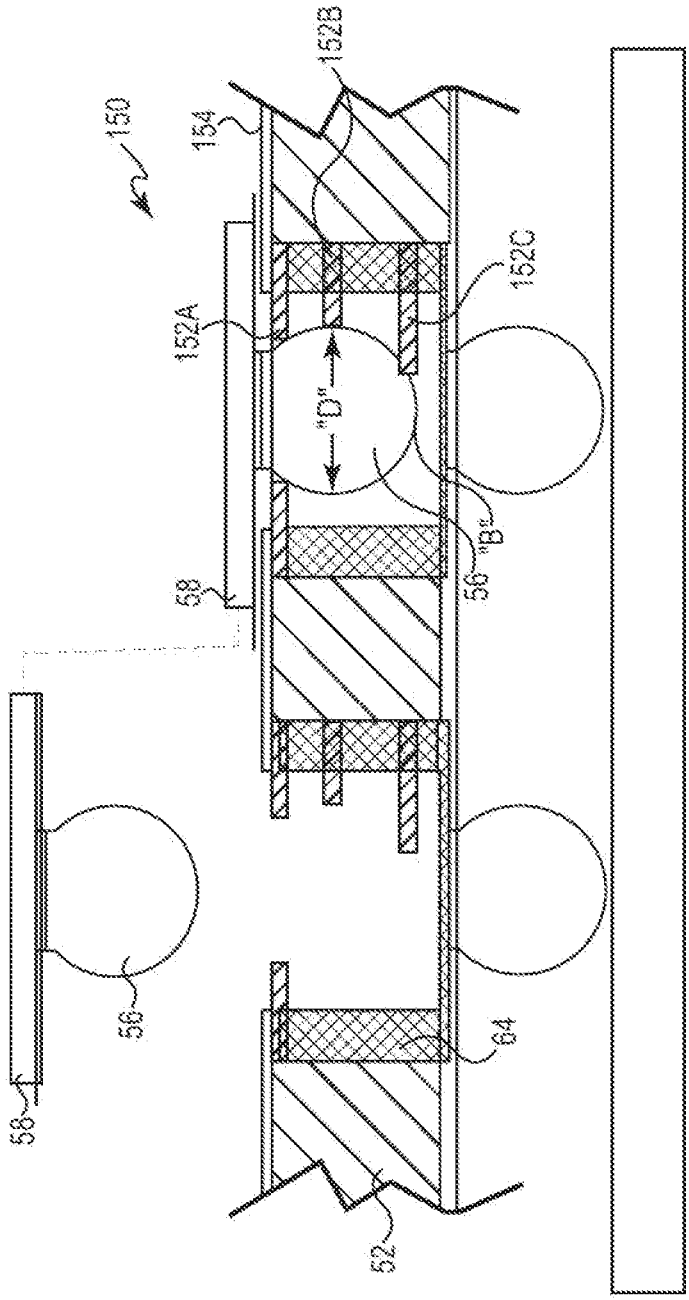
158


150
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152C
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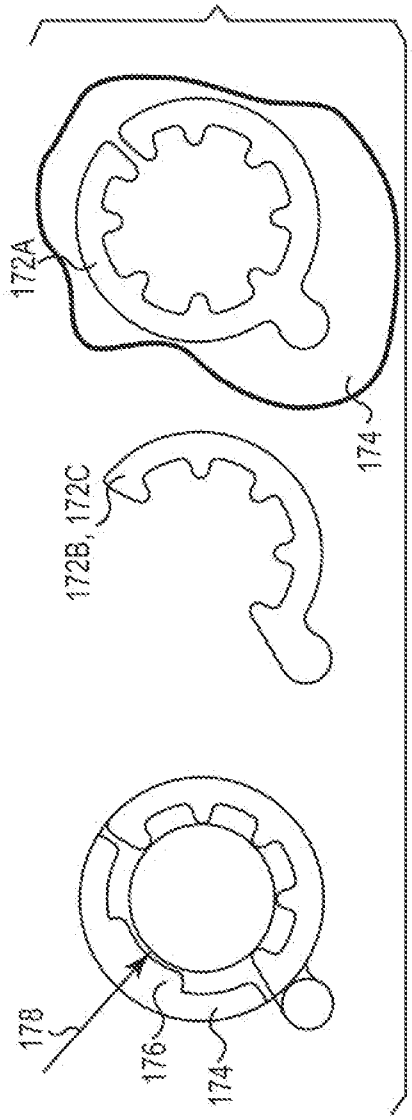
"B"
58
56
56
58
64
52

Fig. 5B

Fig. 6A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174

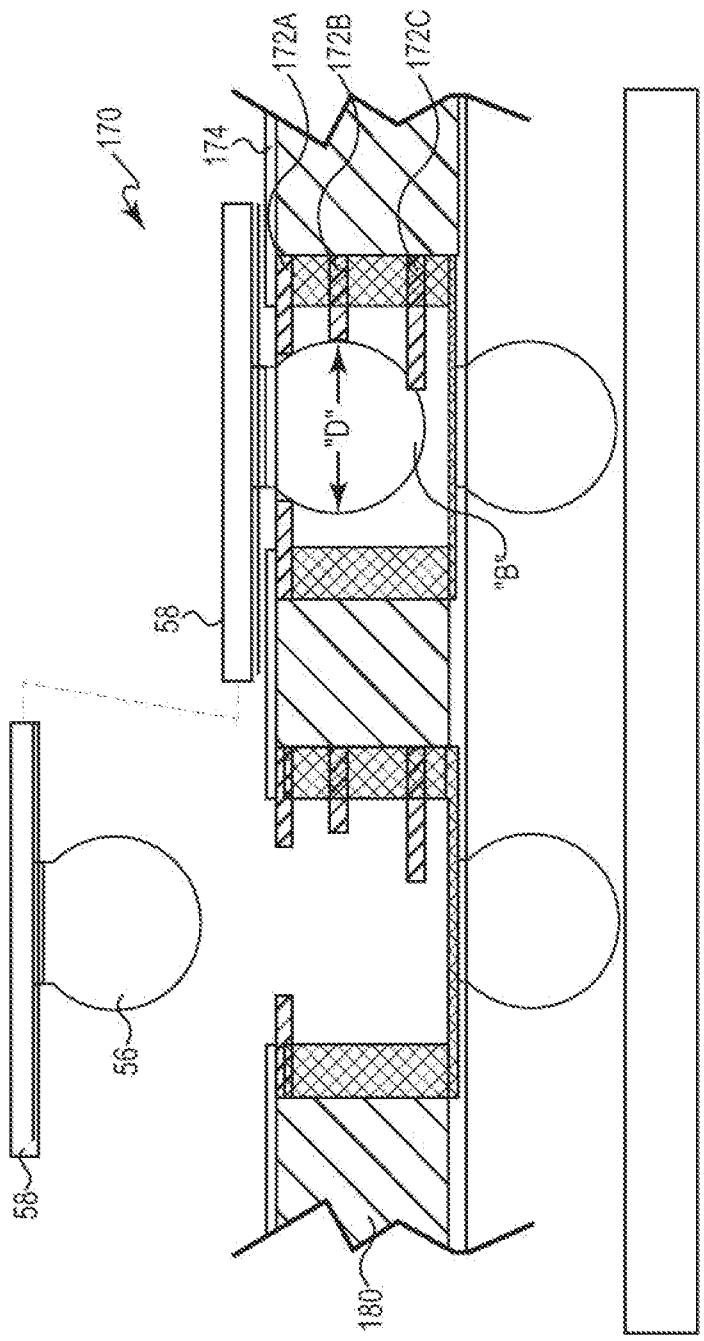
170
174
172A
172B
172C
"D"
"S"
58
56
58
180

Fig. 6B

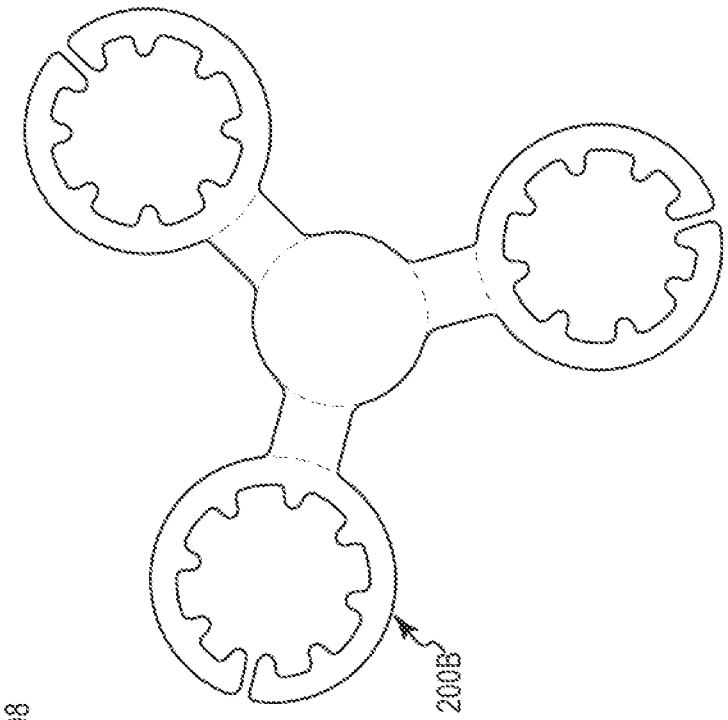

Fig. 7B

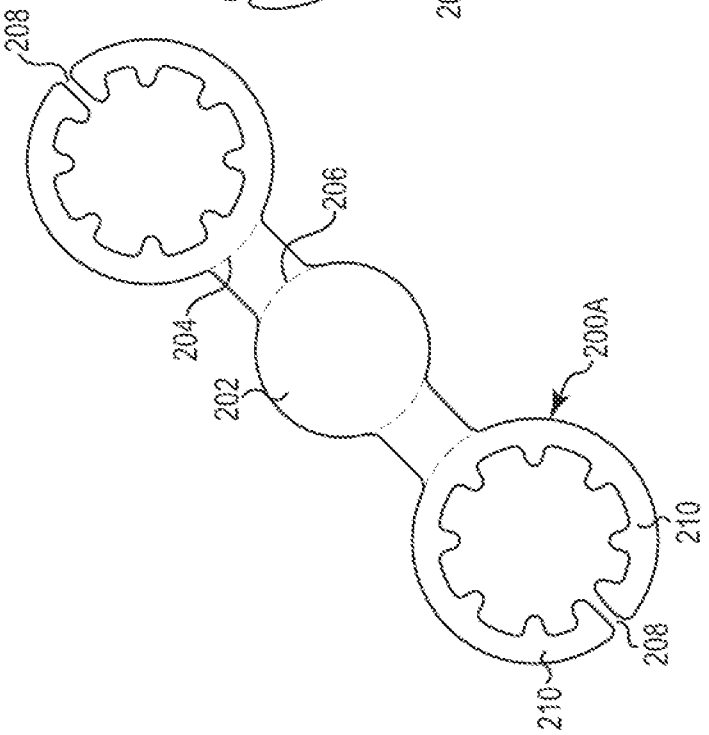

Fig. 7A

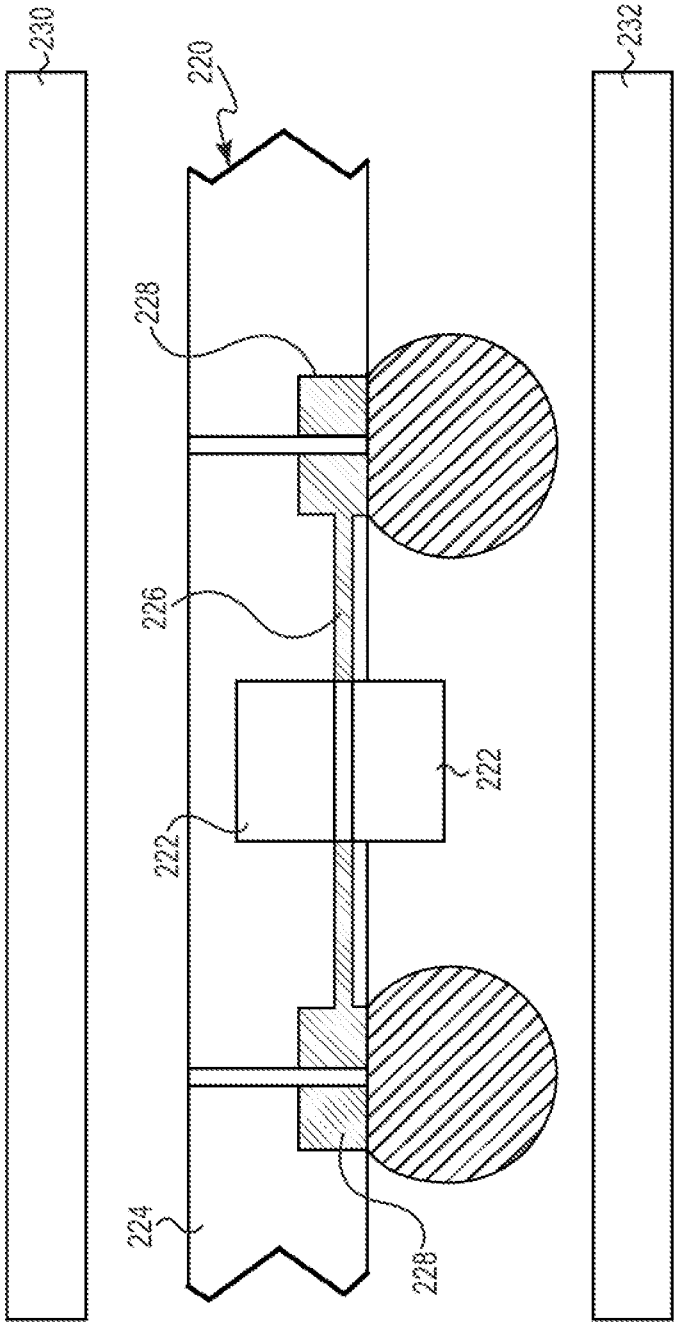

Fig. 8

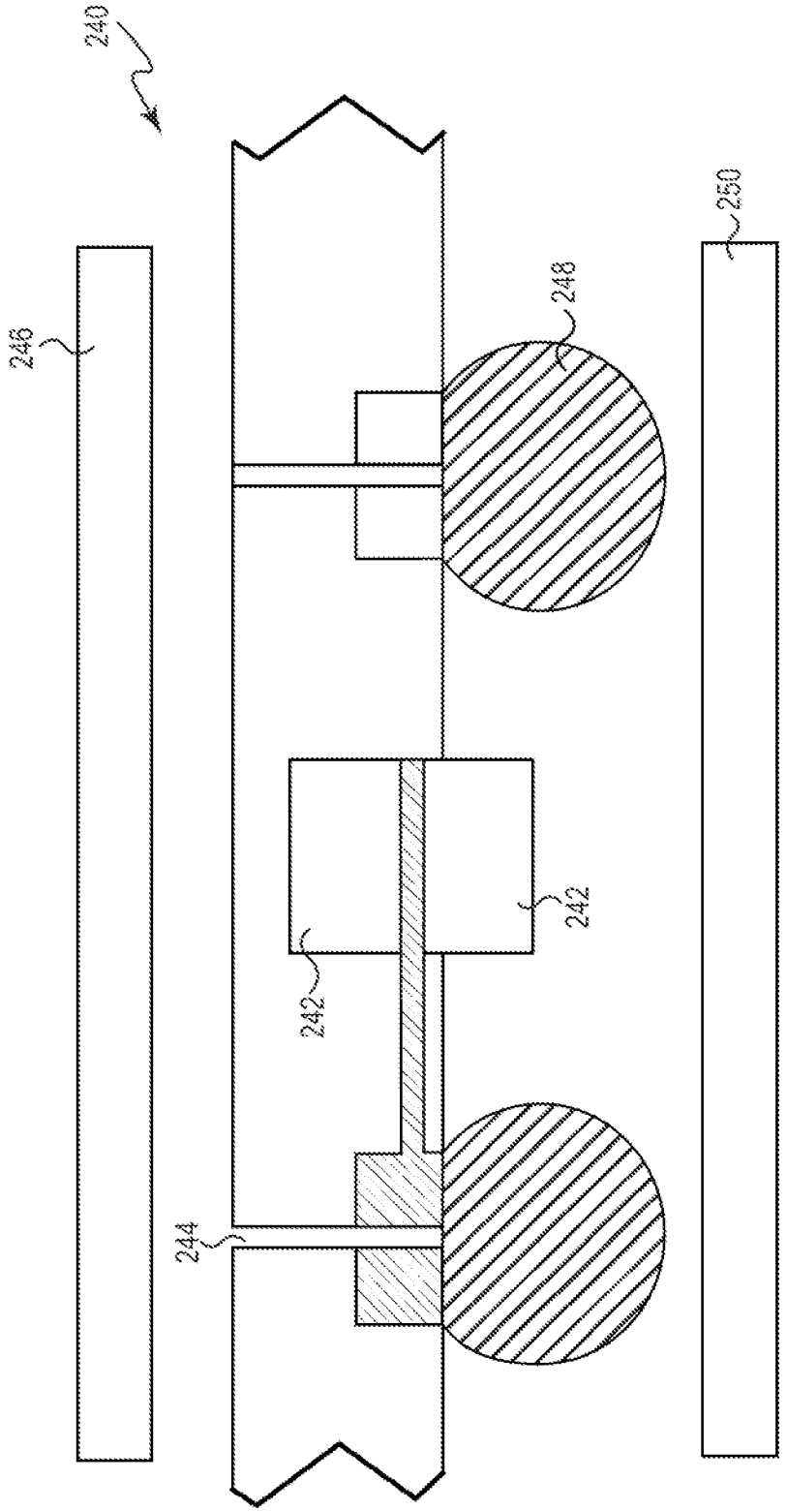

Fig. 9

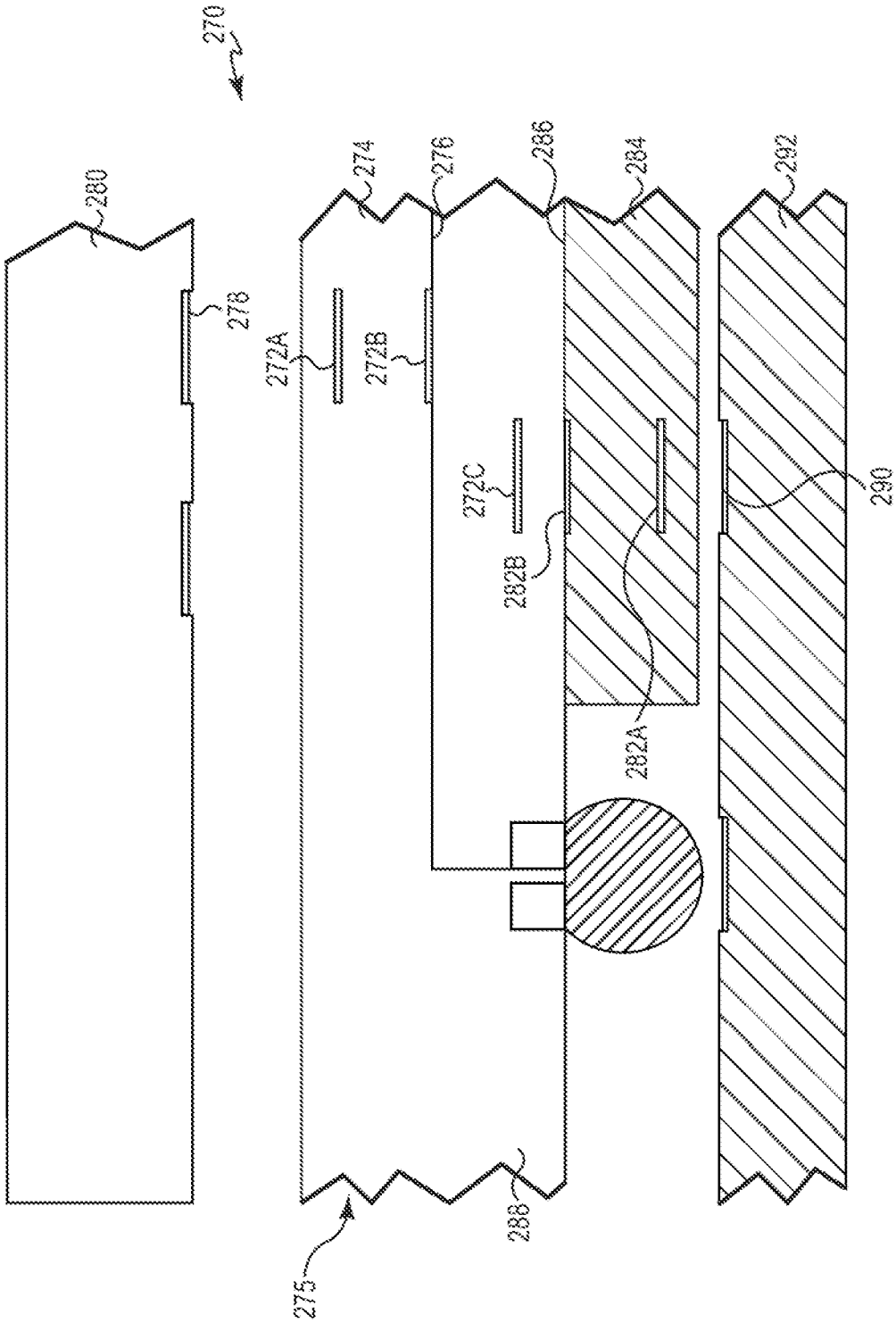
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Fig. 10

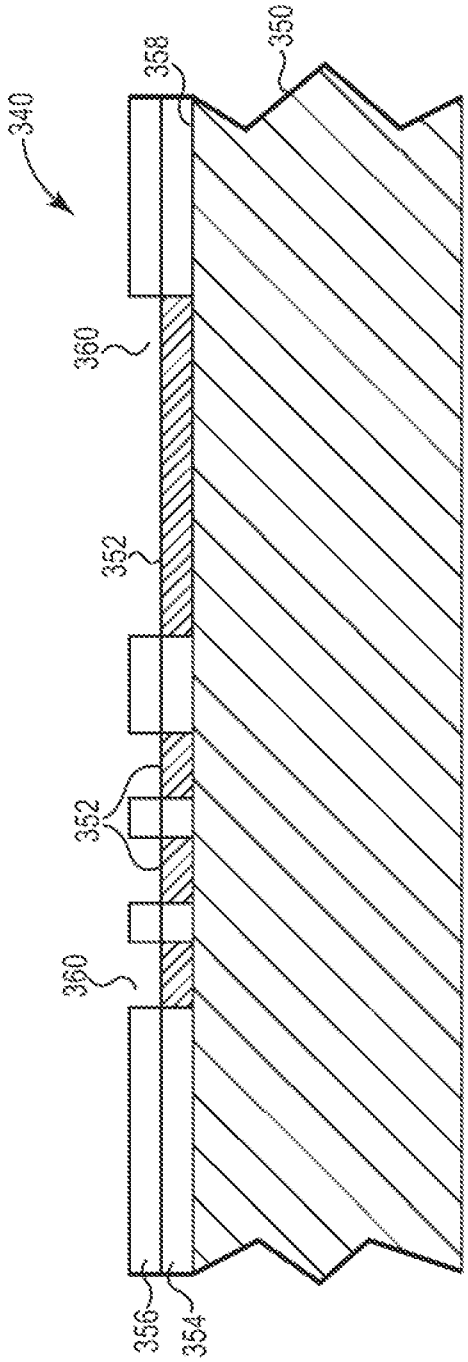

Fig. 11

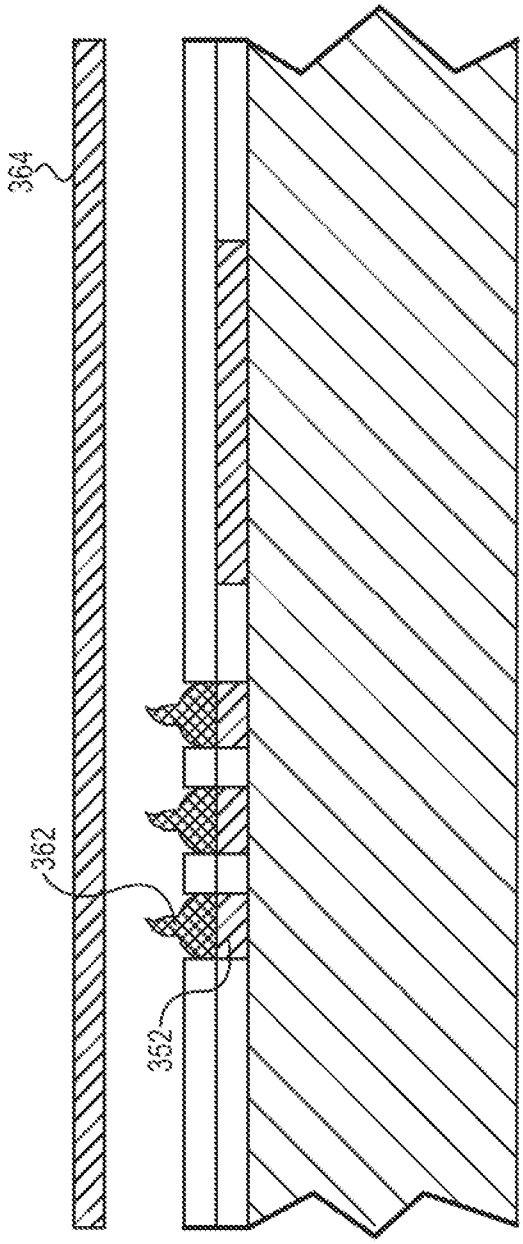

Fig. 12

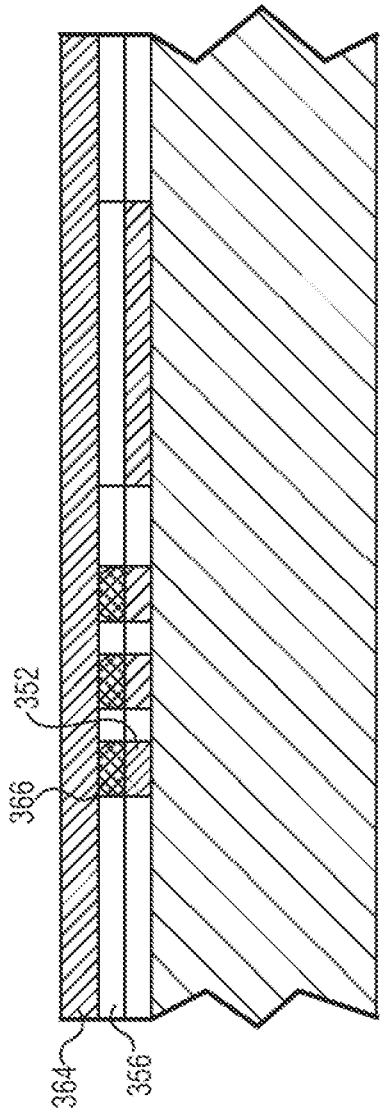

Fig. 13

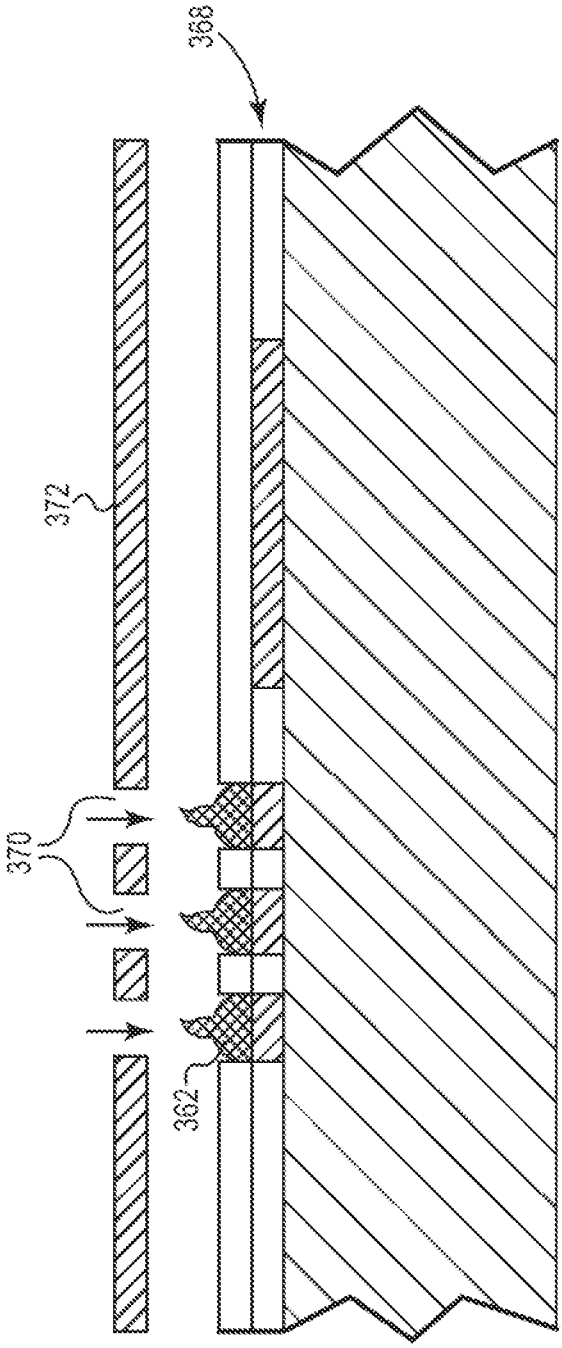

Fig. 14

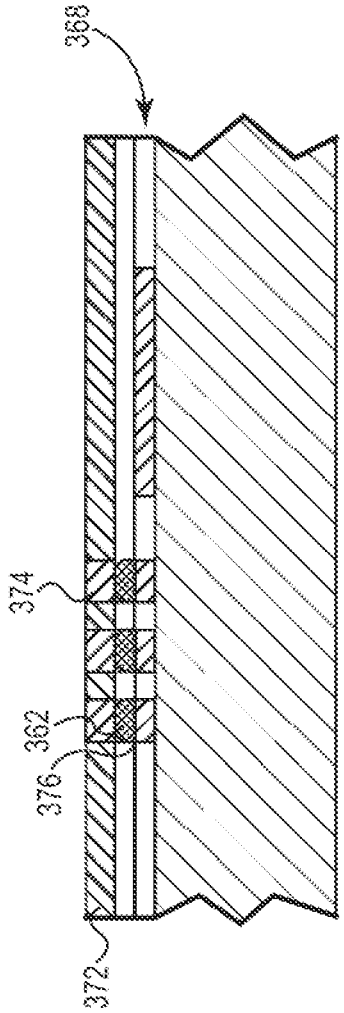

Fig. 15

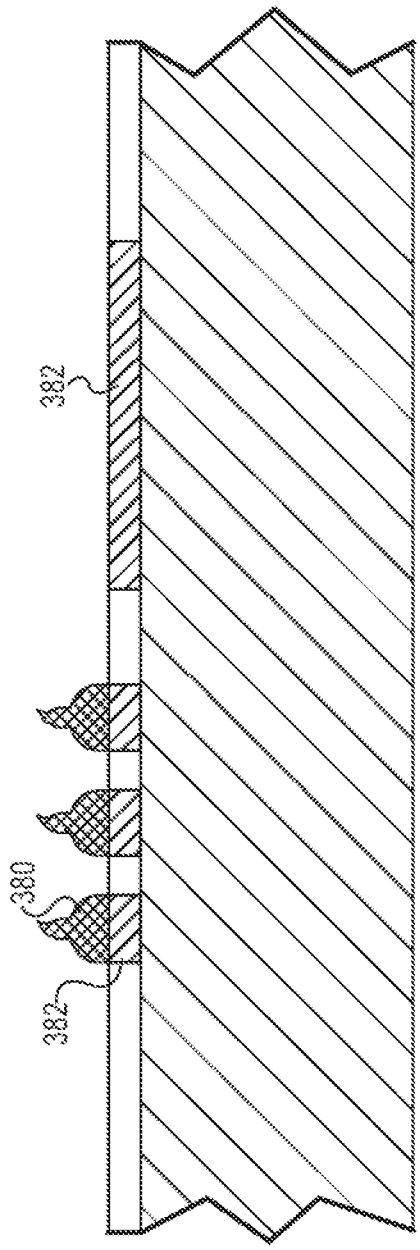

Fig. 16

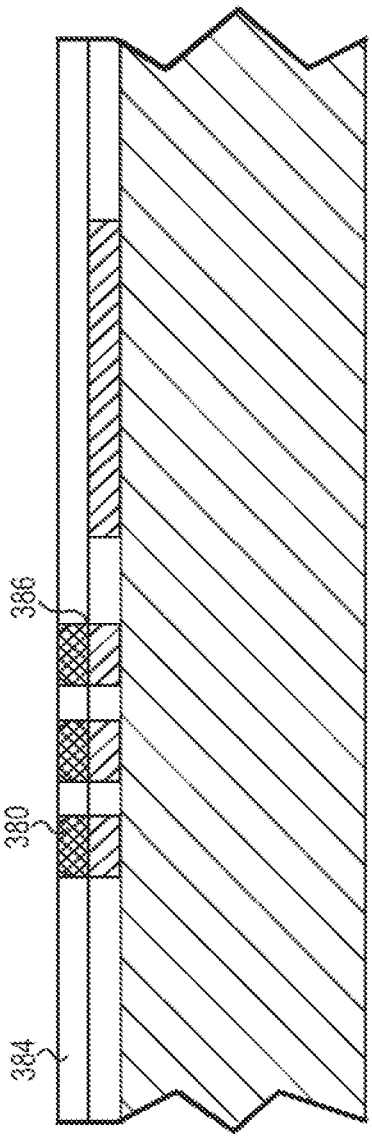

Fig. 17

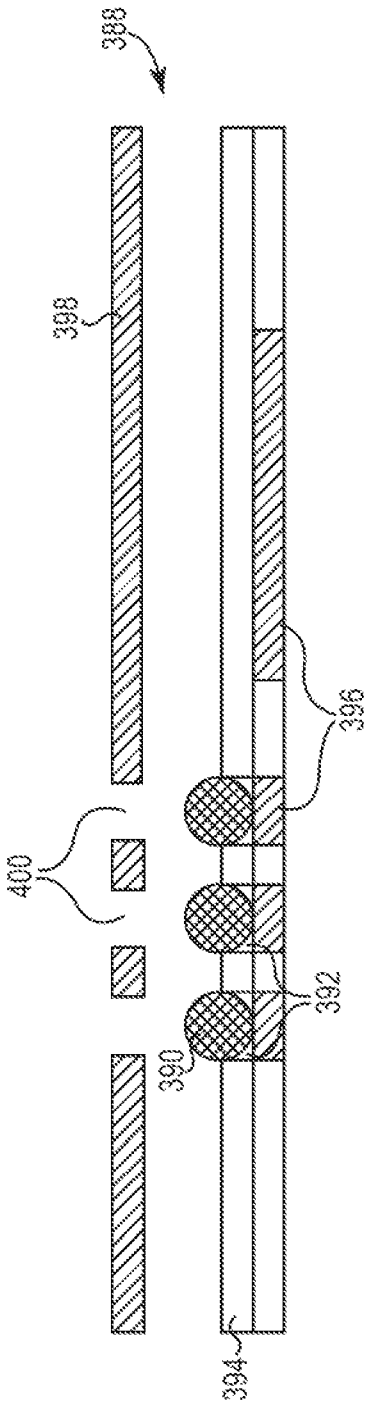

Fig. 18

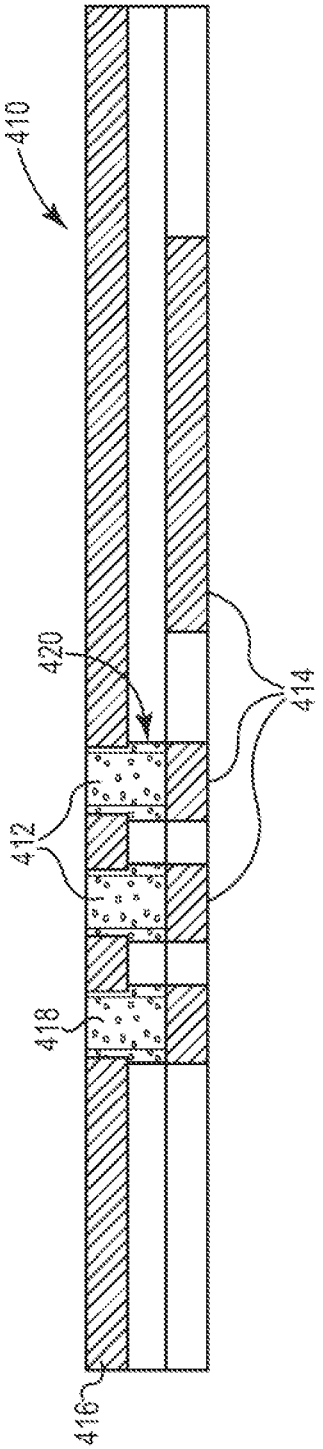

Fig. 19

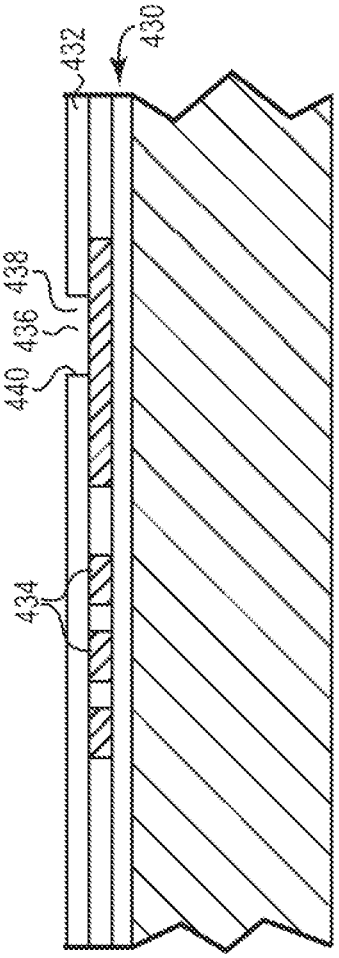

Fig. 20

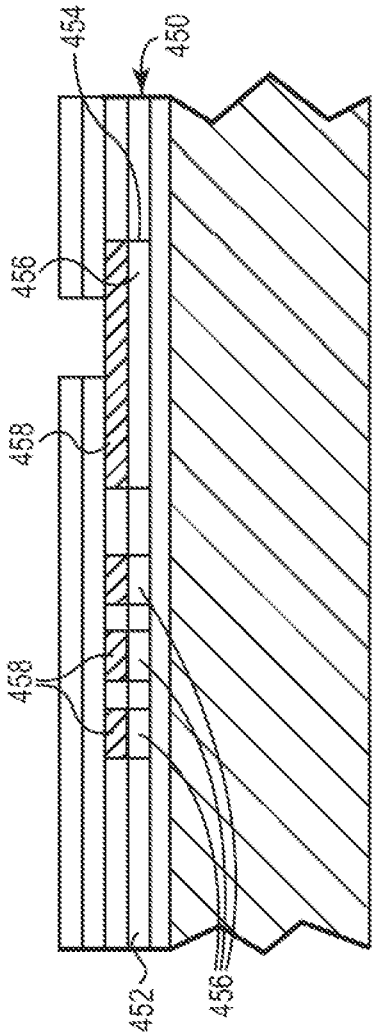

Fig. 21

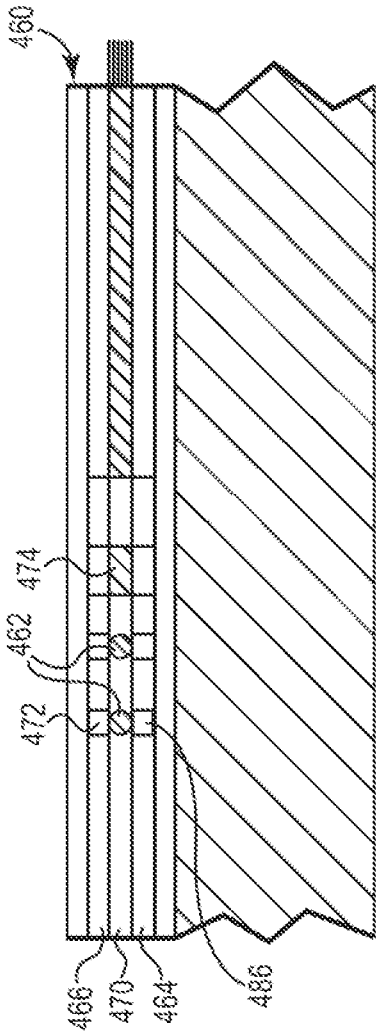

Fig. 22

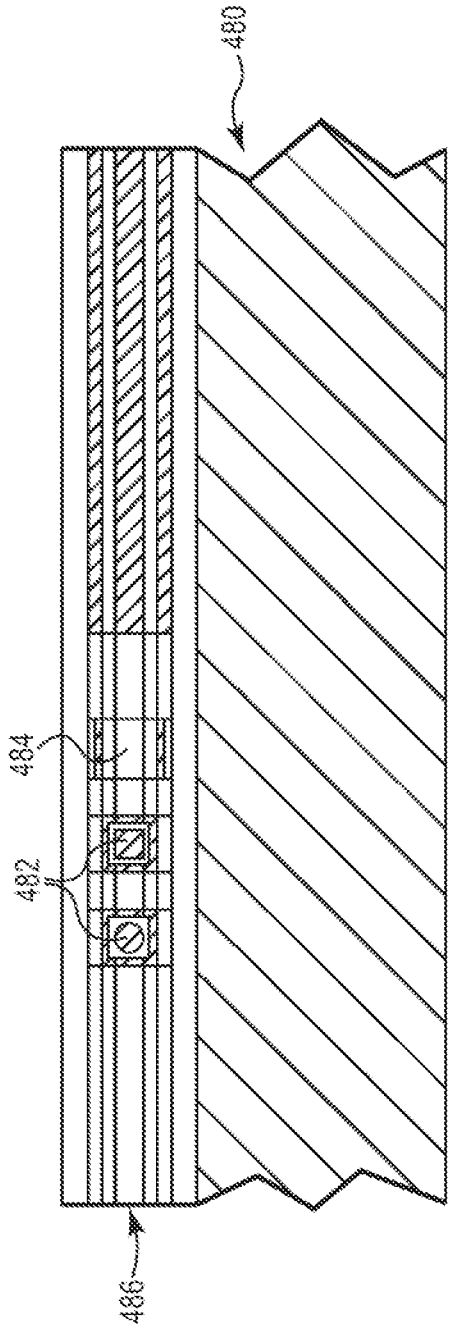

Fig. 23

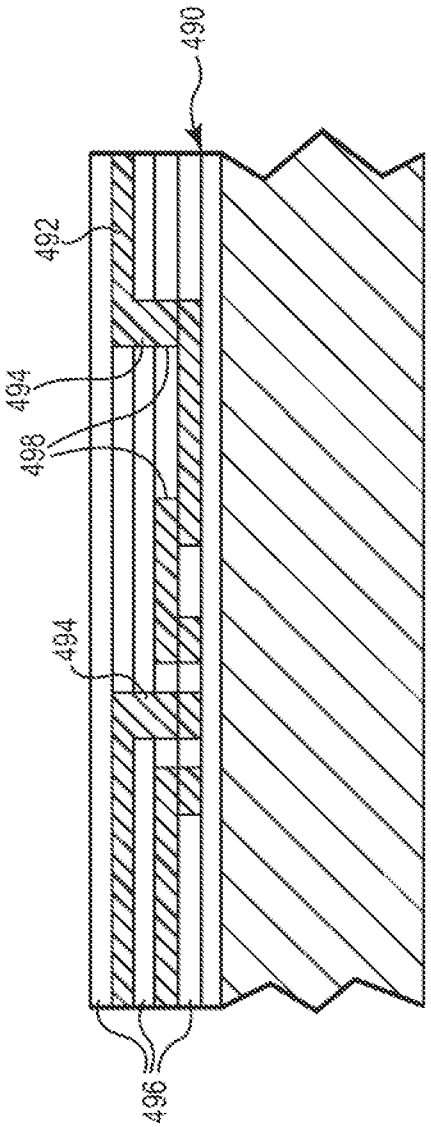

Fig. 24

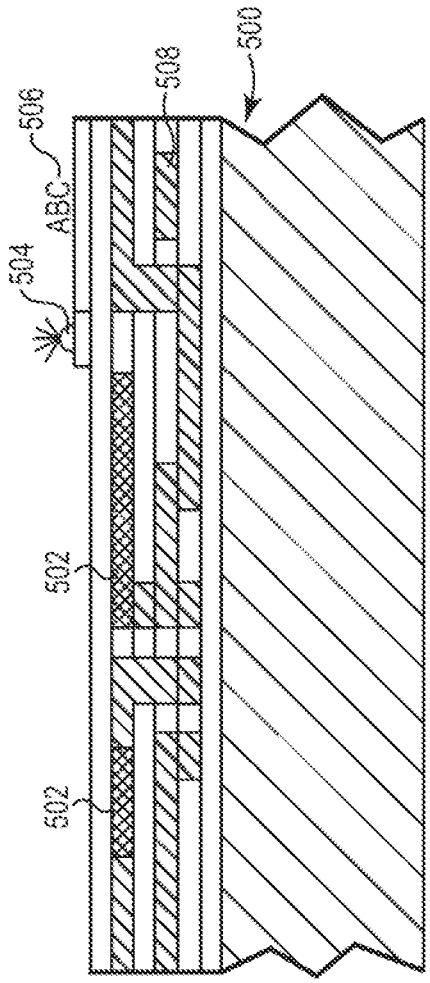

Fig. 25

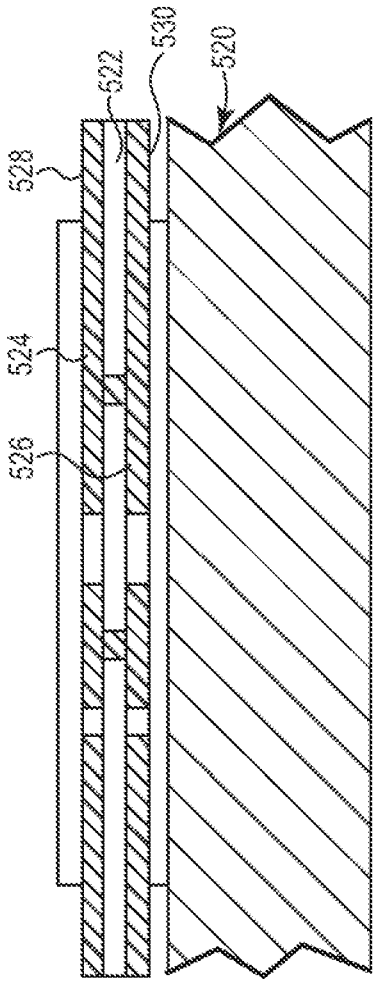

Fig. 26

INTERNATIONAL SEARCH REPORT

International application NO.
PCT/US201 1/062313

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01 R 12/00 (2012.01)
USPC - 439/70
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - See extra sheet
USPC - 174/260, 263; 257/686, 690, 698, 723, 737, 738, 758, 773, 774, 777, 778, 780; 361/760; 438/107, 109, 618, 622, 637;439/70,331

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PatBase, Google Patents, Google

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,200,143 B1 (HABA et al) 13 March 2001 (13.03.2001) entire document	1,4-6,8,9,17,20-22,24,25 --- 2,3,7,10-16,18,19,23,26, 27
Y	US 6,172,879 B1 (CILIA et al) 09 January 2001 (09.01.2001) entire document	2, 10-12, 18. 26-27
Y	US 7,508,076 B2 (JAPP et al) 24 March 2009 (24.03.2009) entire document	3, 12, 19
Y	JP 2003/217774 A (SHIMADA) 31 July 2003 (31.07.2003) abstract, drawings	7, 23
Y	US 6,359,790 B1 (MEYER-BERG) 19 March 2002 (19.03.2002) entire document	13, 14
Y	US 7.217.996 B2 (CHENG et al) 15 May 2007 (15.05.2007) entire document	16
Y	US 2006/0208230 A1 (CHO et al) 21 September 2006 (21.09.2006) entire document	11, 27
Y	US 6,773,302 B2 (GUTIERREZ et al) 10 August 2004 (10.08.2004) entire document	15

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"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 March 2012	27 MAR 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Blaine R. Copenheaver **PCT Helpdesk: 571-272-4300** **PCT OSP: 571-272-7774**

INTERNATIONAL SEARCH REPORT

international application /SO.

PCT/US201 1/06231 3

Continuation of Box B:
H01L21/00,02,44,50,60,70,768,3205,4763;H01 L23/02,12,31 ,48,52,498,522,538;H03K19/177; H05K1/1 1,14,18;H05K 3/34; G06F12/00.13/00 (2012.01)