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(54) Title: DIGITAL AMPLITUDE CONTROL OF VECTOR GENERATOR

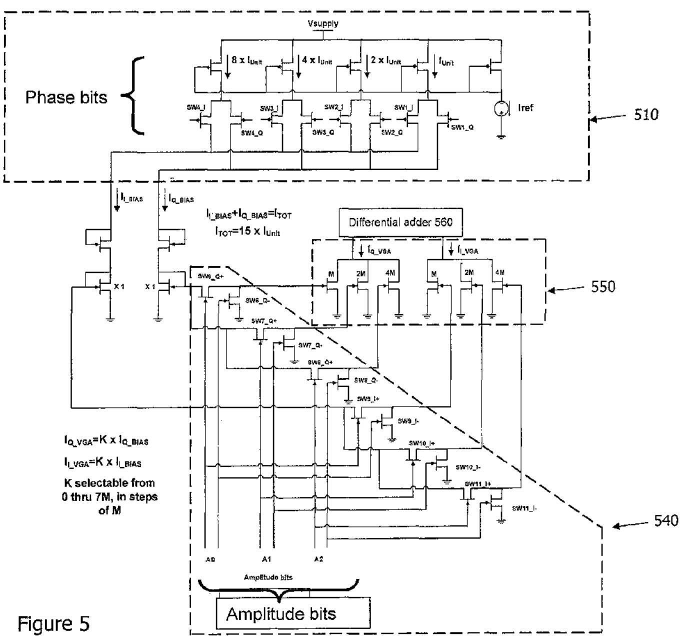

Figure 5

500

(57) Abstract: In an exemplary embodiment, an active vector generator is configured to generate a composite vector with controlled phase and amplitude, where the active vector generator generates the composite vector with independent variable phase control and independent variable amplitude control. Furthermore, in another exemplary embodiment, an active vector generator is configured to generate a unique number of phase states and configured to generate a unique number of amplitude states. Specifically, an exemplary active vector generator comprises a digital-to-analog converter (DAC) configured to set the phase of the composite vector, a current multiplying switch network configured to control the amplitude of the composite vector, a variable current multiplier configured to adjust the amplitude of the composite vector, and a differential adder configured to control the quadrant of the composite vector and generate the composite vector.

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DIGITAL AMPLITUDE CONTROL OF VECTOR GENERATOR

Background Of The Invention

A phased array antenna uses multiple radiating elements to transmit, receive, or transmit and receive radio frequency (RF) signals. Phased array antennas are used in various capacities, including communications on the move (COTM) antennas, satellite communication (SATCOM) airborne terminals, SATCOM mobile communications, and SATCOM earth terminals. The application of mobile terminals typically requires the use of automatic tracking antennas that are able to steer the beam in azimuth, elevation, and polarization to follow the satellite position while the vehicle is in motion.

One well known type of phased array antenna is an electronically steerable phased array antenna. The electronically steerable phased array antenna has full electronic steering capability and is more compact and lower profile than a comparable mechanical phased array antenna. The main drawback of fully electronic steering is that the antenna usually requires the integration of a lot of expensive analog RF electronic components which may prohibitively raise the cost for commercial applications. A typical electronically steerable phased array antenna comprises an assembly of phase shifters, power splitters, power combiners, and quadrature hybrids. Additionally, a typical electronically steerable phased array requires at least a few of these components at every element in the phased array, which increases the cost and complexity of the architecture.

Phase shifters are used in a phased array antenna in order to steer the beam of the signals by controlling the respective phases of the RF signals communicated through the phase shifters. A typical digital phase shifter uses switched delay lines, is physically large, and operates over a narrow band of frequencies due to its distributed nature. Another typical digital phase shifter implements a switched high-pass low-pass filter architecture which has better operating bandwidth compared to a switched delay line but is still physically large.

Also, the phase shifter is often made on gallium arsenide (GaAs). Though other materials may be used, GaAs is a higher quality material designed and controlled to provide good performance of electronic devices. However, in addition to being a higher quality material than the other possible materials, GaAs is also more expensive and more difficult to manufacture. The typical phased array components take up a lot of area on the GaAs, and result in higher costs. Furthermore, a standard phase shifter has high RF loss, which is typically about $n+1$ dB of loss, where n is the number of phase bits in the phase shifter.

Another prior art embodiment uses RF MEMS switches and has lower loss but still consumes similar space and is incompatible with monolithic solutions.

Summary

In an exemplary embodiment, phased array antenna applications implement active vector generators, where the vector generators have amplitude control. In an exemplary embodiment, a vector generator with amplitude control uses a network of current mirror multipliers to digitally vary bias currents supplied to a differential adder. By varying the bias to the differential adder, the amplitude of a resultant vector produced by the network is controllable in binary steps. In an exemplary embodiment, an active vector generator with amplitude control is compatible with multi-beam systems and may be employed over a wide frequency range allowing a single antenna solution to function over multiple operating bands.

Furthermore, in an exemplary embodiment, the addition of amplitude control to the active vector generators allows a variety of system enhancements to be enjoyed. For example, a phased array antenna system may be configured for at least one of amplitude taper for antenna sidelobe management, adaptive nulling for interference rejection, complex beam weighting, and improved array calibration. Moreover, in an exemplary embodiment, a vector generator may also be configured to allow individual beam weights to be turned off, allowing additional system flexibility.

In an exemplary embodiment, an active vector generator is configured to generate a composite vector with controlled phase and amplitude, where the active vector generator generates the composite vector with independent variable phase control and independent variable amplitude control. Furthermore, in another exemplary embodiment, an active vector generator is configured to generate a unique number of phase states and configured to generate a unique number of amplitude states. Specifically, an exemplary active vector generator comprises a digital-to-analog converter (DAC) configured to set the phase of the composite vector, a current multiplying switch network configured to control the amplitude of the composite vector, a variable current multiplier configured to adjust the amplitude of the composite vector, and a differential adder configured to control the quadrant of the composite vector and generate the composite vector.

Brief Description Of The Drawing Figures

A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the drawing figures, wherein like reference numbers refer to similar elements throughout the drawing figures, and:

FIG. 1 illustrates an exemplary embodiment of an active vector generator;

FIG. 2 illustrates a graphic representation of unique phase states in an exemplary vector generator;

FIG. 3 illustrates a schematic of an exemplary embodiment of an active vector generator with phase control;

FIG. 4 illustrates a graphic representation of unique phase and amplitude states in an exemplary vector generator; and

FIG. 5 illustrates a schematic of an exemplary embodiment of an active vector generator with phase and amplitude control.

Detailed Description Of The Invention

While exemplary embodiments are described herein in sufficient detail to enable those skilled in the art to practice the invention, it should be understood that other embodiments may be realized and that logical material, electrical, and mechanical changes may be made without departing from the spirit and scope of the invention. Thus, the following detailed description is presented for purposes of illustration only.

In an exemplary embodiment, a vector generator converts an RF input signal into an output signal (sometimes referred to as an output vector) that is shifted in phase and/or amplitude to a desired level. This replaces the function of a typical phase shifter and adds the capability of amplitude control. In other words, a vector generator is a magnitude and phase control circuit. In the exemplary embodiment, the vector generator accomplishes this function by feeding the RF input signal into a quadrature network resulting in two output signals that differ in phase by about 90°. The two output signals are fed into parallel quadrant select circuits, and then through parallel variable gain amplifiers (VGAs). In an exemplary embodiment, the quadrant select circuits receive commands and may be configured to either pass the output signals with no additional relative phase shift between them or invert either or both of the output signals by an additional 180°. In this fashion, all four possible quadrants of the 360° continuum are available to both orthogonal signals. The resulting composite output signals from the current summer are modulated in phase.

In accordance with an exemplary embodiment and with reference to Figure 1, a vector generator 100 comprises a passive I/Q generator 110, a first VGA 120 and a second VGA 121, a first quadrant select 130 and a second quadrant select 131 each configured for phase inversion switching, and a current summer 140. The first quadrant select 130 is in communication with I/Q generator 110 and first VGA 120. The second quadrant select 131 is in communication with I/Q generator 110 and second VGA 121. Furthermore, in an exemplary embodiment, vector generator 100 comprises a digital controller 150 that controls a first digital-to-analog converter (DAC) 160 and a second DAC 161. The first and second DACs 160, 161 control first and second VGAs 121, 120, respectively. Additionally, digital controller 150 controls first and second quadrant selects 130, 131.

In an exemplary embodiment, vector generator 100 controls the phase and amplitude of an RF signal by splitting the RF signal into two separate vectors, the in-phase (I) vector and the quadrature-phase (Q) vector. In one embodiment, the RF signal is communicated differentially. The differential RF signal communication may be throughout vector generator 100 or limited to various portions of vector generator 100. In another exemplary embodiment, the RF signals are communicated non-differentially. The I vector and Q vector are processed in parallel, each passing through the phase inverting switching performed by first and second quadrant selects 130, 131. The resultant outputs of the phase inverting switches comprise four possible signals: a non-inverted I, an inverted I, a non-inverted Q, and an inverted Q. In this manner, all four quadrants of a phasor diagram are available for further processing by VGAs 120, 121. In an exemplary embodiment, two of the four possible signals non-inverted I, inverted I, non-inverted Q, and inverted Q are processed respectively through VGAs 120, 121, until the two selected signals are combined in current summer 140 to form a composite RF signal. The current summer 140 outputs the composite RF signal with phase and amplitude adjustments. In an exemplary embodiment, the composite RF signal is in differential signal form. In another exemplary embodiment, the composite RF signals are in single-ended form.

In an exemplary embodiment, control for the quadrant shifting and VGA functions is provided by a pair of DACs. In an exemplary embodiment, reconfiguration of digital controller 150 allows the number of phase bits to be digitally controlled after vector generator 100 is fabricated if adequate DAC resolution and automatic gain control (AGC) dynamic range exists. In an exemplary embodiment with adequate DAC resolution and AGC dynamic range, any desired vector phase and amplitude can be produced with selectable fine quantization steps using digital control. In another exemplary embodiment, reconfiguration of DACs 160, 161 can be made after vector generator 100 is fabricated in order to facilitate adjustment of the vector amplitudes.

In accordance with an exemplary embodiment and with reference to Figure 2, an active vector generator may be configured to adjust the phase of a signal. The active vector generator is capable of producing a finite number of unique phase states, which is dependent on the number of phase bits of the DAC. As previously described, the vector generator receives an input signal and generates a phase adjusted composite vector. The composite vector is a combination of an I vector and a Q vector. In this embodiment, the amplitude of the composite vector is the same in each of the unique phase states. In an exemplary embodiment, the total current consumed by the I and Q vectors is constant and only the current ratio between the two vector changes. The adjustment of the current ratio using the phase states alters the phase of the composite vector, while maintaining the amplitude of the composite vector for each of the unique phase states.

In an exemplary embodiment and with reference to Figure 3, a schematic design of an active vector generator is illustrated. In an exemplary embodiment, an active vector generator 300 comprises a DAC 310 and a fixed current multiplier 350. In another exemplary embodiment, active vector generator 300 further comprises a differential adder 360. DAC 310 outputs an I bias current and a Q bias current that passes to fixed current multiplier 350 through a current mirror. In turn, fixed current multiplier 350 is connected to differential adder 360. In this embodiment, the multiplier factor of fixed current multiplier 350 is the same for the I vector and the Q vector.

In an exemplary embodiment, DAC 310 is made of a bank of transistors and corresponding switches that is controlled by phase bits. For example, Figure 3 shows four phase bits and four corresponding switches. However, an exemplary DAC 310 may comprise any number of phase bits and corresponding switches. Furthermore, Iref is a current source that establishes a reference current that is mirrored to the bank of transistors whose peripheries vary in binary fashion. Although the bank of transistors has the peripheries varied in binary fashion, any method of varying the peripheries may be employed. In an exemplary embodiment, DAC 310 adjusts the current ratio between the I and Q vectors based on the phase bits. The switches in the DAC are controlled by the input phase bits. Specifically, the switches of DAC 310 are controlled by the phase bits and whether the current from the binary units are added to the bias currents. Moreover, the bias currents are supplied to the gates of the FETs in fixed current multiplier 350.

In an exemplary embodiment, fixed current multiplier 350 multiplies the current ratios by the same amount for both the I vector and the Q vector. This preserves the amplitude ratio between the I and Q vectors and thus keeps the resultant phase constant. The multiplied I vector and Q vector are communicated to differential adder 360. In an exemplary embodiment, both the I vector and the Q vector are multiplied by 'M' before being applied to differential adder 360. 'M' is the amplitude ratio of the final transistor peripheries in relation to the current mirrors.

In an exemplary embodiment, differential adder 360 is the same as VGAs 120, 121 and current summer 140 of vector generator 100. Furthermore, differential adder 360 can be any component that controls which quadrant the composite vector is in and combines two signals. In other words, differential adder 360 is configured to add the I vector and Q vector, or add an inverted I vector or an inverted Q vector. There is no variable amplitude control in this embodiment; the amplitude of the composite vector remains the same in each unique phase state.

In accordance with an exemplary embodiment and with reference to Figure 4, the graph illustrates an active vector generator with independent phase control and independent amplitude control. As with Figure 2, there are a limited number of unique phase states, which is dependent on the number of control bits. Specifically, the number of phase states is still controlled by the number of phase bits of the DAC. However, in the exemplary embodiment, independent amplitude control allows for the adjusting of the composite vector's amplitude. The number of unique amplitude states is controlled by the number of amplitude bits.

In an exemplary embodiment and with reference to Figure 5, an active vector generator 500 comprises a DAC 510, a current multiplying switch network 540, a variable current multiplier 550, and a differential adder 560. DAC 510 generates an I bias current and a Q bias current which controls the phase of the composite vector. DAC 510 is substantially similar to DAC 310 and will not be discussed in detail. In an exemplary embodiment, the I bias current and the Q bias current pass through a current mirror and are communicated to current multiplying switch network 540. Furthermore, in an exemplary embodiment, current multiplying switch network 540 communicates the I bias current and the Q bias current to variable current multiplier 550 via different current mirror reference lines, as controlled by the amplitude bits.

Current multiplying switch network 540 is configured to implement discrete amplitude states of the composite vector of active vector generator 500. In an exemplary embodiment, current multiplying switch network 540 comprises a plurality of switches in current mirror reference lines. Each current mirror reference line is connected to the current mirror, receiving either the I bias current or the Q bias current. Furthermore, each current mirror reference line is also connected to one of digitally controlled multipliers of variable current multiplier 550. Specifically, in an exemplary embodiment, the I bias current is connected, via multiple current mirror reference lines, to each of the digitally controlled multipliers of the I vector. Similarly, in the exemplary embodiment, the Q bias current is connected, via multiple current mirror reference lines, to each of the digitally controlled multipliers of the Q vector. Each of the current mirror reference lines includes a switch that completes or interrupts the signal path based on the amplitude bits. As an example, Figure 5 shows three amplitude bits and a total of six switches in current multiplying switch network 540, three switches controlling the Q bias vector path and three switches controlling the I bias vector path to variable current multiplier 550. In one embodiment, the amplitude bit lines are single-ended in nature. In another embodiment, the amplitude bit lines are differential in nature for added control. For example, differential signaling might be employed to provide field confinement and improve isolation between lines.

In an exemplary embodiment, variable current multiplier 550 is not a fixed current multiplier but instead comprises a bank of multipliers that can be digitally controlled by the amplitude bits. In an exemplary embodiment, the I bias vector and the Q vector are communicated to the bank of digitally controlled multipliers. In an exemplary embodiment, the transistor peripheries of variable current multiplier 550 vary in size in binary fashion such that the resulting vector varies in amplitude while preserving phase information established by DAC 510. For example, three bits of amplitude control correlates to eight amplitude states per vector, namely 0 to 7M in steps of size M. However, there can any number of amplitude bits greater than two in order to obtain amplitude adjustment.

In an exemplary embodiment, differential adder 560 is the same as VGAs 120, 121 and current summer 140. The differential adder 560 controls which quadrant the composite vector is in. In other words, differential adder 560 is configured to add the I vector and Q vector, or add an inverted I vector or an inverted Q vector. There are also various advantages to having switches to several or all of the binary elements. In one exemplary embodiment, turning off or substantially reducing the DC current to differential adder 560 saves power. In another exemplary embodiment, configuring the on/off states of the switches allows for isolating various signal paths and binary elements, which may be used in array calibration. In an exemplary embodiment of array calibration, all RF paths within the array of current multiplying switch network 540 are turned off except one path. The remaining one path that is still on has the amplitude and phase response measured. In an exemplary embodiment, the amplitude and phase response data is stored in an array calibration look up table by a host system. In this fashion all RF paths may be calibrated independent of all other paths.

The following applications are related to this subject matter: U.S. Application No. 12/759,123, entitled "ACTIVE BUTLER AND BLASS MATRICES," which is being filed contemporaneously herewith (docket no. 36956.7100); U.S. Application No. 12/759,043, entitled "ACTIVE HYBRIDS FOR ANTENNA SYSTEMS," which is being filed contemporaneously herewith (docket no. 36956.7200); U.S. Application No. 12/759,064, entitled "ACTIVE FEED FORWARD AMPLIFIER," which is being filed contemporaneously herewith (docket no. 36956.7300); U.S. Application No. 12/759,130, entitled "ACTIVE PHASED ARRAY ARCHITECTURE," which is being filed contemporaneously herewith (docket no. 36956.7600); U.S. Application No. 12/758,996, entitled "PRESELECTOR AMPLIFIER," which is being filed contemporaneously herewith (docket no. 36956.6800); U.S. Application No. 12/759,148, entitled "ACTIVE POWER SPLITTER," which is being filed contemporaneously herewith (docket no. 36956.8700); U.S. Application No. 12/759,112, entitled "HALF-DUPLEX PHASED ARRAY ANTENNA SYSTEM," which is being filed contemporaneously herewith (docket no. 55424.0500); U.S. Application No. 12/759,059, entitled "MULTI-BEAM ACTIVE PHASED ARRAY ARCHITECTURE," which is being filed contemporaneously herewith (docket no. 36956.6500); the contents of which are hereby incorporated by reference for any purpose in their entirety.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as critical, required, or essential features or elements of any or all the claims. As used herein, the terms “includes,” “including,” "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. Further, no element described herein is required for the practice of the invention unless expressly described as "essential" or "critical."

CLAIMS

1. An active vector generator configured to generate a composite vector with controlled phase and amplitude, wherein the active vector generator generates the composite vector with independent variable phase control and independent variable amplitude control.

2. An active vector generator configured to generate a unique number of phase states and configured to generate a unique number of amplitude states.

3. An active vector generator configured to generate a composite vector, the active vector generator comprising:

a digital-to-analog converter (DAC) configured to set the phase of the composite vector;

a current multiplying switch network configured to control the amplitude of the composite vector;

a variable current multiplier configured to adjust the amplitude of the composite vector; and

a differential adder configured to control the quadrant of the composite vector and generate the composite vector.

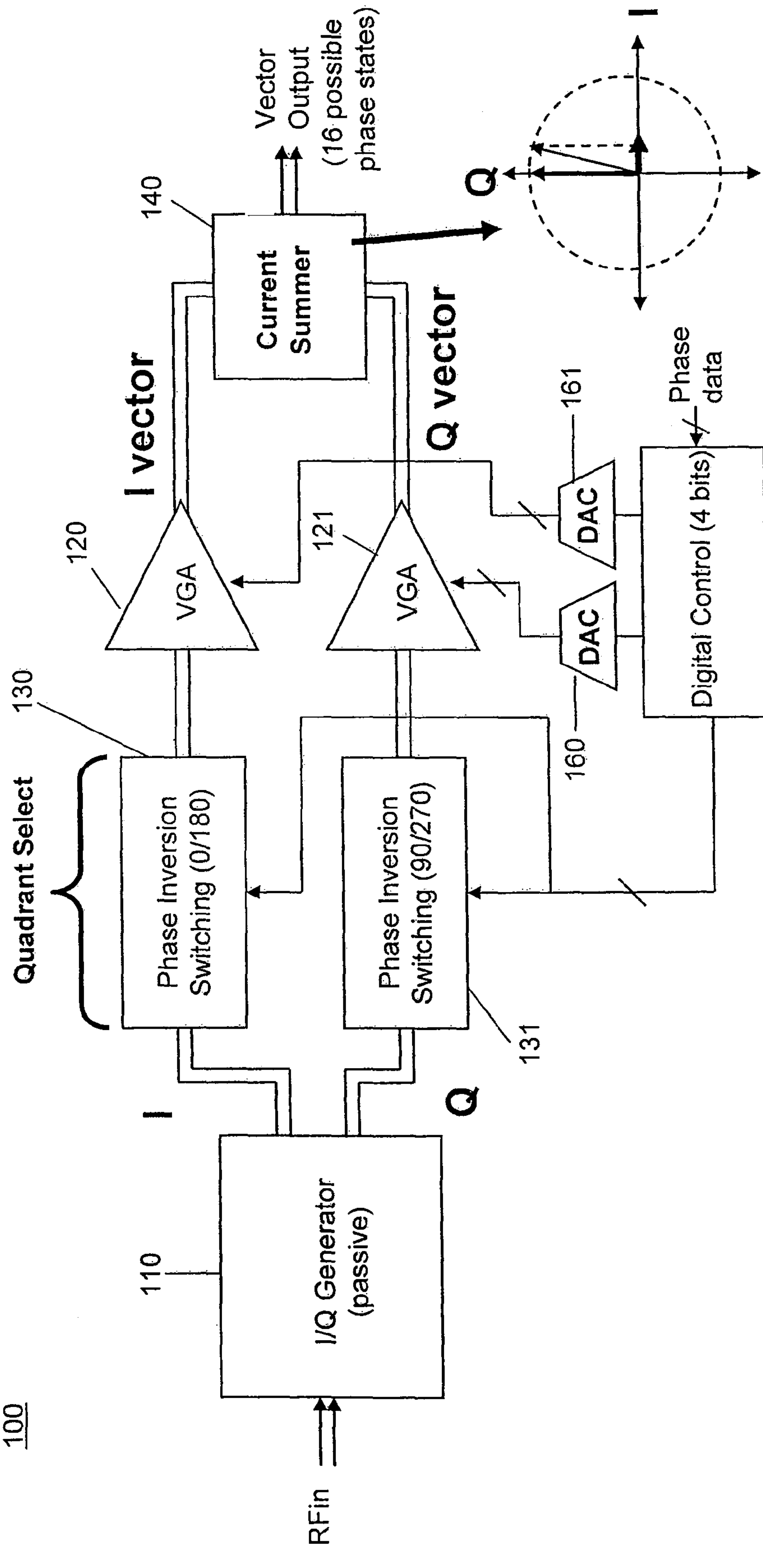
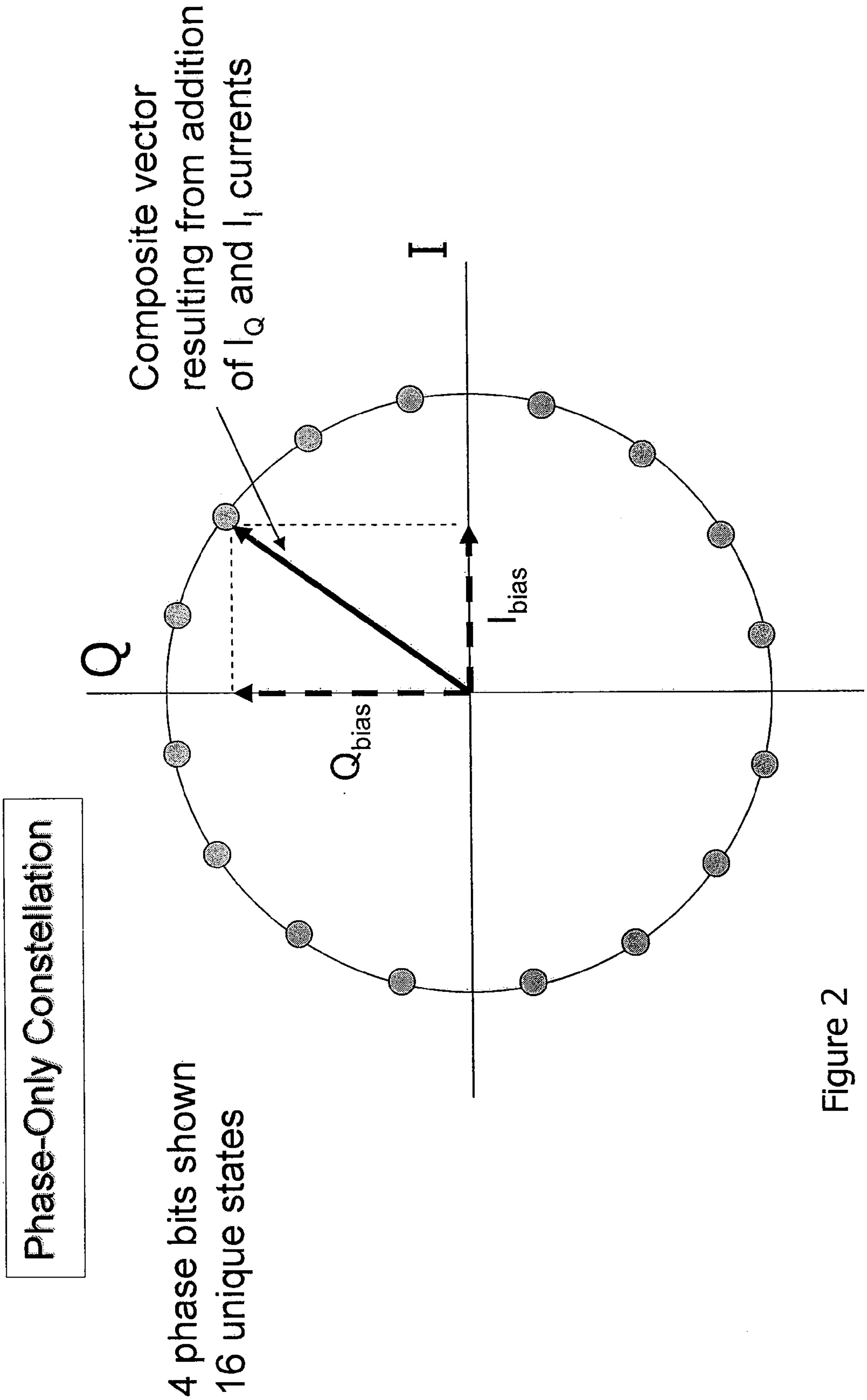

100
RFin
I/Q Generator
(passive)
110
I
Q
Quadrant Select
Phase Inversion
Switching (0/180)
130
Phase Inversion
Switching (90/270)
131
VGA
120
VGA
121
I vector
Q vector
DAC
160
DAC
161
Digital Control (4 bits)
150
Phase
data
Current
Summer
140
Vector
Output
(16 possible
phase states)
Q
I

Figure 1



Phase-Only Constellation
4 phase bits shown
16 unique states
Q
I
Q_{bias}
I_{bias}
Composite vector resulting from addition of I_Q and I_I currents

Figure 2

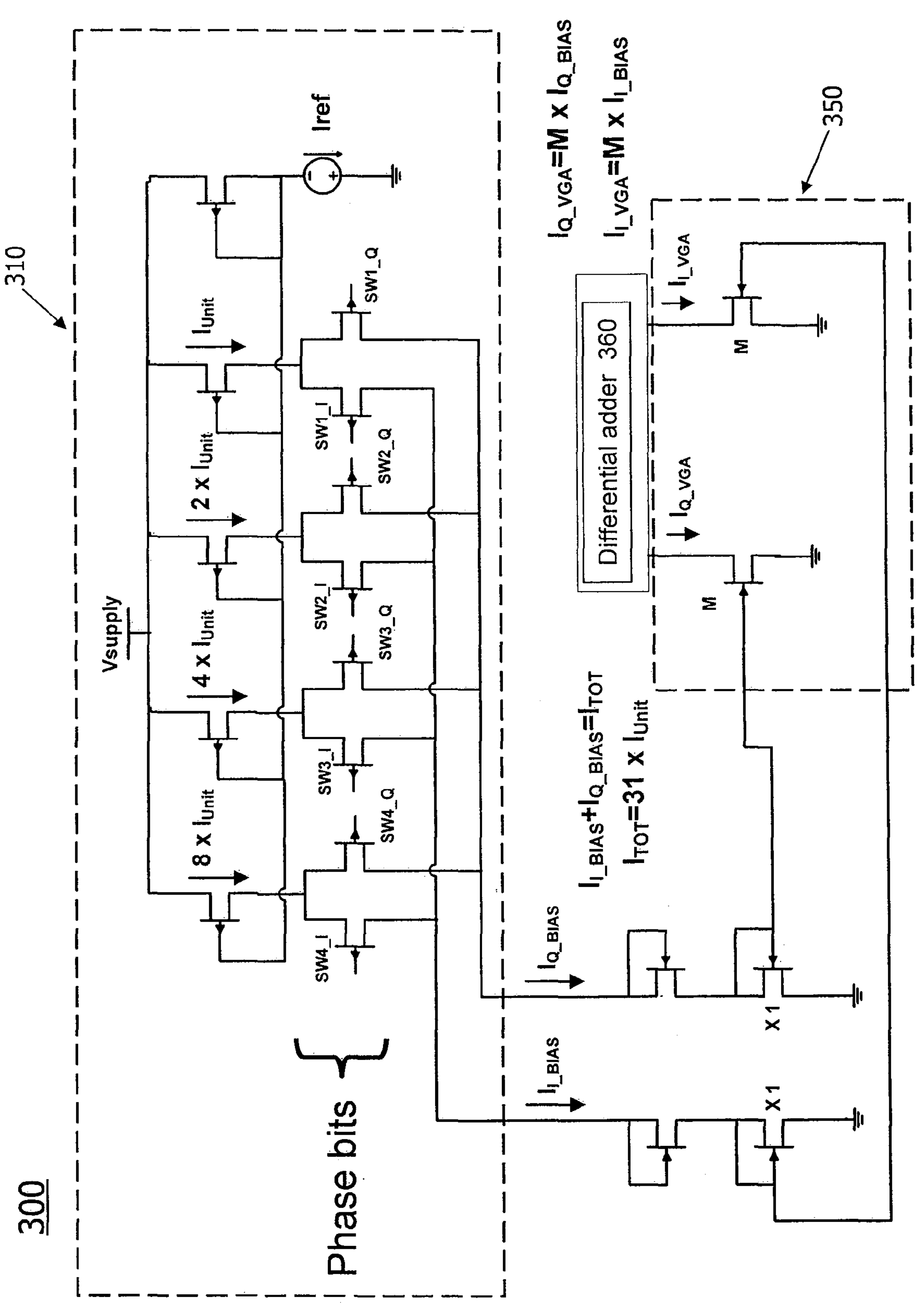

300
310
350
Vsupply
Iref
I_{Unit}
2 x I_{Unit}
4 x I_{Unit}
8 x I_{Unit}
SW1_Q
SW1_I
SW2_Q
SW2_I
SW3_Q
SW3_I
SW4_Q
SW4_I
Phase bits
I_{Q_BIAS}
I_{I_BIAS}
X 1
X 1
M
M
Differential adder 360
I_{Q_VGA}
I_{I_VGA}
I_{Q_VGA}=M x I_{Q_BIAS}
I_{I_VGA}=M x I_{I_BIAS}
I_{I_BIAS}+I_{Q_BIAS}=I_{TOT}
I_{TOT}=31 x I_{Unit}

Figure 3

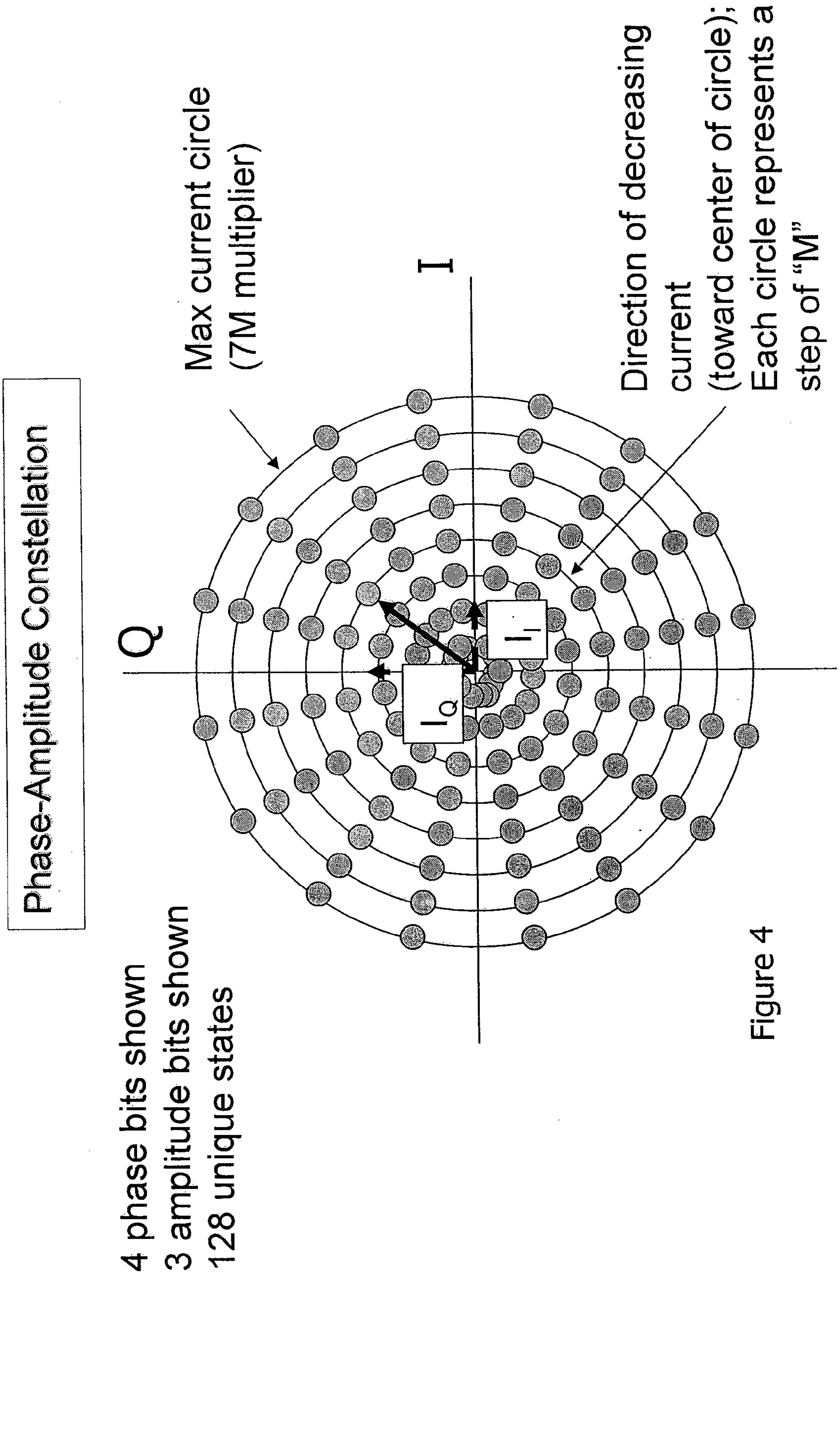

Phase-Amplitude Constellation
Max current circle
(7M multiplier)
Q
I
I_Q
I_I
Direction of decreasing
current
(toward center of circle);
Each circle represents a
step of "M"
4 phase bits shown
3 amplitude bits shown
128 unique states

Figure 4

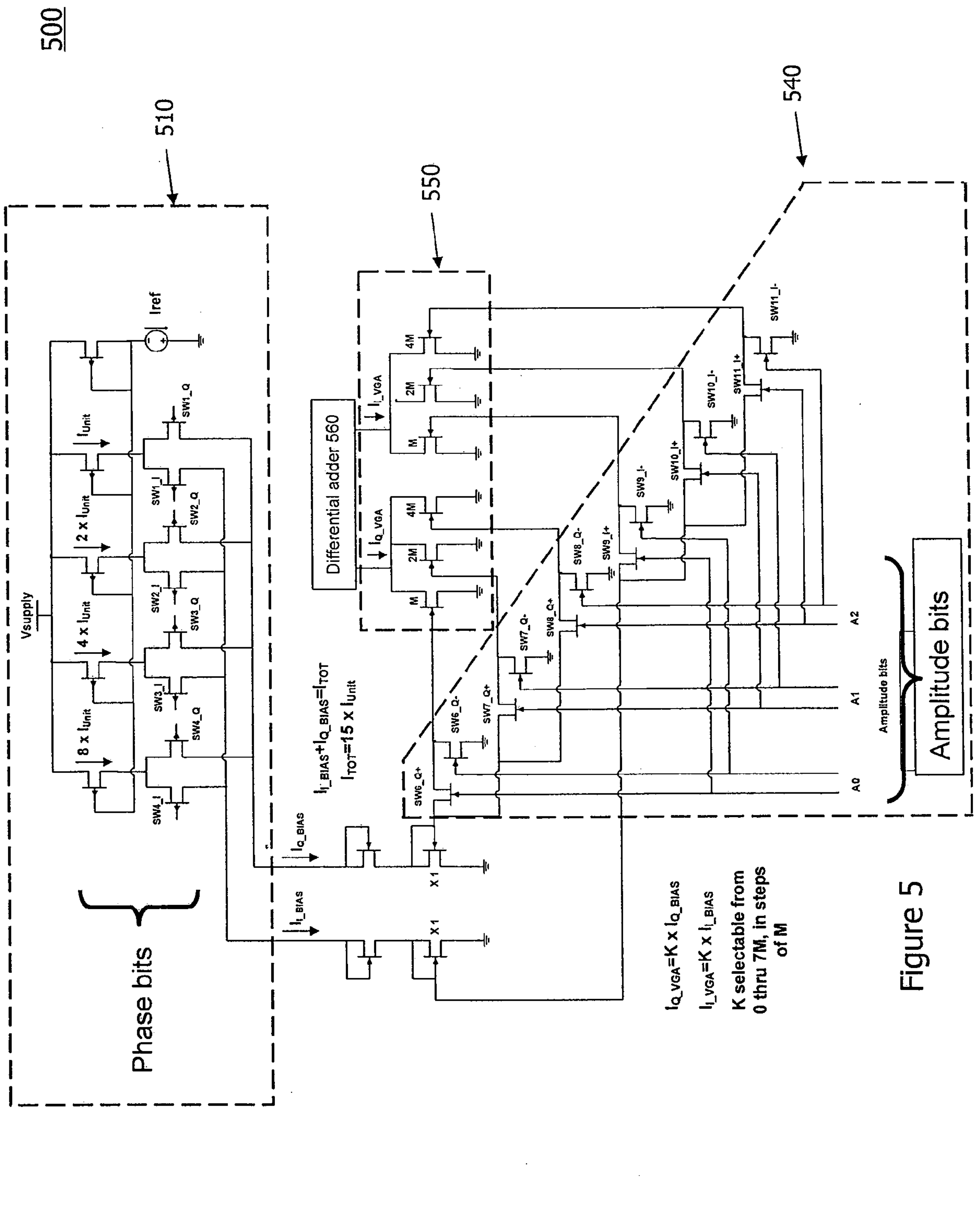

500
510
540
550
Vsupply
Iref
8 x I_Unit
4 x I_Unit
2 x I_Unit
I_Unit
SW1_Q
SW1_I
SW2_Q
SW2_I
SW3_Q
SW3_I
SW4_Q
SW4_I
Phase bits
Differential adder 560
I_Q_VGA
I_I_VGA
M
2M
4M
I_I_BIAS+I_Q_BIAS=I_TOT
I_TOT=15 x I_Unit
I_Q_BIAS
I_I_BIAS
X1
SW6_Q+
SW6_Q-
SW7_Q+
SW7_Q-
SW8_Q+
SW8_Q-
SW9_I+
SW9_I-
SW10_I+
SW10_I-
SW11_I+
SW11_I-
A0
A1
A2
Amplitude bits
I_Q_VGA=K x I_Q_BIAS
I_I_VGA=K x I_I_BIAS
K selectable from 0 thru 7M, in steps of M

Figure 5