FABRICATION OF VERTICAL SIDEWALLS ON (110) SILICON SUBSTRATES FOR USE IN SI/SIGE PHOTODETECTORS

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ABSTRACT

A method of fabricating vertical sidewalls on silicon (110) substrates for use in Si/SiGe photodetectors includes preparing a silicon (110) layer wherein the silicon (110) plane is parallel to an underlying silicon wafer surface. Masking the silicon (110) layer with mask sidewalls parallel to a silicon (111) layer plane and etching the silicon (110) layer to remove an un-masked portion thereof, leaving a patterned silicon (110) layer having vertical silicon (111) sidewalls. Removing the mask; growing SiGe-containing layers on the patterned silicon (110) layer; and fabricating a photodetector.
Fig. 3

14
PREPARE SUBSTRATE

18
BULK Si[110]

20
SOI WITH Si[110] TOP SILICON LAYER

22
APPLY PHOTORESIST OR HARDMASK

36
38
RIE

36
SELECTIVELY WET ETCH

40
GROW SiGe

42
FABRICATE PHOTODETECTOR

Fig. 5

26
28
FABRICATION OF VERTICAL SIDEWALLS ON (110) SILICON SUBSTRATES FOR USE IN SI/SIGE PHOTODETECTORS

FIELD OF THE INVENTION

[0001] This invention relates to photodetectors, and particularly to near-infrared photodetectors integrated on silicon substrates.

BACKGROUND OF THE INVENTION

[0002] Photo detecting in the near infrared regime, i.e., having a wavelength of between 0.7 μm to 2 μm, has many applications, such as in fiber-optic communication, security applications, machine vision and night vision imaging. Although III-V compound semiconductors provide superior optical performance over their silicon-based counterparts, the compatibility of silicon based materials with current silicon-IC technology provides the possibility of making cheap, small and highly integrated optical systems. The following references provide additional background for the invention: Maiti et al., Strained Silicon Heterostructures: Materials and Devices, Chapter 10: Si/SiGe Optoelectronics, The Institution of Electrical Engineer, 2001; Murtaza et al., Room Temperature Electroabsorption in Ge_xSi_1-x PIN Photodiode, IEEE Trans. on Electron Devices, 2297-2300, Vol. 41, No. 12, 1994; Tashiro et al., A Selective Epitaxial SiGe/Si Planar Photodetector for Si-Based OEICs, IEEE Trans. on Electron Devices, 545-550, Vol. 44, No. 4, 1997; Vonsovici et al., Room Temperature Photocurrent Spectroscopy of SiGe/Si p-i-n Photodiodes Grown by Selective Epitaxy, IEEE Trans. on Electron Devices, 538-542, Vol. 45, No. 2, 1998; and Jones et al., Fabrication and Modeling of Gigahertz Photodetectors in Heteroepitaxial Ge-on-Si using Graded Buffer Layer Deposited by Low Energy Plasma Enhanced CVD, IEDM, 2002.

[0003] Silicon photodiodes are widely used as photodetectors for visible light due to their low dark current and compatibility with silicon IC technologies. The use of Si_xGe_y (SiGe) alloys in silicon processing permits photo detection operating in the 0.8 μm to 1.6 μm wavelength regime.

[0004] SiGe alloys have larger lattice constants than pure silicon, thus, the epitaxial growth of SiGe on silicon has a critical thickness, above which the film begins to relax by the nucleation of dislocations. The critical thickness of SiGe depends on the germanium concentration and device process temperature. Houghton, Strain relaxation kinetics in Si_xGe_y/Si heterostructures, J. Appl. Phys. Vol. 780, No. 4, 1991.

[0005] A high germanium concentration and high device process temperature result in a smaller critical thickness. In common practice, the SiGe critical thickness is in the range of few hundred angstroms to a maximum of a couple thousand angstroms. Once the SiGe thickness is grown above its critical thickness, lattice defects in SiGe are inevitable. An IR photo detector built on SiGe containing lattice defects will have a high dark current and produce electronic noise.

[0006] Quantum efficiency is the number of electron-hole pairs generated per incident photon and is a parameter for photo detector sensitivity. The quantum efficiency is defined as:

$$\eta = \frac{I_p}{P_{opt} \cdot h \nu}$$

where I_p is the photo-generated current by the absorption of incident optical power P_{opt} at the light frequency ν, where q is the electron charge, and h is Planck's constant.

[0007] One of the key factors that determines the quantum efficiency is the absorption coefficient, α. Silicon has a cutoff wavelength of about 1.1 μm and is transparent to wavelengths beyond ~1.2 μm. The SiGe absorption edge shifts to the red with increasing germanium mole fraction and is shown in FIG. 1. The absorption coefficient of SiGe alloy is small and the critical thickness limits the absorbing layer thickness. The major aim of SiGe based photo detectors is to achieve high quantum efficiency and integration with existing silicon electronics.

[0008] One way to increase the optical path and improve the quantum efficiency is to illuminate the edge of the photo detector with light so that the light propagates parallel to the heterojunction (SiGe/Si) interfaces. However, this does not allow the device to be used in image detection. Growing strained, defect-free SiGe films or SiGe/Si multilayer structures on the sidewalls of etched silicon structures has been disclosed by Lee et al., Surface-Normal Optical Path Structure for Infrared Photodetection, U.S. Patent Publication No. 2005/0136637-A1, published Jun. 23, 2005; and Tweet et al., Vertical Optical Path Structure for Infrared Photodetection, U.S. Patent Publication No. 2005/013474-A1, published Jul. 1, 2005. In devices incorporating the technology described in the two preceding references, illumination of the device is normal to the silicon substrate, however, light travels parallel to the heterojunction interface to increase the optical path length. Therefore, two-dimensional IR image detection may be achieved within thin SiGe or SiGe/Si film thickenesses.

[0009] Fabrication of high quality, defect-free strained SiGe films requires SiGe growth on a defect-free silicon surface. However, referring to FIG. 2, reactive ion-etching (RIE) of silicon usually results in a sloped sidewall, shown generally at 10, and in poor crystal quality near the sidewall surface, as shown generally at 12, where a damaged area of silicon is formed near an RIE-etched sidewall. Also, the surface is often rather rough. Ideally, these defects may be cured by use of a selective etch, which etches the desired sidewall crystal plane more slowly than it does other planes. For various kinds of silicon device fabrication, silicon substrates having a (001) plane parallel to the wafer surface are most commonly used. Etching of a trench in this substrate renders the sidewalls parallel to the (110) planes or (100) planes, depending on the azimuthal rotation of the wafer. Making these sidewalls more vertical requires a selective etch, which etches the (110) or (100) planes, respectively, more slowly than other planes. However, such an etch process is not known in the prior art. Instead, there are well-known selective etches which etch the (111) plane much more slowly than other planes.

[0010] One way around this problem is to change the substrate to one with the silicon (110) plane parallel to the wafer surface. Liu et al., Multi-Fin Double-Gate MOSFET Fabricated by using (110)-Oriented SOI wafers and Orientation-Dependent Etching, Electrochemical Society Pro-
ceedings, vol. 2003-06, 566 (2003). Then, the sidewall plane may be silicon (111) or any other related, equivalent orthogonal plane. Liu et al. used a 2.38% tetramethylammonium hydroxide (TMAH) solution to etch vertical sidewalls and form a silicon fin structure with rectangular cross-section on silicon-on-insulator wafers. These were then used to fabricate silicon-FINFET (FIN Field-Effect Transistor) devices. Liu et al. report that TMAH etches (110) planes 23-25 times faster than silicon (111) planes. In addition, the use of a selective wet etch instead of RIE results in undamaged crystalline silicon at the sidewall surfaces.

SUMMARY OF THE INVENTION

[0011] A method of fabricating vertical sidewalls on silicon (110) substrates for use in Si/SiGe photodetectors includes preparing a silicon (110) layer wherein the silicon (110) plane is parallel to an underlying silicon wafer surface. Masking the silicon (110) layer with mask sidewalls parallel to a silicon (111) layer plane and etching the silicon (110) layer to remove an un-masked portion thereof, leaving a patterned silicon (110) layer. Finally, the mask is removed, and SiGe-containing layers are grown on the patterned silicon (110) layer. The photodetector is then completed.

[0012] It is an object of the invention to improve the quantum efficiency of photodetectors, e.g., near-IR photodetectors, integrated on silicon substrates.

[0013] Another object of the invention is to provide a method for using silicon (110) substrates and selective chemical etching to fabricate vertical sidewalls on which to grow strained SiGe and/or SiGe/Si multilayer structures for use in photodetectors, such as near-IR photodetectors.

[0014] This summary and objectives of the invention are provided to enable quick comprehension of the nature of the invention. A more thorough understanding of the invention may be obtained by reference to the following detailed description of the preferred embodiment of the invention in connection with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 represents normalized photocurrent spectra for various SiGe sample.

[0016] FIG. 2 is a schematic profile of RIE-etched silicon structures.

[0017] FIG. 3 is a block diagram of the method of the invention.

[0018] FIG. 4 depicts use of a bulk silicon (110) substrate.

[0019] FIG. 5 depicts use of a SOI (110) substrate.

[0020] FIG. 6 depicts bulk silicon (110) substrate following direct use of selective wet etch.

[0021] FIG. 7 depicts SOI (110) substrate following selective wet etch.

[0022] FIG. 8 depicts bulk silicon (110) substrate following anisotropic RIE etch.

[0023] FIG. 9 depicts SOI (110) substrate following anisotropic RIE etch.

[0024] FIG. 10 depicts bulk silicon (110) substrate following anisotropic RIE etch and selective wet etch.

[0025] FIG. 11 depicts SOI (110) substrate following anisotropic RIE etch and selective wet etch.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] The objective of this invention is to improve the quantum efficiency of photodetectors, e.g., near-IR photodetectors, integrated on silicon substrates. This is done by providing silicon structures with nearly vertical sidewalls and low crystalline defects to enable the growth of low-defect strained, epitaxial SiGe and/or SiGe/Si multilayers on the sidewalls. By so doing, the optical path length for absorption of light is be determined by the height of the sidewalls, and not by the SiGe film thickness. In this way the quantum efficiency of the photodetector is improved.

[0027] As previously noted, the use of reactive ion-etching (RIE) to etch silicon structures results in rough, damaged sidewalls with unacceptable large slopes. The readily available selective etch processes do not improve this situation on silicon (001) substrates. The present invention uses silicon (110) substrates and selective chemical etching to fabricate vertical sidewalls on which to grow strained SiGe and/or SiGe/Si multilayer structures for use in photodetectors, such as near-IR photodetectors.

[0028] Referring now to FIG. 3, the method of the invention is depicted generally at 14, includes preparation of a substrate, usually in the form of a silicon wafer, 16. The starting substrate has a silicon (110) plane parallel to the wafer surface. The substrate may be a bulk silicon (110) wafer 18, or it may be a silicon-on-insulator (SOI) wafer in which the top silicon has the (110) plane parallel to the wafer surface, referred to herein as a SOI(110) wafer 20. In the latter case, the top silicon needs to be sufficiently thick, e.g., 0.1 micron to 1.0 micron, or more, so as to result in a longer optical path length of the deposited SiGe film than can be achieved by the usual deposition on a planar substrate, i.e., the critical thickness. Note that it is only necessary for the top silicon to have the (110) plane parallel to the wafer surface. If a wafer-bonding technique, such as SmartCut® or Epitax®, is used, the silicon substrate beneath the buried-oxide (BOX) may have the usual (100) orientation. This procedure is likely less expensive than using a substrate of silicon (110).

[0029] In preparation for forming the vertical silicon surfaces, a photoreist, or hardmask, such as CVD deposited SiO₂, pattern is fabricated, by any state-of-the-art method, 22. It is important that the sidewalls of the photoreist or hardmask are parallel to the silicon (111) or equivalent plane, as shown in FIG. 4, wherein a silicon (110) substrate 24 has a mask 26 thereon. The mask sidewalls are parallel to the silicon (111) plane. FIG. 5 depicts a SOI (110) wafer 28, having a silicon substrate 30, a BOX layer 32 thereon, and a top silicon (110) layer 34. Mask elements 26 are formed on top silicon layer 24, again so that the mask sidewalls are parallel to the silicon (111). Vertical silicon surfaces with silicon (111) sidewalls can then be fabricated by one of two methods:

- Wet Etch Only

- [0030] A selective chemistry, such as a 2.38% tetramethylammonium hydroxide (TMAH) solution, is used to etch the
3. The method of claim 1 wherein said preparing a silicon (110) layer includes preparing a SOI wafer having a silicon (110) top silicon layer thereon.

4. The method of claim 1 wherein said masking the silicon (110) layer includes masking and patterning the silicon (110) layer with a masking taken from the group of maskings consisting of photoresist and hardmasks.

5. The method of claim 1 wherein said etching the silicon (110) layer includes etching by a RIE process and then further etching the silicon (110) layer by a selective wet etch process which etches silicon (110) planes faster than silicon (111) planes, leaving a patterned silicon (110) surface having silicon (111) sidewalls.

7. A method of fabricating vertical sidewalls on silicon (110) substrates for use in Si/SiGe photodetectors, comprising:

preparing a silicon (110) layer wherein the silicon (110) plane is parallel to an underlying silicon wafer surface, wherein said preparing a silicon (110) layer includes preparing a bulk silicon (110) substrate or preparing a SOI wafer having a silicon (110) top silicon layer thereon;

masking the silicon (110) layer with mask sidewalls parallel to a silicon (111) layer plane;

etching the silicon (110) layer to remove an un-masked portion thereof, leaving a patterned silicon (110) layer;

removing the mask;

growing SiGe-containing layers on the patterned silicon (110) layer; and

fabricating a photodetector.

8. The method of claim 7 wherein said masking the silicon (110) layer includes masking and patterning the silicon (110) layer with a masking taken from the group of maskings consisting of photoresist and hardmasks.

9. The method of claim 7 wherein said etching the silicon (110) layer includes etching by a selective wet etch process.

10. The method of claim 7 wherein said etching the silicon (110) layer includes etching by a RIE process and then further etching the silicon (110) layer by a selective wet etch process which etches silicon (110) planes faster than silicon (111) planes, leaving a patterned silicon (110) surface having vertical silicon (111) sidewalls.

11. A method of fabricating vertical sidewalls on silicon (110) substrates for use in Si/SiGe photodetectors, comprising:

preparing a silicon (110) layer wherein the silicon (110) plane is parallel to an underlying silicon wafer surface, wherein said preparing a silicon (110) layer includes preparing a bulk silicon (110) substrate or preparing a SOI wafer having a silicon (110) top silicon layer thereon;

masking the silicon (110) layer with mask sidewalls parallel to a silicon (111) layer plane;

etching the silicon (110) layer to remove an un-masked portion thereof, leaving a patterned silicon (110) layer;

removing the mask;

growing SiGe-containing layers on the patterned silicon (110) layer; and

fabricating a photodetector.

2. The method of claim 1 wherein said preparing a silicon (110) layer includes preparing a bulk silicon (110) substrate.
(111) planes, leaving a patterned silicon (110) surface having vertical silicon (111) sidewalls;
removing the mask;
growing SiGe-containing layers on the patterned silicon (110) layer; and
fabricating a photodetector.
12. The method of claim 11 wherein said preparing a silicon (110) layer includes preparing a bulk silicon (110) substrate.
13. The method of claim 11 wherein said preparing a silicon (110) layer includes preparing a SOI wafer having a silicon (110) top silicon layer thereon.
14. The method of claim 11 wherein said masking the silicon (110) layer includes masking and patterning the silicon (110) layer with a masking taken from the group of maskings consisting of photoresist and hardmasks.
15. The method of claim 11 wherein said etching the silicon (110) layer includes etching by a selective wet etch process.