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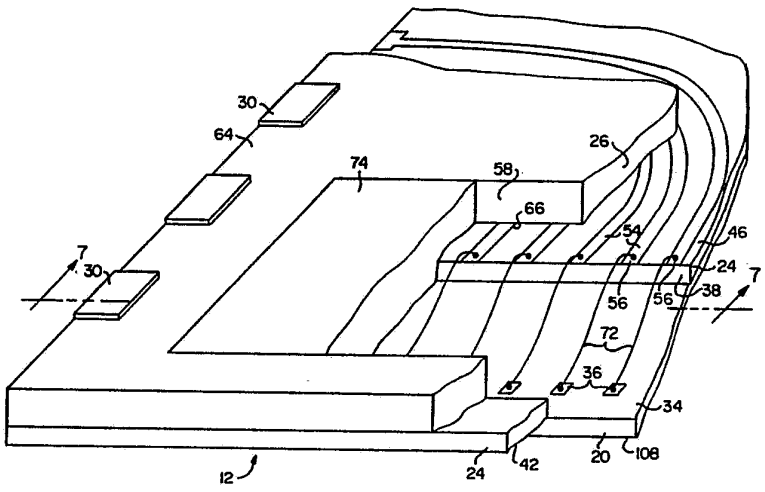

(57) Abstract

An IC chip package (12) and method of making the package (12) includes a chip having an upper active surface (34) bonded to the lower surface (42) of a substrate (24). Terminals (36) on the active surface (34) are wire bonded (32) through apertures (38) in a lower layer (24) of the substrate (22) to bonding pads (56) on the upper surface (46) of the substrate (24). Metallized strips (54) couple the bonding pads (56) to conductive pads (48) at the outer edges (50, 52) of the substrate (24). The substrate (22) includes an upper layer (26) having apertures (58) therein. After wire bonding (32), the apertures (58, 38) in the upper (26) and lower substrate layers are filled with epoxy (74), then the chip package (12) is electrically tested at various temperatures. The chip package (12) is programmed by wire bonding (32) a chip enable trace (37) to one of a plurality of optional bonding pads (57) of a bonding option array (55) on the lower substrate layer (24). The chip package (12) may then be assembled together with other chip packages (12) into a stack (10).

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IC CHIP PACKAGE AND METHOD OF MAKING SAME

1. Field of the Invention

The present invention relates to the high density packaging and stacking of integrated circuit chips to achieve, for example, an increased memory capacity in a memory circuit.

2. Description of Related Art

Known memory circuit systems are provided with several printed circuit boards, each having a plurality of integrated circuit (IC) chips encapsulated within packages mounted on the board. The printed circuit boards are typically arranged in a parallel relationship, with each board being disposed adjacent to and spaced from the other boards. If the chip packages are arranged in a single level on each circuit board, then a relatively large amount of space is required, particularly for large capacity memory systems. Moreover, the space between adjacent printed circuit boards is largely unused.

It has therefore become popular in recent years to arrange the chip packages in stacks so as to increase the density of the IC chips within the space available. U.S. Patent No. 4,956,694 of Floyd Eide, which issued September 11, 1990 and is assigned to the assignee of the present application, describes arrangements in which leadless chip carriers are stacked in order to greatly increase chip density. Each of the leadless chip carriers encapsulates a chip therein and has side faces provided with conductors extending between top and bottom surfaces of the leadless chip carrier. The data signal input and/or output terminals, power and ground terminals of each encapsulated chip are electrically connected to these conductors on the sides of the leadless chip carriers. The chip carriers are stacked, one above the other, such that the various conductors of the chip carriers are in alignment and

are electrically connected to one another. The result is a relatively dense stack of chips wired in parallel. At the same time, each chip is connected to a different set of aligned enable signal conductors so as to be enabled independently of all of the other chips in the stack.

The chip packages or carriers used to accomplish chip stacking can assume various different forms. An example of a chip package or carrier which is externally configurable is described in a copending patent application, Serial No. 07/552,578 of John Forthun, filed July 13, 1990 and commonly assigned with the present application. The Forthun application describes a chip carrier having a central cavity in which the chip is encapsulated. A carrier terminal provided on the outside of the chip carrier is electrically coupled to a circuit terminal on the chip such that the electrical coupling has a removable external configuration link. The configuration of an electronic circuit formed by the chip can be altered by removing the configuration link to break the electrical connection between the carrier terminal and the circuit terminal on the chip.

While the chip packages or carriers described in the Eide patent and in the Forthun application provide relatively compact chip packaging so that high density chip stacking can be accomplished on a printed circuit board, increased packaging density continues to be a desirable goal. Moreover, it would be desirable to provide additional chip packaging configurations and methods of making such chip packages which provide certain additional advantages not present in the prior art. For example, it would be desirable to be able to lap the chip or die to a desired thickness after being made part of a chip package, and it would be desirable to be able to program the package with a bonding wire after package test. The stacking of pre-tested partially packaged chips would also be a desirable feature.

SUMMARY OF THE INVENTION

In accordance with the invention, a chip package is provided in which the upper active surface of the chip is attached to the bottom of a multilayer substrate comprised of at least a lower layer and an upper layer. Various terminals on the active surface of the chip are wire bonded inwardly through a plurality of apertures in the lower substrate layer to bonding pads on an upper surface of the lower substrate layer. The bonding pads are coupled by metallized strips to conductors arranged along opposite side edges of the substrate for parallel electrical connection when a stack of the chip packages is formed. Because the chip terminals are wire bonded inwardly through apertures in the lower substrate layer, such wire bonding is confined within the outer periphery of the chip so as to confine the wire bonding within the X-Y plane of the three dimensional chip package. In this manner, the size of the chip package is minimized, and a stack of the chip packages can be formed within a very small space to provide a very high chip density.

In a preferred embodiment of a chip package according to the invention, the substrate is comprised of lower and upper layers of relatively thin, generally planar configurations which are joined together during formation of the substrate. The lower substrate layer has opposite apertures extending through the thickness thereof to receive bonding wires coupling the terminals on the upper active surface of the chip to bonding pads on an upper surface of the lower substrate layer. The chip is also of thin, planar configuration. Metallized strips on the upper surface of the lower substrate layer couple the bonding pads to conductive pads at the opposite outer edges of the lower substrate layer. The upper active layer of the chip is attached to the lower surface of the lower substrate layer. The upper substrate layer has three apertures extending through

the thickness thereof. Two of the apertures which are adjacent opposite ends of the upper layer overlay and are larger than the apertures in the lower substrate layer. The apertures in the upper and lower substrate layers are filled with epoxy after the wire bonding has been completed. A third aperture in the upper substrate layer provides access to a bonding option array on the upper surface of the lower substrate layer. The bonding option array includes a chip enable trace which is coupled via wire bond to a chip enable terminal on the active surface of the chip at one end of the substrate. By virtue of such access the chip enable trace is wire bonded to a selected one of a plurality of optional bonding pads within the bonding option array to complete connection to a selected input/output pad at the edge of the substrate during testing and programming of the chip assembly. The third aperture in the upper substrate layer is then filled with epoxy which is cured and then ground flat at the upper surface of the upper substrate layer.

In a preferred method of making a chip package according to the invention, the chip and the multilayer substrate are provided as separate elements. The upper active side of the chip is attached to the lower surface of the lower substrate layer with an appropriate adhesive such as epoxy. Next, the terminals on the active surface of the chip are wire bonded to the bonding pads on the upper surface of the lower substrate layer so that the bonding wires pass through the apertures adjacent the opposite ends of the lower substrate layer. The apertures in the lower substrate layer and the corresponding apertures in the upper substrate layer are then filled with epoxy. Following curing of the epoxy, the upper surface of the upper substrate layer is ground to make the epoxy flush with such surface. Next, the lower surface of the chip

is lapped as necessary to provide the chip with a desired thickness.

The chip package is then electrically tested at various different temperatures. One or more input/output (I/O) pins can be programmed by virtue of off-chip wire bonding. This is accomplished by wire bonding the chip enable trace to a selected one of the optimal bonding pads in the bonding option array. The position of the chip within a final stack assembly need not be determined until after the tests are performed and the associated yield loss determined. Following testing and programming, the third aperture in the upper substrate layer is filled with epoxy which is cured and then ground flush with the upper surface of the upper substrate layer.

The chip packages are then assembled into a stack. The conductive pads at the opposite edges of the substrate of each package are formed into vertical arrays of conductors in the stack by soldering, wire bonding or other appropriate connection. The result is a stack of partially packaged but fully tested chips. The stack itself can be tested and repaired as necessary. Thereafter, the stack is attached to a lead frame or substrate and encapsulated using transfer molding or other packaging techniques.

The ability to lap the chip in package form after handling in a thick form as part of the assembled chip package is advantageous. Also advantageous is the ability to post-test package programming with bonding wire, and the ability to form a stack of pre-tested partially packaged chips.

BRIEF DESCRIPTION OF THE DRAWINGS

A detailed description of the invention will be made with reference to the accompanying drawings, in which:

Fig. 1 is a perspective view of a portion of a chip stack employing a plurality of chip packages in accordance with the invention;

Fig. 2 is a side view of a portion of the chip stack of Fig. 1;

Fig. 3 is a plan view of a chip used in each of the chip packages in the stack of Figs. 1 and 2;

Fig. 4 is a plan view of a lower substrate layer forming a part of a multilayer substrate used in each of the chip packages of the chip stack of Figs. 1 and 2;

Fig. 5 is a plan view of an upper substrate layer forming another part of the multilayer substrate used in each of the chip packages of the chip stack of Figs. 1 and 2;

Fig. 6 is a perspective view, partly broken-away, of a portion of one of the chip packages of the chip stack of Figs. 1 and 2;

Fig. 7 is a sectional view of the chip package of Fig. 6 taken along the lines 7-7 thereof;

Fig. 8 is an enlarged plan view of the lower substrate layer of Fig. 4 after the chip of Fig. 3 has been attached to the multilayer substrate and wire bonding at the opposite ends has been accomplished;

Fig. 9 is a side view of a chip and substrate illustrating a prior art wire bonding arrangement;

Fig. 10 is a side view of a chip and substrate illustrating inward wire bonding in accordance with the present invention; and

Fig. 11 is a diagram of the successive steps employed in a method of making a chip package and a stack thereof in accordance with the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a chip stack 10 including a plurality of chip packages 12 in accordance with the invention. Although the chip stack 10 may be comprised of practically any number of the chip packages 12 that is desired, the example of Fig. 1 comprises four of the chip packages 12. The chip packages 12 are stacked in a vertical array on top of a lead frame or substrate 14. Vertical strips of solder 16 extend along side surfaces 18 of the individual chip packages 12 to couple conductive pads on the chip packages 12 in parallel. Such interconnections are shown in greater detail in Fig. 2, to which reference is now made.

Fig. 2 is a side view of the vertical stack of the chip packages 12 shown in Fig. 1. As shown in Fig. 2, each chip package 12 is comprised of an IC chip or die 20 disposed beneath a substrate 22. The substrate 22 is multilayer in nature and is comprised of a lower substrate layer 24 disposed immediately above and attached to the chip 20, and an upper substrate layer 26 disposed over the lower substrate layer 24. The chip 20 of each chip package 12 is disposed on top of the upper substrate layer 26 of the chip package 12 immediately below.

The lower and upper substrate layers 24 and 26 are separately shown and described herein for clarity of illustration. The layers 24 and 26 are joined together as part of the process of forming the substrate 22, before the chip 20 is attached thereto.

Each chip package 12 has a plurality of conductive films 28 spaced along the side surface 18 thereof. As described hereafter, each conductive film 28 is in electrical contact with a different conductive pad within the substrate 22 of the chip package 12. The conductive film 28 is attached to opposite conductive pads 30 and 32 at upper and lower surfaces respectively of the substrate 22 to form a generally U-shaped

electrical contacts during formation of the substrate 22. The solder strips 16 of Fig. 1 contact the conductive film 28 and the opposite conductive pads 30 and 32 of each chip package 12, to form a vertical conductor array, as shown in Fig. 2.

The chip 20, the lower substrate layer 24 and the upper substrate layer 26 of each chip package 12 are shown in Figs. 3, 4 and 5 respectively. As shown in Fig. 3, the chip 20 is rectangular in shape and of relatively thin, generally planar configuration. An upper active surface 34 of the chip 20 includes a plurality of electrical terminals 36 in conventional fashion. The terminals 36 are concentrated at opposite ends of the chip 20, and include a chip enable terminal 37.

The lower substrate layer 24 is shown in Fig. 4 as being a rectangular element of relatively thin, generally planar configuration as is the upper substrate layer 26 of Fig. 5. The lower and upper substrate layers 24 and 26 are of like length and width, but different in thickness, with the upper substrate layer 26 being thicker than the lower substrate layer 24. The lower substrate layer 24 is slightly longer and wider than the chip 20, so that apertures 38 and 40 adjacent the opposite ends thereof overlie the electrical terminals 36 at the opposite ends of the chip 20 when the active surface 34 of the chip 20 is attached to a lower surface 42 at the underside of the lower substrate layer 24. The lower surface 42 of the lower substrate layer 24 is shown in Fig. 2.

As shown in Fig. 4, the lower substrate layer 24 has an upper surface 46 opposite the lower surface 42 thereof. The upper surface 46 has a plurality of conductive pads 48 mounted thereon along opposite side edges 50 and 52 of the lower substrate layer 24 and forming input/output (I/O) terminals for the chip

package 12. The conductive pads 48 make electrical contact with the conductive films 28 on the side edges 18 of the chip packages 12 to couple corresponding ones of the conductive pads 48 within the different chip packages 12 in parallel. The upper surface 46 of the lower substrate layer 24 also includes a plurality of metallized strips 54 which extend from the conductive pads 48 to the edges of the apertures 38 and 40 and to a bonding option array 55 at a central region of the lower substrate layer 24. The metallized strips 54 which extend to the apertures 38 and 40 terminate in bonding pads 56 at the edges of the apertures. The remaining metallized strips 54 terminate at optional bonding pads 57 within the bonding option array 55. A metallized strip 59 which forms a main chip enable trace couples a central terminal 61 within the bonding option array 55 to a chip enable bonding pad 63 at the edge of the aperture 40. The chip enable bonding pad 63 is wire bonded to the chip enable terminal 37 on the chip 20, as described hereafter.

As shown in Fig. 5, the upper substrate layer 26 is provided with opposite apertures 58 and 60 and an intermediate aperture 62. The upper substrate layer 26 has an upper surface 64 shown in Fig. 5 and an opposite lower surface 66 shown in Fig. 2. When the lower and upper substrate layers 24 and 26 are joined during formation of the substrate 22, the apertures 58 and 60 overlay the apertures 38 and 40 in the lower substrate layer 24. At the same time, the intermediate aperture 62 in the upper substrate layer 26 overlays the bonding option array 55 on the lower substrate layer 24.

As also shown in Fig. 5, the various conductive pads 30 are mounted along the upper surface 64 at opposite side edges 68 and 70 of the upper substrate layer 26. The conductive pads 32 shown in Fig. 2 are mounted along the lower surface 42 of the lower substrate layer 24 at the opposite side edges 50 and 52

thereof, in similar fashion. The conductive pads 30 and 32 are joined by the conductive films 28 during formation of the substrate 22.

The lower and upper substrate layers 24 and 26 are separately shown and described herein for clarity of illustration, and are joined together to form the substrate 22 before the chip 20 is attached thereto. In the case of a ceramic substrate 22, the layers 24 and 26 are co-fired together in the same manner as layers in a standard multilayer hybrid substrate.

Fig. 6 is a perspective, partly broken-away view of the chip package 12. As shown therein, the upper active surface 34 of the chip 20 is attached to the lower surface 42 of the lower substrate layer 24. The terminals 36 on the active surface 34 are exposed by the aperture 38 in the lower substrate layer 24 and the aperture 58 in the upper substrate layer 26. Each terminal 36 on the active surface 34 of the chip 20 is attached by a bonding wire 72 to a bonding pad 56 at the end of one of the metallized strips 54 on the upper surface 46 of the lower substrate layer 24. Although not shown in Fig. 6, the chip enable terminal 37 is wire bonded to the chip enable bonding pad 63 in similar fashion. The apertures 38 and 58 are filled with a quantity of epoxy 74 which has been ground flush with the upper surface 64 of the upper substrate layer 26. Several of the conductive pads 30 on the upper surface 64 of the upper substrate layer 26 are shown in Fig. 6.

Fig. 7 is a sectional view of the chip package 12 taken along the line 7-7 of Fig. 6. This further illustrates the manner in which each terminal 36 at the upper active surface 34 of the chip 20 is coupled by a bonding wire 72 to a bonding pad 56 at an edge of the aperture 38 in the lower substrate layer 24. The apertures 38 and 58 are filled with the epoxy 74.

Fig. 8 is an enlarged plan view of the lower substrate layer 24. The chip 20 which is attached to the lower surface 42 of the lower substrate layer 24 is shown in dotted outline in Fig. 8. Fig. 8 illustrates the manner in which the various terminals 36 on the upper active surface 34 of the chip 20 are coupled through the apertures 38 and 40 to the bonding pads 56 by the bonding wires 72. The bonding pads 56 at the edges of the apertures 38 and 40 are coupled by the metallized strips 54 to the conductive pads 48 at the opposite side edges 50 and 52 of the lower substrate layer 24. One of the bonding wires 72 couples the chip enable terminal 37 to the chip enable bonding pad 63 at the end of the metallized strip 59.

During testing and programming of the chip package 12, the aperture 62 in the upper substrate layer 26 exposes the bonding option array 55 with the optional bonding pads 57 disposed adjacent and on opposite sides of the central terminal 61. During programming, a bonding wire 65 is used to couple a selected one of the optional bonding pads 57 to the central terminal 61, as shown in Fig. 8. Thereafter, the aperture 62 is filled with epoxy which is cured and then ground flat at the upper surface 64 of the upper substrate layer 26.

The manner in which inward bonding through the apertures 38 and 40 provides for increased chip density in accordance with the invention can be better appreciated with reference to Figs. 9 and 10. Fig. 9 depicts a typical prior art arrangement in which a chip 76 is mounted on the top of a substrate 78. The chip 76 has terminals 80 and 82 which are coupled by bonding wires 84 and 86 respectively to bonding pads 88 and 90 respectively on an upper surface 92 of the substrate 78. Because of such outward bonding, the width W_1 of the lateral space taken up by the chip 76 and the bonding wires 84 and 86 is substantial.

In the case of the present invention, however, as illustrated in Fig. 10, the inward bonding of the electrical terminals 36 of the chip 20 through apertures 38 and 40 to the bonding pads 56 on the upper surface 46 of the lower substrate layer 24 defines a width W_2 which is no greater than the width of the chip 20. It is this reduction in the X - Y plane of the chip package 12 that provides for substantially greater chip density within the chip stack 10. The various side edges of the chip 20 lie within planes defining an outer periphery of the chip 20. In arrangements according to the invention, as illustrated in Fig. 10, the bonding wires 72 are confined within such planar outer periphery of the chip 20. Arrangements of the chip packages 12 in accordance with the invention have been found to provide a chip density within the chip stack which is as much as 5 - 6 times greater than the chip density of the arrangements described in the previously referred to copending application Serial No. 07/552,578 of Forthun.

Fig. 11 shows the successive steps of a preferred method of making the chip stack 10 and the chip packages 12 in accordance with the invention.

In a first step 94 of the method shown in Fig. 11, the chip 20 and the substrate 22 are separately formed. The formed substrate 22 comprises the lower and upper layers 24 and 26 joined together to form the integral substrate.

In a second step 96 shown in Fig. 11, the upper active surface 34 of the chip 20 is attached to the lower surface 42 of the lower substrate layer 24. This is accomplished using epoxy or other appropriate adhesive.

In a third step 98 shown in Fig. 11, the terminals 36 on the upper active surface 34 of the chip 20 are wire bonded to the bonding pads 56 on the upper surface 46 of the lower substrate layer 24 using the bonding

wires 72. As previously described, the bonding wires 72 extend through the apertures 38 and 40 in the lower substrate layer 24. At the same time, the chip enable terminal 37 is wire bonded to the chip enable bonding pad 63 through the aperture 38.

In a fourth step 100 shown in Fig. 11, the apertures 38 and 40 in the lower substrate layer 24 and the overlying apertures 58 and 60 in the upper substrate layer 26 are filled with epoxy which is then cured.

Following curing of the epoxy, and in a fifth step 102 shown in Fig. 11, the upper surface 64 of the upper substrate layer 26 is ground to remove excess epoxy. This is accomplished by grinding the surface 64 so that it is flat.

The processing as described thus far allows the chip package 12 to be formed with the chip 20 attached thereto in a relatively thick form. In accordance with a sixth step 104 of the method shown in Fig. 11, a lower surface 108 of the chip 20 opposite the upper active surface 34 thereof is lapped to provide the chip 20 with a desired thickness. In the present example, described in detail herein for purposes of illustration only, the chip 20 is lapped to a thickness of 0.005 inches. The substrate 22 has a thickness of approximately 0.021 inches. This results in the chip package 12 having a total thickness of less than 0.030 inches. The chip 20 of the present example has a length of approximately 0.550 inches and a width of approximately 0.225 inches. The substrate 22 has a length of approximately 0.650 inches and a width of approximately 0.300 inches.

In a seventh step 110 of the method shown in Fig. 11, the chip package 12 as so produced is electrically tested. Testing is carried out at various different temperatures, and determines whether the chip package 12 is acceptable or whether it should be rejected. The

testing also determines the operating speed of the chip package 12 and other factors such as whether it should be classified as high power or low power. Later, when a chip stack is formed, chip packages with similar operating speed characteristics are assembled together.

In an eighth step 112 shown in Fig. 11, the chip package is programmed by connecting a length of bonding wire, such as the bonding wire 65 shown in Fig. 8, between the central terminal 61 and a desired one of the optional bonding pads 57 within the bonding option array 55. The aperture 62 in the control region of the upper layer 26 of the substrate 22 provides the necessary access. This has the effect of coupling the chip enable terminal 37 to a desired I/O terminal in the form of one of the conductive pads 48 on the upper surface 46 of the lower substrate layer 24.

In a ninth step 114 shown in Fig. 11, the aperture 62 in the upper substrate layer 26 is filled with epoxy and cured.

In a tenth step 116 shown in Fig. 11, the upper surface 64 of the upper substrate layer 26 is ground to remove excess epoxy and make the surface 64 flat.
In an eleventh step 118 shown in Fig. 11, a stack of the chip packages 12 is assembled to form the chip stack 10. The electrical terminals formed by the conductive film 28 together with the conductive pads 30 and 32 at the opposite edges of the substrate 22 of each chip package 12 are vertically connected by soldering to form the solder strips 16 shown in Fig. 1.

In a final step 120 shown in Fig. 11, the stack of chip packages 12 is secured to the lead frame 14. The stack of chip packages 12 is thereafter encapsulated using transfer molding or other conventional packaging techniques to form the completed chip stack 10.

It will be appreciated by those skilled in the art that apparatus and methods in accordance with the present invention provide a number of important

advantages. As previously described, mounting of the chip at the underside of the substrate and then wire bonding inwardly through apertures in the lower substrate layer provides a chip package of compact size and a chip stack having very high chip density. It is also advantageous to be able to mount the chip on the substrate and thereafter process the chip package with the chip in a relatively thick and durable form. Only after the chip package is formed is the chip lapped to its final thickness. The chip assembly may be tested by coupling the main enable trace to a bonding pad at one of the outer edges of the substrate to determine the speed and other characteristics of the assembly. In this manner, chip assemblies with similar speed characteristics can be assembled into the same stack. Programming may then take place, with the main chip enable trace being wire bonded to a desired one of the optional bonding pads. This is advantageously done with the chip already encapsulated within the chip package and thereby protected. A stack of the pre-tested and partially packaged chips is then formed, with the stack being attached to a frame and encapsulated. The stack can be later disassembled to replace a faulty chip.

The presently disclosed embodiments are to be considered in all respects illustrative and not restrictive. The scope of the invention is indicated by the appendant claims, rather than the foregoing description. All changes which come within the meaning and range of equivalency of the claims are intended to be embraced therein.

WHAT IS CLAIMED IS:

1. A method of making a chip package comprising the steps of:

providing a chip having a plurality of terminals on a surface thereof;

providing a substrate having a plurality of bonding pads on a surface thereof and at least one aperture therein;

attaching the chip to the substrate; and

wire bonding the terminals of the chip to the bonding pads of the substrate through the at least one aperture in the substrate.

2. A method of making a chip package in accordance with claim 1, comprising the further steps of:

filling the at least one aperture in the substrate with epoxy after the step of wire bonding the terminals is completed; and

grinding the epoxy flush with an upper surface of the substrate.

3. A method of making a chip package in accordance with claim 2, further comprising the step of:

lapping the chip to a desired thickness after the step of grinding the epoxy is completed.

4. A method of making a chip package in accordance with claim 3, further comprising the step of:

electrically testing the chip package after the step of lapping the chip is completed.

5. A method of making a chip package in accordance with claim 4, further comprising the step of:

programming the chip package after the step of electrically testing the chip package is completed, the step of programming being carried out by wire bonding a chip enable trace to one of a plurality of optional bonding pads in a bonding option array located within the substrate.

6. A method of making a chip package in accordance with 1, wherein:

the chip has an active side on which the plurality of terminals is located;

the substrate has a lower layer having a lower side and an opposite upper side on which the plurality of bonding pads is located; and

the step of attaching the chip comprises attaching the active surface of the chip to the lower side of the lower substrate layer.

7. A method of making a chip package in accordance with claim 6, wherein:

the step of wire bonding comprises coupling at least some of the plurality of terminals of the chip to corresponding ones of the plurality of bonding pads by wires extending through the at least one aperture in the substrate.

8. A method of making a chip package comprising the steps of:

providing a chip;

providing a substrate;

attaching the chip to the substrate to form a chip package; and

lapping the chip of the chip package to a desired thickness.

9. A method of making a chip package in accordance with claim 8, wherein:

the chip has a plurality of electrical terminals thereon and an outer periphery defined by a plurality of outer edges;

the substrate has a plurality of electrical terminals therein; and

conducting the further step of wire bonding the plurality of electrical terminals of the chip to the plurality of electrical terminals of the substrate so that the wire bonding is confined within the outer periphery of the chip.

10. A method of making a chip package comprising the steps of:

providing a chip having a plurality of electrical terminals thereon;

providing a substrate having a plurality of electrical terminals thereon;

attaching the chip to the substrate;

electrically coupling the plurality of electrical terminals on the chip to the plurality of electrical terminals on the substrate to form a chip package; and

electrically testing the chip package.

11. A method of making a chip package in accordance with claim 10, wherein:

the step of electrically testing the chip package is carried out at a plurality of different temperatures.

12. A method of making a chip package in accordance with claim 10, comprising the further step of:

programming the coupling of one of the plurality of electrical terminals of the chip to one of the plurality of electrical terminals on the substrate after the step of electrically testing has been completed.

13. A method of making a stack of chip packages comprising the steps of:

making a plurality of chip packages, each having a chip attached to a substrate;

electrically testing each of the chip packages; and

assembling the electrically tested chip packages into a stack.

14. A chip package comprising the combination of:

a chip having opposite side edges defining a peripheral wall of the chip;

a substrate coupled to the chip and having a plurality of electrical terminals contained within the peripheral wall of the chip; and

a plurality of bonding wires contained within the peripheral wall of the chip and each coupling one of the plurality of electrical terminals of the chip to one of the plurality of electrical terminals of the substrate.

15. A chip package in accordance with claim 14, wherein the substrate extends beyond the peripheral wall of the chip at opposite sides thereof.

16. A chip package in accordance with claim 14, wherein the chip has at least one aperture therein for receiving the plurality of bonding wires.

17. A chip package comprising the combination of:

a chip having a plurality of terminals on an active surface thereof;

a lower substrate layer having opposite upper and lower surfaces and at least one aperture extending between the upper and lower surfaces and a plurality of bonding pads on the upper surface, the lower surface of the lower substrate being coupled to the active surface of the chip;

a plurality of bonding wires, each extending through the at least one aperture in the lower substrate layer and coupling one of the plurality of terminals on the active surface of the chip to one of the plurality of bonding pads on the upper surface of the lower substrate layer; and

an upper substrate layer disposed on the upper surface of the lower substrate layer.

18. A chip package in accordance with claim 17, wherein the upper substrate layer has at least one aperture therein communicating with the at least one aperture in the lower substrate layer; and

the at least one aperture in the upper substrate layer and the at least one aperture in the lower substrate layer are filled with epoxy.

19. A chip package in accordance with claim 17, wherein the lower substrate layer has a plurality of conductive pads on an outer periphery of the upper surface thereof coupled to the plurality of bonding pads on the upper surface by metallized strips.

20. A chip package in accordance with claim 19, wherein the lower substrate layer and the upper substrate layer together define a plurality of outer edges of the chip package, and further including a plurality of conductive elements mounted on at least one of the plurality of outer edges of the chip package and coupled to the plurality of conductive pads on the lower substrate layer.

21. A chip package in accordance with claim 17, wherein the plurality of terminals on the active surface of the chip are divided into first and second groups of terminals adjacent opposite ends of the chip, the lower substrate layer has two apertures therein disposed over the first and second groups of terminals respectively on the chip, and the plurality of bonding pads on the upper surface of the lower substrate layer are divided into first and second groups of bonding pads adjacent the first and second apertures respectively in the lower substrate layer.

22. A chip package in accordance with claim 21, wherein the upper substrate layer has first and second apertures therein disposed over and larger in size than the first and second apertures respectively in the lower substrate layer.

23. A chip package in accordance with claim 22, wherein the first and second apertures in the lower substrate layer and the first and second apertures in the upper substrate layer are filled with epoxy.

24. A chip package in accordance with claim 17, further including a bonding option array disposed on the upper surface of the lower substrate layer and including a central terminal coupled to one of the plurality of bonding pads, a plurality of optional bonding pads and a bonding wire coupling the central terminal to one of the plurality of optional bonding pads.

25. A chip package in accordance with claim 24, wherein the upper substrate layer has an aperture therein disposed over the bonding option array.

26. A chip package in accordance with claim 25, wherein the aperture in the upper substrate layer is filled with epoxy.

27. A stack of chip packages comprising the combination of:

a base;

a stack of chip packages mounted on the base and each of the chip packages having a plurality of conductors at an outer periphery thereof coupled to a plurality of conductors on the other chip packages by a plurality of vertical conductors; and

each of the chip packages comprising a chip bonded to an underside of a substrate and having a plurality of electrical terminals wire bonded within the chip package to a plurality of electrical terminals within the substrate.

28. A stack of chip packages in accordance with claim 27, wherein each chip package includes a lower substrate layer bonded to the chip and having the plurality of electrical terminals on an upper surface thereof adjacent at least one aperture therein, and the plurality of electrical terminals on the chip are bonded to the plurality of electrical terminals on the upper surface of the lower substrate layer by bonding wires extending through the at least one aperture in the lower substrate layer.

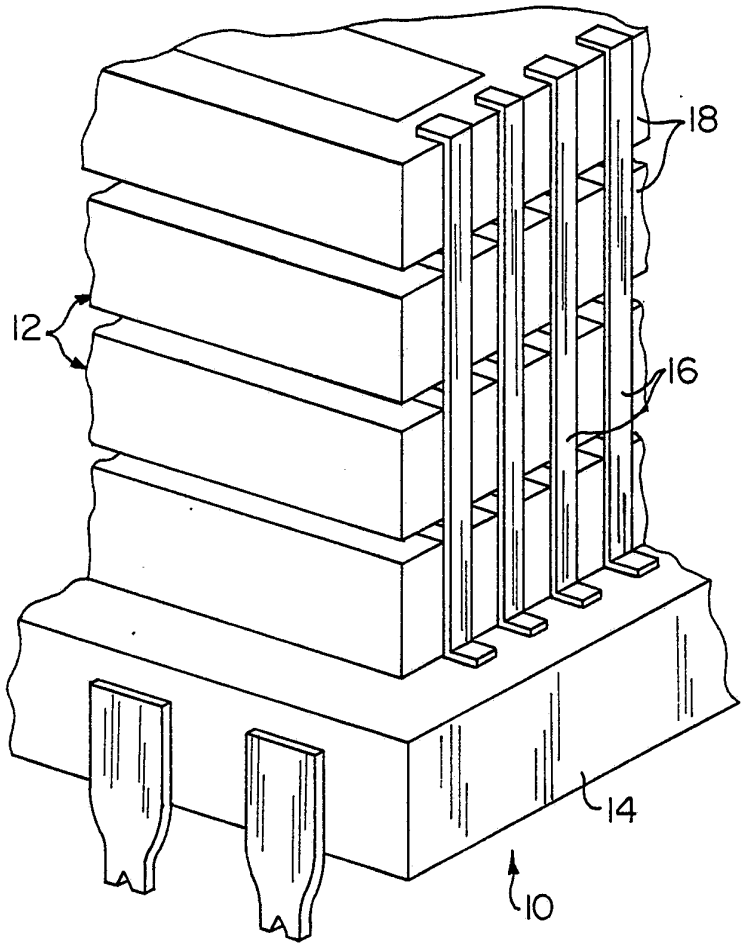


FIG. 1

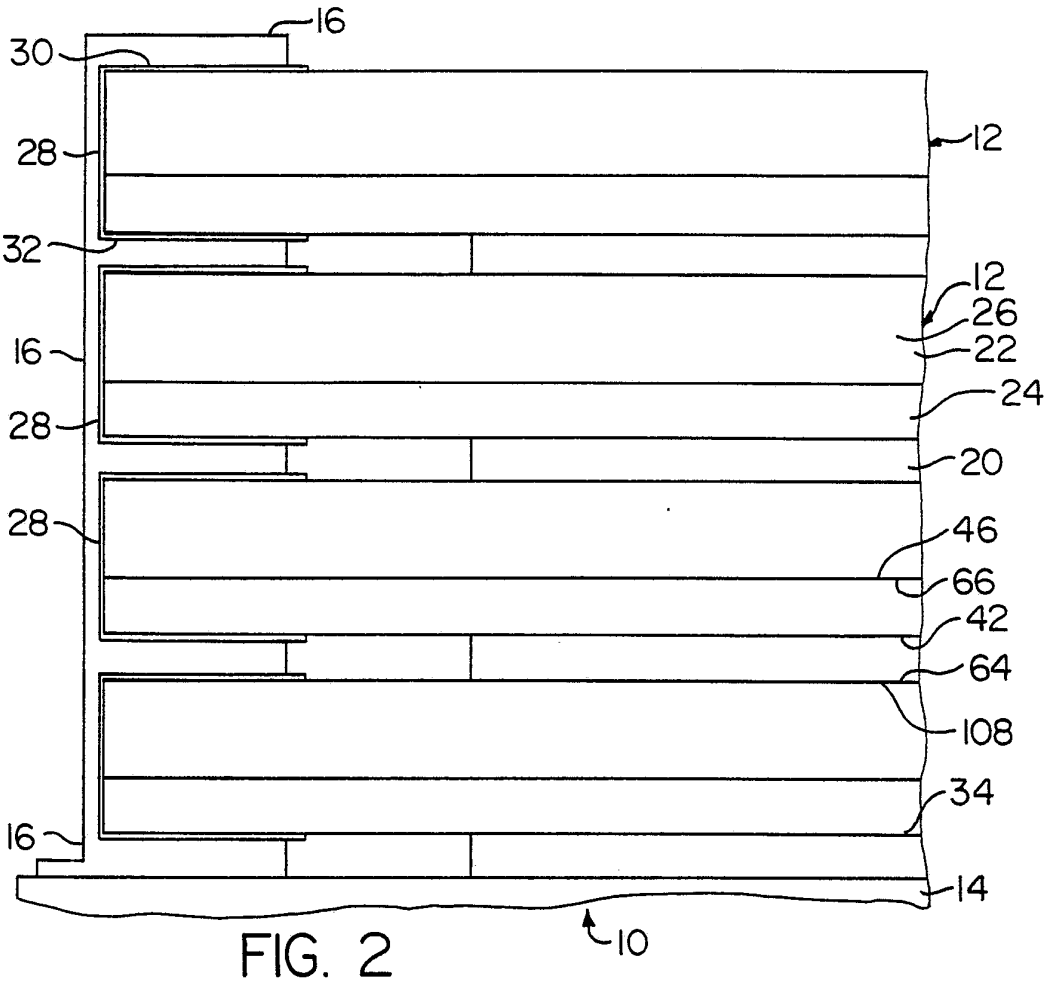


FIG. 2

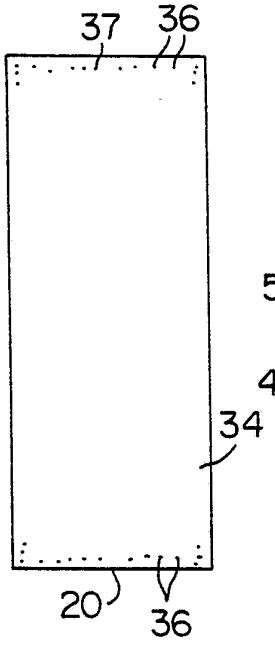


FIG. 3

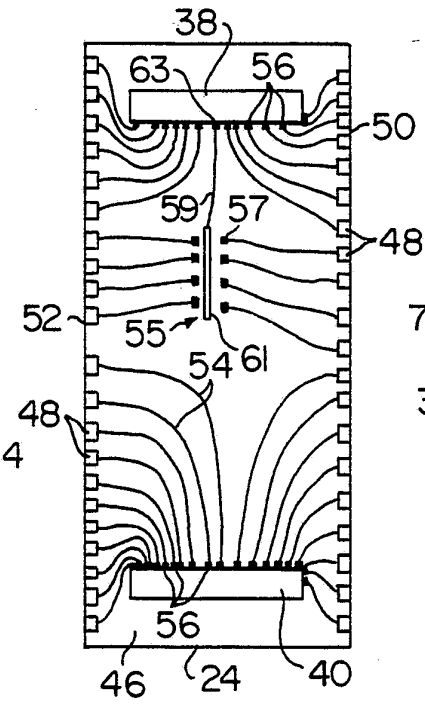


FIG. 4

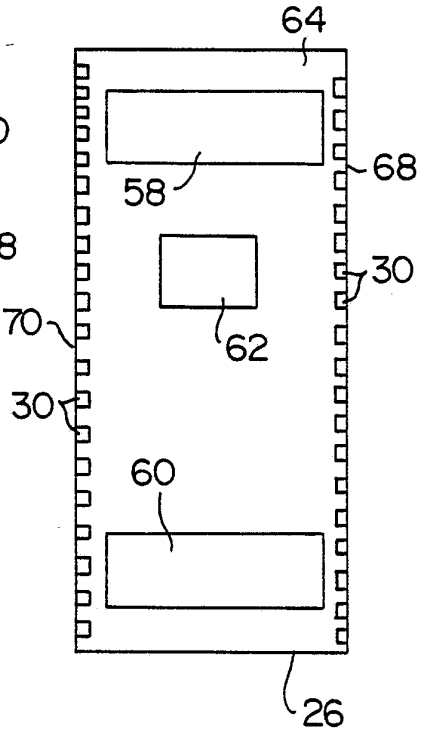


FIG. 5

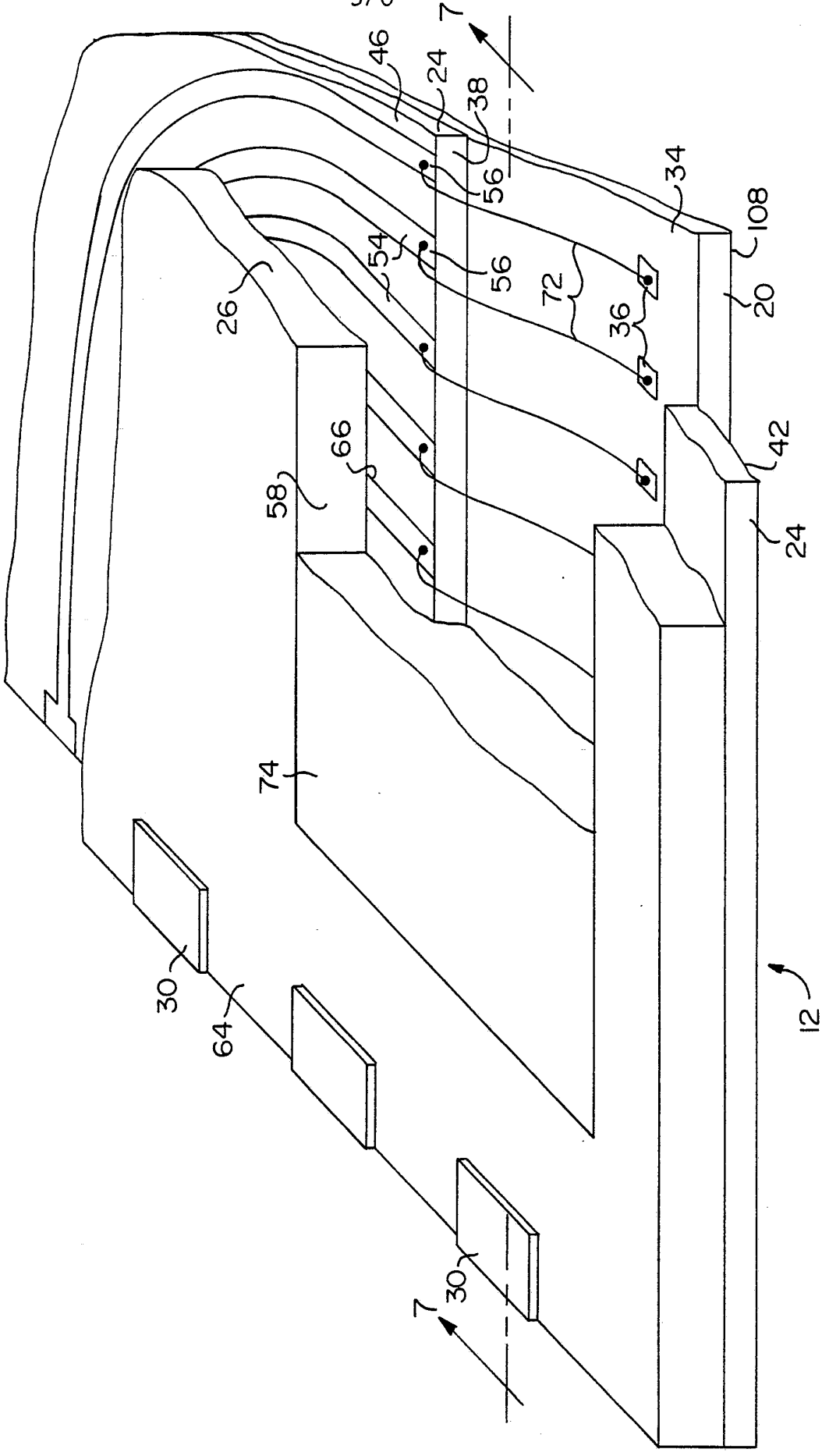
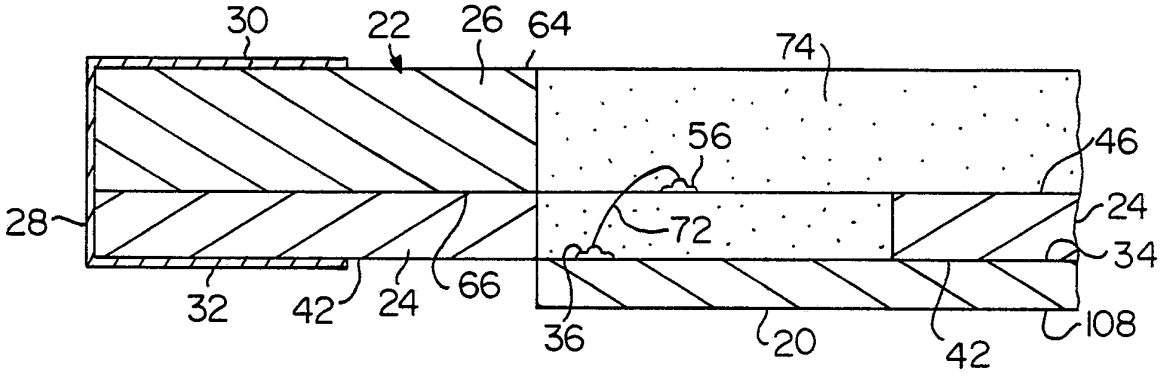


FIG. 6

FIG. 7



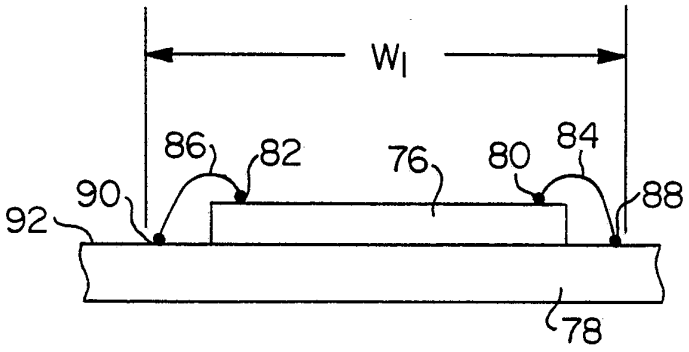


FIG. 9
PRIOR ART

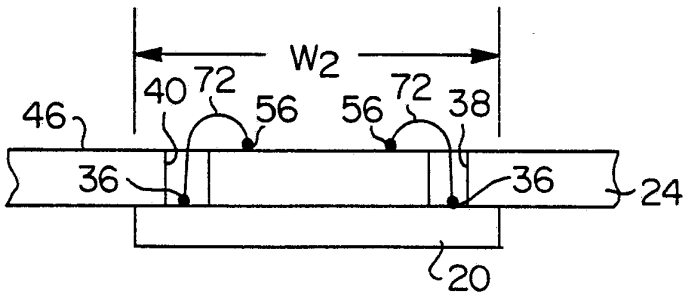


FIG. 10

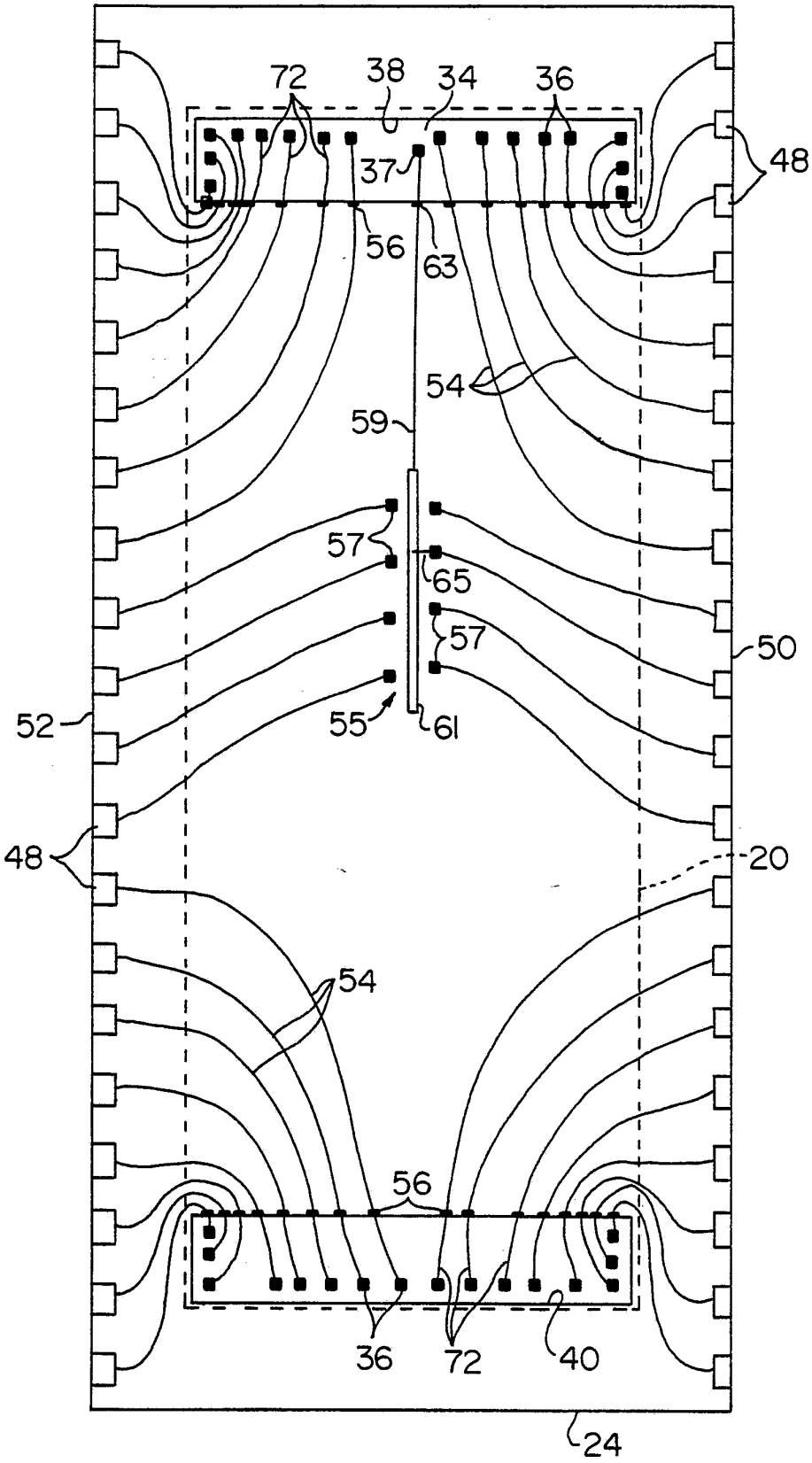

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FIG. 8

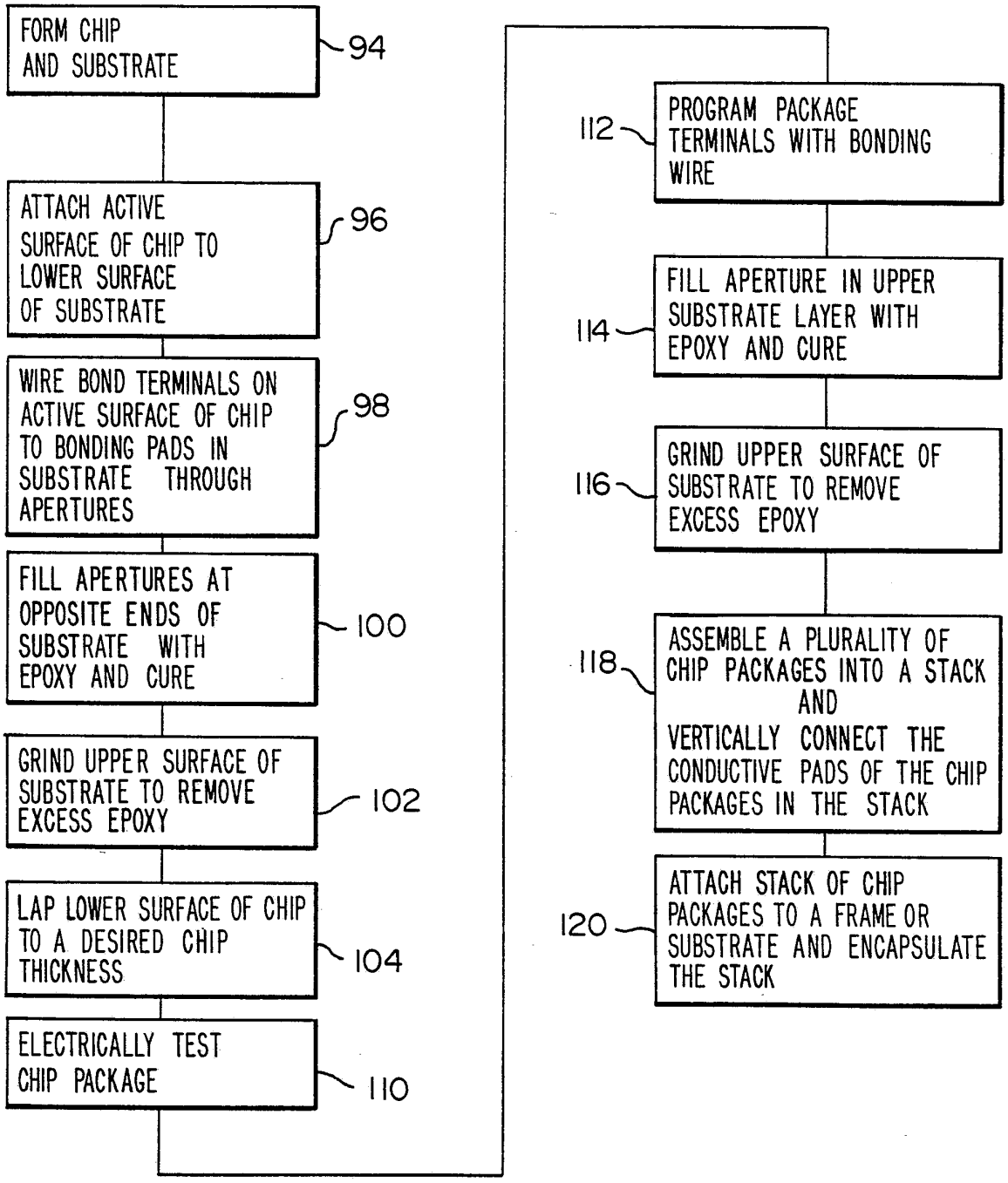
FORM CHIP AND SUBSTRATE
94
ATTACH ACTIVE SURFACE OF CHIP TO LOWER SURFACE OF SUBSTRATE
96
WIRE BOND TERMINALS ON ACTIVE SURFACE OF CHIP TO BONDING PADS IN SUBSTRATE THROUGH APERTURES
98
FILL APERTURES AT OPPOSITE ENDS OF SUBSTRATE WITH EPOXY AND CURE
100
GRIND UPPER SURFACE OF SUBSTRATE TO REMOVE EXCESS EPOXY
102
LAP LOWER SURFACE OF CHIP TO A DESIRED CHIP THICKNESS
104
ELECTRICALLY TEST CHIP PACKAGE
110
112
PROGRAM PACKAGE TERMINALS WITH BONDING WIRE
114
FILL APERTURE IN UPPER SUBSTRATE LAYER WITH EPOXY AND CURE
116
GRIND UPPER SURFACE OF SUBSTRATE TO REMOVE EXCESS EPOXY
118
ASSEMBLE A PLURALITY OF CHIP PACKAGES INTO A STACK AND VERTICALLY CONNECT THE CONDUCTIVE PADS OF THE CHIP PACKAGES IN THE STACK
120
ATTACH STACK OF CHIP PACKAGES TO A FRAME OR SUBSTRATE AND ENCAPSULATE THE STACK

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/02202

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 21/56, 21/58, 21/60, 21/66; H05K 3/36, 13/04

US CL :437/8,208,219,915,974;257/686,784

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/226, 8, 208, 219, 915, 974; 257/686, 784

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS:Temperature;VARIOUS; CYCLE# CYCLING; 437/8; BURN IN; 437/CLAS; TEST?; DYNAMIC; EXPAND CARSON, J/IN; IRVINE SENSORS/AS; GO,TIONG/IN; EXPAND GO/IN

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US,A, 5,155,068 (Tada) 13 October 1992 See column 3, lines 26-28.	3-5,8,9
X Y,P	US,A, 5,107,328 (Kinsman) 21 April 1992 See column 3, line 4 to column 4, line 15.	1,6,7,14-22,24,25 2-5,10,11, 12,23,26-28
X Y	US,A, 5,086,018 (Conru et al.) 04 February 1992 See column 2, line 46 to column 3, line 44.	1,6,7,14, 22,24,25 2,5,10,11, 12,23,26-28, 13

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 20 MAY 1993	Date of mailing of the international search report 23 JUN 1993
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer Diane Moffitt for DAVIS E. GRAYBILL Telephone No. (703) 308-2947

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/02202

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 5,041,395 (Steffen) 20 August 1991 see column 4, line 59 to column 5, line 27.	2-5,18,23,26
Y	US,A, 4,956,694 (Eide) 11 September 1990 See column 5, lines 20-42 and column 1, lines 4-32.	13,5,12,27, 28
Y	US,A, 4,379,259 (Varadi et al.) 05 April 1983 See column 8 line 14 to column 9, liine 8.	11
X Y	JP,A, 6,113,335 (Sakamaki) 25 June 1986 See English abstract.	1,6,7,14-22,24,25 2-5,10,11, 12,23,26-28