(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
05 October 2017 (05.10.2017)

WIPO | PCT

(10) International Publication Number
WO 2017/172341 A3

(51) International Patent Classification:
G06F 1/08 (2006.01)

(21) International Application Number:
PCT/US2017/022142

(22) International Filing Date:
13 March 2017 (13.03.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
15/087,171 31 March 2016 (31.03.2016) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(54) Title: ON-CHIP CLOCK CONTROLLER

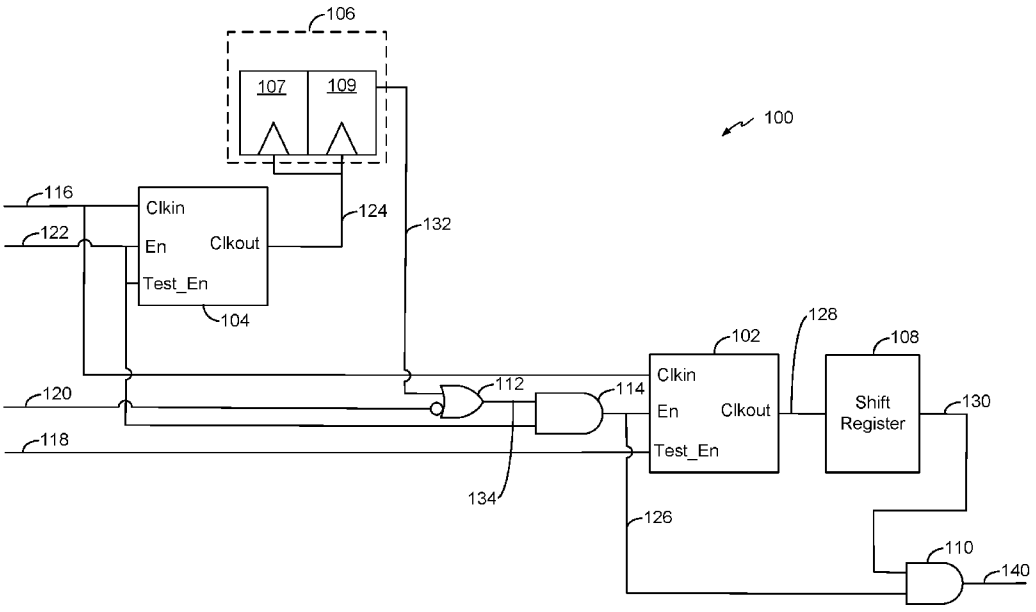

FIG. 1

(57) Abstract: An on-chip clock controller includes a primary clock gating cell and a secondary clock gating cell. The primary clock gating cell includes a first clock input terminal coupled to receive an input clock signal and a first enable input terminal coupled to receive an enable signal. The primary clock gating cell also include a first clock output terminal configured to generate a first output clock signal based at least in part on the input clock signal and the enable signal. The secondary clock gating includes a second clock input terminal coupled to receive the input clock signal and a second clock output terminal configured to generate a second output clock signal based at least in part on the input clock signal. The enable signal is based at least in part on the second output clock signal.

WO 2017/172341 A3

[Continued on next page]

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(88) Date of publication of the international search report:
15 March 2018 (15.03.2018)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/022142

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1, 2, 29

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/022142

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F1/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F H05K H03K G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010/033229 A1 (IRIE KAZUYUKI [JP]) 11 February 2010 (2010-02-11) columns 4-79; figures 1-7	1,2,29
X	US 2009/125769 A1 (NGUYEN THAI-MINH [US] ET AL) 14 May 2009 (2009-05-14) paragraphs [0024] - [0062]; figures 1-11	1,2,29
X	US 5 313 470 A (SIMPSON DAVID L [US]) 17 May 1994 (1994-05-17) column 2, line 57 - column 5, line 58; figures 1-1B	1,2,29

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 December 2017	15/02/2018

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2017/022142

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010033229 A1	11-02-2010	JP 2010045483 A	25-02-2010
		TW 201034379 A	16-09-2010
		US 2010033229 A1	11-02-2010
US 2009125769 A1	14-05-2009	NONE	
US 5313470 A	17-05-1994	NONE	

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1, 2, 29

An on-chip clock controller circuit comprising: a primary clock gating cell comprising: a first clock input terminal coupled to receive an input clock signal;a first enable input terminal coupled to receive an enable signal; and a first clock output terminal configured to generate a first output clock signal based at least in part on the input clock signal and the enable signal; and a secondary clock gating cell comprising: a second clock input terminal coupled to receive the input clock signal; and a second clock output terminal configured to generate a second output clock signal based at least in part on the input clock signal, wherein the enable signal is based at least in part on the second output clock signal, wherein the primary clock gating cell further comprises a first test enable input terminal coupled to receive a first test enable signal, wherein first output clock signal is generated based on the input clock signal, the enable signal, and the first test enable signal.

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2. claims: 3, 4

An on-chip clock controller circuit comprising: a primary clock gating cell comprising: a first clock input terminal coupled to receive an input clock signal;a first enable input terminal coupled to receive an enable signal; and a first clock output terminal configured to generate a first output clock signal based at least in part on the input clock signal and the enable signal; and a secondary clock gating cell comprising: a second clock input terminal coupled to receive the input clock signal; and a second clock output terminal configured to generate a second output clock signal based at least in part on the input clock signal, wherein the enable signal is based at least in part on the second output clock signal, further comprising a shift register coupled to receive the first output clock signal, the shift register configured to generate a data signal based at least in part on the first output clock signal.

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3. claims: 5-8

An on-chip clock controller circuit comprising: a primary clock gating cell comprising: a first clock input terminal coupled to receive an input clock signal;a first enable input terminal coupled to receive an enable signal; and a first clock output terminal configured to generate a first output clock signal based at least in part on the input clock signal and the enable signal; and a secondary clock

gating cell comprising: a second clock input terminal coupled to receive the input clock signal; and a second clock output terminal configured to generate a second output clock signal based at least in part on the input clock signal, wherein the enable signal is based at least in part on the second output clock signal, further comprising a synchronization circuit coupled to receive the second output clock signal from the second clock output terminal of the secondary clock gating cell, the synchronization circuit configured to generate a synchronization signal based at least in part on the second output clock signal.

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4. claims: 9, 11-28, 30

A method of reducing glitches at an on-chip clock controller circuit, the method comprising: generating a first output clock signal at a primary clock gating cell of the on-chip clock controller circuit, the first output clock signal generated based at least in part on an input clock signal and an enable signal; and generating a second output clock signal at a secondary clock gating cell of the on-chip clock controller circuit, the second output clock signal generated based at least in part on the input clock signal, wherein the enable signal is based at least in part on the second output clock signal,wherein the input clock signal bypasses multiplexer operations at the on-chip clock controller circuit to reduce glitches at the on-chip clock controller circuit.

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5. claim: 10

An on-chip clock controller circuit comprising: a primary clock gating cell comprising: a first clock input terminal coupled to receive an input clock signal;a first enable input terminal coupled to receive an enable signal; and a first clock output terminal configured to generate a first output clock signal based at least in part on the input clock signal and the enable signal; and a secondary clock gating cell comprising: a second clock input terminal coupled to receive the input clock signal; and a second clock output terminal configured to generate a second output clock signal based at least in part on the input clock signal, wherein the enable signal is based at least in part on the second output clock signal, wherein the primary clock gating cell comprises a first latch, and wherein the secondary clock gating cell comprises a second latch.
