(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
19 May 2023 (19.05.2023)

WIPO | PCT

(10) International Publication Number
WO 2023/086789 A1

(51) International Patent Classification:
H03F 1/26 (2006.01) *H03F 3/193* (2006.01)
H03F 1/22 (2006.01)

(21) International Application Number:
PCT/US2022/079467

(22) International Filing Date:
08 November 2022 (08.11.2022)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
17/523,584 10 November 2021 (10.11.2021) US

(71) Applicant: **PSEMI CORPORATION** [US/US]; 9369 Carroll Park Drive, San Diego, California 92121 (US).

(72) Inventors: **AYRANCI, Emre**; c/o pSemi Corporation, 9369 Carroll Park Drive, San Diego, California 92121 (US). **SANNER, Miles**; c/o pSemi Corporation, 9369 Carroll Park Drive, San Diego, California 92121 (US).

(74) Agent: **CASH, Brian J.** et al.; STEINFL + BRUNO LLP, 155 N. Lake Avenue, Suite 700, Pasadena, California 91030 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,

(54) Title: HYBRID INPUT LNA RF FRONTEND ARCHITECTURE

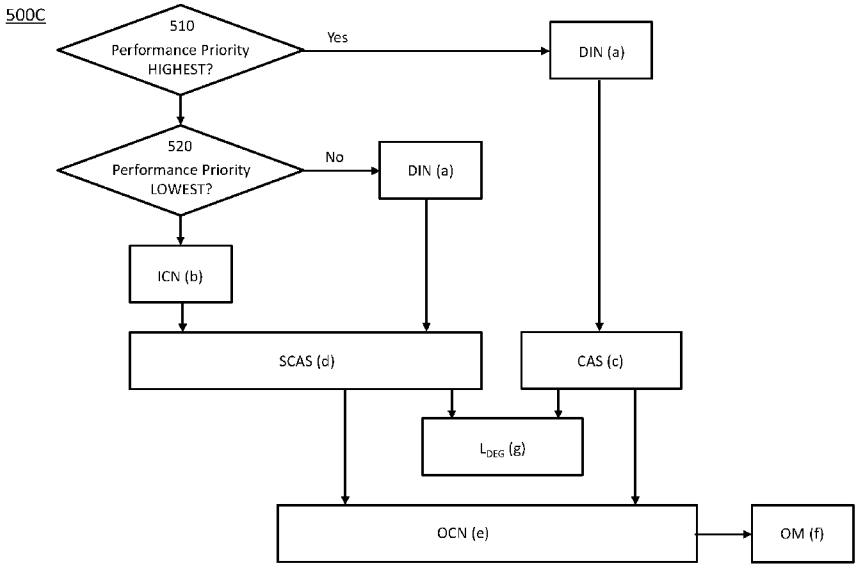


FIG. 5C

(57) Abstract: Methods and devices for realizing RF processing paths associated to different frequency bands are presented. According to one aspect, the RF processing paths are provided by a hybrid input LNA RF frontend that includes RF processing paths that are dedicated to specific frequency bands and RF processing paths that are shared between several frequency bands. Sharing of the RF processing paths is provided by an input combiner network and/or a multi-input cascode amplifier that includes a cascode transistor that is coupled to at least two input transistors. Further presented in a toolkit that includes circuit blocks that can be used in specific combinations to customize the RF processing paths to achieve specific performance or cost optimization. A decision tree based on performance and cost priorities assigned to each of the frequency bands is used to provide the specific combinations.

WO 2023/086789 A1

[Continued on next page]

TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

HYBRID INPUT LNA RF FRONTEND ARCHITECTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to U.S. Patent Application No. 17/523,584, filed on November 10, 2021, for a "Hybrid Input LNA RF Frontend Architecture," which is herein incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure is related to electronic radio frequency (RF) circuits, and more particularly to a hybrid input architecture of an RF frontend (RFFE) that considers different input performance priorities to optimize performance and cost of the RFFE.

BACKGROUND

[0003] Processing of an input RF signal through an RF system (e.g., RFFE) may be provided via a combination of switches, filters and matching circuits, coupled to an amplifier, which in combination may provide an RF processing path for amplification of the input RF signal. In a traditional RFFE architecture used in, for example, a handheld device, different input RF signals corresponding to different frequency bands may require different RF processing paths. When designing an RFFE module, circuit designers may be required to take into consideration cost versus performance tradeoff of the RFFE module while supporting the different frequency bands.

[0004] FIG. 1A shows a prior art RFFE (receive side) architecture (100A) that reduces cost by providing a combined amplification path, CAP, for processing of all of the supported frequency bands. Such frequency bands may include a plurality of (over-the-air) frequency bands (e.g., B_a, B_b, …, B_k) and one or more auxiliary frequency bands (e.g., AUX_1, AUX_2). An RF signal corresponding to each of the frequency bands (e.g., B_a, B_b, …, B_k) is received at the antenna, ANT, and is selectively routed through a respective filter (e.g., *a*, *b*, …, *k*) of a filter bank, FB, via an antenna switch, ASW. A switch, B_SEL, selectively couples one of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2 coupled to respective throws of the switch B_SEL) to the combined amplification path, CAP (e.g. coupled to the single pole of the switch B_SEL). For example, as shown in FIG. 1A, the switch, B_SEL, may couple an RF signal, RF_{SEL}, corresponding to the selected frequency band, B_a, to an input matching circuit,

IM, of the combined amplification path, CAP. In turn, an amplifier, AP, and an output matching circuit, OM, of the combined amplification path, CAP, may further process the RF signal, RF_{SEL}, for output of an amplified output RF signal, RF_{OUT}.

[0005] The prior art RFFE architecture (100A) of FIG. 1A reduces cost of a corresponding RFFE module by reducing a number of components required for processing of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2). In particular, use of the combined amplification path, CAP, allows processing of the supported frequency bands via a single input matching circuit, IM, and a single amplifier, AP. Such reduction in the number of components may allow for a reduction in die area, and therefore a (physical) size, of a corresponding RFFE module. On the other hand, an insertion loss (inherent) of the switch, B_SEL, may degrade a noise figure (NF) performance of the RFFE architecture (100A) with respect to all of the supported frequency bands. Furthermore, use of a same input match, IM, and amplifier, AP, may reduce flexibility in optimizing a performance (e.g., matching, gain, power, linearity, etc.) of the RFFE architecture (100A) with respect to a specific frequency band of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2). Such performance shortcoming may be addressed by the prior art RFFE architecture (100B) of FIG. 1B.

[0006] The prior art RFFE architecture (100B) of FIG. 1B increases performance of a corresponding RFFE module by providing a dedicated RF amplification path (e.g., DAP_a, DAP_b, …, DAP_k, DAP_1, DAP_2) for each of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2). Use of such dedicated amplification paths (e.g., DAP_a, DAP_b, …, DAP_k, DAP_1, DAP_2, coupled to a same output matching circuit, OM) may remove requirement for the switch, B_SEL, of the RFFE architecture (100A) of FIG. 1A, and therefore may improve a noise figure (NF) performance of the RFFE architecture (100B). Furthermore, a dedicated input matching circuit (e.g., IM_a, IM_b, …, IM_k, IM_1, IM_2 of a bank of input matching circuits, IMB) and a dedicated amplifier (e.g., AP_a, AP_b, …, AP_k, AP_1, AP_2 of a bank of amplifiers, APB) of the dedicated RF amplification paths (e.g., DAP_a, DAP_b, …, DAP_k, DAP_1, DAP_2) may allow increased flexibility in optimizing a performance (e.g., matching, gain, power, linearity, etc.) of the RFFE architecture (100B) with respect to a specific frequency band of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2).

[0007] The increased performance provided by the prior art RFFE architecture (100B) of FIG. 1B over the prior art RFFE architecture (100A) of FIG. 1A may be associated to an increased cost of components used in the dedicated RF amplification paths (e.g., DAP_a, DAP_b,

…, DAP_k, DAP_1, DAP_2) and an increase in die area, and therefore a (physical) size and cost, of a corresponding RFFE module.

[0008] Based on the above, it would be clear to a person skilled in the art, that the prior art architectures (100A, 100B) provide a binary choice between optimizing a performance or a cost of a corresponding RFFE module when considered globally. Teachings according to the present disclosure provide circuit designers and/or system integrators tools that allow flexibility in choice between optimizing a performance or a cost of each individual RF processing path of different frequency bands supported by an RFFE module. Accordingly, by deploying such tools based on specific performance priorities of corresponding input RF signals of the supported frequency bands, performance and cost of the RFFE module may be simultaneously optimized.

SUMMARY

[0009] According to a first aspect of the present disclosure, a multi-input multi-band low noise amplifier (LNA) is presented, comprising: a dedicated RF processing path for processing of an input RF signal of a first frequency band, the dedicated RF processing path comprising: a dedicated cascode amplifier comprising a dedicated input transistor and a dedicated output cascode transistor that is coupled to a high side node; and a shared RF processing path for processing of at least two input RF signals of respective second and third frequency bands, the shared RF processing path comprising: an input band selection switch; and a multi-input shared cascode amplifier comprising a plurality of input transistors and a shared output cascode transistor coupled to the plurality of input transistors, wherein: the shared output cascode transistor is coupled to the high side node, and the input band selection switch is configured to selectively couple each of the at least two input RF signals to a shared input transistor of the plurality of input transistors.

[0010] According to a second aspect of the present disclosure, a multi-input multi-band low noise amplifier (LNA) is presented, comprising: a dedicated first band RF processing path for processing of a first frequency band RF signal received from an antenna through a dedicated first band filter, the dedicated first band RF processing path comprising: a dedicated first band input matching circuit coupled to a dedicated first band cascode amplifier, the dedicated first band cascode amplifier comprising: a dedicated first band input transistor and a dedicated first band output cascode transistor that is coupled to a high side node; and a shared RF processing

path for processing of a second frequency band RF signal received from the antenna through a dedicated second band filter and of a first auxiliary frequency band RF signal that is not received from the antenna, the shared RF processing path comprising: an input band selection switch; a multi-input shared cascode amplifier comprising a plurality of input transistors and a shared output cascode transistor coupled to the plurality of input transistors; and a shared input matching circuit coupled between the input band selection switch and a shared input transistor of the plurality of input transistors, wherein: the shared output cascode transistor is coupled to the high side node, and the input band selection switch is configured to selectively couple one of the second frequency band RF signal or the first auxiliary frequency band RF signal to the shared input transistor.

[0011] According to a third aspect of the present disclosure, a method for optimizing performance and cost of a receive side of an RF front end (RFFE) is presented, the method comprising: assigning a performance priority to each band of a plurality of frequency bands for processing by the RFFE, the performance priority including a range from low to high; based on the assigning, establishing an RF processing performance for a respective RF processing path of the each band; based on the establishing, realizing the respective RF processing path based on circuit blocks provided by a toolkit; and based on the realizing, optimizing RF processing performance and cost of the RFFE.

[0012] Further aspects of the disclosure are provided in the description, drawings and claims of the present application.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more embodiments of the present disclosure and, together with the description of example embodiments, serve to explain the principles and implementations of the disclosure.

[0014] FIG. 1A shows a simplified schematic of a prior RFFE architecture that optimizes cost over performance.

[0015] FIG. 1B shows a simplified schematic of a prior RFFE architecture that optimizes performance over cost.

[0016] FIG. 2A shows a simplified schematic of an exemplary embodiment of a combined amplification path comprising a single-input cascode amplifier that may be used in the configuration of FIG. 1A.

[0017] FIG. 2B shows a simplified schematic of an exemplary embodiment of dedicated amplification paths comprising a plurality of dedicated single-input cascode amplifiers that may be used in the configuration of FIG. 1B.

[0018] FIG. 3A shows a simplified schematic of an exemplary multi-input cascode amplifier comprising a shared cascode configuration.

[0019] FIG. 3B shows a simplified schematic of an exemplary multi-input cascode amplifier comprising a shared cascode configuration with branch decoupling switches.

[0020] FIG. 3C shows a simplified schematic of another exemplary multi-input cascode amplifier comprising a shared cascode configuration with branch decoupling switches.

[0021] FIG. 4A shows a simplified schematic of an input combiner circuit according to an embodiment of the present disclosure.

[0022] FIG. 4B shows an exemplary embodiment of inductors used in input matching circuits.

[0023] FIG. 5A shows various circuit blocks according to the present disclosure that may be used for optimizing performance or cost of an RF processing path of a hybrid input RFFE architecture according to the present disclosure.

[0024] FIG. 5B shows various circuit blocks that may be common to the RF processing paths of hybrid input RFFE architecture according to the present disclosure.

[0025] FIG. 5C shows a decision tree that may be used to realize the hybrid input RFFE architecture according to the present disclosure.

[0026] FIG. 5D shows another decision tree that may be used to realize the hybrid input RFFE architecture according to the present disclosure.

[0027] FIG. 6A shows a block diagram of a hybrid input RFFE architecture according to the present disclosure realized via the decision tree of FIG. 5C.

[0028] FIG. 6B shows a simplified schematic of a hybrid input RFFE architecture according to the present disclosure.

[0029] FIG. 6C shows the simplified schematic of the hybrid input RFFE architecture of FIG. 6B with added details related to coupling to an antenna.

[0030] FIG. 7 shows various process steps of a method according to the present disclosure for optimizing performance and cost of a receive side of an RF front end (RFFE).

[0031] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0032] FIG. 2A shows a simplified schematic of an exemplary embodiment of a combined amplification path, CAP, comprising a single-input cascode amplifier, AP, that may be used in the configuration of FIG. 1A described above. The combined amplification path, CAP, receives a selected input RF signal, RF_{SEL}, and outputs an amplified RF signal, RF_{OUT}, to a load, R_L. The selected input RF signal, RF_{SEL}, is coupled to an input transistor, M1, of the single-input cascode amplifier, AP, through an input matching circuit, IM, which as shown in FIG. 2A, may include a series-connected inductor, L_{IN}. Input matching to the amplifier, AP, may be provided via a combination of the input matching circuit, L_{IN}, and a degeneration inductor, L_{DEG}, coupled to a source of the input transistor, M1. For operation across the plurality of supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2 of FIG. 1A), the degeneration inductor, L_{DEG}, may be adjustable (e.g., tunable, configurable, programmable, etc.), for example, via inductance selection switches as shown in FIG. 2A.

[0033] With continued reference to FIG. 2A, the amplifier, AP, may include one or more cascode transistors (e.g., M2) in series connection with the input transistor, M1. A person skilled in the art is well aware of a principle of operation of the cascode configuration, CAS, comprising a common-source input transistor (e.g., M1) coupled to one or more common-gate (cascode) transistors (e.g., M2). Biasing of the cascode configuration, CAS, may be provided via a supply voltage, V_{DD}, and a reference ground, Gnd, coupled between a high side node, CAS_{OUT} (e.g., drain of output cascode transistor M2) and a low side node, CAS_{LS} (e.g., source of the input transistor M1) of the cascode configuration, CAS. As shown in FIG. 2A, the high side node, CAS_{OUT}, may be coupled to the supply voltage, V_{DD}, through an output network,

OCN, and the low side node, CAS_{LS}, may be coupled to the reference ground, Gnd, through the degeneration inductor, L_{DEG}. Furthermore, gate voltages (e.g., V_{G1}, V_{G2}, etc.) to gates of the transistors (e.g., M1, M2, etc.) may control a DC current (e.g., amplifier gain) through the cascode configuration, CAS, as well as operating conditions (i.e., biasing points) of each of the transistors (e.g., M1, M2, etc.).

[0034] The output network, OCN, of FIG. 2A may include at least one inductor, L_{OCN}, in series connection with the cascode configuration, CAS. Similar to the inductor, L_{DEG}, in some embodiments, the inductor, L_{OCN}, may be adjustable (e.g., via switches shown in FIG. 2A). In some embodiments, the output network, OCN, may include an adjustable capacitor (e.g., C_{OCN}) and/or an adjustable resistor (e.g., R_{OCN}) in parallel with the inductor, L_{OCN}. Elements (e.g., L_{OCN}, C_{OCN}, LR_{OCN}) of the output network, OCN, combined with the output matching circuit, OM, may be used to provide gain and/or output matching that is specific to a frequency band of the plurality of supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2 of FIG. 1A).

[0035] As shown in FIG. 2A, the output matching circuit, OM, coupled to the high side node, CAS_{OUT}, may include at least one series-connected capacitor, C_{OUT} (that may also be used as a DC decoupling capacitor). In some embodiments, the capacitor, C_{OUT}, may be an adjustable capacitor for providing output matching that is specific to a frequency band of the plurality of supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2 of FIG. 1A).

[0036] As described above with reference to FIG. 1A, the combined amplification path, CAP, of FIG. 2A may not provide (complete) flexibility in optimizing performance with respect to a specific frequency band of the plurality of supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2 of FIG. 1A). For example, no flexibility may be provided with respect to elements (e.g., L_{IN}) of the input matching circuit, IM, or with respect to elements (e.g., M1, M2) of the cascode configuration, CAS. A person skilled in the art would know that, for example, value and/or type (in-circuit vs. out-of-circuit/SMD) of the inductor, L_{IN}, and/or characteristics (e.g., size, width) of the transistors (M1, M2) may affect performance of the cascode configuration, CAS, differently for the different supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2 of FIG. 1A).

[0037] FIG. 2B shows a simplified schematic of an exemplary embodiment of dedicated amplification paths (e.g., IM_b, CAS_b, OCN, L_{DEG} associated to frequency band B_b) comprising a plurality of dedicated single-input cascode amplifiers (e.g., CAS_b, OCN, L_{DEG} associated to

frequency band B_b) that may be used in the configuration of FIG. 1B described above. A person skilled in the art would clearly realize that the configuration (200B) of FIG. 2B is based on the configuration described above with reference to FIG. 2A by providing dedicated input matching circuits (e.g., IM_a, IM_b, …, IM_k, IM_1, IM_2) coupled to respective dedicated cascode configurations (e.g., CAS_a, CAS_b, …, CAS_k, CAS_1, CAS_2) that are coupled (e.g., via nodes CAS_{OUT} and CAS_{LS}) to common elements (e.g., OCN, L_{DEG}) to provide respective dedicated amplification paths for each of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2).

[0038] With continued reference to FIG. 2B, considering the dedicated amplification path (IM_b, CAS_b, OCN, L_{DEG}) associated to the frequency band, B_b, the input matching circuit, IM*b*, comprising for example a series-connected inductor, L_{INb}, receives an input RF signal at the frequency band, B_b, and converts it to an RF signal, RF_b, that is fed to the input transistor, $M1_b$, of the cascode configuration, CAS_b. In turn, the cascode configuration CAS_b, comprising transistors ($M1_b$, $M2_b$) coupled between the supply voltage, V_{DD}, and the reference ground, Gnd, via high side and low side nodes, CAS_{OUT} and CAS_{LS}, amplifies the RF signal, RF_b, for output as RF_{OUT} through the output matching circuit, OM, that is coupled to the load, R_L. While amplifying/processing the frequency band, B_b, other cascode configurations (e.g., CAS_n, $n \neq b$) associated to other frequency bands (e.g., B_n, $n \neq b$) may be deactivated via, for example, a gate biasing voltage to one or more of the transistors (e.g., $M1_n$ and/or $M2_n$ $n \neq b$).

[0039] As shown in FIG. 2B, the dedicated amplification paths include respective dedicated cascode configurations (e.g., CAS_a, CAS_b, …, CAS_k, CAS_1, CAS_2) that are coupled in parallel between the high side node, CAS_{OUT}, and the low side node, CAS_{LS}, and configured to receive dedicated RF signals (e.g., RF_a, RF_b, …, RF_k , RF_1, RF_2) through dedicated input matching circuits (e.g., IM_a, IM_b, …, IM_k , IM_1, IM_2), and output amplified versions thereof through common elements (e.g., OCN, OM) coupled to the high side node, CAS_{OUT}. Accordingly, the configuration shown in FIG. 2B overcomes shortcomings of the configuration of FIG. 2A described above by allowing flexibility in choice of elements of the input matching circuits (e.g., IM_a, IM_b, …, IM_k , IM_1, IM_2) and/or of elements/transistors of the cascode configurations (e.g., CAS_a, CAS_b, …, CAS_k, CAS_1, CAS_2), at the expense of added cost (e.g., cost of added elements and larger die area).

[0040] As described above, while amplifying/processing the frequency band, B_b, other cascode configurations (e.g., CAS_n, $n \neq b$) associated to other frequency bands (e.g., B_n, $n \neq b$)

may be deactivated via, for example, a gate biasing voltage to one or more of the transistors (e.g., $M1_n$ and/or $M2_n$ $n \neq b$). For example, by applying respective gate voltages to the (output) cascode transistors ($M2_n$ $n \neq b$) such transistors can be turned OFF, and therefore the corresponding cascode configurations (e.g., CAS_n, $n \neq b$) can be deactivated (e.g., no conduction through the cascode configurations). However, while turned OFF, the cascode transistors ($M2_n$ $n \neq b$) may present a capacitive load to the high side node, CAS_{OUT}, which in turn may affect performance (e.g., linearity) of the frequency band, B_b, being processed. In other words, the dedicated amplification paths provided by the configuration of FIG. 2B may introduce some undesired effects that can degrade an optimal performance of a specific frequency band.

[0041] Teachings according to the present disclosure allow to consider performance priorities of the supported frequency bands and tailor/design/customize respective RF processing paths to achieve desired/specific performances. Performance priority of a frequency band may be in view of, for example, a minimum required sensitivity provided by the corresponding RF processing path which may be achieved by controlling/selecting elements of the RF processing path that may impact sensitivity. Such elements may include elements of the RF processing path that may impact/degrade noise figure (i.e., signal-to-noise figure) such as, for example, insertion loss introduced by switches, or a Q-factor of an inductor used, for example, in an input matching circuit. In other words, by considering a performance priority of a frequency band, a specific performance to be provided by a corresponding RF processing path may not necessarily require a dedicated RF processing path shown in the configuration of FIG. 2B, rather, a combined RF processing path according to the configuration of FIG. 2A may be sufficient. Teaching according to the present disclosure provide the tools (e.g., FIGs. 5A-5C later described) that can be used to customize the respective RF processing paths to achieve the desired/specific performances.

[0042] Other elements that may impact a performance of an RF processing path may include elements of other RF processing paths. For example, considering the configuration of FIG. 2B, as described above, output cascode transistors ($M2_n$ $n \neq b$) of deactivated cascode configurations (e.g., CAS_n, $n \neq b$) coupled to the high side node, CAS_{OUT}, can affect/degrade performance of the activated cascode configuration (e.g., CAS_b). FIG. 3A shows a multi-input cascode amplifier (300A) comprising a branched/shared cascode configuration (e.g., SCAS)

that may be used to reduce a number of output cascode transistors coupled to the high side node, CAS_{OUT}, while supporting a same number of frequency bands (e.g., input RF signals).

[0043] As shown in FIG. 3A, the shared cascode configuration, SCAS, may be provided by coupling (e.g., connecting) a source of a (shared) cascode transistor (e.g., $M2_2$) to drains of at least two input transistors (e.g., $M1_k$, ..., $M1_2$). In other words, the transistors of the shared cascode configuration, SCAS, form a tree structure that connects a shared cascode transistor (e.g., $M2_2$) to at least two transistors located at a level below a level of the shared cascode transistor. In this context, levels of the transistors being defined by their positions within a stack of transistors (e.g., $M1_k$, ..., $M1_2$, $M2_2$) that forms the shared cascode configuration, SCAS, with a first level (e.g., input level) corresponding to the input transistors (e.g., $M1_k$, ..., $M1_2$) having respective sources coupled to the low side node, CAS_{LS}, and the last level (e.g., output level) corresponding to the output transistor (e.g., $M2_2$) having a drain coupled to the high side node, CAS_{OUT}. It should be noted that although the shared cascode configuration, SCAS, of FIG. 3A includes two levels, teachings according to the present disclosure may equally apply to configurations that include more than two levels, such as three levels or more (e.g., input level, intermediate cascode levels, and output level), wherein a corresponding tree structure may be provided by one or more shared cascode transistors located at different levels.

[0044] With continued reference to FIG. 3A, by using the shared cascode configuration, SCAS, for processing of, for example, frequency bands (e.g., B_k, ..., AUX_2) having lower performance priorities, increased performance may be provided to the dedicated RF processing paths (e.g., using dedicated cascode configurations CAS_a, CAS_b, ..., etc.) having, for example, higher performance priorities. In other words, the shared cascode configuration, SCAS, and the dedicated cascode configuration (e.g., CAS_a, CAS_b, ..., etc.) shown in FIG. 3A may be considered as elements that are part of a toolkit according to the present disclosure that can be used to customize the RF processing paths of the supported frequency bands (e.g., B_a, B_b, ..., B_k, ..., AUX_2) to achieve the desired/specific performances.

[0045] FIG. 3B shows a simplified schematic of a multi-input cascode amplifier (300B) comprising a shared cascode configuration, SCAS, as described above with reference to FIG. 3A. The configuration of FIG. 3B further includes series switches (e.g., SW_{2a}, SW_{2b}, SW_{22}) that may be coupled between (output nodes of) each of the cascode configurations (CAS_a, CAS_b, SCAS) and the high side node, CAS_{OUT}, and/or series switches (e.g., SW_{1k}, ..., SW_{12}) that may be coupled between the shared cascode transistor (e.g., $M2_2$) and the lower level

(input) transistors (e.g., $M1_k$, …, $M1_2$). Such switches may be used for selective activating/deactivating of corresponding RF processing paths instead (or in addition) of use of gate voltages as described above. Use of such switches may be advantageous since, in contrast to transistors (e.g., $M1_k$, …, $M1_2$, $M1_2$) used as active elements of an amplifier, characteristics of the transistors used to form such switches may be optimized for operation as a switch with no regards to operation as an amplifier. As known to a person skilled in the art, such switches may be designed to provide a low ON resistance to reduce attenuation of a conducted RF signal when the RF processing path containing a switch is activated, and a low OFF capacitance to reduce capacitive loading on other processing paths when the RF processing path containing the switch is deactivated. It should be noted that although FIG. 3B shows each of the available RF processing paths including at least one switch, according to some embodiments of the present disclosure one or more of the RF processing paths may not include any switch. This is shown in the exemplary configuration (300C) of FIG. 3C, wherein the RF processing path for the frequency band, B_a, does not include a switch coupled between a respective cascode configuration, CAS_a, and the high side node, CAS_{OUT}. Or in other words, the cascode configuration, CAS_a, (i.e., output cascode transistor $M2_a$) is unconditionally coupled to the high side node, CAS_{OUT}, whereas, for example, the cascode configuration, CAS_b, (i.e., output cascode transistor $M2_b$) and the shared cascode configuration, SCAS, (i.e., output cascode transistor $M2_2$) are selectively coupled to the high side node, CAS_{OUT}, via respective switches SW_{2b} and SW_{22}. The configuration (300C) of FIG. 3C may allow increased performance for processing of the frequency band, B_a, when compared to the performance provided for processing of the frequency band, B_b.

[0046] FIG. 4A shows a simplified schematic of an input combiner circuit, ICN, according to an embodiment of the present disclosure that may be used to combine processing paths of at least two frequency bands to a common/shared processing path. For example, as shown in FIG. 4A, a band selection switch, B_SEL, may combine processing paths for the frequency bands B_k and AUX_1 to a common processing path that includes one input match circuit (e.g., IM_k). In the configuration (400A) shown in FIG. 4A, a performance priority of the bands B_k and AUX_1 may be lower than respective performance priorities of the bands B_a, B_b, and AUX_2. Such lower performance priority may allow the bands B_k and AUX_1 to be subjected, for example, to a higher insertion loss provided by the switch, B_SEL, and by a Q-factor of the input match circuit, IM_k (which cannot be optimized across both frequency bands). On the other hand, the lack of a switch and provision of dedicated input matching circuits (e.g., IM_a, IM_b, IM_2), may

allow higher performance RF processing paths for the respective frequency bands (e.g., B_a, B_b, AUX_2) having higher performance priorities.

[0047] The configuration (400) of FIG. 4A shows processing of the supported frequency bands (e.g., B_a, B_b, …, B_k, AUX_1, AUX_2) for provision of the RF signals (RF_a, RF_b, …, RF_k, RF_2) that may be input to the cascode configurations (e.g., CAS_a, CAS_b, …, SCAS) of any one of the configurations shown in FIG. 3A, FIG. 3B or FIG. 3C. In particular, RF signals (e.g., RF_a, RF_b) of the higher performance priority frequency bands (e.g., B_a, B_b) may be processed through dedicated cascode configurations (e.g., CAS_a, CAS_b), the (combined) RF signal (e.g., RF_k) of the lower performance priority frequency bands (e.g., B_k, AUX_1) may be processed through one branch (e.g., $M1_k$, $M2_2$) of the shared cascode configuration, SCAS, and the RF signal (e.g., RF_2) of the higher performance priority frequency band (e.g., AUX_2) may be processed through another branch (e.g., $M1_2$, $M2_2$) of the shared cascode configuration, SCAS.

[0048] With continued reference to FIG. 4A in view of FIGs. 3A-3C, routing of the higher performance priority frequency bands (e.g., B_a, B_b) through the respective dedicated cascode configurations (e.g., CAS_a, CAS_b) and of the higher performance priority frequency band (e.g., AUX_2) through the shared cascode configuration, SCAS, further differentiates the higher performance priorities based on a highest performance priority wherein no sharing of a cascode configuration is provided, and a relatively lower performance priority wherein sharing of the cascode configuration is provided. In other words, teachings according to present disclosure is based on a multitier approach that assigns different tiers to different (groups of) frequency bands, each tier being assigned to a different set/combination of elements/circuits from a toolkit to tailor/design/customize an RF processing path with a desired/specific performance. A first tier (e.g., tier one, highest performance priority) may be assigned to the frequency bands (e.g., B_a, B_b) which may not share the input matching circuit and the cascode configuration; a second tier (e.g., tier two, medium or lower performance priority) may be assigned to the frequency bands (e.g., AUX_2) which may not share the input matching circuit but may share the cascode configuration; and a third tier (e.g., tier three, lowest performance priority) may be assigned to the frequency bands (e.g., B_k, AUX_1) which may share the input matching circuit and the cascode configuration.

[0049] FIG. 4B shows an exemplary embodiment of inductors (e.g., L_{INa}, L_{INb}, L_{INk}, L_{IN2}) used in respective input matching circuits (e.g., IM_a, IM_b, IM_k, IM_2). A person skilled in the art would know that in some (traditional) RF frequency range of operation, optimal value of

respective Q-factors of the inductors (e.g., L_{INa}, L_{INb}, L_{INk}, L_{IN2}), and therefore optimal noise figure performance provided by such inductors when used in matching circuits, may be provided via fixed value SMD (surface mount device) inductors. In other words, via out-of-circuit inductors that may be coupled/fixated/soldered to the respective RF processing paths via bumps (e.g., B1 and B2 shown in FIG. 4B) formed on the RFFE module. As known to a person skilled in the art, provision of such bumps (e.g., B1, B2) may require considerable die area which can therefore affect size and cost of the RFFE module.

[0050] The multitier approach according to the present disclosure may allow to reduce cost/size of tier three frequency bands by reducing a number of inductors of the input matching circuits of the corresponding RF processing paths via the input combiner circuit, ICN, shown in FIG. 4B. On the other hand, the multitier approach according to the present disclosure may allow to increase performance of tiers one and two frequency bands via dedicated inductors (e.g., L_{INa}, L_{INb}, L_{IN2}) of dedicated input matching circuits (e.g., IM_a, IM_b, IM_2) shown in FIG. 4B. It should be noted that teachings according to the present disclosure are not limited to SMD inductors, and therefore for (higher) frequency ranges of operation where performance of such SMD inductors degrade, in-circuit inductors (e.g., per FIG. 4A) that do not require bumps may be used. As known by a person skilled in the art, such in-circuit inductors may be formed via appropriate routing geometries of traces/conductors in a circuit

[0051] FIG. 5A shows various circuit blocks (e.g., a, b, c, d, s) according to the present disclosure that may be used for optimizing performance or cost of an RF processing path of a hybrid input RFFE architecture according to the present disclosure. Such circuit blocks (e.g., circuits with specific functionalities) are based on the above description with reference to FIGs. 3-4, and include: a dedicated input matching circuit, DIN, represented by the circuit block (a); an input combiner circuit, ICN, represented by the circuit block (b); a dedicated cascode amplifier/configuration represented by the circuit block (c); and a shared cascode amplifier/configuration represented by the circuit block (d). The circuit blocks (a, b, c, d, s) may be considered part of the toolkit according to the present teachings that may be used to tailor/design/customize an RF processing path with a desired/specific performance according to the multitier approach described above. In particular, each RF processing path may include a combination of one of (a) or (b), with one of (c) or (d). Furthermore, each RF processing path may be further combined with the circuit block (s). In turn, such combination may be coupled

to the common circuit blocks (e, f, g) (or instead to e', g) shown in FIG. 5B to complete the RF processing path.

[0052] FIG. 5B shows various circuit blocks (e.g., e, f, g, e') that may be common to the RF processing paths of hybrid input RFFE architecture according to the present disclosure. Such circuit blocks are based on the above description with reference to FIGs. 3-4, and include: an output combining network, OCN, represented by the circuit block (e); an output matching circuit, OM, represented by the circuit block (f); and a degeneration inductor, L_{DEG}, represented by the circuit block (g). As shown in FIG. 5B, the blocks (e) and (f) may be combined to form an output combining and matching network, OCMN, that is represented by the circuit block (e').

[0053] The RF processing paths of the hybrid input RFFE architecture according to the present disclosure may be realized by combining one of the circuit block pairs (a, c), (a, d) or (b, d) of FIG. 5A with the common circuit blocks (e, f, g) of FIG. 5B, wherein a selection of the circuit block pairs for realizing a given RF processing path may be based on the multitier approach according to the present disclosure described above, and summarized in the decision tree (500C) shown in FIG. 5C. As shown in FIG. 5C, realization of each of the RF processing paths may be based on at least two decisions represented by decision blocks (510) and (520). Decision block (510) establishes whether or not the RF processing path is of (e.g., associated to) a highest performance priority (e.g., tier one), and decision block (520) establishes whether or not the RF processing path is of (e.g., associated to) the lowest performance priority (e.g., tier three). It should be noted that such decisions may be equivalent to requirement or not for a dedicated cascode configuration (e.g., decision block 510), and requirement or not for a dedicated input matching circuit (e.g., decision block 520).

[0054] With continued reference to FIG. 5C, according to one exemplary embodiment of the present disclosure, if the top decision block (510) establishes that the RF processing path is of the highest performance priority (e.g., tier one), then the RF processing path may be assigned (e.g., realized via) circuit blocks (a, c) coupled to the common circuit blocks (e, f, g). If the combination of the decision blocks (510) and (520) establish that the RF processing path is of the medium performance priority (e.g., not of the lowest or highest performance priority, tier two), then the RF processing path may be assigned (e.g., realized via) circuit blocks (a, d) coupled to the common circuit blocks (e, f, g). On the other hand, if the combination of the decision blocks (510) and (520) establish that the RF processing path is of the lowest

performance priority (e.g., tier three), then the RF processing path may be assigned (e.g., realized via) circuit blocks (b, d) coupled to the common circuit blocks (e, f, g).

[0055] In an alternative embodiment according to the present disclosure and as shown in the decision tree (500D) of FIG. 5D, if the top decision block (510) establishes that the RF processing path is of a higher performance priority (e.g., tier one as described above, or a tier 1.5 that is higher than the tier 2 but lower than the tier 1), then the RF processing path may be assigned (e.g., realized via) circuit blocks (a, c) coupled to the common circuit blocks (e, f, g). Furthermore, distinction between the tier 1 (highest priority) or tier 1.5 (higher priority without being the highest priority) may be made via the decision block (530). Based on the outcome of the decision block (530), for the highest priority RF processing path, the circuit blocks (a, c) may be coupled to the common circuit block (e) directly and therefore without use of a series switch provided by the circuit block (s). On the other hand, for the higher (but not highest) priority RF processing path, the circuit blocks (a, c) may be coupled to the common circuit block (e) through the series switch provided by the circuit block (s). As described above (e.g., with reference to FIG. 3C), coupling of RF processing paths other than a highest priority RF processing path to the common circuit block (e) through the series switch provided by the circuit block (s) can allow reducing off (path) capacitances presented to the highest priority RF processing path at the high side node CAS_{OUT}. Accordingly, as shown in the decision tree (500D) of FIG. 5D, all of the RF processing paths that are not of the highest priority are coupled to the common circuit block (e) through a series switch provided by the circuit block (s).

[0056] FIG. 6A shows a block diagram of a hybrid input RFFE architecture (600A) according to the present disclosure realized via the decision tree of FIG. 5C. Accordingly, RF processing paths corresponding to the highest performance priority (e.g., tier one) frequency bands (B_1, …, B_{k-1}) are realized via respective dedicated circuit blocks (a) (e.g., DIN_1, …, DIN_{k-1}), coupled to respective dedicated circuit blocks (c) (e.g., CAS_1, …, CAS_{k-1}), coupled to common circuit blocks (e, f, g) (e.g., OCN, OM, L_{DEG}), or to common circuit blocks (e', g) (e.g., OCMN, L_{DEG}). The RF processing path corresponding to the medium performance priority (e.g., tier two) frequency band, B_k, is realized via a dedicated circuit block (a) (e.g., DIN_k), coupled to an input transistor (e.g., M_{IN1}) of a shared circuit block (d) (e.g., SCAS), and coupled via a shared output cascode transistor (e.g., M_{OUT}) of the shared circuit block (d) to the common circuit blocks (e', g). Finally, the RF processing paths corresponding to the lowest performance priority (e.g., tier three) frequency bands, (B_{k+1}, …, B_n) are realized via two shared

circuit blocks (b) (e.g., ICN_1, ICN_2), coupled to respective input transistors (e.g., M_{IN2}, M_{IN3}) of the shared circuit block (d) (e.g., SCAS), and coupled via the shared output cascode transistor (e.g., M_{OUT}) of the shared circuit block (d) to the common circuit blocks (e', g). It should be noted that the block diagram of FIG. 6A shows an exemplary architecture which may be expanded to support any number of frequency bands, including zero, within any of the tiers.

[0057] FIG. 6B shows a simplified schematic of a hybrid input RFFE architecture (600B) according to the present disclosure. In particular, the architecture (600B) is based on application of the decision tree of FIG. 5C on the frequency bands (e.g., B_a, B_b, ..., B_k, AUX_1, AUX_2) supported by the prior art RFFE architectures shown in FIG. 1A and 1B. Accordingly, the tier one frequency bands (B_a, B_b) are processed via respective dedicated RF processing paths provided by dedicated input matching circuits (IM_a, IM_b) (respectively comprising inductors L_{INa} and L_{INb}) that are respectively coupled to dedicated cascode amplifier configurations (CAS_a, CAS_b); the tier two frequency band, AUX_2, is processed via a dedicated input matching circuit (e.g., IM_2 comprising inductor L_{IN2}) coupled to a dedicated input (e.g., input transistor $M1_2$) of a shared cascode configuration, SCAS; and the tier three frequency bands (B_c, AUX_1) are processed via a selection switch, B_SEL, coupled to a shared input matching circuit (e.g., IM_k comprising inductor L_{INk}) of an input combiner network, ICN, coupled to a dedicated input (e.g., input transistor $M1_k$) of the shared cascode configuration, SCAS. Furthermore, each of the RF processing paths is coupled to the output combiner network, OCN, and to the output matching circuit, OM, via the high side node, CAS_{OUT}, and to the degeneration inductor, L_{DEG}, via the low side node, CAS_{LS}.

[0058] With continued reference to FIG. 6B, amplification of the RF signals (e.g., RF_a, RF_b, ..., RF_k, RF_2) associated to the supported frequency bands (e.g., B_a, B_b, ..., B_k, AUX_1, AUX_2) may be provided via a multi-input single-output cascode low noise amplifier (e.g., CAS_a, CAS_b, SCAS, operating as an LNA) comprising a combination of stacked transistors (e.g., $M1_a$, $M1_b$, $M1_k$, $M1_2$, $M2_a$, $M2_b$, $M2_2$) that include input transistors (e.g., $M1_a$, $M1_b$, $M1_k$, $M1_2$) coupled to corresponding output cascode transistors (e.g., $M2_a$, $M2_b$, $M2_2$). As can be seen in FIG. 6C, RF signals (e.g., RF_a, RF_b) corresponding to tier one frequency bands (e.g., B_a, B_b) are amplified via input transistors (e.g., $M1_a$, $M1_b$) coupled to respective output cascode transistors (e.g., $M2_a$, $M2_b$) of the multi-input single-output amplifier (CAS_a, CAS_b, SCAS). On the other hand, RF signals (e.g., RF_k, RF_2) corresponding to tier two or three frequency bands (e.g., B_c, AUX_1, AUX_2) are amplified via input transistors (e.g., $M1_k$, $M1_2$) coupled to a

single output cascode transistor (e.g., $M2_2$) of the multi-input single-output amplifier (CAS_a, CAS_b, SCAS). In other words, amplification of the tier one frequency bands (e.g., B_a, B_b) is provided via dedicated output cascode transistors (e.g., $M2_a$, $M2_b$), whereas amplification of the tier two or three frequency bands (e.g., B_c, AUX_1, AUX_2) is provided via a shared output cascode transistor (e.g., $M2_2$).

[0059] FIG. 6C shows the simplified schematic of the hybrid input RFFE architecture of FIG. 6B with added details related to coupling to an antenna, ANT, via an antenna switch, ASW, as described above with reference to FIG. 1A. An RF signal corresponding to each of the frequency bands (e.g., B_a, B_b, B_c) is received at the antenna, ANT, and is selectively routed through a respective filter (e.g., *a*, *b*, *c*) of a filter bank, FB, via the antenna switch, ASW. As understood by a person skilled in the art, the filters (e.g., *a*, *b*, *c*) may be of a variety of different types known in the art with performance characteristics, including insertion loss, that may be based on the type and/or a (bandpass) frequency range of a filter. In other words, the filters (*a*, *b*, *c*) associated to the frequency bands (B_a, B_b, B_c) may have different RF performances which may impact sensitivity provided by the corresponding RF processing paths at different degrees. Accordingly, information about quality of the filters (e.g., *a*, *b*, *c*) used for processing of the frequency bands (e.g., B_a, B_b, B_c) may be used to assign a performance priority to the frequency bands. In the exemplary configuration (600C) shown in FIG. 6C, over-the-air frequency bands (B_a, B_b) may be processed by filters (*a*, *b*) that may have a lower insertion noise performance (e.g., higher insertion loss) compared to the filter *c* used for processing the over-the-air band, B_c. Accordingly, since the filters (*a*, *b*) may consume a larger portion of an available sensitivity budget of corresponding RF processing paths compared to the filter *c*, a higher performance priority (e.g., tier one) may be assigned to the frequency bands (B_a, B_b), and a lower performance priority (e.g., tier three) may be assigned to the frequency band, B_c. Accordingly, teachings according to the present disclosure may include equalization of sensitivity across the supported frequency bands at a lower possible cost (e.g., via usage of shared input matchings circuits and/or shared cascode configurations when possible).

[0060] With continued reference to FIG. 6C, auxiliary frequency bands (AUX_1, AUX_2) may include different frequency ranges of operation. These may include, for example, a narrow frequency range (e.g., single-band) similar to one of the over-the-air frequency bands (B_a, B_b, B_c), or a broader/wider frequency range (e.g., multi-band) which accordingly may require special care in a corresponding input matching circuit. Furthermore, such auxiliary frequency

bands may be pre-conditioned and therefore may not be processed by filters as shown in FIG. 6C. Because AUX_1 and AUX_2 are not processed by a filter, they may not be subjected to a corresponding filter insertion loss, and therefore such signals may be assigned a lower performance priority (e.g., tier two or three). Assuming that AUX_1 includes a narrow frequency range of operation and AUX_2 a broader frequency range of operation, then as shown in FIG. 6C, AUX_1 may be processed via the shared input matching circuit, IM_k, of the input combiner network, ICN, whereas AUX_2 may be processed via a dedicated input matching circuit, IM_2 (that may include, for example, an adjustable inductor, L_{IN2}). In other words, a medium performance priority (e.g., tier two) may be assigned to AUX_2, and a lowest performance priority (e.g., tier three) may be assigned to AUX_1. Accordingly, (a priori) assignment of the performance priority to a specific frequency band may not be solely based on band-specific elements (e.g., filters *a*, *b*, *c*), but may also be based on information about spectral content of the frequency band, and/or any other band specific parameter that may impact processing of a corresponding RF signal.

[0061] FIG. 7 is a process chart (700) showing various steps of a method according to the present disclosure for optimizing performance and cost of a receive side of an RF front end (RFFE). As can be seen in the process chart (700, such steps include: assigning a performance priority to each band of a plurality of frequency bands for processing by the RFFE, the performance priority including a range from low to high, per step (710); based on the assigning, establishing an RF processing performance for a respective RF processing path of the each band, per step (720); based on the establishing, realizing the respective RF processing path based on circuit blocks provided by a toolkit, per step (730); and based on the realizing, optimizing RF processing performance and cost of the RFFE, per step (740).

[0062] The term "MOSFET", as used in this disclosure, includes any field effect transistor (FET) having an insulated gate whose voltage determines the conductivity of the transistor, and encompasses insulated gates having a metal or metal-like, insulator, and/or semiconductor structure. The terms "metal" or "metal-like" include at least one electrically conductive material (such as aluminum, copper, or other metal, or highly doped polysilicon, graphene, or other electrical conductor), "insulator" includes at least one insulating material (such as silicon oxide or other dielectric material), and "semiconductor" includes at least one semiconductor material.

[0063] As used in this disclosure, the term "radio frequency" (RF) refers to a rate of oscillation in the range of about 3 kHz to about 300 GHz. This term also includes the frequencies used in wireless communication systems. An RF frequency may be the frequency of an electromagnetic wave or of an alternating voltage or current in a circuit.

[0064] Various embodiments of the invention can be implemented to meet a wide variety of specifications. Unless otherwise noted above, selection of suitable component values is a matter of design choice. Various embodiments of the invention may be implemented in any suitable integrated circuit (IC) technology (including but not limited to MOSFET structures), or in hybrid or discrete circuit forms. Integrated circuit embodiments may be fabricated using any suitable substrates and processes, including but not limited to standard bulk silicon, high-resistivity bulk CMOS, silicon-on-insulator (SOI), and silicon-on-sapphire (SOS). Unless otherwise noted above, embodiments of the invention may be implemented in other transistor technologies such as bipolar, BiCMOS, LDMOS, BCD, GaAs HBT, GaN HEMT, GaAs pHEMT, and MESFET technologies. However, embodiments of the invention are particularly useful when fabricated using an SOI or SOS based process, or when fabricated with processes having similar characteristics. Fabrication in CMOS using SOI or SOS processes enables circuits with low power consumption, the ability to withstand high power signals during operation due to FET stacking, good linearity, and high frequency operation (*i.e.*, radio frequencies up to and exceeding 300 GHz). Monolithic IC implementation is particularly useful since parasitic capacitances generally can be kept low (or at a minimum, kept uniform across all units, permitting them to be compensated) by careful design.

[0065] Voltage levels may be adjusted, and/or voltage and/or logic signal polarities reversed, depending on a particular specification and/or implementing technology (*e.g.*, NMOS, PMOS, or CMOS, and enhancement mode or depletion mode transistor devices). Component voltage, current, and power handling capabilities may be adapted as needed, for example, by adjusting device sizes, serially "stacking" components (particularly FETs) to withstand greater voltages, and/or using multiple components in parallel to handle greater currents. Additional circuit components may be added to enhance the capabilities of the disclosed circuits and/or to provide additional functionality without significantly altering the functionality of the disclosed circuits.

[0066] Circuits and devices in accordance with the present invention may be used alone or in combination with other components, circuits, and devices. Embodiments of the present

invention may be fabricated as integrated circuits (ICs), which may be encased in IC packages and/or in modules for ease of handling, manufacture, and/or improved performance. In particular, IC embodiments of this invention are often used in modules in which one or more of such ICs are combined with other circuit blocks (*e.g.*, filters, amplifiers, passive components, and possibly additional ICs) into one package. The ICs and/or modules are then typically combined with other components, often on a printed circuit board, to form part of an end product such as a cellular telephone, laptop computer, or electronic tablet, or to form a higher-level module which may be used in a wide variety of products, such as vehicles, test equipment, medical devices, *etc*. Through various configurations of modules and assemblies, such ICs typically enable a mode of communication, often wireless communication.

[0067] A number of embodiments of the invention have been described. It is to be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, some of the steps described above may be order independent, and thus can be performed in an order different from that described. Further, some of the steps described above may be optional. Various activities described with respect to the methods identified above can be executed in repetitive, serial, and/or parallel fashion.

[0068] It is to be understood that the foregoing description is intended to illustrate and not to limit the scope of the invention, which is defined by the scope of the following claims, and that other embodiments are within the scope of the claims. In particular, the scope of the invention includes any and all feasible combinations of one or more of the processes, machines, manufactures, or compositions of matter set forth in the claims below. (Note that the parenthetical labels for claim elements are for ease of referring to such elements, and do not in themselves indicate a particular required ordering or enumeration of elements; further, such labels may be reused in dependent claims as references to additional elements without being regarded as starting a conflicting labeling sequence).

CLAIMS

1. A multi-input multi-band low noise amplifier (LNA) comprising:

a dedicated RF processing path for processing of an input RF signal of a first frequency band, the dedicated RF processing path comprising:

a dedicated cascode amplifier comprising a dedicated input transistor and a dedicated output cascode transistor that is coupled to a high side node; and

a shared RF processing path for processing of at least two input RF signals of respective second and third frequency bands, the shared RF processing path comprising:

an input band selection switch; and

a multi-input shared cascode amplifier comprising a plurality of input transistors and a shared output cascode transistor coupled to the plurality of input transistors,

wherein:

the shared output cascode transistor is coupled to the high side node, and

the input band selection switch is configured to selectively couple each of the at least two input RF signals to a shared input transistor of the plurality of input transistors.

2. The multi-input multi-band low noise amplifier (LNA) of claim 1, wherein:

the dedicated RF processing path further comprises a dedicated input matching circuit coupled to the dedicated input transistor of the dedicated cascode amplifier, and

the shared RF processing path further comprises a shared input matching circuit coupled between the input band selection switch and the shared input transistor of the multi-input shared cascode amplifier.

3. The multi-input multi-band low noise amplifier (LNA) of claim 1, further comprising:

an additional RF processing path for processing of an input RF signal of a fourth frequency band, the additional RF processing path comprising:

a dedicated input matching circuit coupled to a dedicated input transistor of the plurality of input transistors of the multi-input shared cascode amplifier.

4.. The multi-input multi-band low noise amplifier (LNA) of claim 1, wherein:

the dedicated output cascode transistor is unconditionally coupled to the high side node, and

the shared output cascode transistor is selectively coupled to the high side node via a switch.

5. The multi-input multi-band low noise amplifier (LNA) of claim 3, wherein:

processing of the first through fourth frequency bands via respective dedicated, shared and additional RF processing paths is based on a priori assignment of a performance priority to each band of said frequency bands.

6. The multi-input multi-band low noise amplifier (LNA) of claim 5, wherein:

the a priori assignment of the performance priority to each band of the said frequency bands is based on at least one of:

insertion loss of a band filter used to process a corresponding RF signal,

frequency spectrum of the each band, or

a target sensitivity performance for the each band.

7. The multi-input multi-band low noise amplifier (LNA) of claim 5, wherein:

the RF processing performance is based on at least one of:

an insertion loss performance,

a sensitivity performance,

a linearity performance, or

a power consumption performance.

8. The multi-input multi-band low noise amplifier (LNA) of claim 7, wherein:

the a priori assignment of the performance priority is configured to equalize an RF processing performance of the each band through the multi-input multi-band LNA with a reduced cost and physical size of said LNA.

9. The multi-input multi-band low noise amplifier (LNA) of claim 7, wherein:

the a priori assignment of the performance priority is configured to equalize an RF sensitivity performance of said frequency bands through the multi-input multi-band LNA with a reduced cost and physical size of said LNA.

10. The multi-input multi-band low noise amplifier (LNA) of claim 1, wherein:

a source of the dedicated output cascode transistor is coupled to a drain of the dedicated input transistor of the dedicated cascode amplifier, and

a source of the shared output cascode transistor is coupled to respective drains of the plurality of input transistors of the multi-input shared cascode amplifier.

11. The multi-input multi-band low noise amplifier (LNA) of claim 10, wherein:

respective sources of the dedicated input transistor of the dedicated cascode transistor and of the plurality of input transistors of the multi-input shared cascode amplifier are coupled to a low side node.

12. The multi-input multi-band low noise amplifier (LNA) of claim 11, wherein:

the low side node is coupled to a reference ground through a degeneration inductor.

13. The multi-input multi-band low noise amplifier (LNA) of claim 12, wherein:

the degeneration inductor is tunable.

14. The multi-input multi-band low noise amplifier (LNA) of claim 1, wherein:

the high side node is coupled to a supply voltage through an inductor.

15. The multi-input multi-band low noise amplifier (LNA) of claim 14, wherein:

the inductor is tunable.

16. The multi-input multi-band low noise amplifier (LNA) of claim 14, wherein:

the high side node is further coupled to the supply voltage through at least a resistor or a capacitor.

17. The multi-input multi-band low noise amplifier (LNA) of claim 14, wherein:

the high side node is further coupled to a load through an output matching circuit.

18. The multi-input multi-band low noise amplifier (LNA) of claim 17, wherein:

the output matching circuit comprises at least one capacitor.

19. The multi-input multi-band low noise amplifier (LNA) of claim 18, wherein:

the at least one capacitor is tunable.

20. The multi-input multi-band low noise amplifier (LNA) of claim 2, wherein:

each of the dedicated input matching circuit and the shared input matching circuit comprises an inductor.

21. The multi-input multi-band low noise amplifier (LNA) of claim 20, wherein:

the inductor of the each of the dedicated input matching circuit and the shared input matching circuit is a fixed inductance surface mount device.

22. The multi-input multi-band low noise amplifier (LNA) of claim 3, wherein:

the dedicated input matching circuit of the additional RF processing path comprises an inductor.

23. The multi-input multi-band low noise amplifier (LNA) of claim 22, wherein:

the inductor of the dedicated input matching circuit of the additional RF processing path is a surface mount device with tunable inductance.

24. The multi-input multi-band low noise amplifier (LNA) of claim 22, wherein:

the inductor of the dedicated input matching circuit of the additional RF processing path is an in-circuit inductor.

25. The multi-input multi-band low noise amplifier (LNA) of claim 1, wherein:

the dedicated RF processing path is coupled to an antenna switch through a first band filter,

the shared RF processing path is coupled to the antenna switch through a second band filter that is coupled to a first throw of the input band selection switch, and

the shared RF processing path is further coupled to a first auxiliary circuit that is coupled to a second throw of the input band selection switch.

26. The multi-input multi-band low noise amplifier (LNA) of claim 3, wherein:

the dedicated RF processing path is coupled to an antenna switch through a first band filter,

the shared RF processing path is coupled to the antenna switch through a second band filter that is coupled to a first throw of the input band selection switch,

the shared RF processing path is further coupled to a first auxiliary circuit that is coupled to a second throw of the input band selection switch, and

the additional RF processing path is coupled to a second auxiliary circuit.

27. The multi-input multi-band low noise amplifier (LNA) of claim 1, wherein:

the dedicated cascode amplifier is a low noise amplifier (LNA), and

the multi-input shared cascode amplifier is a multi-input LNA that comprises a plurality of amplification paths corresponding to the plurality of input transistors, each of the plurality of amplification paths passing through the shared output cascode transistor.

28. The multi-input multi-band low noise amplifier (LNA) of claim 27, wherein:

transistors of the dedicated cascode amplifier and of the multi-input shared cascode amplifier comprises metal-oxide-semiconductor (MOS) field effect transistors (FETs), or complementary metal-oxide-semiconductor (CMOS) field effect transistors (FETs).

29. The multi-input multi-band low noise amplifier (LNA) of claim 28, wherein:

said transistors are fabricated using one of: a) silicon-on-insulator (SOI) technology, and b) silicon-on-sapphire technology (SOS).

30. An electronic module comprising the multi-input multi-band low noise amplifier (LNA) of claim 1.

31. A method, comprising:

using the electronic module of claim 30 in one or more electronic systems comprising: a) a cellular telephone, b) a laptop computer, c) an electronic tablet, d) a vehicle, e) a test equipment, f) a medical device, or g) other electronic systems.

32. A multi-input multi-band low noise amplifier (LNA) comprising:

a dedicated first band RF processing path for processing of a first frequency band RF signal received from an antenna through a dedicated first band filter, the dedicated first band RF processing path comprising:

a dedicated first band input matching circuit coupled to a dedicated first band cascode amplifier, the dedicated first band cascode amplifier comprising:

a dedicated first band input transistor and a dedicated first band output cascode transistor that is coupled to a high side node; and

a shared RF processing path for processing of a second frequency band RF signal received from the antenna through a dedicated second band filter and of a first auxiliary frequency band RF signal that is not received from the antenna, the shared RF processing path comprising:

an input band selection switch;

a multi-input shared cascode amplifier comprising a plurality of input transistors and a shared output cascode transistor coupled to the plurality of input transistors; and

a shared input matching circuit coupled between the input band selection switch and a shared input transistor of the plurality of input transistors,

wherein:

the shared output cascode transistor is coupled to the high side node, and

the input band selection switch is configured to selectively couple one of the second frequency band RF signal or the first auxiliary frequency band RF signal to the shared input transistor.

33. The multi-input multi-band low noise amplifier (LNA) of claim 32, further comprising:

an additional RF processing path for processing of a second auxiliary frequency band RF signal that is not received from the antenna, the additional RF processing path comprising:

a dedicated second auxiliary band input matching circuit coupled to a dedicated second auxiliary band input transistor of the plurality of input transistors.

34. The multi-input multi-band low noise amplifier (LNA) of claim 33, further comprising:

a dedicated third band RF processing path for processing of a third frequency band RF signal from the antenna through a dedicated third band filter, the dedicated third band RF processing path comprising:

a dedicated third band input matching circuit coupled to a dedicated third band cascode amplifier, the dedicated third band cascode amplifier comprising:

a dedicated third band input transistor and a dedicated third band output cascode transistor that is coupled to a high side node.

35. The multi-input multi-band low noise amplifier (LNA) of claim 32, further comprising:

an antenna switch coupled to the antenna, wherein the antenna switch is configured to selectively couple:

the first frequency band RF signal to the dedicated first band filter; or

the second frequency band RF signal to the dedicated second band filter.

36. The multi-input multi-band low noise amplifier (LNA) of claim 32, wherein:

the dedicated first band output cascode transistor is unconditionally coupled to the high side node, and

the shared output cascode transistor is selectively coupled to the high side node via a switch.

37. The multi-input multi-band low noise amplifier (LNA) of claim 33, wherein:

the dedicated first band output cascode transistor is unconditionally coupled to the high side node, and

at least one of the shared input transistor or the dedicated second auxiliary band input transistor is selectively coupled to the shared output cascode transistor via a switch.

38. The multi-input multi-band low noise amplifier (LNA) of claim 34, wherein:

the dedicated first band output cascode transistor is unconditionally coupled to the high side node,

the dedicated third band output cascode transistor and the shared output cascode transistor are selectively coupled to the high side node via a respective switch.

39. A method for optimizing performance and cost of a receive side of an RF front end (RFFE), the method comprising:

assigning a performance priority to each band of a plurality of frequency bands for processing by the RFFE, the performance priority including a range from low to high;

based on the assigning, establishing an RF processing performance for a respective RF processing path of the each band;

based on the establishing, realizing the respective RF processing path based on circuit blocks provided by a toolkit; and

based on the realizing, optimizing RF processing performance and cost of the RFFE.

40. The method according to claim 39, wherein the circuit blocks of the toolkit comprise:

a dedicated input matching circuit block, DIN;

an input combiner circuit block, ICN, comprising a band selection switch;

a dedicated cascode amplifier circuit block, CAS; and

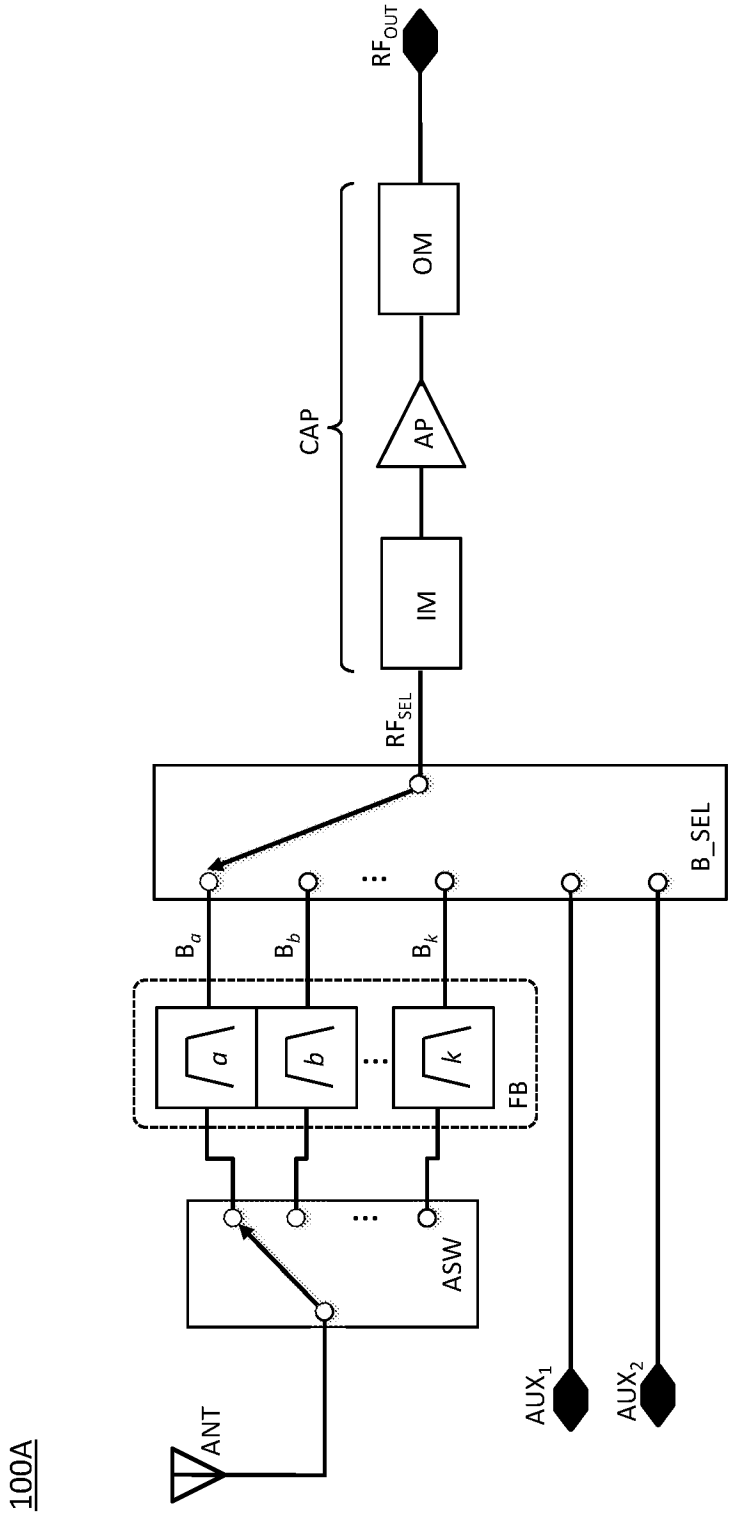
a multi-input shared cascode amplifier circuit block, SCAS.

41. The method according to claim 40, wherein:

for a low performance priority, the realizing includes realizing via the ICN and the SCAS;

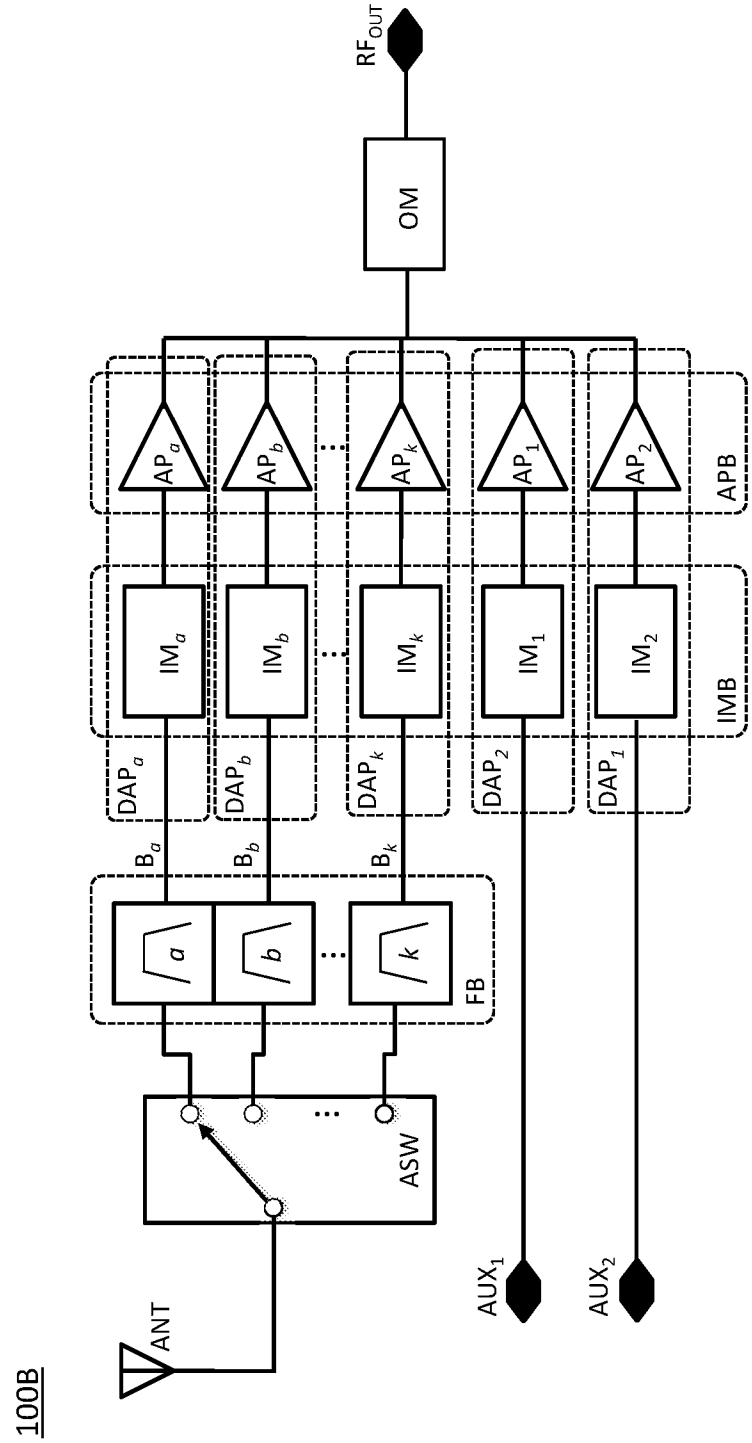
for a medium performance priority, the realizing includes realizing via the DIN and the SCAS; and

for a high performance priority, the realizing includes realizing via the DIN and the CAS.



PRIOR ART

FIG. 1A



PRIOR ART

FIG. 1B

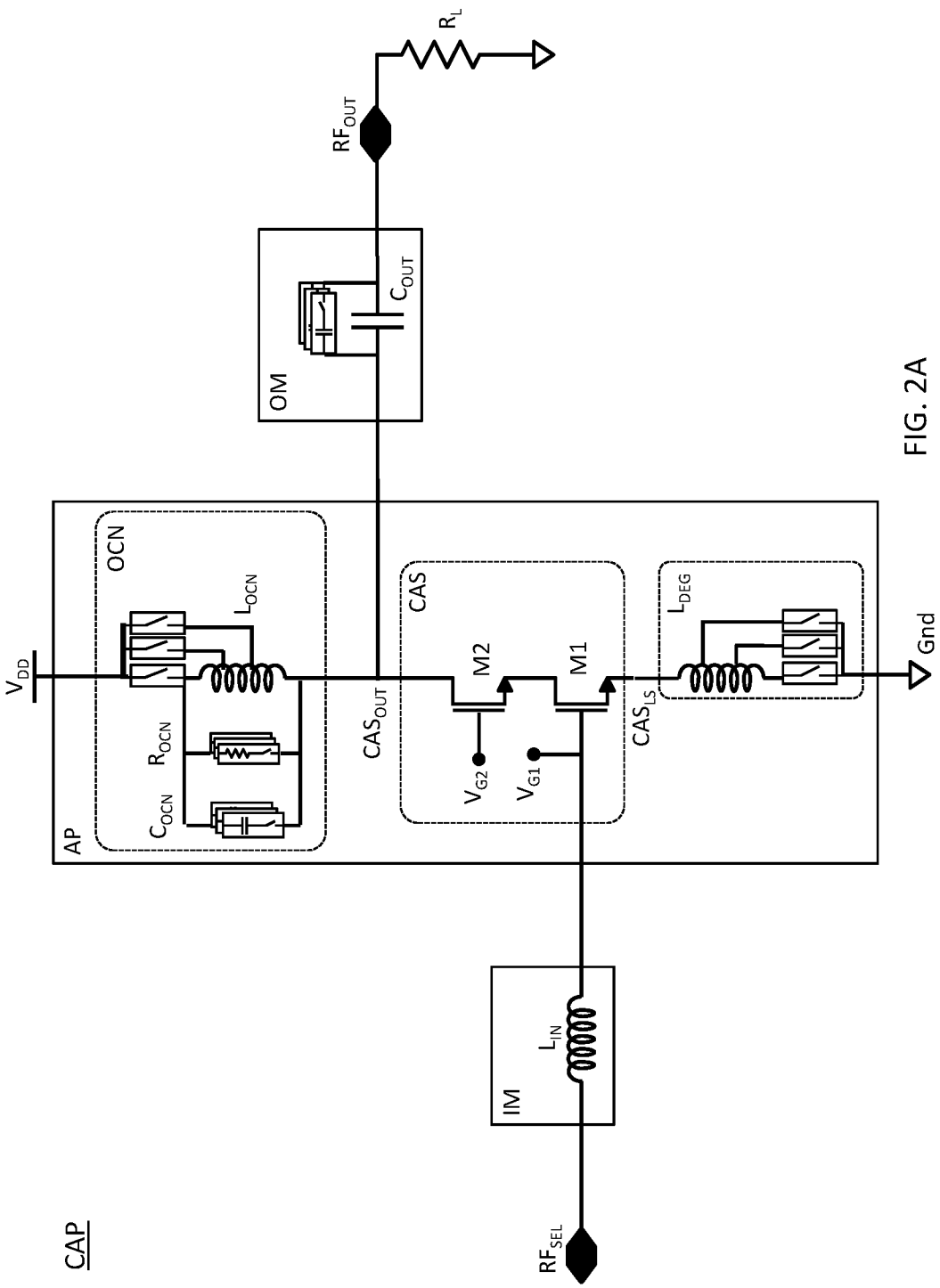

CAP
RL
RFOUT
COUT
OM
AP
OCN
LOCN
ROCN
COCN
VDD
CASOUT
CAS
M2
M1
VG2
VG1
CASLS
LDEG
Gnd
LIN
IM
RFSEL

FIG. 2A

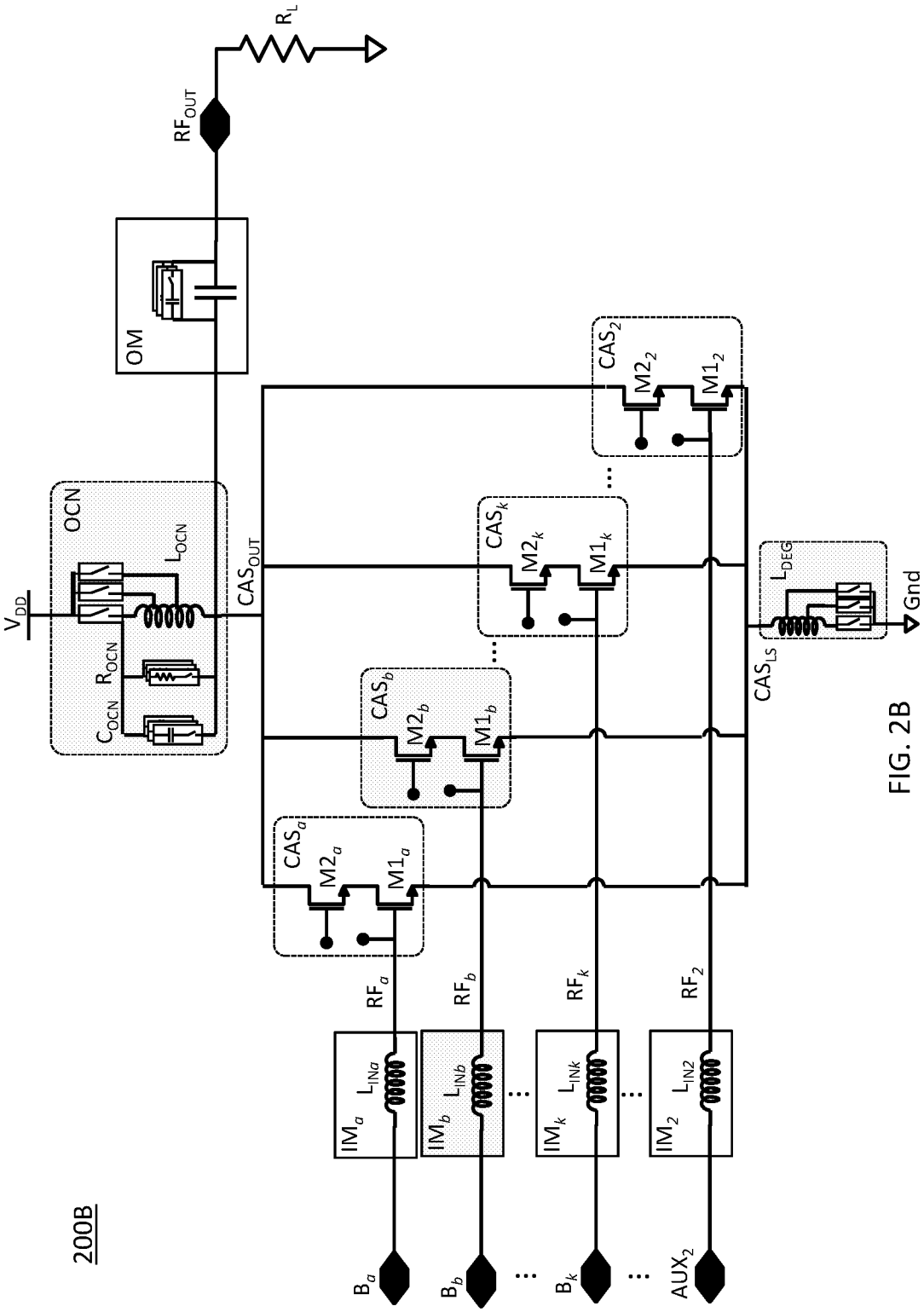

200B
R_L
RF_{OUT}
OM
OCN
L_{OCN}
R_{OCN}
C_{OCN}
V_{DD}
CAS_{OUT}
CAS_2 $M2_2$ $M1_2$
CAS_k $M2_k$ $M1_k$
CAS_b $M2_b$ $M1_b$
CAS_a $M2_a$ $M1_a$
CAS_{LS}
L_{DEG}
Gnd
RF_a RF_b RF_k RF_2
IM_a L_{INa}
IM_b L_{INb}
IM_k L_{INk}
IM_2 L_{IN2}
B_a B_b B_k AUX_2

FIG. 2B

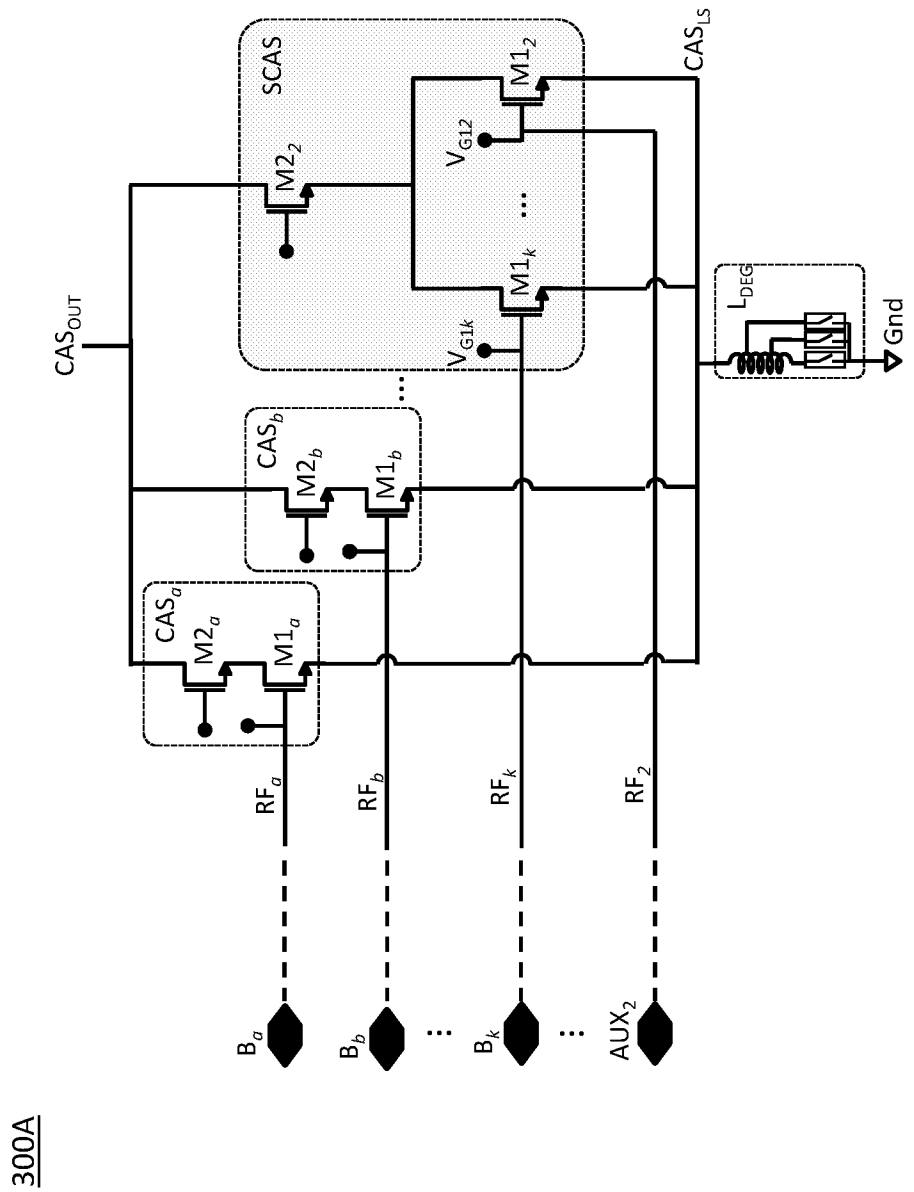

300A
SCAS
M2$_2$
M1$_2$
V_{G12}
M1$_k$
V_{G1k}
CAS$_{OUT}$
CAS$_{LS}$
L_{DEG}
Gnd
CAS$_b$
M2$_b$
M1$_b$
CAS$_a$
M2$_a$
M1$_a$
RF$_a$
RF$_b$
RF$_k$
RF$_2$
B$_a$
B$_b$
B$_k$
AUX$_2$

FIG. 3A

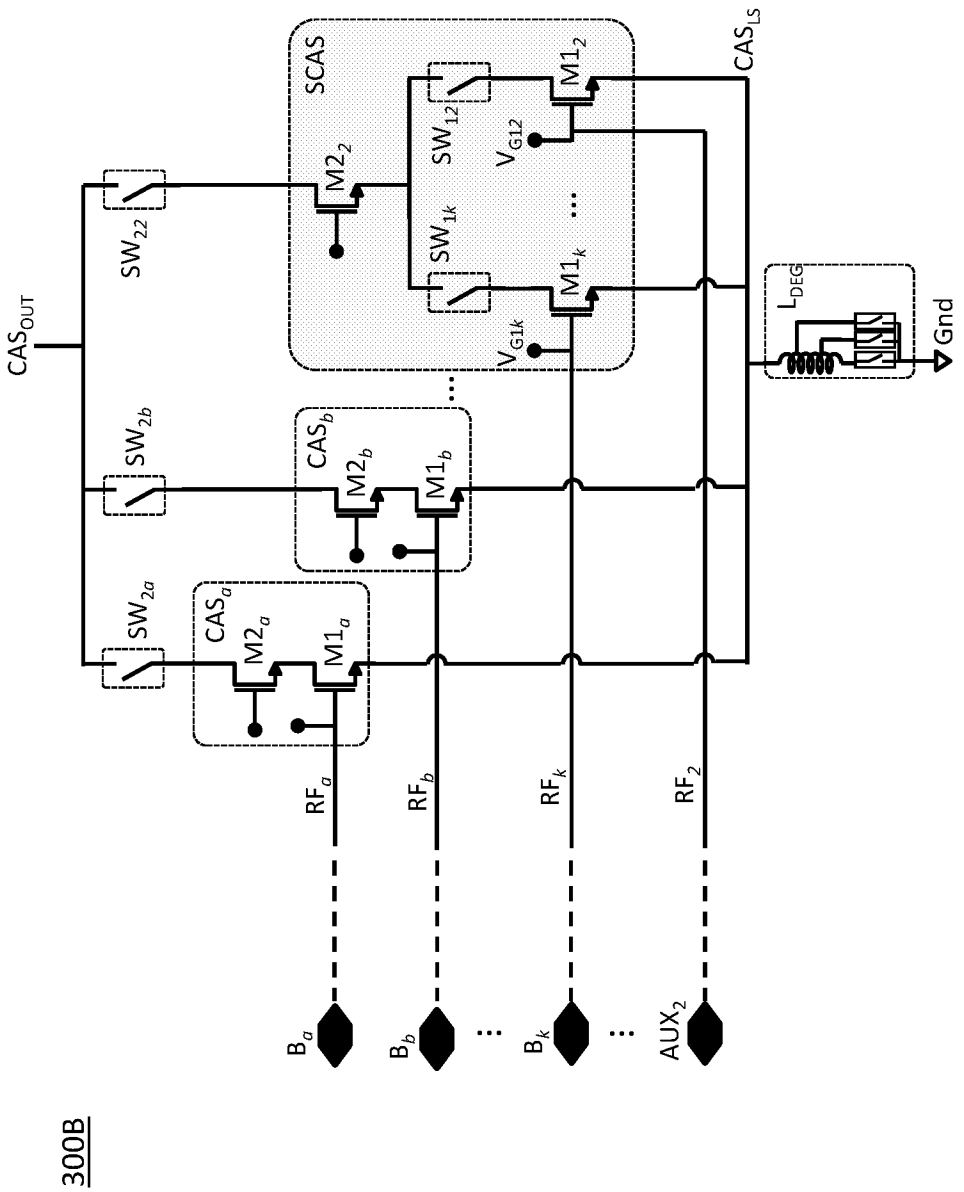

300B
SCAS
CAS_OUT
CAS_LS
SW_22
M2_2
SW_12
M1_2
V_G12
SW_1k
M1_k
V_G1k
L_DEG
Gnd
SW_2b
CAS_b
M2_b
M1_b
SW_2a
CAS_a
M2_a
M1_a
RF_a
RF_b
RF_k
RF_2
B_a
B_b
B_k
AUX_2

FIG. 3B

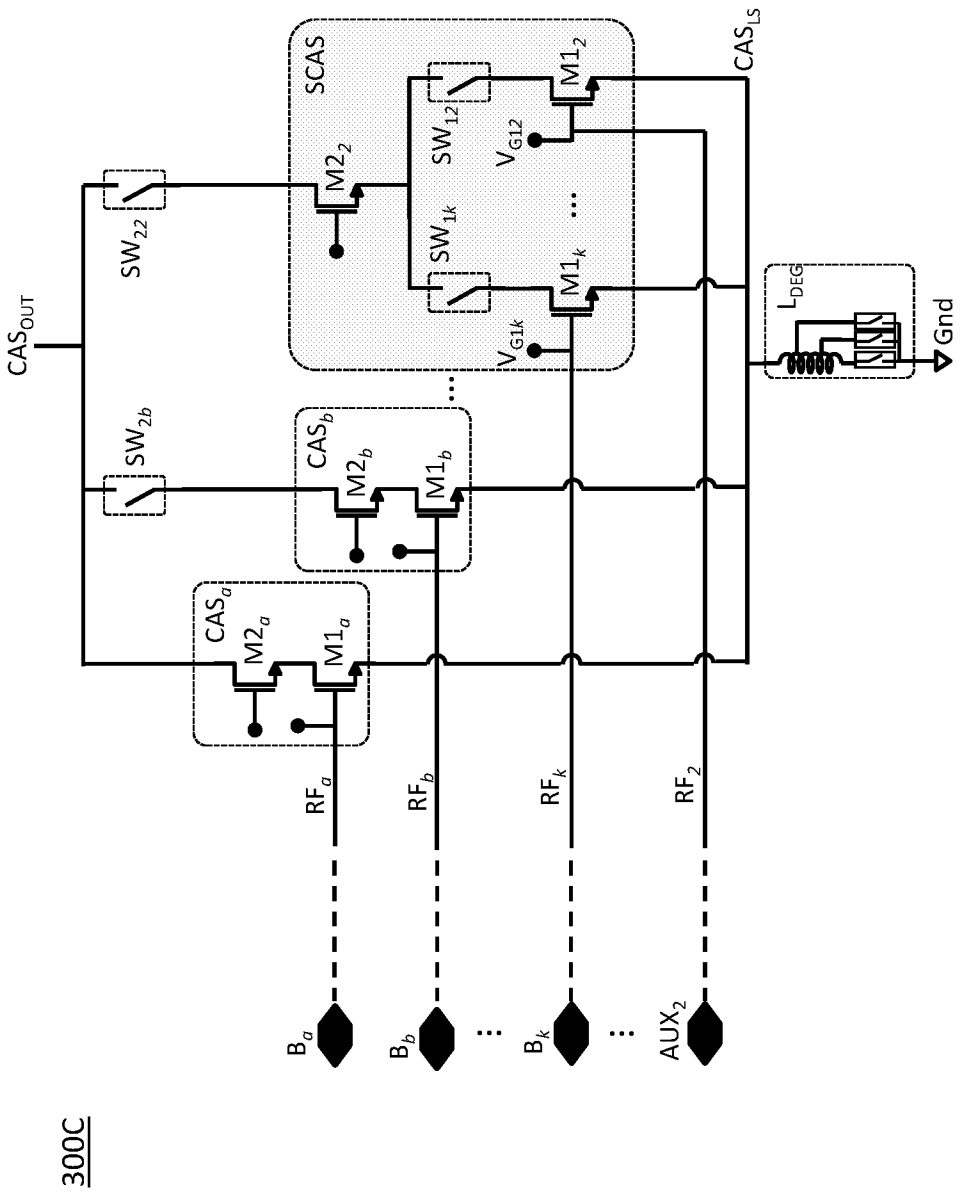

300C
SCAS
CAS_OUT
CAS_LS
SW_22
SW_2b
SW_12
SW_1k
M2_2
M1_2
M1_k
V_G12
V_G1k
CAS_b
M2_b
M1_b
CAS_a
M2_a
M1_a
L_DEG
Gnd
RF_a
RF_b
RF_k
RF_2
B_a
B_b
B_k
AUX_2

FIG. 3C

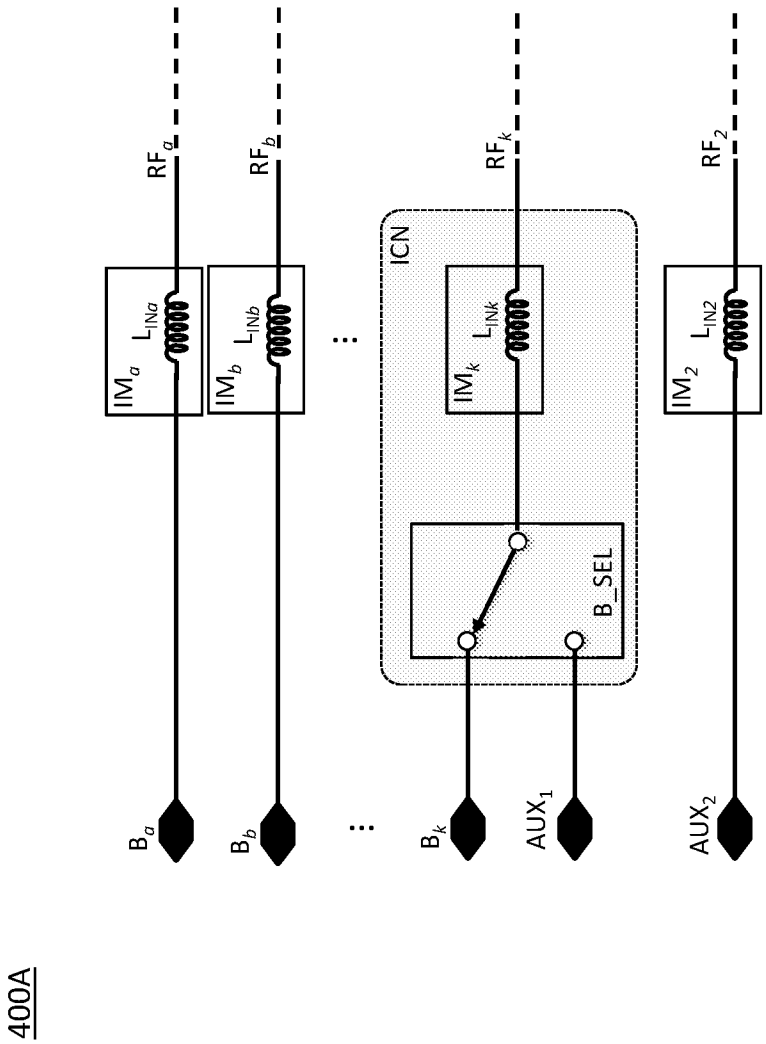

400A
RF$_a$
RF$_b$
RF$_k$
RF$_2$
ICN
IM$_a$ L$_{INa}$
IM$_b$ L$_{INb}$
IM$_k$ L$_{INk}$
IM$_2$ L$_{IN2}$
B_SEL
B$_a$
B$_b$
B$_k$
AUX$_1$
AUX$_2$

FIG. 4A

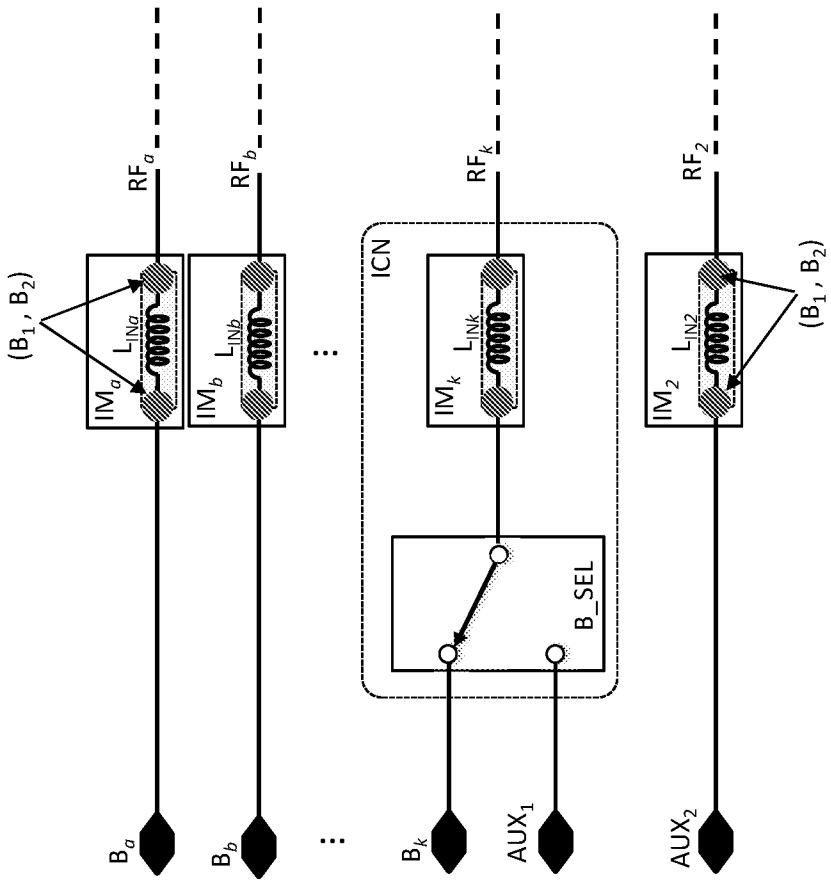

RF_a
RF_b
RF_k
RF_2
(B_1, B_2)
IM_a
L_INa
IM_b
L_INb
ICN
IM_k
L_INk
IM_2
L_IN2
(B_1, B_2)
B_SEL
B_a
B_b
B_k
AUX_1
AUX_2

FIG. 4B

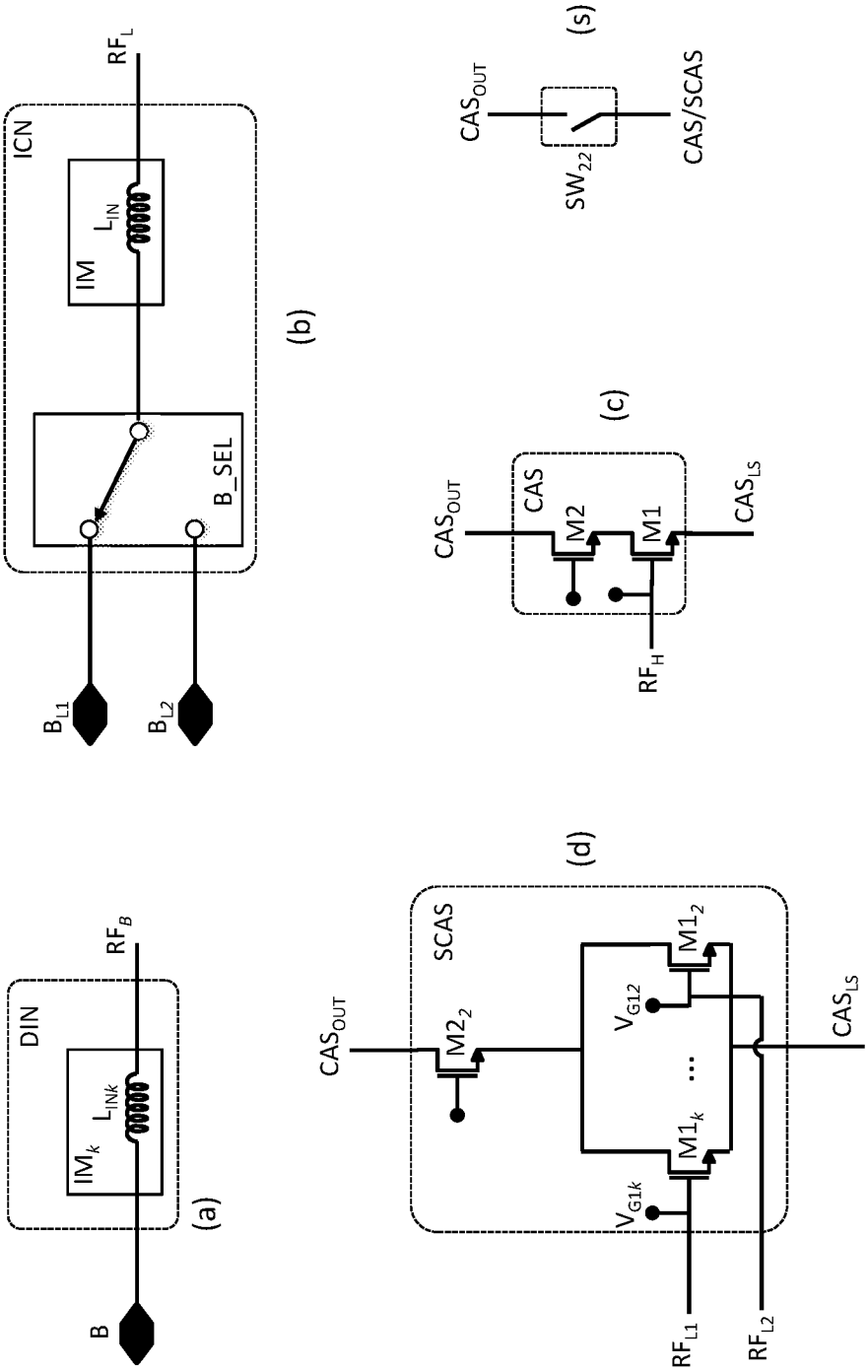

DIN
RF_B
IM_k
L_{INk}
B
(a)
ICN
RF_L
IM
L_{IN}
B_SEL
B_{L1}
B_{L2}
(b)
CAS_{OUT}
CAS
M2
M1
CAS_{LS}
RF_H
(c)
CAS_{OUT}
SCAS
$M2_2$
V_{G12}
$M1_2$
$M1_k$
V_{G1k}
CAS_{LS}
RF_{L1}
RF_{L2}
(d)
CAS_{OUT}
SW_{22}
CAS/SCAS
(s)

FIG. 5A

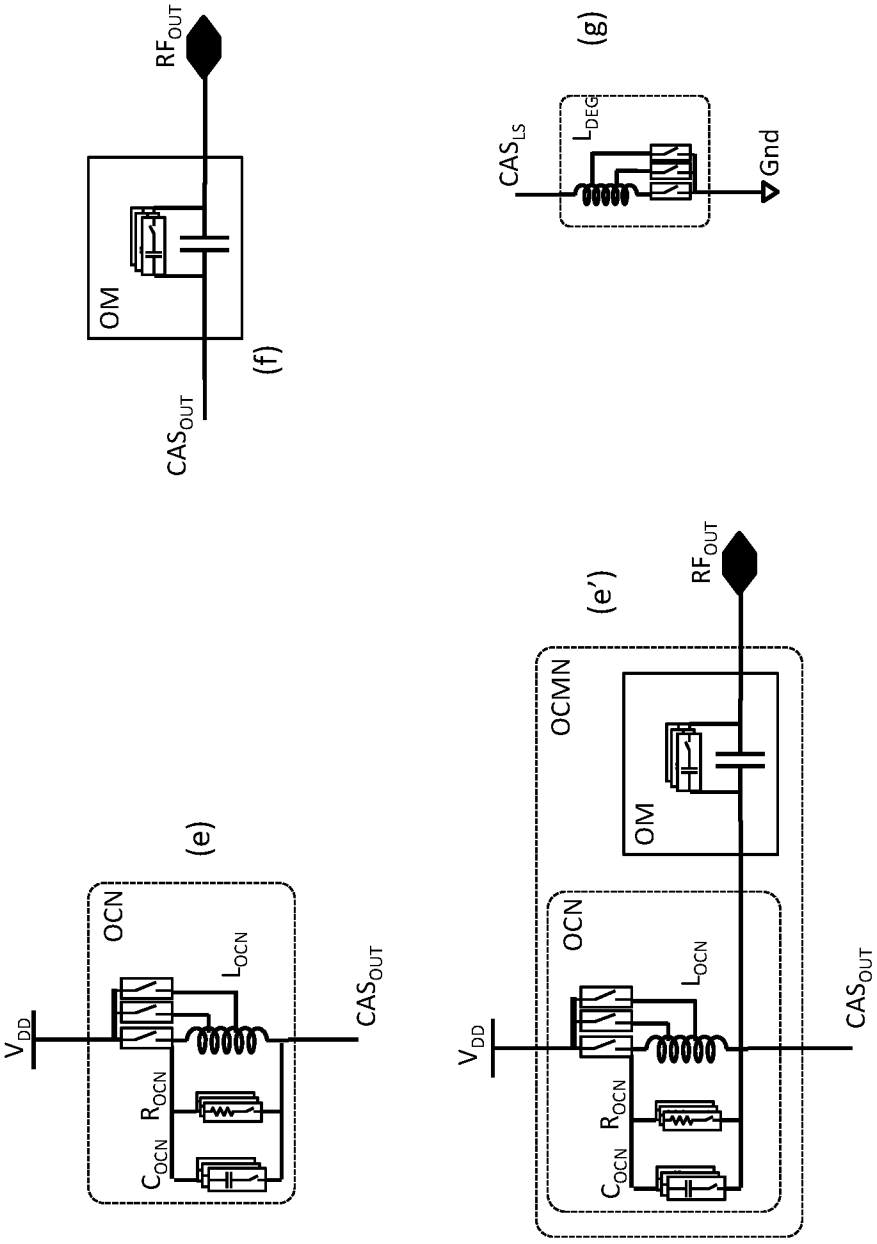

RF_OUT
OM
CAS_OUT
(f)
(g)
CAS_LS
L_DEG
Gnd
(e')
OCMN
OM
OCN
L_OCN
R_OCN
C_OCN
V_DD
CAS_OUT
(e)
OCN
L_OCN
R_OCN
C_OCN
V_DD
CAS_OUT

FIG. 5B

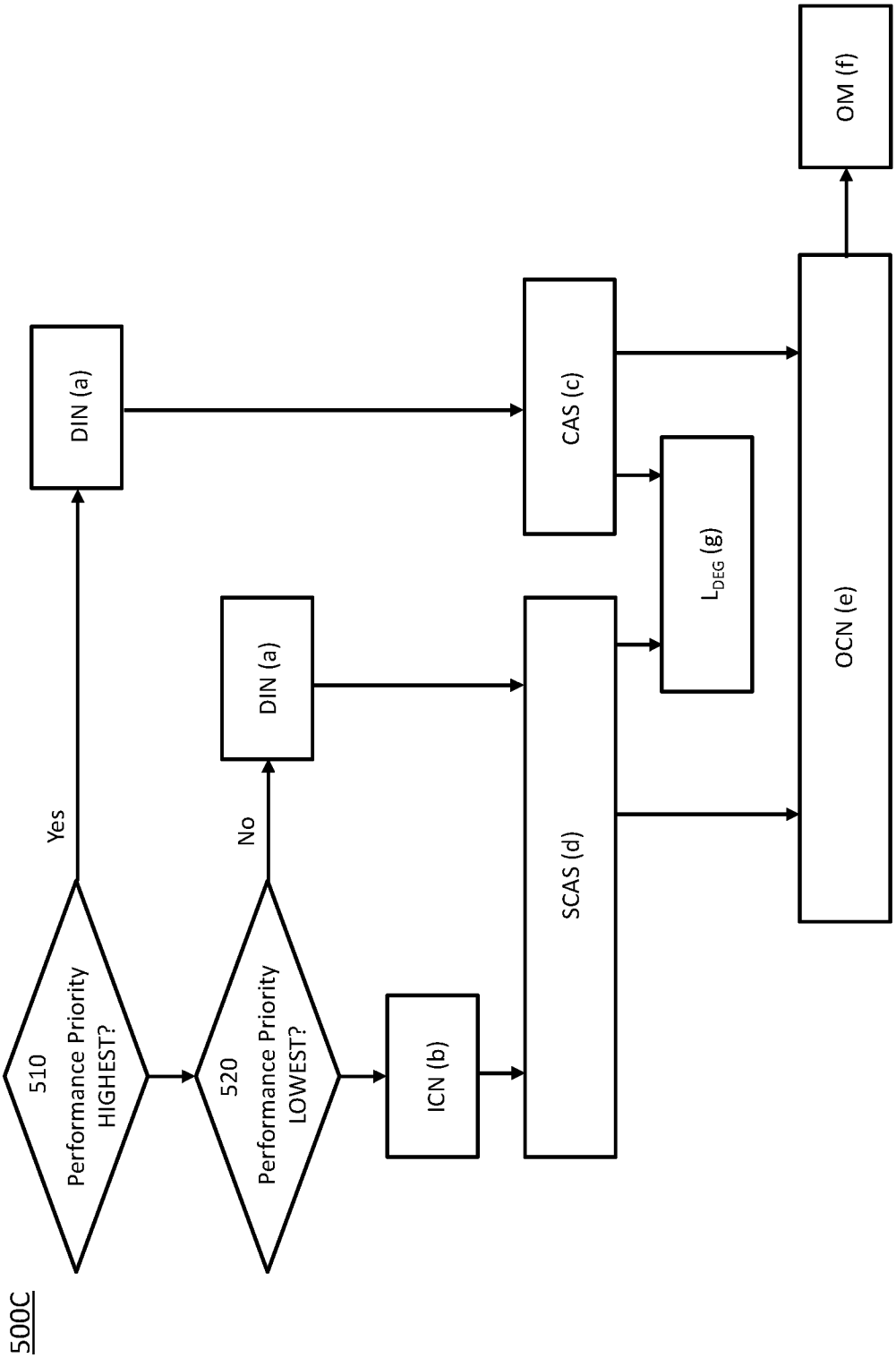

500C
510
Performance Priority
HIGHEST?
Yes
DIN (a)
520
Performance Priority
LOWEST?
No
DIN (a)
ICN (b)
SCAS (d)
CAS (c)
L_{DEG} (g)
OCN (e)
OM (f)

FIG. 5C

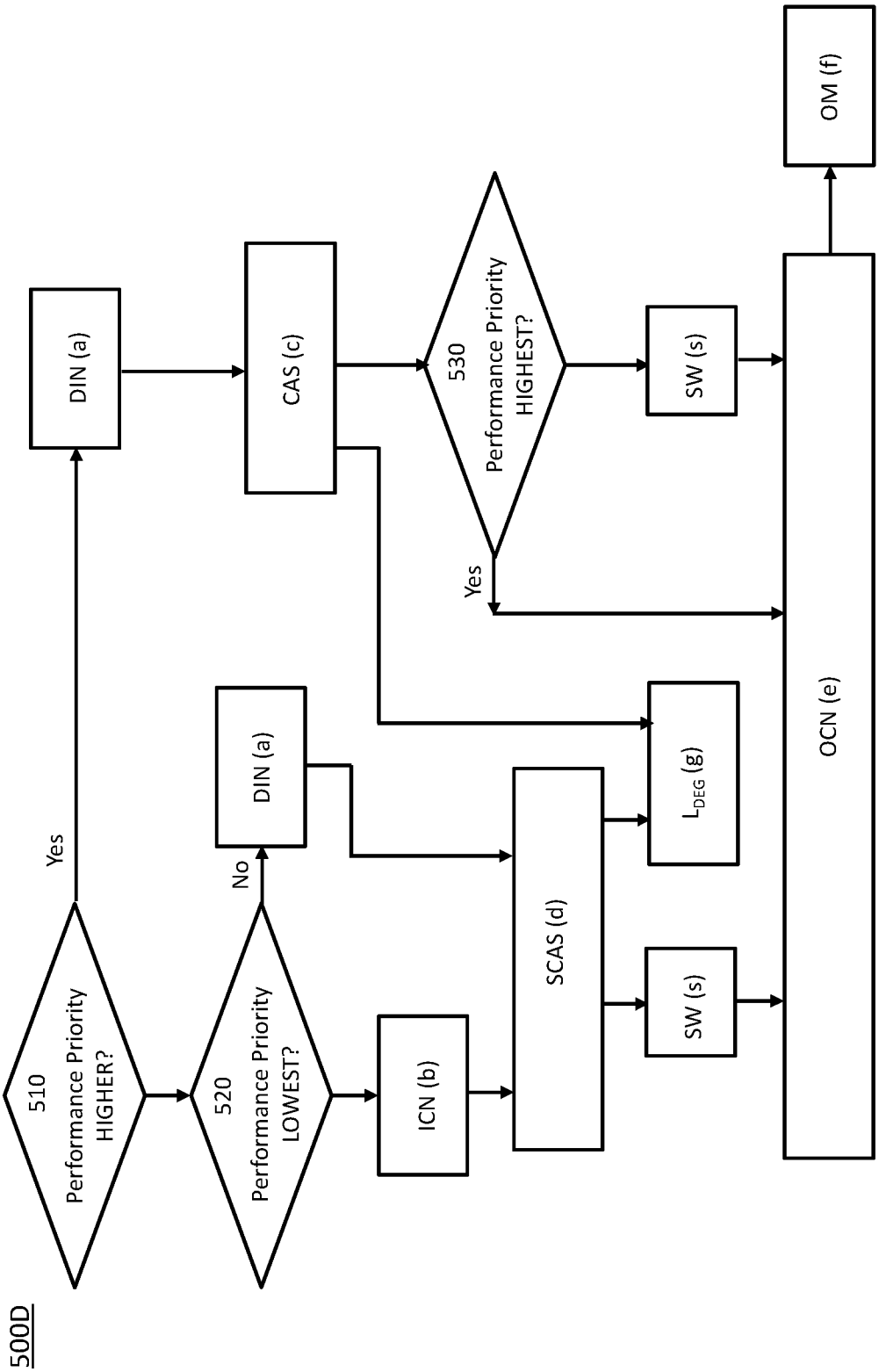

500D
510
Performance Priority
HIGHER?
Yes
520
Performance Priority
LOWEST?
No
DIN (a)
ICN (b)
SCAS (d)
SW (s)
L_{DEG} (g)
DIN (a)
CAS (c)
530
Performance Priority
HIGHEST?
Yes
SW (s)
OCN (e)
OM (f)

FIG. 5D

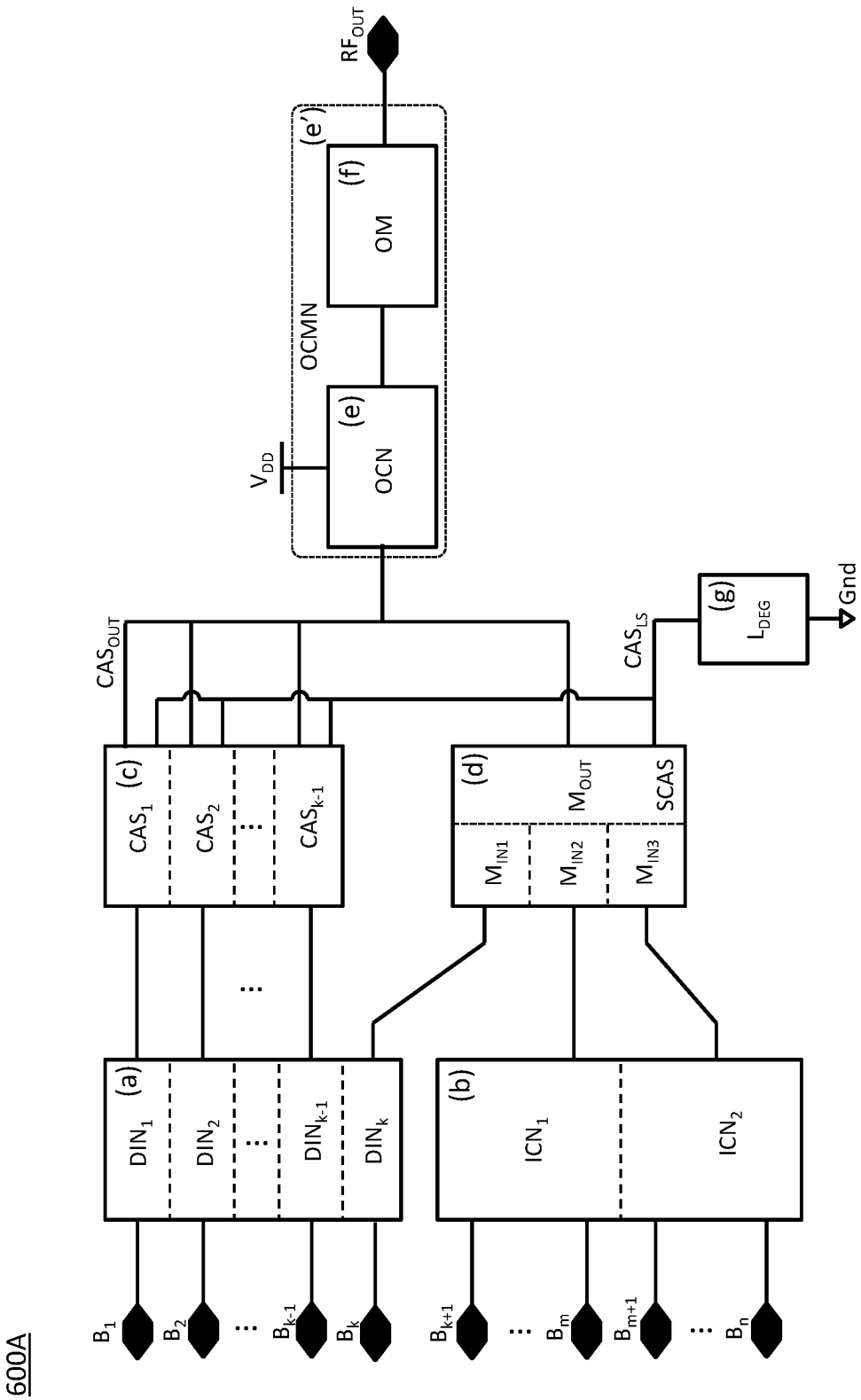

600A
B1
B2
Bk-1
Bk
Bk+1
Bm
Bm+1
Bn
(a)
DIN1
DIN2
DINk-1
DINk
(b)
ICN1
ICN2
(c)
CAS1
CAS2
CASk-1
CASOUT
(d)
MIN1
MIN2
MIN3
MOUT
SCAS
CASLS
(e)
OCN
VDD
OCMN
(e')
(f)
OM
RFOUT
(g)
LDEG
Gnd

FIG. 6A

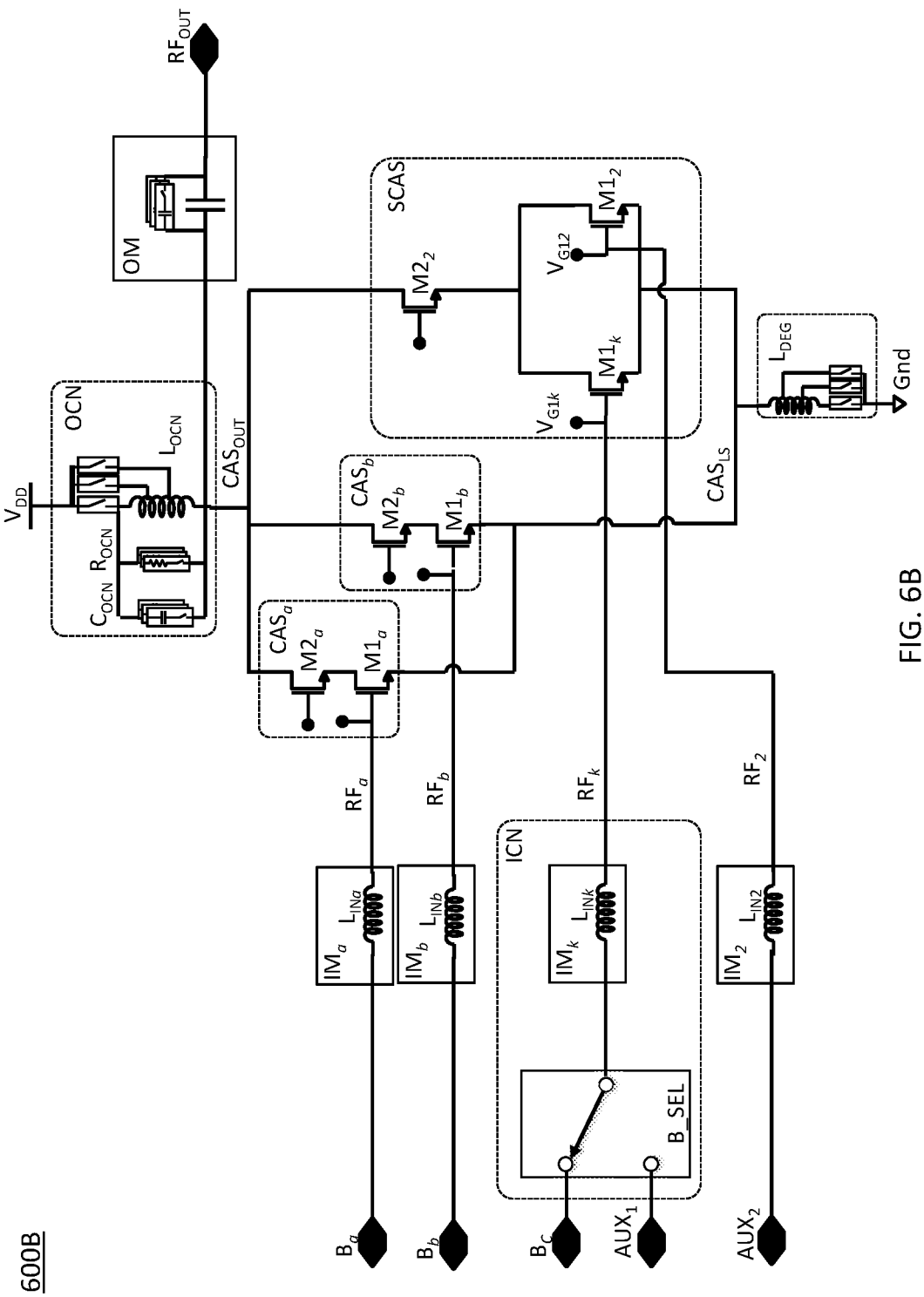

600B
RF_OUT
OM
OCN
L_OCN
R_OCN
C_OCN
V_DD
CAS_OUT
SCAS
M2_2
M1_2
V_G12
M1_k
V_G1k
L_DEG
Gnd
CAS_LS
CAS_b
M2_b
M1_b
CAS_a
M2_a
M1_a
RF_a
RF_b
RF_k
RF_2
ICN
IM_a
L_INa
IM_b
L_INb
IM_k
L_INk
IM_2
L_IN2
B_SEL
B_a
B_b
B_c
AUX_1
AUX_2

FIG. 6B

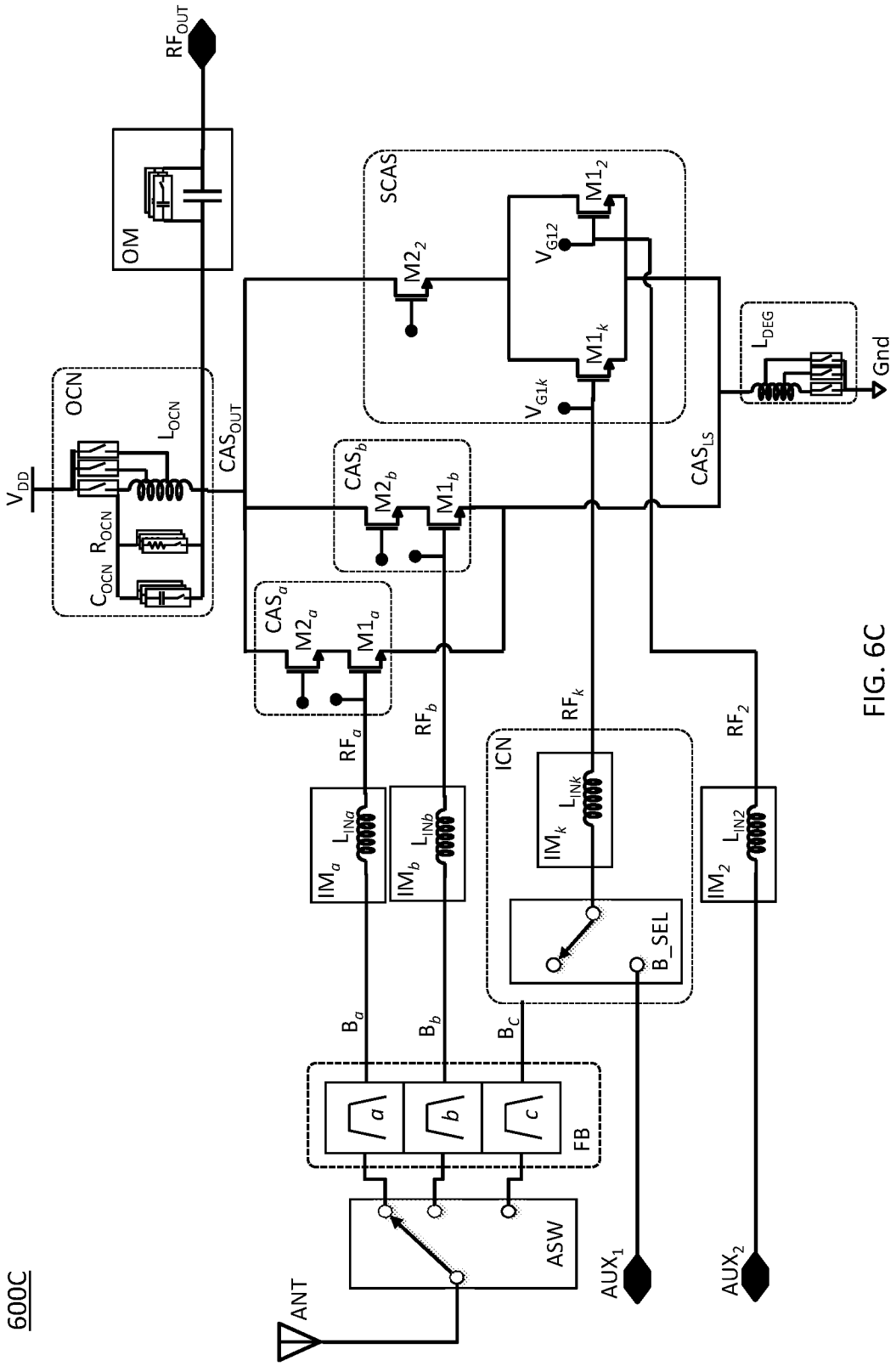

600C
RF_OUT
OM
OCN
L_OCN
C_OCN
R_OCN
V_DD
CAS_OUT
SCAS
M2_2
V_G12
M1_2
M1_k
V_G1k
L_DEG
Gnd
CAS_LS
CAS_b
M2_b
M1_b
CAS_a
M2_a
M1_a
RF_a
RF_b
RF_k
RF_2
ICN
IM_a
L_INa
IM_b
L_INb
IM_k
L_INk
IM_2
L_IN2
B_SEL
B_a
B_b
B_c
FB
a
b
c
ASW
ANT
AUX_1
AUX_2

FIG. 6C

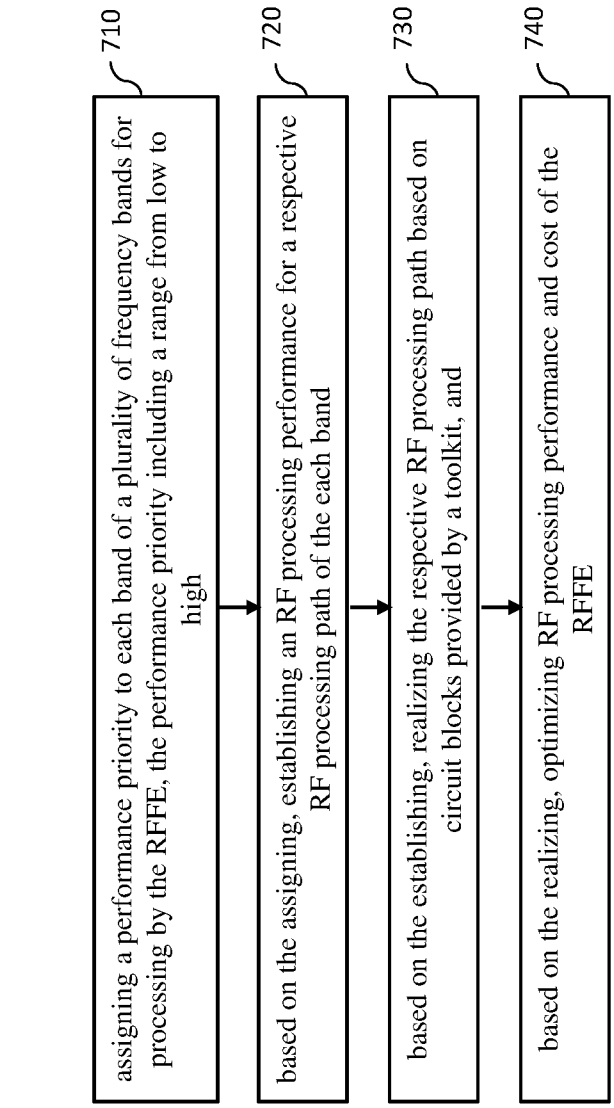

700
710
assigning a performance priority to each band of a plurality of frequency bands for processing by the RFFE, the performance priority including a range from low to high
720
based on the assigning, establishing an RF processing performance for a respective RF processing path of the each band
730
based on the establishing, realizing the respective RF processing path based on circuit blocks provided by a toolkit, and
740
based on the realizing, optimizing RF processing performance and cost of the RFFE

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/079467

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/26(2006.01)i; **H03F 1/22**(2006.01)i; **H03F 3/193**(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F 1/26(2006.01); H03F 1/02(2006.01); H03F 1/56(2006.01); H03F 3/16(2006.01); H03F 3/19(2006.01); H03F 3/193(2006.01); H03F 3/195(2006.01); H03F 3/21(2006.01); H04B 1/18(2006.01); H04B 7/00(2006.01); H04B 7/08(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: multi-input, amplifier, frequency, band, dedicated RF processing path, shared RF processing path, selection switch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2020-0127617 A1 (PSEMI CORPORATION) 23 April 2020 (2020-04-23) claims 1-20	1-41
A	US 2015-0381124 A1 (SKYWORKS SOLUTIONS, INC.) 31 December 2015 (2015-12-31) claims 1-20	1-41
A	US 2021-0143779 A1 (PSEMI CORPORATION) 13 May 2021 (2021-05-13) paragraph [0039] and figure 7	1-41
A	US 2006-0189286 A1 (IREI KYU et al.) 24 August 2006 (2006-08-24) paragraphs [0113]-[0119] and figure 10	1-41
A	US 2019-0103843 A1 (MURATA MANUFACTURING CO., LTD.) 04 April 2019 (2019-04-04) paragraphs [0045]-[0078] and figure 1	1-41

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 March 2023	**20 March 2023**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office **189 Cheongsa-ro, Seo-gu, Daejeon** **35208, Republic of Korea**	**JUNG, Jong Han**
Facsimile No. **+82-42-481-8578**	Telephone No. **+82-42-481-5642**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2022/079467

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2020-0127617 A1	23 April 2020	US 10461704 B2	29 October 2019
		US 11025208 B2	01 June 2021
		US 2019-0190468 A1	20 June 2019
US 2015-0381124 A1	31 December 2015	US 10312864 B2	04 June 2019
		US 11152894 B2	19 October 2021
		US 2017-0302227 A1	19 October 2017
		US 2020-0162027 A1	21 May 2020
		US 9595921 B2	14 March 2017
US 2021-0143779 A1	13 May 2021	US 10476453 B2	12 November 2019
		US 10862441 B2	08 December 2020
		US 2018-0358938 A1	13 December 2018
		US 2020-0127618 A1	23 April 2020
		US 9941849 B1	10 April 2018
US 2006-0189286 A1	24 August 2006	CN 1825757 A	30 August 2006
		EP 1693957 A1	23 August 2006
		JP 2006-237711 A	07 September 2006
		NO 20060410 A	23 August 2006
US 2019-0103843 A1	04 April 2019	CN 109586756 A	05 April 2019
		JP 2019-068205 A	25 April 2019
		US 10381989 B2	13 August 2019