



(51) International Patent Classification:

G02B 1/11 (2006.01) **C09D 5/00** (2006.01)
B29D 11/00 (2006.01)

(21) International Application Number:

PCT/US2014/016404

(22) International Filing Date:

14 February 2014 (14.02.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: **APPLE INC.** [US/US]; 1 Infinite Loop, M/S 36-2PAT, Cupertino, CA 95014 (US).

(72) Inventors: **DORJGOTOV, Enkhamgalan**; 20400 Mariani Ave, M/S 83-D, Cupertino, CA 95014 (US). **CHEN, Cheng**; 1 Infinite Loop, M/S 83-D, Cupertino, CA 95014 (US). **KUWABARA, Masato**; 870-TOC, 3-20-2, Nishishinjyuku, Shinjyuku-ku, Tokyo, 163-1480 (JP). **ROGERS, Matthew, S.**; 1 Infinite Loop, M/S 305-1PH, Cupertino, CA 95014 (US). **ZHONG, John, Z.**; 1 Infinite Loop, M/S 83-D, Cupertino, CA 95014 (US).

(74) Agent: **TREYZ, G. Victor**; Treyz Law Group, 870 Market Street, Suite 984, San Francisco, CA 94102 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— of inventorship (Rule 4.17(iv))

[Continued on next page]

(54) Title: METHODS FOR FORMING ANTIREFLECTION COATINGS FOR DISPLAYS

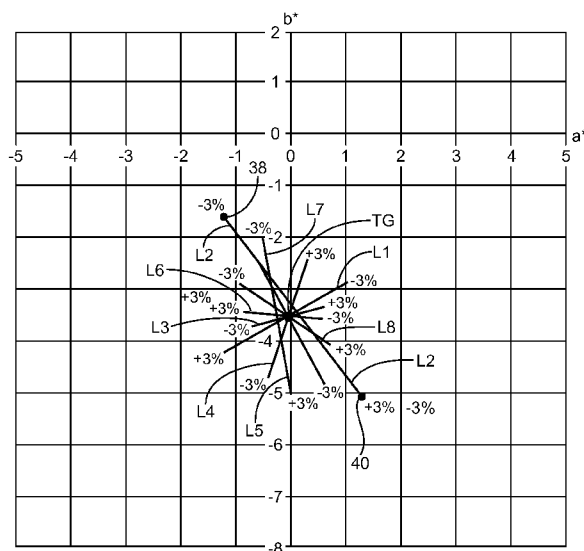


FIG. 8

(57) Abstract: A display may be provided with display layers. Ambient light reflections may be suppressed by forming antireflection coatings on one or more surfaces of the display layers. An antireflection coating may be formed by depositing alternating high and low index of refraction dielectric layers using a sputtering tool. A controller may control the operation of a spectrometer and the sputtering tool. To ensure that the antireflection coating exhibits a desired color, the controller may direct the sputtering tool or other equipment to deposit a subset of the dielectric layers for the antireflection coating. A spectrum may then be measured with the spectrometer. Based on the measured light spectrum, thickness adjustments or other adjustments may be made to remaining dielectric layers to ensure that the antireflection coating color matches a target color.



Published:

— *with international search report (Art. 21(3))*

Methods for Forming Antireflection Coatings for Displays

Background

[0001] This relates generally to electronic devices and, more particularly, to electronic devices with displays having antireflection coatings.

[0002] Electronic devices often include displays. For example, cellular telephones, computers, and televisions have displays.

[0003] Display performance can be adversely affected by ambient light reflections from the layers of glass in a display. For example, in an outdoors environment, images on a display can be obscured by excessive reflections from the surface of the display. To address this issue, displays are often provided with antireflection coatings. An antireflection coating may be formed by depositing layers of dielectric with alternating high and low indices of refraction onto a display surface.

[0004] Antireflection coatings often exhibit undesired color cast due to inaccuracies in the layer thicknesses of the deposited dielectric layers. This can lead to low yields when manufacturing displays with antireflection coatings.

[0005] It would therefore be desirable to be able to provide improved ways to form antireflection coatings on electronic device displays.

Summary

[0006] Ambient light reflections may be suppressed by forming an antireflection coating on one or more display layers in a display.

[0007] An antireflection coating may be formed by depositing alternating high index of refraction and low index of refraction dielectric layers using a sputtering tool. A controller may control the operation of a spectrometer and the sputtering tool.

[0008] To ensure that the antireflection coating exhibits a target color so that images may be displayed by the display without an undesired color cast, the controller may direct the sputtering tool or other equipment to deposit a subset of the dielectric layers for the antireflection coating. A spectrum may then be measured with the spectrometer. Based on the measured light spectrum from the subset of layers, thickness adjustments or other adjustments may be made when depositing remaining dielectric layers. The thickness adjustments help ensure that the antireflection coating color matches the target color.

Brief Description of the Drawings

[0009] FIG. 1 is a perspective view of an illustrative electronic device such as a laptop computer with a display having an antireflection coating in accordance with an embodiment.

[0010] FIG. 2 is a perspective view of an illustrative electronic device such as a handheld electronic device with a display having an antireflection coating in accordance with an embodiment.

[0011] FIG. 3 is a perspective view of an illustrative electronic device such as a tablet computer with a display having an antireflection coating in accordance with an embodiment.

[0012] FIG. 4 is a perspective view of an illustrative electronic device such as a display for a computer or television with a display having an antireflection coating in accordance with an embodiment.

[0013] FIG. 5 is a cross-sectional side view of an illustrative display having an antireflection coating in accordance with an embodiment.

[0014] FIG. 6 is a cross-sectional side view of an illustrative antireflection coating in accordance with an embodiment.

[0015] FIG. 7 is a graph of a reflection spectrum at visible light wavelengths for an illustrative antireflection coating in accordance with an embodiment.

[0016] FIG. 8 is a color space diagram showing the impact on display color from antireflection layer thickness variations in accordance with an embodiment.

[0017] FIG. 9 is a color space diagram showing the impact on display color of adjustments to two dielectric layer thicknesses at the top of an antireflection layer in accordance with an embodiment.

[0018] FIG. 10 is a diagram showing equipment that may be used in forming an antireflection layer in accordance with an embodiment.

[0019] FIG. 11 is a flow chart of illustrative steps involved in forming an antireflection layer by making dielectric layer thickness adjustments to one or more of the uppermost dielectric layers in the antireflection layer in accordance with an embodiment.

[0020] FIG. 12 is a flow chart of illustrative steps involved in forming an antireflection layer by making thickness adjustments to dielectric layers in the antireflection layer in accordance with an embodiment.

Detailed Description

[0021] Electronic devices may be provided with displays. The displays may be provided with antireflection layers to suppress light reflections.

[0022] Illustrative electronic devices of the types that may be provided with displays having antireflection layers are shown in FIGS. 1, 2, 3, and 4.

[0023] Electronic device 10 of FIG. 1 has the shape of a laptop computer and has upper housing 12A and lower housing 12B with components such as keyboard 16 and touchpad 18. Device 10 has hinge structures 20 (sometimes referred to as a clutch barrel) to allow upper housing 12A to rotate in directions 22 about rotational axis 24 relative to lower housing 12B. Display 14 is mounted in housing 12A. Upper housing 12A, which may sometimes be referred to as a display housing or lid, is placed in a closed position by rotating upper housing 12A towards lower housing 12B about rotational axis 24.

[0024] FIG. 2 shows an illustrative configuration for electronic device 10 based on a handheld device such as a cellular telephone, music player, gaming device, navigation unit, or other compact device. In this type of configuration for device 10, housing 12 has opposing front and rear surfaces. Display 14 is mounted on a front face of housing 12. Display 14 may have an exterior layer that includes openings for components such as button 26 and speaker port 28.

[0025] In the example of FIG. 3, electronic device 10 is a tablet computer. In electronic device 10 of FIG. 3, device 10 has opposing planar front and rear surfaces. Display 14 is mounted on the front surface of device 10. As shown in FIG. 3, display 14 may have an opening to accommodate button 26.

[0026] FIG. 4 shows an illustrative configuration for electronic device 10 in which device 10 is a computer display, a computer that has an integrated computer display, or a television. Display 14 is mounted on a front face of device 10. With this type of arrangement, housing 12 for device 10 may be mounted on a wall or may have an optional structure such as support stand 30 to support device 10 on a flat surface such as a tabletop or desk.

[0027] Display 14 may be a liquid crystal display, an organic light-emitting diode display, a plasma display, an electrophoretic display, an electrowetting display, a display using other types of display technology, or a display that includes display structures formed using more than one of these display technologies.

[0028] A cross-sectional side view of an illustrative display is shown in FIG. 5. As shown

in FIG. 5, display 14 may have display layers such as display layers 32. The types of layers that are included in display layers 32 depend on the type of technology used in forming display 14. If, for example, display 14 is a liquid crystal display, layers 32 may include a backlight, upper and lower polarizers, and a color filter layer, liquid crystal layer, and thin-film transistor layer interposed between the upper and lower polarizers. In configurations in which display 14 is an organic light-emitting diode display, layers 32 may include layers such as a substrate layer on which an array of light-emitting diodes and thin-film transistor circuitry is formed.

[0029] Display 14 may include an optional cover layer such as display cover layer 34. Display cover layer 34 may overlap other layers in display 14 such as display layers 32 and may help to protect display layers 32 during use of display 14 and device 10. Display cover layer 34 may be formed from a sheet of clear plastic, a transparent glass layer, a layer of ceramic, or other transparent layer.

[0030] Display 14 may have one or more antireflection coatings. For example, display 14 may have an antireflection layer such as layer 36. Layer 36 may be formed on the surface of a display substrate in display 14. For example, layer 36 may be formed on the upper surface of display cover layer 34 or on one or more other display layer surfaces (e.g., one or more of the surfaces of display layers 32). If desired, cover layer 34 may be omitted and a color filter layer or other layer in display layers 32 may serve as the outermost layer of display 14 and may be coated with layer 36. Configurations for display 14 in which antireflection layer 36 is formed on the outermost layer for display 14 such as illustrative display cover layer 34 of FIG. 5 are sometimes described herein as an example. This is, however, merely illustrative. Antireflection layer 36 may be formed on any suitable surface of the layers in display 14.

[0031] FIG. 6 is a cross-sectional side view of an illustrative antireflection coating on display layer 64 (e.g., layer 34, etc.). As shown in FIG. 6, antireflection layer 36 may have multiple layers 36L of dielectric such as dielectric layers L1, L2, L3, L4, L5, L6, L7, L8, and L9 having respective thicknesses T1, T2, T3, T4, T5, T6, T7, T8, and T9. Dielectric layers 36L may have alternating high and low indices of refraction. Any suitable dielectric materials may be used in forming layers 36L. As an example, layers 36L may be formed from dielectrics such as silicon nitride (having an index of refraction of 1.75) and silicon oxide (having an index of refraction of 1.45). The silicon nitride layers in this illustrative configuration form “high” index of refraction layers that alternate with “low” index of

refraction layers formed from silicon oxide. In the arrangement of FIG. 6, for example, layers L1, L3, L5, L7, and L9 may be formed from silicon oxide and layers L2, L4, L6, and L8 may be formed from silicon nitride. Other types of dielectric may be used in forming a high-low dielectric stack or other dielectric layers for an antireflection coating, if desired. The use of alternating silicon nitride and silicon oxide layers to form antireflection coating 36 of FIG. 6 is merely illustrative.

[0032] FIG. 7 is a graph of a reflection spectrum (reflectance R plotted as a function of light wavelength) for an illustrative antireflection layer such as layer 36 of FIG. 6. In the example of FIG. 7, reflections have been suppressed over the visible wavelengths ranging from 380 nm to 780 nm).

[0033] Using an antireflection coating computer model, desired thicknesses can be computed for the dielectric layers 36L of antireflection layer 36. These thickness values can be used as nominal values in depositing dielectric to form antireflection layer 36. Due to manufacturing variations, the actual thicknesses of the deposited layers 36L may deviate slightly from their nominal thicknesses. These thickness variations impact the color cast of antireflection layer 36 and therefore display 14.

[0034] Consider, as an example, a display having an antireflection layer such as layer 36 of FIG. 6. In general, layer 36 may have five or more dielectric layers, seven or more dielectric layers, more than eight dielectric layers, or other suitable numbers of dielectric layers. In the example of FIG. 6, antireflection layer 36 has nine dielectric layers of varying thicknesses. FIG. 8 is a color space diagram of a display coated with an antireflection layer such as antireflection layer 36 of FIG. 6. The graph of FIG. 8 depicts the Lab color space and represents colors using color coordinates a^* and b^* . The desired ("target") color for layer 36 and display 14 in the example of FIG. 8 is represented by target color TG. This color may be selected by a display designer to avoid undesired strong color casts for display 14.

[0035] If it were possible to manufacture layers 36L exactly as desired (i.e., with indices of refraction and thicknesses that do not vary from their desired values), display 14 and layer 36 would be characterized by desired target color TG. In real world situations, however, unavoidable manufacturing variations are present that can cause layers 36L to deviate somewhat from their intended characteristics. As an example, thickness variations in each layer 36L may result in changes in color, as indicated in lines L1 ... L9 in the graph of FIG. 8. As one example, if layer L2 is deposited with a thickness that is 3% less than intended, the

resulting color of layer 36 and display 14 will be represented by point 38 rather than target color point TG, whereas deposition of layer L2 with a thickness that is 3% more than intended will cause layer 36 and display 14 to exhibit the color represented by point 40 in the graph of FIG. 8. Variations in the thicknesses of other layers 36L may also cause the color of layer 36 and display 14 to vary from target color TG.

[0036] To overcome these manufacturing variations, one or more spectral measurements may be used during the process of depositing layers 36L. Corrective adjustments can then be made during dielectric deposition operations to ensure satisfactory antireflection layer performance. With one suitable arrangement, layer thickness adjustments are made to the upper two dielectric layers 36L of antireflection coating 36 after depositing a subset of layers 36L (e.g., after depositing five or more layers 36L, after depositing seven or more layers 36L, after depositing more than seven layers 36L or after depositing fewer than seven layers 36L, etc.). With another suitable arrangement, the thicknesses of one, two, or more than two of layers 36L other than just the upper two layers are adjusted during deposition.

[0037] FIG. 9 is a Lab color space diagram showing how adjustments to the thicknesses T8 and T9 of the uppermost (outermost) two dielectric layers 36L of antireflection layer 36 may be made to ensure that the color of layer 36 is accurately matched to a desired, target color TG. With the arrangement of FIG. 9, layers L1...L7 are initially deposited. A spectrum is then taken to measure the color of the partially formed antireflection layer 36. Real world manufacturing variations will cause the color of display 14 to vary from the color expected when forming layers L1...L7 exactly with their nominal thicknesses. As a result of these variations in layers L1...L7, the computed color to be produced by a completed stack for antireflection coating 36 will deviate from target color TG if nominal thicknesses T8 and T9 are to be used for forming layers L8 and L9. The impact of the manufacturing variations in layers L1...L7 can be computed based on the spectrum measured from layers L1...L7. As an example, the measured spectrum data may be used as an input to the antireflection layer model to predict that antireflection layer 36 and display 14 will, once completed, have a color represented by point 42 on the color space graph of FIG. 9 if layers L8 and L9 are deposited with their nominal thicknesses as originally planned.

[0038] To determine appropriate thicknesses to use for layers L8 and L9, the antireflection layer model may predict the color that will be associated with layer 36. In particular, the antireflection coating model can be used to compute the final color for layer 36 that will be

produced after the L8 and L9 layers are deposited based on the measured spectrum and using a variety of different potential thicknesses of layers L8 and L9 as inputs. This modeling process may be used to identify thickness adjustments $\Delta T8$ and $\Delta T9$ to be used when depositing the last two layers of antireflection layer 36 to ensure that the final color does not deviate from the target color TG. Thickness adjustment $\Delta T8$ represents a computed deviation from nominal thickness T8 of layer L8 that can be used to change the color of layer 36 from point 42 to point 44. Thickness adjustment $\Delta T9$ represents a computed deviation from nominal thickness T9 of layer L9 that can be used to adjust the color of layer 36 from point 44 to target color TG. Because the values of $\Delta T8$ and $\Delta T9$ are computed before layers L8 and L9 are deposited (in this example), the thicknesses of layers L8 and L9 can be deposited in a way that ensures that the final color of display 14 matches target color TG. If desired, more layers of antireflection coating 36 can be deposited with adjusted thicknesses (e.g., three or more layers can have thicknesses that are modified from their nominal values). The example of FIG. 9 is merely illustrative.

[0039] FIG. 10 is a system diagram showing illustrative equipment that may be used in depositing antireflection layer 36. As shown in FIG. 10, deposition system 46 may have a coating source such as source 58 for depositing layers of dielectric on surface 62 of substrate 64. Substrate 64 may be a display layer such as a display cover layer 34 or other display layer 32 for display 14. Coating source 58 may be a sputtering tool or other equipment for depositing dielectric layers such as silicon nitride layers, silicon oxide layers, or other dielectric layers 36L for antireflection layer 36 on surface 62.

[0040] At one or more times during the process of depositing layer 36 on substrate 64, a spectrum (e.g., a reflection spectrum for a range of wavelengths such as visible light wavelengths) may be gathered to characterize the color of the deposited layers on substrate 64. For example, light source 48 may emit light 50 that is reflected from surface 62 of substrate 64 as reflected light 52 and controller 56 may direct spectrometer 54 to measure the amount of reflected light 52 at each wavelength within a range of wavelengths such as the visible light wavelengths of the illustrative spectrum of FIG. 7. Light source 48 may be, for example, a white light source that produces white light 50. Spectrometer 54 may have a tunable band pass filter. Controller 56 may adjust the tunable filter to sweep the band pass filter across all of the wavelengths of the graph of FIG. 7 or an appropriate subset of these wavelengths.

[0041] Once controller 56 has gathered a spectrum, controller 56 can process the gathered spectral data for the materials deposited on substrate 64 to determine what corrective actions should be taken during subsequent deposition operations. As an example, controller 56 can implement a model for a nine layer antireflection layer (or an antireflection layer with a different number of layers 36L). Based on measured spectral data, controller 56 can use the antireflection layer model to compute desired adjusted thicknesses for some of the layers of antireflection layer 36. Using an approach of the type shown in FIG. 9, for example, controller 56 can determine new optimum thickness to use when depositing layers L8 and L9 from coating source 58. Controller 56 can then direct coating source 58 to deposit layers L8 and L9 with appropriate adjusted thicknesses.

[0042] In general, controller 56 may use spectral data to determine how to adjust the sputtering settings being used by sputtering tool 58 when depositing sputtered dielectric 60 onto surface 62 of substrate 64. The settings may be adjusted to adjust the index of refraction of the deposited material and/or the thickness of the deposited material. Configurations in which thickness adjustments are made are sometimes described herein as an example, but in general, index of refraction adjustments, thickness adjustments, and/or other deposition parameter adjustments may be made by controlling source 58 with controller 56.

[0043] Illustrative steps involved in forming antireflection layer 36 using an arrangement of the type described in connection with FIG. 9 are shown in FIG. 11.

[0044] At step 66, an initial set of layers 36L for antireflection layer 36 are deposited on substrate 64. The number of layers 36L that are deposited at step 66 is less than the total number of layers 36L for antireflection layer 36. For example, in a nine-layer antireflection layer design, a subset of the nine layers such as the first seven layers 36L may be deposited at step 66, leaving two remaining upper layers (i.e., layers L7 and L8) to be deposited later. The layers 36L that are deposited during the operations of step 66 may be deposited by using controller 56 to direct coating source 58 to deposit each of these layers with its nominal thickness, as computed using an antireflection layer model.

[0045] At step 68, after layers L1...L7 have been deposited, controller 56 may use light source 48 and spectrometer 54 to gather spectral measurements on light reflected from the deposited layers. For example, spectrometer 54 may gather a visible light reflection spectrum for the deposited layers.

[0046] Due to manufacturing variations, the actual values of the thicknesses of the

deposited layers will generally vary somewhat from their desired nominal thicknesses. The actual deposited thicknesses of the layers deposited during step 66 (i.e., the thicknesses of the first seven layers 36L) may be determined by using iterative techniques to vary each of the layer thicknesses in the antireflection layer model until the modeled spectrum matches the spectrum measured at step 68.

[0047] At step 72, the antireflection layer model may use the actual deposited thicknesses of the first seven layers 36L and information on the desired target color TG to compute appropriate adjusted values to use for the thicknesses T8 and T9 of layers L8 and L9, respectively. Due to the manufacturing variations present when depositing the first seven layers 36L, the values of T8 and T9 will deviate slightly from the nominal values for T8 and T9 that would have been computed when modeling the antireflection layer before any deposition operations had taken place. The adjusted values of T8 and T9 can then be used to deposit the last two layers (L8 and L9 in this example), at step 74. Because the adjustments to thicknesses T8 and T9 compensate for the manufacturing variations present during the formation of layers L1-L7, antireflection layer 36 will have a color that matches target color TG. This can be confirmed by gathering a spectrum of layer 36 and performing pass-fail testing (step 76). If the color of layer 36 is not as desired, display 14 can be scrapped. Otherwise layer 36 will pass testing and can be used in display 14 of electronic device 10.

[0048] If desired, spectral measurements can be made at other times during the process of fabricating layer 36. For example, it is not necessary to make only a single spectral measurement. A first spectral measurement may be made, for example, before depositing layer L8 and a second spectral measurement may be made before depositing layer L9. The first spectral measurement may be used to adjust the thickness value for T8 and the second spectral measurement may be used to tune the value of thickness T9. If desired, three or more spectral measurements may be made followed by three or more respective layer thickness adjustments or other deposition parameter adjustments. Spectral data may also be acquired partway through the process of depositing a layer 36L. As an example, spectral data may be acquired at one or more points partway through the deposition of layer L9 and this spectral data used in adjusting in real time the thickness of layer L9. A flow chart of illustrative steps involved in forming layer 36 using techniques such as these is shown in FIG. 12.

[0049] As shown in FIG. 12, one or more full or partial layers 36L for antireflection layer

36 may be deposited at step 78 using coating source 58 (FIG. 10).

[0050] At step 80, controller may use spectrometer 54 to measure a reflected light spectrum from surface 62 of substrate 64, and characterize the color of the deposited dielectric material.

[0051] Using the antireflection layer model implemented on controller 56, controller 56 may, at step 82, compute the thickness(es) of deposited layer(s) 36 at step 82 and may determine what corrective actions should be taken (e.g., thickness adjustments for subsequently deposited layers, etc.). As indicated by line 84, operation may then loop back to step 78 during which the layer thickness adjustments and other corrective actions identified during step 82 can be taken into account when depositing one or more additional full or partial layers of dielectric material. The operations of FIG. 12 can be performed continuously, until layer 36 has been fully formed. Because of the real time adjustments made during the process of depositing the layers 36L for antireflection layer 36, the color exhibited by layer 36 will match desired target color TG.

[0052] The foregoing is merely illustrative and various modifications can be made by those skilled in the art without departing from the scope and spirit of the described embodiments. The foregoing embodiments may be implemented individually or in any combination.

Claims

What is Claimed is:

1. A method for forming an antireflection coating on a surface of a display layer, comprising:
 - depositing dielectric layers for the antireflection coating on the surface of the display layer;
 - measuring a light spectrum for light reflected from the deposited dielectric layers; and
 - determining at least one dielectric layer thickness adjustment to make for at least one additional dielectric layer for the antireflection coating based at least partly on the measured light spectrum.
2. The method defined in claim 1 further comprising:
 - depositing the at least one dielectric layer to a thickness that has been adjusted based on the dielectric layer thickness adjustment.
3. The method defined in claim 2 wherein depositing the dielectric layers comprises depositing alternating high and low index of refraction dielectric layers.
4. The method defined in claim 3 wherein depositing the dielectric layers comprises depositing at least seven dielectric layers.
5. The method defined in claim 4 wherein depositing the at least one dielectric layer comprises depositing an eighth dielectric layer on top of the seven dielectric layers.
6. A method of forming an antireflection coating on a surface of a display substrate, wherein the antireflection coating includes a plurality of dielectric layers, the method comprising:
 - depositing a subset of the plurality of dielectric layers for the antireflection coating on the surface of the display substrate;
 - measuring a light spectrum for light reflected from the deposited subset

of the plurality of dielectric layers; and

depositing two remaining dielectric layers for the antireflection coating on top of the deposited subset of the plurality of dielectric layers.

7. The method defined in claim 6 wherein depositing the two remaining dielectric layers comprises depositing the two remaining layers with thicknesses adjusted based on the measured light spectrum.

8. The method defined in claim 6 wherein depositing the subset of the plurality of dielectric layers comprises depositing alternating high and low index of refraction dielectric layers.

9. The method defined in claim 6 wherein the display substrate comprises an outermost display layer in an electronic device display and wherein depositing the subset of the plurality of dielectric layers comprises depositing dielectric with a sputtering tool.

10. The method defined in claim 9 wherein the outermost display layer comprises a display cover layer and wherein depositing the subset of the plurality of dielectric layers comprises depositing at least one silicon oxide layer.

11. The method defined in claim 9 wherein depositing the subset of the plurality of dielectric layers comprises depositing silicon oxide layers and silicon nitride layers.

12. The method defined in claim 7 wherein depositing the subset of the plurality of dielectric layers comprises depositing at least five dielectric layers.

13. The method defined in claim 7 wherein depositing the subset of the plurality of layers comprises depositing seven dielectric layers and wherein depositing the two remaining dielectric layers comprises depositing eighth and ninth dielectric layers on top of the seven dielectric layers.

14. The method defined in claim 7 wherein measuring the light spectrum comprises measuring a visible light spectrum.
15. The method defined in claim 7 wherein depositing the two remaining dielectric layers comprises depositing the two remaining layers with respective first and second thicknesses adjusted to ensure that the antireflection coating exhibits a color that matches a target color.
16. The method defined in claim 15 wherein depositing the subset of the plurality of dielectric layers comprises depositing alternating high and low index of refraction dielectric layers.
17. Apparatus for forming an antireflection coating on a surface of a substrate, comprising:
- a coating source that deposits dielectric layers for the antireflection coating on the surface of the substrate;
 - a spectrometer that acquires a light spectrum from light reflected from the dielectric layers on surface of the substrate; and
 - a controller configured to adjust deposition parameters associated with depositing the dielectric layer for the antireflection coating from the coating source onto the surface of the substrate based at least partly on the light spectrum.
18. The apparatus defined in claim 17 wherein the coating source comprises a sputtering tool controlled by the controller.
19. The apparatus defined in claim 18 wherein the sputtering tool is configured to deposit the dielectric layers with alternating high and low indices of refraction when depositing the dielectric layers for the antireflection coating and wherein the controller is configured to adjust a layer thickness of at least one of the dielectric layers based on the light spectrum.
20. The apparatus defined in claim 18 wherein the sputtering tool is

configured to deposit dielectric layers with alternating high and low indices of refraction when depositing the dielectric layers for the antireflection coating and wherein the controller is configured to adjust layer thicknesses of a top two of the dielectric layers based on the light spectrum.

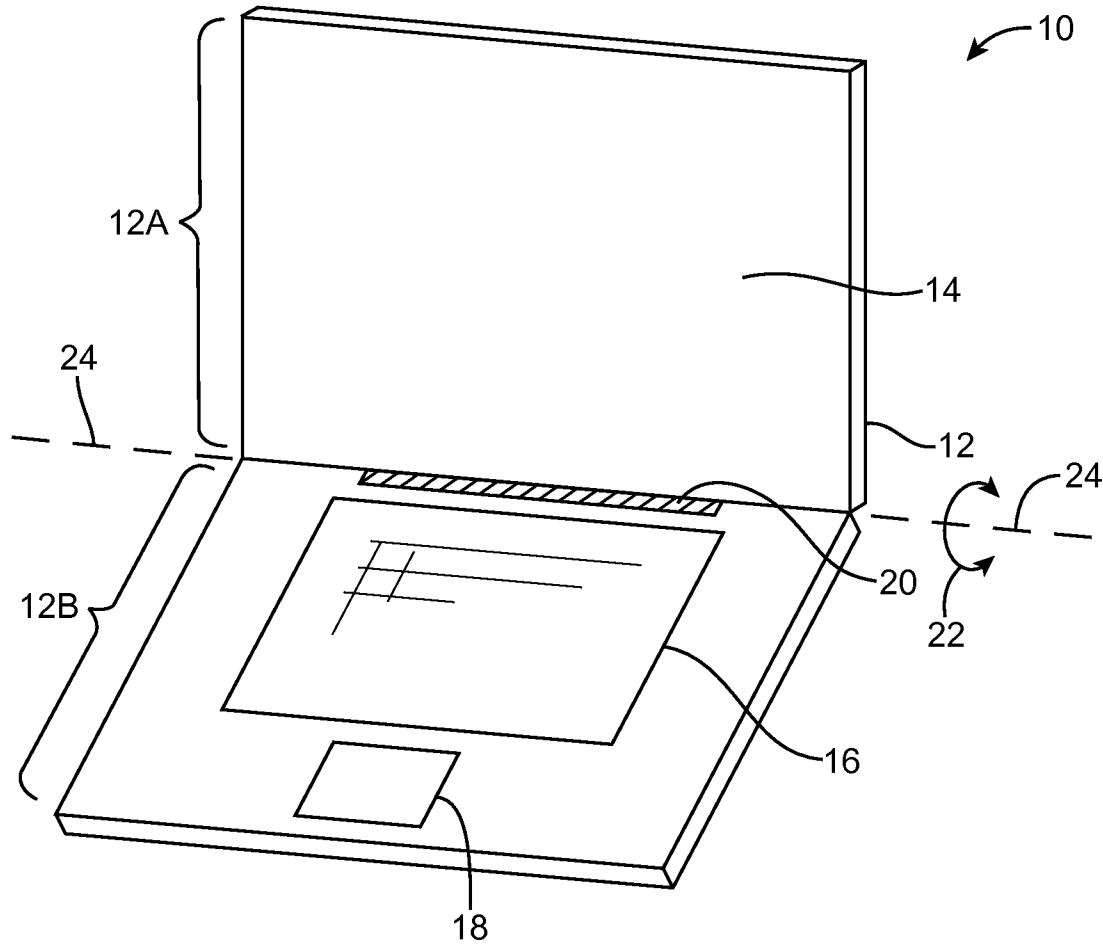


FIG. 1

2 / 11

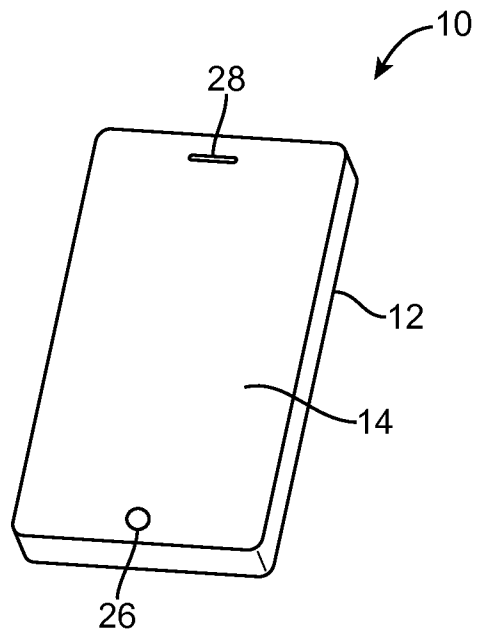


FIG. 2

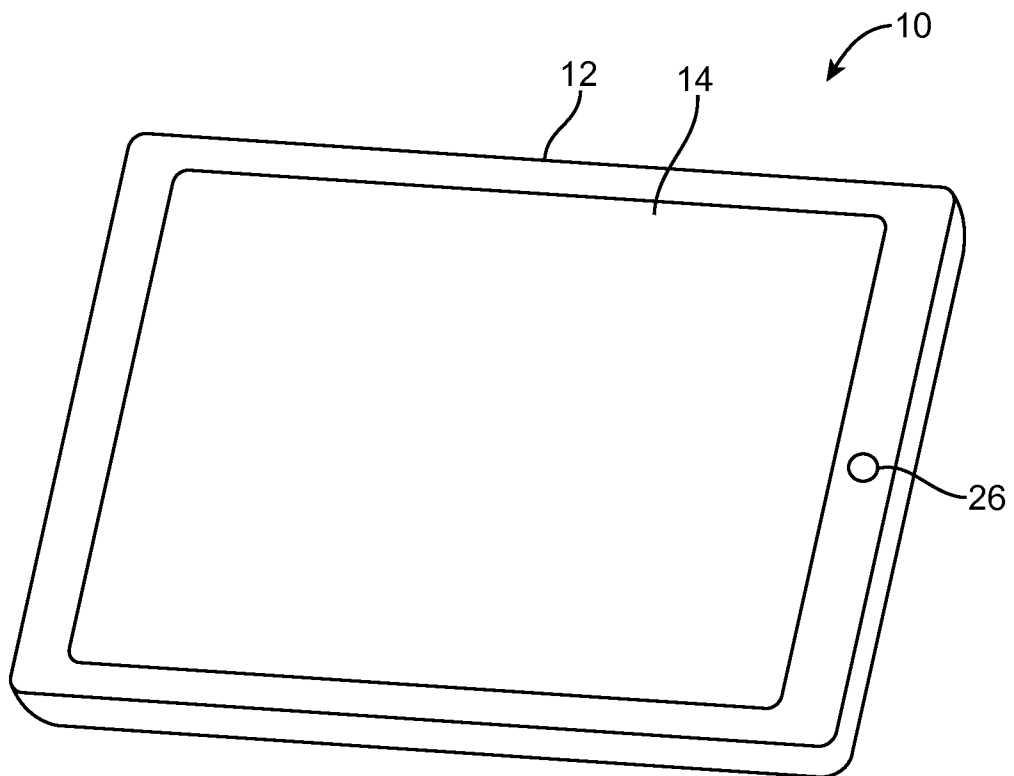


FIG. 3

3 / 11

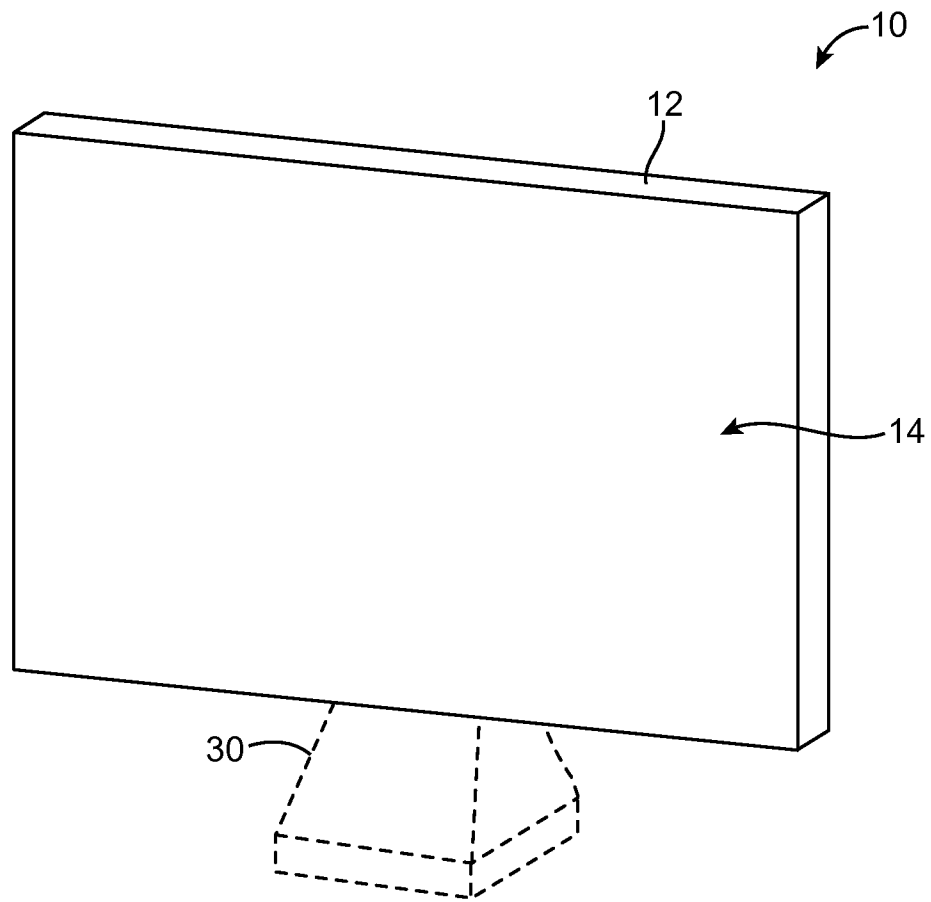


FIG. 4

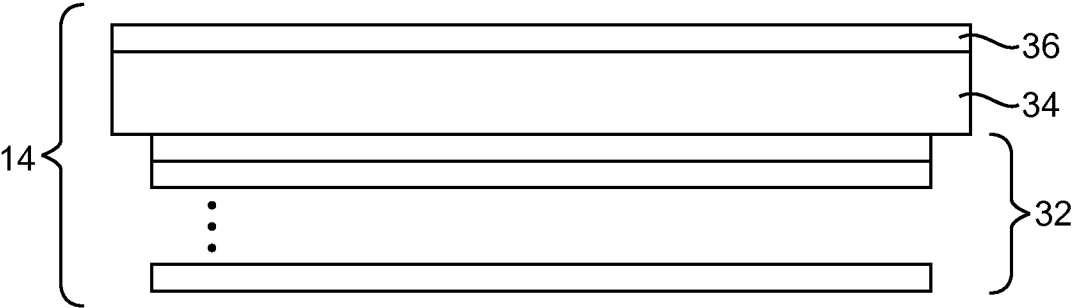


FIG. 5

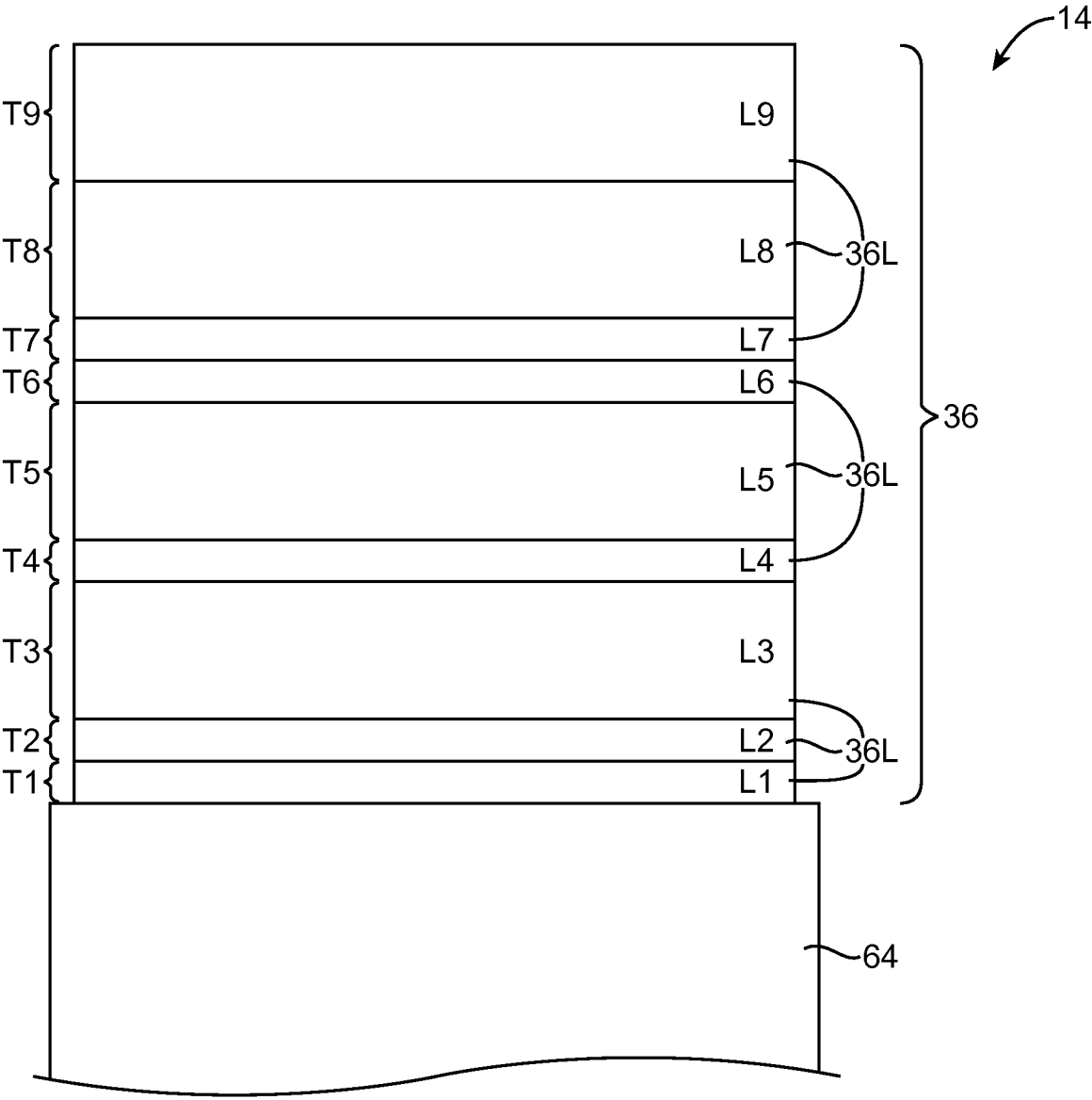


FIG. 6

6 / 11

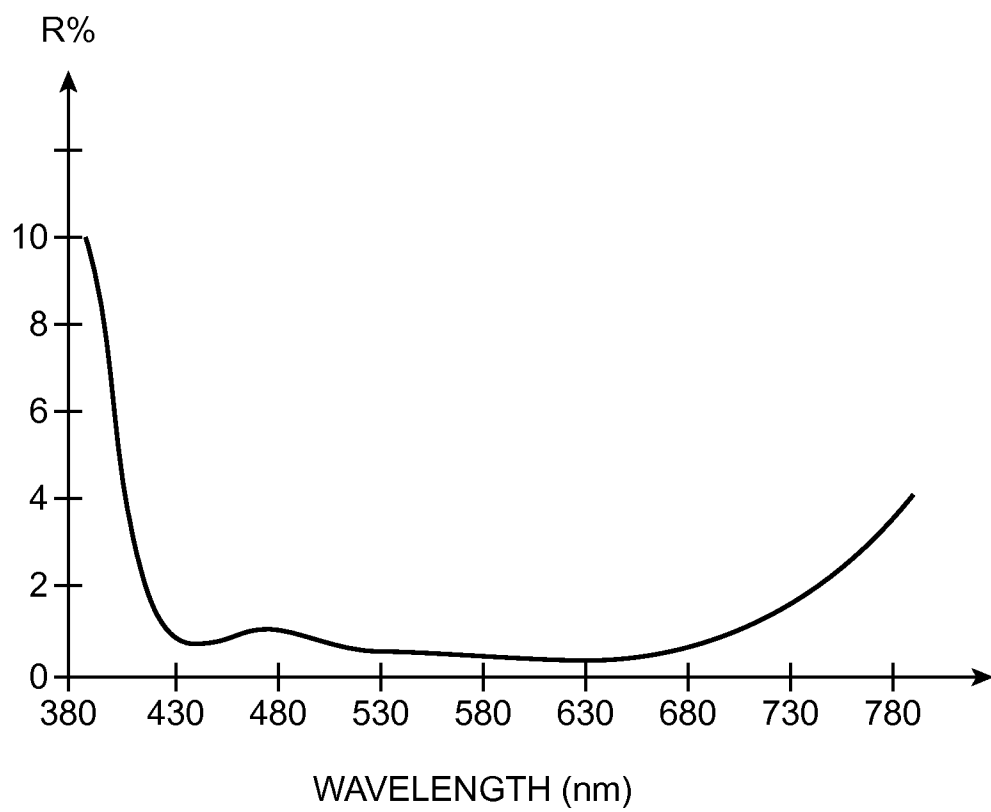


FIG. 7

7 / 11

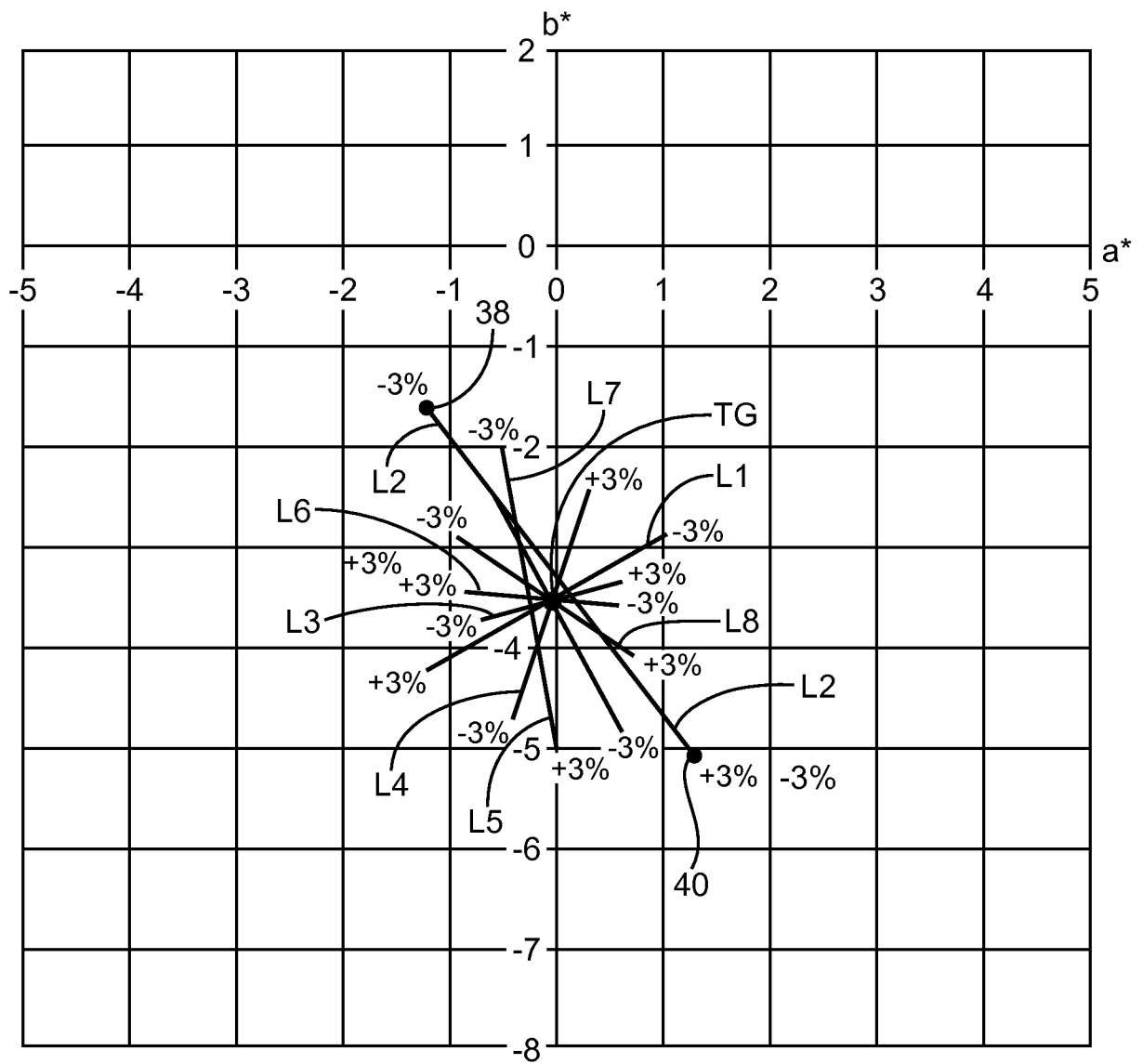


FIG. 8

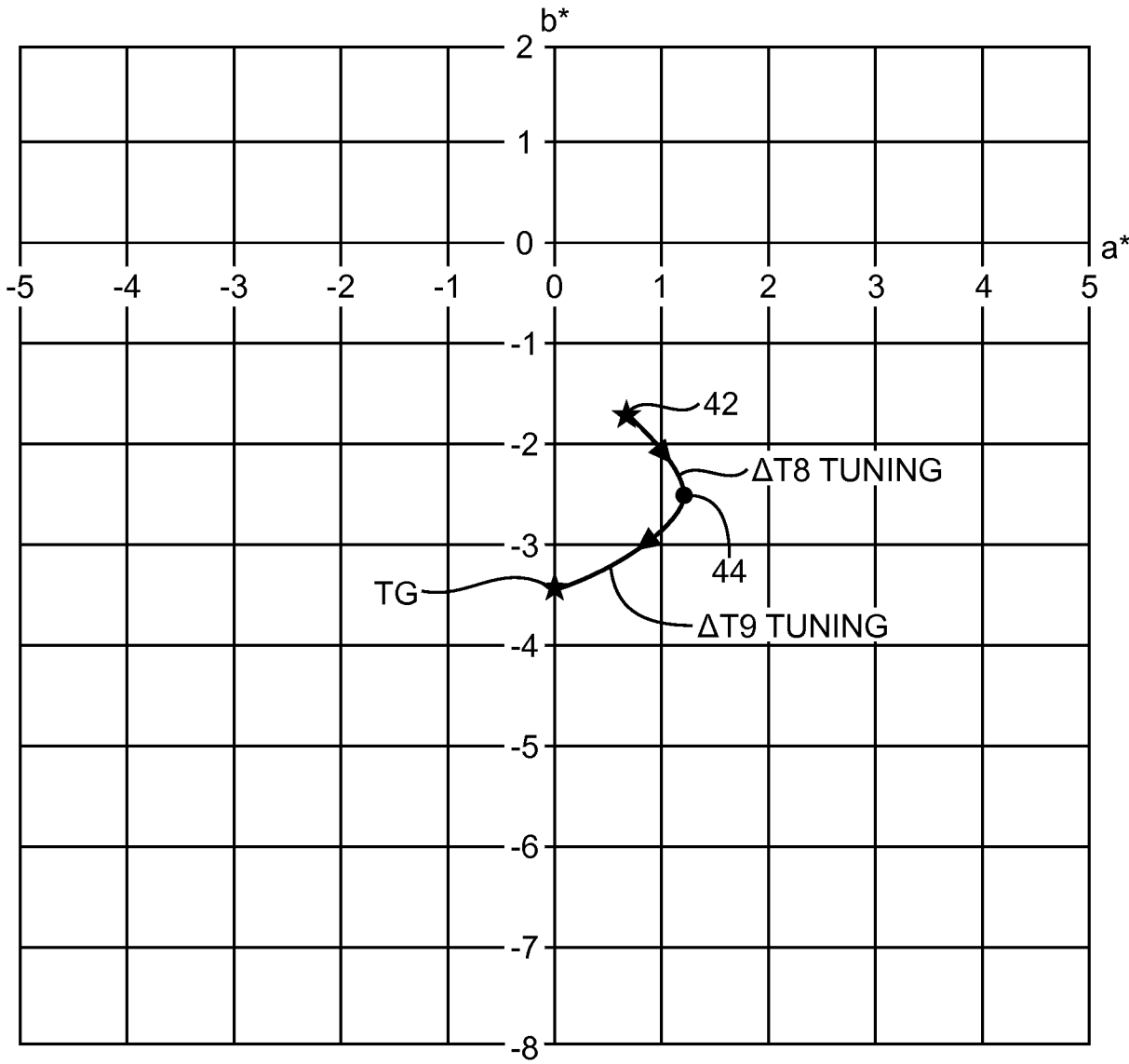


FIG. 9

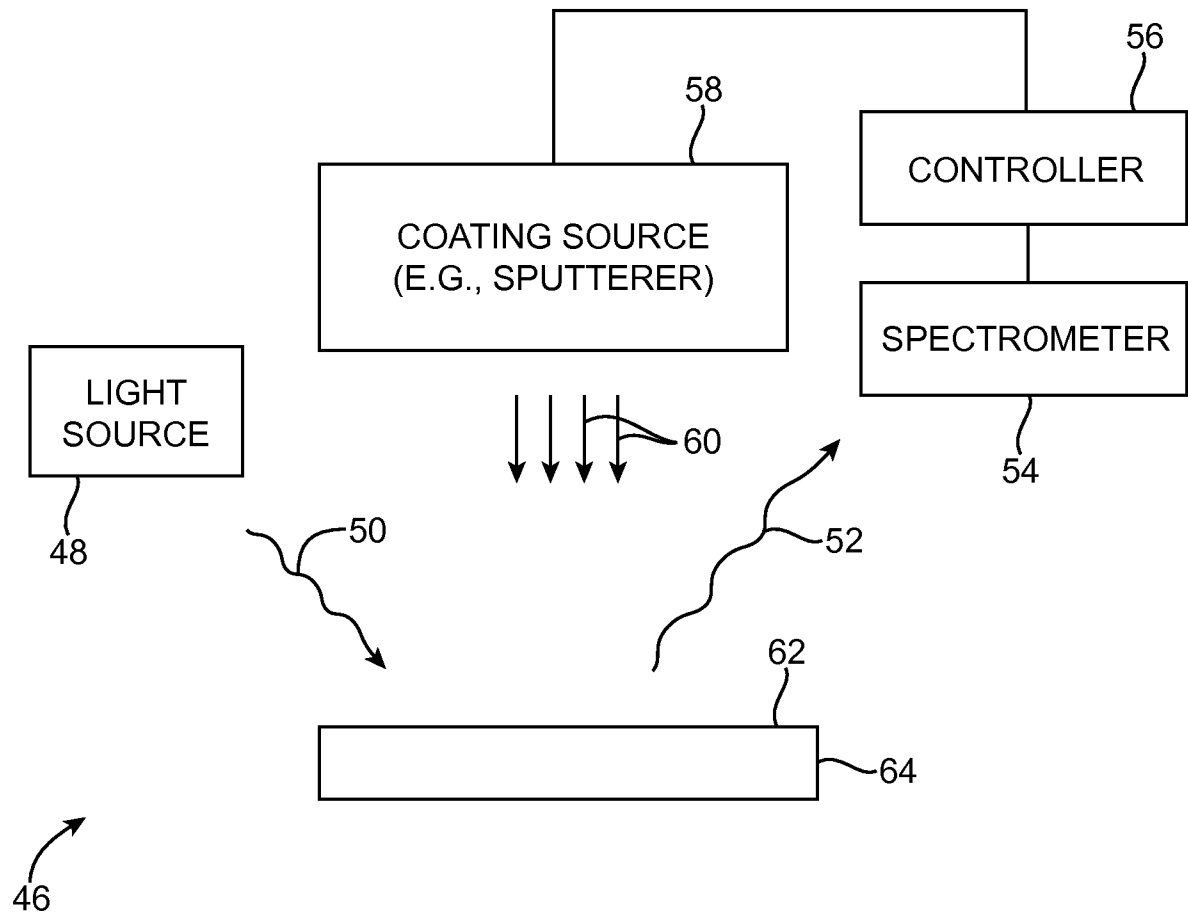


FIG. 10

10 / 11

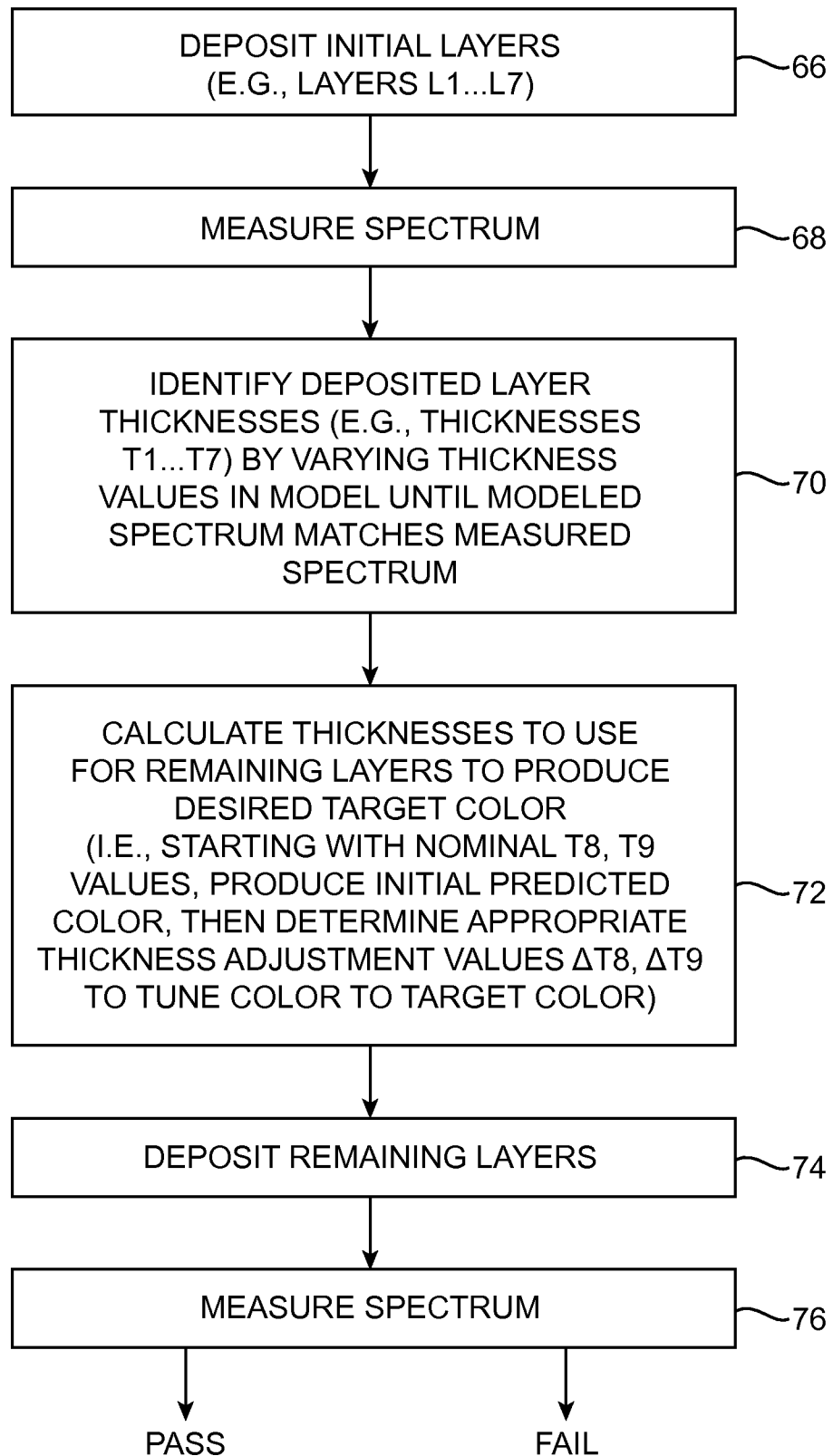


FIG. 11

11 / 11

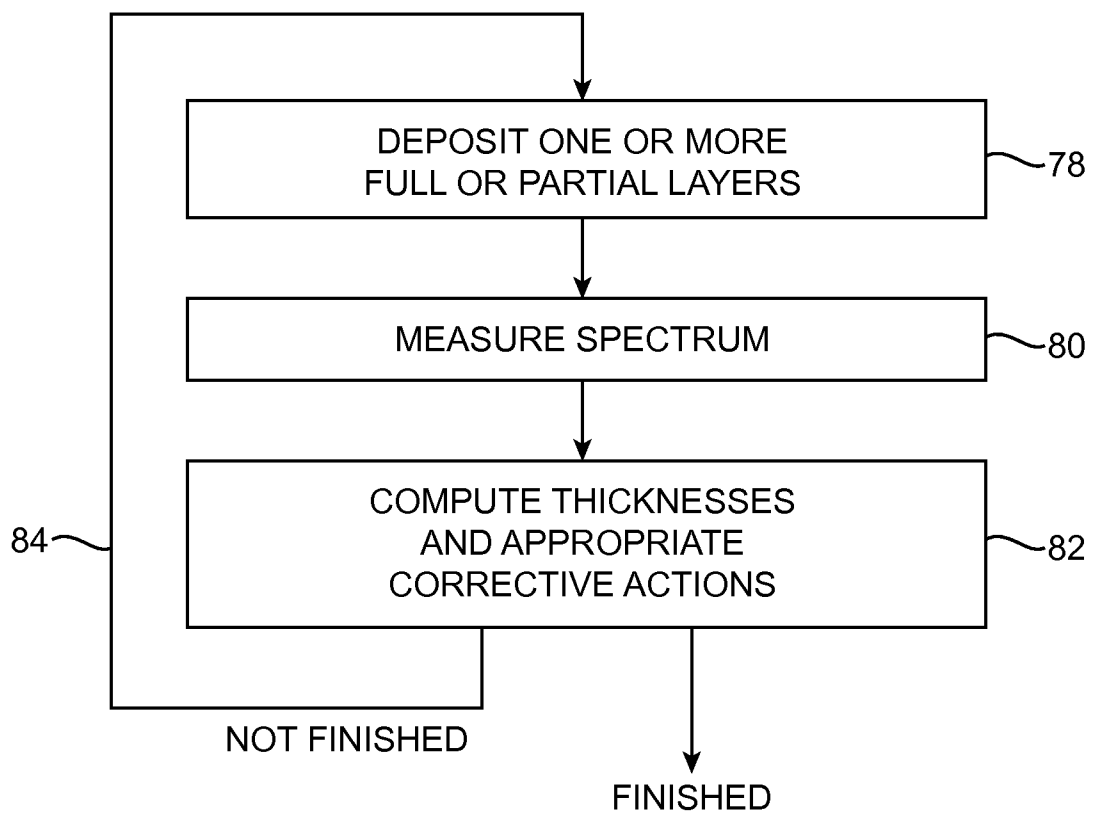


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2014/016404

A. CLASSIFICATION OF SUBJECT MATTER

INV. G02B1/11 B29D11/00 C09D5/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G02B B29D C09D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 356 523 A (LIBBERT BARBARA A) 5 December 1967 (1967-12-05) the whole document	1-20
X	US 2003/211755 A1 (LU ZHI-CHERNG [TW] ET AL) 13 November 2003 (2003-11-13) the whole document	1-20
A	EP 2 149 540 A1 (SEIKO EPSON CORP [JP]) 3 February 2010 (2010-02-03) paragraph [0002] - paragraph [0003] paragraph [0035] - paragraph [0140]	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

2 October 2014

Date of mailing of the international search report

13/10/2014

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Szachowicz, Marta

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2014/016404

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 3356523	A	05-12-1967	NONE
US 2003211755	A1	13-11-2003	NONE
EP 2149540	A1	03-02-2010	CN 101639663 A 03-02-2010
			CN 103011618 A 03-04-2013
			EP 2149540 A1 03-02-2010
			JP 5326407 B2 30-10-2013
			JP 2010037115 A 18-02-2010
			US 2010027383 A1 04-02-2010
			US 2013260115 A1 03-10-2013