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(54) Title:  
OFF-MEMORY-MODULE ECC-SUPPLEMENTAL MEMORY SYSTEM

(ECC MEMORY SYSTEM 100)  

OFF-MEMORY-MODULE ECC-SUPPLEMENTAL (OMMES) MEMORY 104  

(NON-ECC) MEMORY MODULE SET 106  

FIG. 1

(57) Abstract:  
A system includes off-memory-module ECC-supplemental memory. In a process, an ECC-capable memory controller converts non-ECC data words to ECC data words and distributes each ECC data word between a non-ECC memory module set (of one or more non-ECC memory modules) and the ECC-supplemental memory. A host computer system can include a baseboard on which are mounted an ECC-capable memory controller, off-memory-module ECC-supplemental memory, and sockets for installing non-ECC memory modules.
Declarations under Rule 4.17:

— as to the identity of the inventor (Rule 4.17(i))

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OFF-MEMORY-MODULE ECC-SUPPLEMENTAL MEMORY SYSTEM

[01] BACKGROUND

[02] High-availability computing can avoid downtime due to inevitable data errors by using error-correcting code (ECC) memory systems. Error-correcting codes such as Hamming code or triple modular redundancy (TMR) employ redundancy to allow the most common data errors to be detected and corrected. To accommodate the redundancy, ECC memory modules typically provide nine bytes of storage (9 x 8 = 72 bits) for each eight bytes of data (64 bits) in a memory rank. Like non-ECC memory, memory can be provided in memory modules (e.g., SIMMs and DIMMs) to be installed on a baseboard. The actual error detection and correction is performed by an ECC-capable memory controller, which is typically on the baseboard. "ECC on SIMMs" (EOS) memory, which have controllers on the memory modules, can be used for systems without built-in ECC support.

[03] BRIEF DESCRIPTION OF THE DRAWINGS

[04] The following figures represent examples and not the invention itself.

[05] FIGURE 1 is a schematic diagram of an ECC memory system in accordance with an example.

[06] FIGURE 2 is a flow chart of an ECC memory process in accordance with an example.
[07] FIGURE 3 is a schematic diagram of a computer system hosting an ECC memory system.

[08] FIGURE 4 is a flow chart of an ECC memory process that can be implemented on the ECC memory system of FIG. 3 in accordance with an example.

[09] DETAILED DESCRIPTION

[10] ECC memory modules can be expensive relative to non-ECC memory not only due to the extra capacity required for the redundant ECC codes, but also due to the economies of scale that favor the more widely used non-ECC memory modules. Thus, while capacity considerations alone would yield an about 12% premium for ECC memory modules, the actual premium can be up to 100% due largely to economies of scale. The premium for an EOS memory is even greater due to the incorporation of an ECC controller on each EOS memory module.

[11] An ECC system 100 addresses the cost considerations associated with ECC memory modules by providing the extra capacity required by ECC encoded data words using off-memory-module ECC-supplemental (OMMES) memory. Thus, the cost-savings due to the economies of scale associated with non-ECC memory modules can be achieved in ECC-capable systems.

[12] ECC system 100 includes an ECC-capable memory controller 102, OMMES memory 104, and a non-ECC memory module set 106. Herein, "non-ECC memory module set" refers to a set of one or more non-ECC memory modules. Those skilled in the art can readily differentiate ECC memory modules from non-ECC modules.
[13] As is well known, computers typically store and communicate data as physical (e.g., electrical, magnetic, or optical) encodings of strings of zeroes and ones. One binary value can represent one "bit" of data. These bits are typically arranged in "data words" in the form of strings of binary values; the data words are typically a power of two bits long, e.g., 64 bits long. Eight bits is often referred to as a "byte", so a 64-bit data word can also be characterized as an 8-byte data word.

[14] Rather than store an entire data word on a single memory device, segments of a data word can be distributed among plural memory devices so that the segments can be accessed in parallel. Herein, "memory device" refers to a monolithic integrated circuit designed primarily to store data; typically, memory devices are SDRAM (synchronous dynamic random access memory). Thus, in a non-ECC memory, an 8-byte data word can be distributed among eight x8, four x16, or sixteen x4 memory devices. The devices among which a word is distributed are referred to collectively as a "rank". Thus, a typical non-ECC dual-inline memory module (DIMM) can include two ranks of eight integrated circuit memories on a printed-circuit board (PCB).

[15] ECC encoding typically adds eight bits per eight bytes so that a 64-bit (8-byte) word consumes 72 bits (nine bytes) in ECC encoded form. Thus, instead of being distributed over eight memory devices, an ECC encoded word is distributed over nine integrated circuit memories. Thus, a typical ECC memory module (e.g., DIMM) includes nine memory devices, and a typical dual-rank ECC DIMM includes 18 integrated circuit memories. Other configurations are known as well. Generally, non-ECC memory modules have an integer multiple of eight integrated circuit memories,
while ECC memory modules can have one additional memory device per rank to handle the excess capacity required by ECC encoding.

[16] In the case of an EOS memory module, both the ECC controller and the ECC excess capacity are provided on the memory module(s). In the case of a conventional (non-EOS) ECC memory module, the controller is off-module, e.g., on a baseboard, but the excess capacity is provided on the module. In the case of ECC memory system 100, both ECC-capable memory controller 102 and OMMES memory 104 that provides the excess capacity are off module, that is, not on a conventional memory module. This allows ECC functionality (hardening against errors in stored data) using conventional non-ECC memory modules.

[17] In a controller-implemented process 200, flow-charted in Fig. 2, data words are ECC encoded at 201. For example, the ECC encoding can use Hamming encoding or TMR encoding. The resulting ECC-encoded data words are stored in a distributed manner between non-ECC memory modules and OMMES memory at 202.

[18] "Off-module", as used herein, can be understood in the context of computer 300, shown schematically in Fig. 3. Computer 300 includes a baseboard 302 on which are mounted a processor 304, communications devices 306, an ECC controller 308, and off-memory-module ECC-supplemental (OMMES) memory 310. Note that while baseboard 302 may be characterized as a "module" that has memory mounted on it, it is not a "memory module" as the phrase is used herein and by those skilled in the art. However, baseboard does include sockets 312 into which non-ECC memory modules can be installed. In variations, the number of sockets can vary, e.g., from 1 socket to 16 sockets. OMMES memory 310 is located
close to sockets 312, and memory control, address, command, and data signal lines (not shown) are routed so as to ensure signal integrity.

[19] As illustrated in Fig. 3, two 4 GB (Gigabyte) non-ECC DIMMs 314 and 316 of a memory module set 318 are installed in sockets 312 using connectors 315 and 317, respectively. DIMM 314 includes eight 4 Gb (Giga-bit) integrated circuit memories 321-328, while DIMM 316 includes eight 4 Gb integrated circuit memories 331-338. Thus, each DIMM 314, 316 can store 4 GB (Giga-Bytes) of data. However, when ECC encoded, 4 GB of data requires an extra 4 Gb (Giga-bits) capacity. For DIMM 314 this is provided by the 4 Gb memory device (SDRAM) 342 of OMMES memory 310; likewise, for DIMM 316, the excess capacity is handled by memory device 344 of OMMES memory 310.

[20] Collectively, ECC controller 308, ECC-supplemental memory 310, and memory module set 318 define a populated ECC memory system 340 that is a subsystem of computer 300. Alternatively, ECC memory system 340 may be unpopulated, e.g., when no memory modules are installed in sockets 312.

[21] To accommodate more than two memory modules or memory modules with more than one rank of memory devices per memory module, ECC-supplemental memory 310 may have additional memory devices installed, e.g., memory devices 346 and 348. Instead of having one ECC-supplemental memory device per eight memory devices on memory modules, other ratios can be implemented, either using memory devices of different widths (e.g., x4, x8, x16), different capacities, or different dice per package or to accommodate ECC encoding schemes that add more than one bit per byte. For example, a dual-die SDRAM can take the place of two
single-die SDRAM for two ranks. Also, a higher capacity supplemental SDRAM can supplement for a DIMM with lower capacity SDRAMs.

[22] Some alternative configurations for the OMMES memory include the following. 1) One single-die DRAM device to support a single-ranked SO-DIMM. 2) Two single-die DRAM devices to support dual-ranked SO-DIMMs (single-die DRAM devices are much cheaper than dual-die ones). 3) One dual-die DRAM device to support single-ranked SO-DIMM (and single and dual density configurations), dual-ranked SO-DIMM (for emulating two single-density configuration to support a dual-ranked SO-DIMM)

[23] While, in some embodiments, ECC encoding adds one bit per byte of non-ECC-encoded data words, in other embodiments, more than one-bit per byte may be added, e.g., to allow correction of multi-bit data errors. In most cases, the ECC-capable memory controller will distribute at least 80% of each data word to memory modules and at most 20% to ECC-supplemental memory 310.

[24] In addition to including memory devices, memory modules typically include serial presence detect (SPD) devices that are intended to inform memory controllers of the capabilities of and requirements for the host memory modules. Thus, SPD devices store SPD data that may specify information about capacity, timing, organization, and other aspects of configuration including whether or not it supports for the host memory module. For example, memory module 314 includes SPD 329 that specifies, among other things, that its host memory module is a non-ECC memory module; memory module 316 includes an essentially similar SPD 339. Thus, SPD data is used, among other purposes, to distinguish ECC memory modules from non-ECC memory modules.
Conventionally, as a computer is booted, firmware code (e.g., including BIOS code, system firmware, and memory-controller code) reads the SPD data for installed memory modules and programs a memory controller accordingly. ECC memory system 340 includes firmware code 352, encoded on firmware (e.g., flash memory on baseboard 302) media 350, that includes an SPD filter 354. SPD filter 354 when executed by processor 304, in effect, filters out SPD data indicating that a memory module is a non-ECC memory module and replaces that memory-controller programming indicating that the available memory is ECC memory. In other respects, SPD data from installed modules may be, in effect, passed through to memory controller 308.

One approach to filtering is to provide ECC SPD, e.g., on the baseboard rather than on a memory module, that indicates the presence of an ECC memory module even when no ECC memory module is present. The filtering can include substituting the ECC SPD data for some of the memory-module SPD data. In any event, memory controller 308, which is capable of using either ECC memory or non-ECC memory, will operate as if ECC memory modules are installed even though only non-ECC memory modules are installed.

OMMES memory 310 is selected to be at least as capable (e.g., in size and speed) as any memory expected to be installed in sockets 312. If the capabilities of installed memory modules exceed those of OMMES memory 310, filter 354 can alter the SPD data to effectively downgrade the memory modules to match the capabilities of OMMES memory. Note that firmware code 352 can serve other purposes, e.g., other functions associated with a basic input output system (BIOS), extensible firmware interface (EFI), or other system firmware. The OMMES memory may but need not store ECC
check bits; the OMMES memory may store data bits only or a combination of data bits and check bits. For example, the 72-bits of an ECC-encoded data word can be distributed in any suitable manner between the memory module(s) and the OMMES memory.

[28] Firmware code 352 further provides memory controller programming to accommodate the timing and training variations (due to flight time and distance differences) between the first SDRAM device and the last SDRAM device on the DIMM. This programming involves a training sequence for calibrating address, clock, and data timing for each byte associated with each DRAM device. For each data group, BIOS will program the timing between a data strobe to latch data and the data signals in the memory controller to accommodate the difference in signal propagation delay from the memory controller to the embedded (on-board) devices and that of the DRAM devices on the SO-DIMM. In the illustrated example, the training sequence can accommodate variations across a rank including OMMES memory on baseboard 302 along with devices on the memory modules. Note that the supplemental SDRAM devices can be placed on the baseboard close to the memory module connectors and route memory control, address, command, data signals appropriately to provide the right level of signal integrity.

[29] SPD filter 354 makes it possible to use OMMES memory 342 with a conventional memory controller that then functions with no awareness that the memory modules are non-ECC memory modules. In an alternative embodiment, an OMMES-aware memory controller may be used, obviating the need for an SPD filter.
Computer system 300 supports a process 400 flow charted in FIG. 4. Process 400 includes a boot phase 410 and an operating phase 420. In boot phase 410, e.g., after a system start or restart, the computer is booted beginning at 411. During booting, boot firmware is executed so that, among other actions, SPD data is read at 412 from installed memory modules. In system 300, the SPD data indicates that the installed memory modules are non-ECC memory modules. At 413, the ECC-capable memory controller is programmed by processor 304 executing firmware code 352 for operation using ECC memory. From the perspective of ECC-capable memory controller 308 and contrary to fact, the installed memory modules are ECC memory modules.

If at 411, it turns out that the SPD data indicates that the memory modules are ECC modules, then firmware code 352 will cause processor 304 to program ECC-capable memory controller 308 to work with the ECC memory modules and not use the OMMES memory. Alternatively, firmware code could program sufficiently capable memory controller to use the OMMES memory to achieve a more robust ECC code, e.g., adding two bits per byte to be able to correct at least some multi-bit errors. In some examples, ECC-only memory controllers are used that are not designed to be used in a non-ECC mode.

Thus, in an example, depending on whether ECC or non-ECC memory modules are installed, a ratio of the lengths of said ECC data words to the lengths of said non-ECC data words can be between 9:8 and 10:8 inclusive. Likewise, the ratio of the portion of an ECC-encoded data word stored on devices on ECC-supplemental memory to the portion of that ECC-encoded data word stored on said memory module set can be between 1:9 and 1:8 inclusive.
[33] During operating phase 420, memory controller 308 ECC encodes 64-bit non-ECC data words into 72-bit ECC-encoded data words at 421. Each data word is distributed, at 422, among the nine devices of the corresponding ECC rank. For example, a data word can be distributed among on-module DRAMS 321-328 and OMMES DRAM 342. Likewise, during a read operation, 72-bit words are read (across memory modules and OMMES memory) and decoded by memory controller 308 into non-ECC encoded data words for consumption by processor 304. Of course, ECC and non-ECC data words of other sizes can be accommodated in other examples.

[34] Typical SPD data includes a Factory/Vendor Data region which may be READ-only and a Writable region for tagging the DIMM, for example, with diagnostic information. Some small-outline DIMMs (SO-DIMMs) may not lock the Vendor region.) A major portion of the SPD information describes the DRAM device. SPD data can describe the Module configuration. Factory, BIOS, Management Processor, e.g., an internal lights-out (iLO) processor, can write and read SPD data.

[35] Various examples invoke different approaches to filtering or updating SPD data. The following list is meant to be illustrative but is non-limiting. 1) Use the module (e.g. SO-DIMM) SPD data as is without updating or filtering it. Get the BIOS to program the memory controller based on the embedded DRAM device; allow an SO-DIMM which matches the necessary characteristics of the embedded DRAM device. 2) Update the SPD content as spare/option part; this will create a new SKU part number. 3) Reprogram the "off-the-shelf" SO-DIMM SPD (before installation) with data representing the new ECC configuration at the factory for example. 4) Via system BIOS or iLO (management processor),
reprogram the SO-DIMM SPD after it has been installed (into the server.

5) Redirect SPD access to a new location (away from the SO-DIMM) for the
sake of the initial memory controller/system configuration; keep SPD
access to the SO-DIMM for the sake of diagnostic information (READ and
WRITE).

[36] Herein, a "system" is a set of interacting process actions or non-
transitory tangible elements, wherein the elements can be, by way of
example and not of limitation, mechanical components, electrical
elements, atoms, physical encodings of instructions. Herein, "process"
refers to a system, the elements of which are process actions that cause
physical transformations.

[37] Herein, a "computer" refers to a hardware machine for manipulating
physically encoded data in accordance with physically encoded
instructions. Depending on context, reference to a computer may or may
not include software installed on the computer. Herein, "processor",
"controller", "media", "memory", and "device" refer to hardware elements
that may or may not be programmed or programmable. Herein, "media"
and "memory" refer to devices including non-transitory tangible material
in or on which information is or can be encoded with information
including data and instructions. Herein, "processor" refers to hardware
for executing instructions. A processor can be a monolithic device, e.g.,
integrated circuit, a portion of a device, e.g., core of a multi-core integrated
circuit, or a distributed or collocated set of devices. Herein,
"communications devices" refers to devices used for communication,
including both network devices and devices used for input and output,
e.g., human interface devices.
Herein, a "memory-module set" is a set of one or more memory modules, as the term "memory module" is understood by those skilled in the art. As used herein, a "memory module" includes plural integrated-circuit memory devices attached to a common structure, typically a printed circuit board. Herein, "ECC-supplemental memory" refers to memory used to supplement non-ECC memory devices to complete a rank in an ECC memory system. Off-memory-module ECC-supplemental (OMMES) memory is ECC-supplemental memory that is not on a memory module. SPD devices and data are provided for memory modules but not for the OMMES memory disclosed herein. Herein, a "memory device" is an integrated circuit package designed for storage and retrieval of data; the memory devices of interest herein store at least 1 Gb of data per device.

Herein, an "ECC-capable memory controller" is a memory controller that can, at least when suitably programmed, encode non-ECC data into ECC data and decode ECC data into non-ECC data. Typically, an ECC-capable memory controller can be selectively programmed to operate either with non-ECC memory modules and ECC memory modules. In the present context, an ECC-capable memory controller can be programmed to operate with ECC memory even though it is actually reading from and writing to non-ECC memory modules (plus ECC-supplemental memory).
In this specification, related art is discussed for expository purposes. Related art labeled "prior art", if any, is admitted prior art. Related art not labeled "prior art" is not admitted prior art. In the claims, "said" introduces elements for which there is explicit verbatim antecedent basis; "the" introduces elements for which the antecedent basis may be implicit. The illustrated and other described embodiments, as well as modifications thereto and variations thereupon are within the scope of the following claims.

What Is Claimed Is:
CLAIMS

1. A memory system comprising:
   a memory module set of one or more non-ECC memory modules;
   off-memory-module ECC-supplemental memory not on a memory module of said memory module set; and
   an ECC-capable memory controller coupled to said memory module set and said ECC-capable memory for distributing each of plural ECC-encoded data words between said memory module set and said ECC-supplemental memory.

2. A memory system as recited in Claim 1 further comprising a baseboard having slots into which respective ones of said non-ECC memory modules are inserted, said ECC-capable memory controller and said ECC-supplemental memory being mounted on said baseboard and not on a non-ECC memory module of said memory module set.

3. A memory system as recited in Claim 2 further comprising media encoded with code that, when executed by a processor:
   reads module serial presence detect (SPD) data from SPD devices on respective ones of said non-ECC memory modules, said module SPD data indicating said non-ECC memory modules are non-ECC memory modules; and
   programs said ECC-capable controller to operate as though it were to control ECC memory modules.
4. A memory system as recited in Claim 3 further comprising ECC SPD data tangibly encoded on a device attached to said baseboard not via said slots, said ECC data indicating presence of an ECC memory module even when no ECC memory module is present, said filter replacing some of said module SPD data with said ECC SPD data.

5. A memory system as recited in Claim 1 wherein each of said non-ECC memory modules has an integer multiple of eight memory devices.
6. A process comprising:

   encoding non-ECC data words to ECC data words; and

   writing said ECC data words so that each of said ECC data words is
   distributed between a memory set of one or more non-ECC memory
   modules and ECC-supplemental memory not on a memory module of said
   memory module set.

7. A process as recited in Claim 6 wherein said writing includes writing a
   portion of an ECC data word to a memory device mounted on a baseboard
   and writing another portion of said ECC data word to a memory device
   included in a memory module installed on said baseboard.

8. A process as recited in Claim 6 further comprising:

   reading module serial presence detect (SPD) data from SPD devices on
   respective ones of said non-ECC memory modules said module SPD data
   indicating said non-ECC memory modules are non-ECC memory modules;
   and

   programming an ECC-capable memory controller to operate as though
   it was controlling ECC memory modules, said ECC-capable memory
   controller performing said converting and said writing.

9. A process as recited in Claim 8 further comprising replacing as least
   some of said module SPD data with ECC SPD data stored on a device
   mounted of said baseboard.

10. A process as recited in Claim 6 wherein said writing distributes a word
    among nine memory devices, eight of which are in said memory module
    set and one of which is included in said ECC-supplemental memory.
11. A system comprising:
   a baseboard having slots for receiving non-ECC memory modules;
   ECC-supplemental memory mounted on said baseboard; and
   an ECC controller for converting non-ECC encoded data words into
   ECC-encoded data words, said ECC controller being coupled to said slots
   and said ECC-supplemental memory for distributing bits of each of said
   ECC encoded words between said non-ECC memory modules and said ECC-
   supplemental memory.

12. A system as recited in Claim 11 further comprising:
   a processor mounted on said baseboard, said processor being coupled
   to said ECC-capable memory controller for providing said non-ECC
   encoded data words thereto; and
   media, mounted on said baseboard, encoded with code that, when
   executed by said processor, causes said processor to:
   read module serial presence detect (SPD) data from SPD devices
   on respective ones of said non-ECC memory modules said module
   SPD data indicating said non-ECC memory modules are non-ECC
   memory modules; and
   program said ECC-capable controller to operate as though it was
   controlling ECC memory modules.

13. A system as recited in Claim 12 wherein said code further includes
   ECC SPD data indicating presence of an ECC memory module even when
   no ECC memory module is present, said code causing said processor to
   program said ECC-capable memory controller using at least some of said
   module SPD data and using at least some said ECC SPD data.
14. A system as recited in Claim 11 further comprising said non-ECC memory modules, said non-ECC memory modules including plural ranks of memory devices, said ECC-supplemental memory including at least one memory device for each of said ranks.

15. A system as recited in Claim 11 wherein said ECC controller is arranged to distribute each of said ECC-encoded data words among n memory devices such that the ratio of the portion of an ECC-encoded data word stored on devices on ECC-supplemental memory to the portion of that ECC-encoded data word stored on said memory module set is between 1:9 and 1:8 inclusive.

16. A system as recited in Claim 15 wherein each ECC-encoded data word is distributed among eight memory devices on said memory module set and one memory device of said ECC-supplemental memory.
FIG. 1

ECC MEMORY SYSTEM 100

ECC-CAPABLE MEMORY CONTROLLER 102

OFF-MEMORY-MODULE ECC-SUPPLEMENTAL (OMMES) MEMORY 104

(NON-ECC) MEMORY MODULE SET 106

FIG. 2

200
ECC ENCODE NON-ECC DATA WORDS

201

DISTRIBUTE EACH ECC-ENCODED DATA WORD BETWEEN NON-ECC MEMORY-MODULE MEMORY DEVICES & OFF-MEMORY MODULE ECC-SUPPLEMENTAL (OMMES) MEMORY 202
BOOT PHASE 410

BOOT USING Firmware Code 411

READ (NON-ECC) Memory- Module SPDs 412

PROGRAM
ECC-CAPABLE Memory CONTROLLER
FOR
ECC Memory 413

OPERATING PHASE 420

ECC Encode NON-ECC DATA Words 421

Distribute Each ECC-Encoded Word
Between
On-Memory-Module Memory &
Off- Memory-Module
ECC-Supplemental (OMMES) Memory 422

FIG. 4
INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/052943

A. CLASSIFICATION OF SUBJECT MATTER

G11C 29/42(2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 29/42; G11C 5/00; G11C 7/00; H03M 13/00; G11C 8/18; G11C 29/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
kOMPASS(KIPO internal) & Keywords: ECC, controller, memory, system, module, set, encode, DRAM, non-ECC, off-memory-module ECC, SIMM, DImm

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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<tbody>
<tr>
<td>Y</td>
<td>US 7117421 Bl (RADOSLAV DANILAK) 03 October 2006 See column 4, lines 31-36; column 7, lines 10-25; column 8, lines 24-25, 35-37; and figures 3-5.</td>
<td>1,5-6,11,14</td>
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<td>A</td>
<td>Y</td>
<td>2-4,7-10,12-13</td>
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<td>Y</td>
<td>US 2006-0123320 Al (PETE D. Vogt) 08 June 2006 See paragraphs [0003], [0020], [0050]; and figures 1, 4A, 7.</td>
<td>1,5-6,11,14</td>
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<td>A</td>
<td>US 2004-0163028 Al (SOMPONG P. OLARIG) 19 August 2004 See paragraphs [0044]-[0056]; and figure 3.</td>
<td>1-16</td>
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<tr>
<td>A</td>
<td>US 2012-0075902 Al (PETER MACHILLIAMS et a1.) 29 March 2012 See paragraphs [0195]-[0196]; and figure 14.</td>
<td>1-16</td>
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<td>A</td>
<td>US 2007-0250756 Al (KEVIN C. GOIER et a1.) 25 October 2007 See paragraphs [0032]-[0033]; and figure 1.</td>
<td>1-16</td>
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Further documents are listed in the continuation of Box C.

See patent family annex.

# Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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Date of the actual completion of the international search 25 April 2014 (25.04.2014)

Date of mailing of the international search report 25 April 2014 (25.04.2014)

Name and mailing address of the ISA/KR
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FormPCT/ISA/210 (second sheet) (July 2009)
<table>
<thead>
<tr>
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