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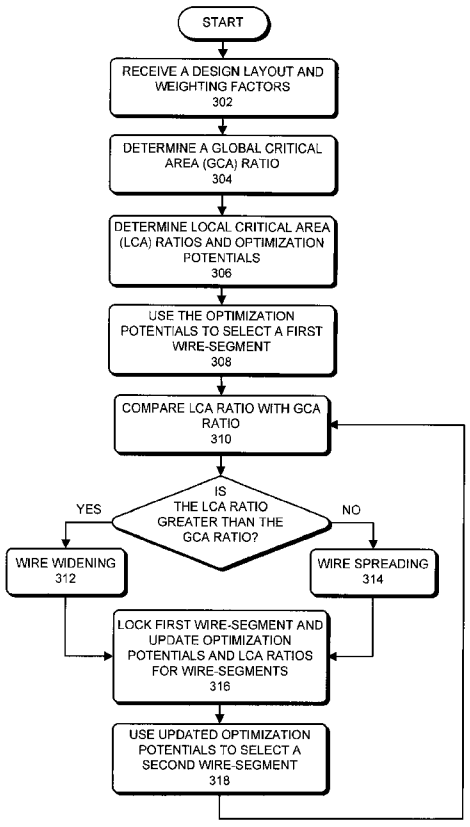


FIG. 3

(57) Abstract: One embodiment of the present invention provides a system that reduces random yield loss. During operation, the system can receive a design layout. The system may also receive weighting factors that are associated with the particle densities in the metal regions and the empty regions. Next, the system can determine local critical area ratios and optimization potentials for a set of wire segments. The system can then select a wire segment, and compare its local critical area ratio with a global critical area ratio. Next, the system can use the result of the comparison to determine a layout optimization. The system can then apply the layout optimization to the wire segment to obtain an improved layout.

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# RANDOM YIELD IMPROVEMENT BASED ON COMPARISON BETWEEN WIRE AND GLOBAL CRITICAL AREA

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## BACKGROUND

### Field of the Invention

**[0001]** The present invention relates to integrated circuit design and fabrication. More specifically, the present invention relates to a method and an apparatus to reduce random yield loss.

### Related Art

**[0002]** As semiconductor manufacturing technologies move into deep sub-micron era, manufacturability and yield related issues are becoming increasingly important. In current processes, yield loss can be caused by many factors, which include random contamination particles, distortions of the printed features during the lithography process, thickness variations from the polishing process, etc. The portion of the yield loss that is caused by random contamination particles is referred to as random yield loss. Reducing the random yield loss is desirable because it can decrease manufacturing costs, thereby increasing the profitability of a semiconductor chip.

## SUMMARY

**[0003]** One embodiment of the present invention provides a system that reduces random yield loss. An embodiment may perform layout optimizations that are intelligently guided by a critical area evaluator, thereby ensuring that the layout optimization decreases the random yield loss.

**[0004]** An embodiment of the present invention dynamically selects a layout optimization technique. An embodiment can handle different particle densities for metal and empty regions.

**[0005]** During operation, a system can receive a design layout. The system may also receive weighting factors that are associated with the particle densities in the metal regions and the empty regions. Next, the system can determine local critical-area-ratios and optimization potentials for a set of wire-segments. The system can then select a wire segment using the optimization potentials, and compare its local critical-area-ratio with a global critical-area-ratio. Next, the system can use the result of the comparison to determine a layout optimization. The system can then apply the layout optimization to the wire segment to obtain an improved layout.

## BRIEF DESCRIPTION OF THE FIGURES

**[0006]** FIG. 1 illustrates various stages in the design and fabrication of an integrated circuit in accordance with an embodiment of the present invention.

**[0007]** FIG. 2A illustrates a short critical area in accordance with an embodiment of the present invention.

**[0008]** FIG. 2B illustrates an open critical area in accordance with an embodiment of the present invention.

**[0009]** FIG. 3 presents a flowchart that illustrates a process for reducing random yield loss in accordance with an embodiment of the present invention.

**[0010]** FIG. 4 illustrates exemplary spacing-visible neighbors of a wire segment in accordance with an embodiment of the present invention.

**[0011]** FIG. 5 illustrates how a system can apply wire-widening to a wire segment in accordance with an embodiment of the present invention.

**[0012]** FIG. 6 illustrates how a system can apply wire-spreading to a wire segment in accordance with an embodiment of the present invention.

## DETAILED DESCRIPTION

### Integrated Circuit (IC) Design Flow

**[0001]** FIG. 1 illustrates various stages in the design and fabrication of an integrated circuit in accordance with an embodiment of the present invention.

**[0002]** The process starts with the conception of the product idea (step 100) which is realized using an EDA software design process (step 110). When the design is finalized, it

can be taped-out (event 140). After tape out, the fabrication process (step 150) and packaging and assembly processes (step 160) are performed which ultimately result in finished chips (result 170).

**[0003]** The EDA software design process (step 110), in turn, comprises steps 112-130, which are described below. Note that the design flow description is for illustration purposes only. This description is not meant to limit the present invention. For example, an actual integrated circuit design may require the designer to perform the design steps in a different sequence than the sequence described below. The following discussion provides further details of the steps in the design process.

**[0004]** System design (step 112): In this step, the designers describe the functionality that they want to implement. They can also perform what-if planning to refine functionality, check costs, etc. Hardware-software architecture partitioning can occur at this stage. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Model Architect, Saber, System Studio, and DesignWare® products.

**[0005]** Logic design and functional verification (step 114): At this stage, the VHDL or Verilog code for modules in the system is written and the design is checked for functional accuracy. More specifically, the design is checked to ensure that it produces the correct outputs. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include VCS, VERA, DesignWare®, Magellan, Formality, ESP and LEDA products.

**[0006]** Synthesis and design for test (step 116): Here, the VHDL/Verilog is translated to a netlist. The netlist can be optimized for the target technology. Additionally, tests can be designed and implemented to check the finished chips. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Design Compiler®, Physical Compiler, Test Compiler, Power Compiler, FPGA Compiler, Tetramax, and DesignWare® products.

**[0007]** Netlist verification (step 118): At this step, the netlist is checked for compliance with timing constraints and for correspondence with the VHDL/Verilog source code. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Formality, PrimeTime, and VCS products.

**[0008]** Design planning (step 120): Here, an overall floorplan for the chip is constructed and analyzed for timing and top-level routing. Exemplary EDA software

products from Synopsys, Inc. that can be used at this step include Astro and IC Compiler products.

**[0009]** Physical implementation (step 122): The placement (positioning of circuit elements) and routing (connection of the same) occurs at this step. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include the Astro and IC Compiler products.

**[0010]** Analysis and extraction (step 124): At this step, the circuit function is verified at a transistor level, this in turn permits what-if refinement. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include AstroRail, PrimeRail, Primetime, and Star RC/XT products.

**[0011]** Physical verification (step 126): In this step, the design is checked to ensure correctness for manufacturing, electrical issues, lithographic issues, and circuitry. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include the Hercules product.

**[0012]** Resolution enhancement (step 128): This step involves geometric manipulations of the layout to improve manufacturability of the design. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Proteus, ProteusAF, and PSMGen products.

**[0013]** Mask data preparation (step 130): This step provides the "tape-out" data for production of masks to produce finished chips. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include the CATS(R) family of products.

**[0014]** Embodiments of the present invention can be used during one or more of the above-described steps. One embodiment can be used during the design planning step 120.

**Random yield loss**

**[0015]** Random yield loss can depend on the critical area of a layout. The critical area measures the susceptibility of the design to random contamination particles. Critical area can be defined as the region on the chip where the falling of a contamination particle can cause a catastrophic failure. The critical area can be categorized as open critical area or short critical area based on the type of failure – open or short – that would occur if a random contamination particle were to fall in the critical area. Random yield loss can be viewed as a function of the open and short critical areas.

**[0016]** The particle density can be another parameter that affects the random yield loss. Particle density can be defined as the total particle count divided by the total chip or wafer area. Since particles can be of different sizes, a set of particle density values may be used, wherein each particle density value corresponds to the density of particles whose size is within a specific range.

**[0017]** In order to reduce random yield loss of a layout design, the critical area can be used to guide layout optimization. Layout optimizations may be performed to reduce the critical area, thereby reducing the random yield loss.

**[0018]** Layout optimization has traditionally been driven by area, timing, and power. Conventionally, layout optimizations to reduce critical area are usually added as an afterthought. Critical area optimization is usually performed at the post-routing stage when the layout design has already been optimized for area, timing, and power. Prior art techniques are typically not yield aware, and they usually cannot provide guarantees that the random yield loss will be reduced.

**[0019]** Decreasing the open critical area can increase the short critical area, and vice-versa. For example, increasing the spacing between the wire segments (i.e., wire-spreading) typically reduces the short critical area but increases the open critical area. Similarly, increasing the width of the wire segments (i.e., wire-widening) typically reduces the open critical area but increases the short critical area. Hence, optimization techniques that apply only one type of layout optimization cannot guarantee a reduction in the total critical area. Further, techniques that use one type of optimization before the other also suffer from similar drawbacks. This is because such static approaches implicitly favor one technique over the other, irrespective of which critical area component is larger.

**[0020]** The above-described problems with prior art techniques are further aggravated in current processes due to the fact that particles may preferentially cluster in metal regions or empty regions. In other words, the particle densities may be different in the metal regions versus the empty regions and may vary from one fabrication plant to another and may also vary across process lines. Since particles that fall in the metal regions can cause opens and those that fall in the empty regions can cause shorts, a difference in the particle densities between the metal and empty regions can cause the yield loss contribution to be significantly different for the short and open critical areas. One embodiment of the present invention

simultaneously considers both open and short critical areas, as well as the corresponding particle densities, thereby guaranteeing a reduction in random yield loss.

**[0021]** Embodiments can use any type of random yield model to reduce random yield loss. For example, an embodiment can use the Poisson model, in which the random yield $Y_r$, is given by $Y_r = e^{-A_{cr} \cdot D_0}$, where $A_{cr}$ is the critical area and $D_0$ is the particle density. Alternatively, the system can use the Negative Binomial model.

**[0022]** FIG. 2A illustrates a short critical area in accordance with an embodiment of the present invention.

**[0023]** Wire segments 202 and 204 are part of a design layout. Particle 206 overlaps with wire segment 204, but not with wire segment 202. However, particle 208 overlaps with both wire segment 202 and wire segment 204, and hence, can cause a catastrophic failure in the circuit by shorting wire segments 202 and 204. If particle 208's center is located anywhere within area 210, it may cause a short between wire segments 202 and 204. The size of the short critical area may depend on a number of factors, including the size of the particle. Area 210 can be the short critical area that is associated with particles whose size is the same as particle 208. The short critical area associated with larger particles will usually be larger, and the short critical area associated with smaller particles will usually be smaller.

**[0024]** FIG. 2B illustrates an open critical area in accordance with an embodiment of the present invention.

**[0025]** Wire segment 252 is part of a design layout. Particle 254 partially overlaps with the width of wire segment 252. However, particle 256 completely overlaps with the width of wire segment 252 and hence can cause a catastrophic failure in the circuit by causing wire segment 252 to become open circuited. If particle 256's center is located anywhere within area 258, it may cause wire segment 252 to become open circuited. The size of the open critical area may depend on a number of factors, including the size of the particle. Area 258 can be the open critical area that is associated with particles whose size is the same as particle 256. The open critical area associated with larger particles will usually be larger, and the open critical area associated with smaller particles will usually be smaller.

**[0026]** Once the critical areas for all the wire segments are extracted individually, the geometric union of these areas can give the total critical area $A_c(x)$ for particle size $x$. Next, the total average critical area can be determined by averaging over all the particle sizes. For example, the total average critical area, $A_{cr}$, can be determined using the expression

$$A_{cr} = \int_{x_{min}}^{x_{max}} A_c(x) f(x) dx, \quad (1)$$

where $x_{min}$ and $x_{max}$ are the minimal and maximal particle sizes and $f(x)$ is the particle size distribution function.

**[0027]** If a pair of wire segments $(i, j)$ belonging to different nets have segments visible to one another, the short critical area at a particular particle size $x$ can be determined using the expression

$$A_s(x) = \begin{cases} 0 & if\ x < s_{ij}, \\ (x - s_{ij}) \cdot b_{ij} & if\ x \geq s_{ij}, \end{cases} \quad (2)$$

where $s_{ij}$ is the spacing between the pair of wire segments and $b_{ij}$ is the visible length.

**[0028]** The open critical area can be determined using the expression

$$A_o(x) = \begin{cases} 0 & if\ x \leq w_i, \\ (x - w_i) \cdot l_i & if\ w_i < x \leq D_{\max}, \end{cases} \quad (3)$$

where $w_i$ is the wire segment width and $l_i$ is the wire-segment length.

**[0029]** The above equations can be used to determine the average short and average open critical areas analytically. For example, under a specific set of assumptions, the expressions for average open and short critical area may be turn out to be

$$A_s = \frac{b_{ij}}{2 \cdot s_{ij}}, \quad (4)$$

$$A_o = \frac{l_i}{2 \cdot w_i}. \quad (5)$$

**[0030]** Equation ( 4 ) shows that for same visible length $b_{ij}$, an increase in spacing $s_{ij}$ makes the short critical area smaller. This is the rationale behind wire-spreading techniques, which move a wire segment or a portion of a wire segment away from the neighboring wire-segment with which it has small spacing and large visible length. Similarly, equation ( 5 ) shows that wire-widening can reduce the open critical area.

**[0031]** However, only using wire-spreading or wire-widening can negatively impact the total critical area. For example, wire-spreading typically introduces jogs and hence increases the wire-segment length. The wire-segment length may increase by $2 \cdot \delta$, where $\delta$

is the amount by which a wire segment is moved during wire-spreading. Hence, the open critical area may increase to $\hat{A}_o = \frac{l_i + 2 \cdot \delta}{2 \cdot w_i}$.

**[0032]** Similarly, increasing the wire-segment width by $\delta$ may reduce the open critical area, but it may increase the short critical area from $A_s = \frac{b_{ij}}{2 \cdot s_{ij}} + \frac{b_{ik}}{2 \cdot s_{ik}}$ to $\hat{A}_s = \frac{b_{ij}}{2 \cdot (s_{ij} - \delta/2)} + \frac{b_{ik}}{2 \cdot (s_{ik} - \delta/2)}$, where wire segment $i$ is between wire segments $j$ and $k$, $b_{ij}$ is the visible length between wire segments $i$ and $j$, $b_{ik}$ is the visible length between wire segments $i$ and $k$, $s_{ij}$ is the spacing between wire segments $i$ and $j$, and $s_{ik}$ is the spacing between wire segments $i$ and $k$. Hence, reducing only the short or open critical area may not reduce the total critical area.

**[0033]** Further, prior art techniques that perform both wire-spreading and wire-widening in a static order also suffer from drawbacks. First, always performing wire-spreading before wire-widening can be wasteful if the short critical area is not a dominant factor in the total yield loss of a given design. An example of such a scenario is when the original open critical area is much larger than the short critical area and hence contributes more to yield loss. Short critical area reduction in this case is undesirable and wasteful since it may not reduce the total critical area because the open critical area might increase. Further, it could introduce manufacturing problems due to the increased presence of jogs.

**[0034]** In addition, a static technique does not take into account the possibility that the short and open critical areas might not necessarily be equally weighted in the random yield calculation. Recall that the random yield loss relies on the critical area and the particle density. Prior art techniques typically assume a uniform particle density across the chip. However, in modern semiconductor manufacturing processes, contamination particles may preferentially cluster in the metal or empty regions of the chip. In contrast to prior art techniques, an embodiment of the present invention handles different particle densities for metal and empty regions.

## Weighted critical area

**[0035]** One embodiment of the present invention determines the total critical area by weighting the short critical area and the open critical area using weighting factors. The

weighting factors may relate to the impact of the two types of critical areas on the random yield loss. Specifically, the weighting factors may be derived from the contamination particle densities in the metal area and the empty area in the design layout.

**[0036]** Recall that the short critical areas are centered between the wire segments, and the open critical areas are centered on the wire segments. To properly account for large particle sizes, the total critical area may be determined by taking the union of the short critical area and the open critical area. Note that, for large particle sizes, the short critical area may overlap with the open critical area. Hence, taking the union ensures that the overlapping critical area is not double counted. However, since large particles are rare, the probability of an overlap between the open critical area and the short critical area is low. Therefore, we can approximate the total critical area to be the sum of short critical area and open critical area.

**[0037]** As mentioned above, the particle density in metal regions may be different from that in empty regions. One embodiment handles this difference in particle densities by introducing weighting factors $w_s$ and $w_o$ for short and open critical areas, respectively, while using the same average particle density $D_0$. This approach for handling the different weighting factors may be advantageous because it can enable the routing tool to use this weight information to guide the optimization suitably. Specifically, the weighted critical area can be determined using the expression

$$A_{wtotal} = w_s \cdot A_{short} + w_o \cdot A_{open}, \qquad (6)$$

where $A_{wtotal}$ is the weighted total critical area, $A_{short}$ is the short critical area, and $A_{open}$ is the open critical area. Hereinafter, the expression $(w_s \cdot A_{short})$ will be referred to as the weighted short critical area, and the expression $(w_o \cdot A_{open})$ will be referred to as the weighted open critical area.

**[0038]** Note that the weighted critical area can be determined for a wire segment, a group of wire segments, or for all wire segments in a layer. The weighted critical area may be viewed as a proxy for the random yield and reducing this quantity is expected to reduce the random yield loss. One embodiment uses the weighted critical area as the cost function that the layout optimization process tries to minimize.

## Layout optimization

**[0039]** An embodiment performs layout optimizations one layer at a time. During optimization, an embodiment may move wire segments, but not vias. Another embodiment optimizes multiple layers at once, and hence, can move vias in addition to wire segments. Each layer may have a preferred direction of routing, either horizontal or vertical. Since the majority of the wire segments in a layer are expected to be in the preferred direction, an embodiment moves the wire segments in a direction that is orthogonal to the preferred direction of the layer.

**[0040]** In one embodiment, the system may compute an optimization potential for all the wire segments. The optimization potential of a wire segment may be a function of its weighted short and weighted open critical area and can be a measure of both the severity of the problem in the local area and the flexibility available for improvement. An embodiment can select the wire segment with the highest optimization potential and "lock" it, thereby preventing the same wire segment from being optimized in consecutive iterations. The wire segment can then be widened or spread depending on the ratio between the weighted open and the weighted short critical area of the wire segment. The weighted open and weighted short critical areas can provide an indication of which type of critical area has a larger contribution to the weighted critical area of the layer.

**[0041]** The system may then try to reduce the dominant type of critical area using an appropriate layout optimization technique, which can include wire-widening and/or wire-spreading. After layout optimization is performed on a wire segment, the optimization potentials of the remaining unlocked wire-segments can be updated as needed. Alternatively, the optimization potentials may be updated after layout optimization is performed on multiple wire segments. After the optimization potentials are updated, the wire segment with the largest optimization potential among the "unlocked" wire-segments may be selected and the process may be repeated.

**[0042]** Note that the process can dynamically adjust the number of wire segments that are widened and spread in accordance with the weighted open and short critical areas. The amount by which a wire segment is spread or widened may also vary depending on the configuration of its neighboring wire-segments. Since the weighted critical area of the entire layer can be approximated by summing the weighted critical areas of the individual wire segments, reducing the weighted critical area of the individual wire segments can reduce the weighted critical area of the entire layer.

**Process for reducing random yield loss**

**[0043]** FIG. 3 presents a flowchart that illustrates a process for reducing random yield loss in accordance with an embodiment of the present invention.

**[0044]** The process can begin by receiving a design layout and weighting factors (step 302).

**[0045]** The weighting factors can be associated with the particle densities in the metal and empty regions of the design layout. The particle densities are usually specific to the semiconductor manufacturing processes and/or fabrication plant that is expected to be used to fabricate the design layout.

**[0046]** Next, the system can determine a global critical area ratio (step 304). The global critical area ratio can be a function of the weighted open and weighted short critical area of the layer. In one embodiment, the global critical area ratio can be determined by dividing the weighted open critical area for the layer by the weighted short critical area of the layer.

**[0047]** The system can then determine local critical area ratios and optimization potentials for a set of wire-segments in the design layout (step 306). A wire segment can be a portion of a wire or it can be the longest continuous portion of a wire in a specific direction or it can be the whole wire. In one embodiment, the system can determine optimization potentials for a set of wire-segments in the preferred direction of the layout.

**[0048]** The system can determine the local critical area ratio using the weighted open and weighted short critical area of a set of wire-segments. In one embodiment, the system can first determine a weighted open-critical-area for a wire segment. Specifically, the system can determine the weighted open-critical-area by adjusting the open-critical-area with a factor that is associated with the particle density in metal areas. Next, the system can determine a weighted short-critical-area for the wire segment. Specifically, the system can determine the weighted short-critical-area by adjusting the short-critical-area with a factor that is associated with the particle density in empty areas. The system can then determine the local critical-area-ratio using the weighted open-critical-area and the weighted short-critical-area. In one embodiment, the system can divide the weighted open-critical-area by the weighted short-critical-area to obtain the local critical area ratio.

**[0049]** Next, the system can use the optimization potentials to select a first wire-segment (step 308).

**[0050]** In one embodiment, the system can determine the optimization potential for a candidate wire-segment by using the open and short critical areas associated with the candidate wire-segment. The optimization potential of a wire segment may be high if applying a layout optimization to the wire segment is expected to substantially reduce the random yield loss. For example, a candidate wire-segment may have a high optimization potential if the open area on one side of the candidate wire-segment is substantially larger than the open area on the other side of the candidate wire-segment. Similarly, a candidate wire-segment may have a high optimization potential if the width of the candidate wire-segment can be substantially increased without violating a design rule.

**[0051]** In one embodiment, the optimization potential of a wire segment depends on the type of layout optimization that is performed on the wire segment. For example, if wire-spreading is performed, the optimization potential may be equal to the absolute value of the difference between the open critical area on one side of the wire segment and the open critical area on the other side of the wire segment. On the other hand, if wire-widening is performed, the optimization potential may be equal to the maximum increase in width that can be tolerated without violating a design rule. Note that the system may determine the optimization potential using the weighted open-critical-areas and the weighted short-critical-areas.

**[0052]** Once the optimization potentials are determined, the system may select a wire segment with the highest optimization potential. Alternatively, the system may select a group of wire segments that have a high optimization potential, and then randomly select a wire segment from this group of wire segments.

**[0053]** The system can then compare the first wire-segment's local critical area ratio with the global critical area ratio (step 310).

**[0054]** The system can then use the result of the comparison to determine a layout optimization. Next, the system can apply the layout optimization to the first wire-segment to obtain an improved layout. The layout optimization can generally include any polygon manipulation technique that is expected to reduce the random yield loss.

**[0055]** For example, if the local critical area ratio of the selected wire-segment is greater than the global critical area ratio, the system can apply wire-widening to the first wire-segment (step 312). Note that applying wire-widening to the first wire-segment may involve increasing the width of the wire segment.

**[0056]** On the other hand, if the local critical area ratio of the selected wire-segment is less than the global critical area ratio, the system can apply wire-spreading to the first wire-segment (step 314). Note that applying wire-spreading to the first wire-segment may involve moving the wire segment.

**[0057]** In one embodiment, the system determines the spacing-visible neighbors, which are neighboring wire-segments that are "visible" from the first wire-segment and which will be the first to cause a design rule violation. Next, the system uses these spacing-visible neighbors to determine the amount of wire-widening or wire-spreading that can be performed without violating a design rule. The system can represent the "spacing-visible neighbor" relationship using a graph. For example, each wire segment may be represented by a vertex in the graph, and an edge may exist between vertex *u* and vertex *v* if and only if the wire segments associated with these vertices are spacing-visible neighbors. A technique for determining spacing-visible neighbors is explained in J. Fang, J.S.K Wong, K. Zhang, and P. Tang, "A new fast constraint graph generation algorithm for VLSI layout compaction," *IEEE International Symposium on Circuits and Systems*, 1991, which is hereby incorporated by reference.

**[0058]** FIG. 4 illustrates exemplary spacing-visible neighbors of a wire segment in accordance with an embodiment of the present invention.

**[0059]** Wire segments 404, 406, 408, and 410 are in proximity to wire segment 402. Wire segments 404, 406, and 410 are "visible" from wire segment 402, but wire segment 408 is not. According to one definition, a second wire-segment may be "visible" from a first wire-segment only if we can draw a line from the first wire-segment to the second wire-segment without intersecting an intervening polygon, wherein the line is drawn in a direction that is orthogonal to the wire segment's direction. For example, wire segments 404, 406, and 410 are visible from wire segment 402 because we can draw lines 412, 414, and 416, respectively. Note that, even if wire segment 410 is a visible neighbor of wire segment 402, wire segment 410 may not be spacing-visible neighbor because applying excessive wire-spreading or wire-widening to wire segment 402 will most likely violate a design rule due to wire segments 404 and/or 406 before it violates a design rule due to wire segment 410. Hence, the spacing-visible neighbors of wire segment 402 may include wire segments 404 and 406, but not wire segment 410.

**[0060]** FIG. 5 illustrates how a system can apply wire-widening to a wire segment in accordance with an embodiment of the present invention.

**[0061]** Wire segments 502, 504, 506, 508, and 510 are part of a design layout. Wire segment 512 (dotted line) is part of wire segment 506. The system may apply wire-widening to wire segment 506 to obtain the polygon shown by the solid line. Note that the system may reduce the spacing between the wire segments when it applies wire-widening, thereby increasing the short critical area of the wire segment.

**[0062]** In one embodiment, the system determines an optimal widening for the wire segment using a modified version of the skyline procedure which is described in Udi Manber, "Introduction to Algorithms: A Creative Approach," Addison-Wesley Publishing Company Inc., 1989, which is hereby incorporated by reference. Specifically, the spacing-visible neighbors on both sides of the wire segment can be used. A skyline may be generated for each side of the wire segment such that design rules are not violated. Next, a modified skyline that merges the two skylines (one of the skyline is flipped to ensure both are in the same direction) can be determined and can be used to obtain the optimal width of the wire segment. Suitable restrictions may be imposed to ensure that too many short segments are not created.

**[0063]** FIG. 6 illustrates how a system can apply wire-spreading to a wire segment in accordance with an embodiment of the present invention.

**[0064]** Wire segments 602, 604, 606, 608, and 610 are part of a design layout. Wire segment 612 (dotted line) is part of wire segment 608. The system may apply wire-spreading to wire segment 608 to obtain the polygon shown by the solid line. Note that the system may introduce jogs when it applies wire-spreading to the wire segment, thereby increasing the length of the wire segment, and hence, increasing the open critical area of the wire segment.

**[0065]** In one embodiment, the system determines the optimal location of the wire segment. For example, this may be the location at which the short critical area is balanced on both sides and is typically set to be a multiple of the manufacturing grid. Next, the system may push a portion of the wire segment to the optimal location without violating a design rule. Different portions of the wire segment may not be moved by the same amount.

**[0066]** Specifically, in one embodiment, the system may determine an optimal location for different portions of the wire segment using a modified version of the skyline procedure. Design rules can be used to determine the desired distance from each spacing-

visible neighbor and the skyline created from these displacements can give the final profile. Thus, the original wire-segment may be replaced by a new wire-segment so that portions of the original wire-segment are at the optimal position. Further, jogs may be introduced to maintain connectivity. Suitable restrictions can be imposed to ensure that the jog length is not smaller than a certain pre-specified amount, as lithographic correction techniques may have problems with short jogs.

**[0067]** The foregoing descriptions of layout optimizations, i.e., wire-widening and wire-spreading, have been presented only for purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be readily apparent to practitioners skilled in the art.

**[0068]** Continuing with the discussion of FIG. 3, the system can lock the first wire-segment and update the local critical area ratios and the optimization potentials for other wire segments (step 316).

**[0069]** In one embodiment, the system can update local critical area ratios and optimization potentials for the first wire-segment's neighbors that are "visible" from the first wire-segment. The system can represent the "visible neighbor" relationship between the wire segments using a graph. For example, each wire segment may be represented by a vertex in the graph, and an edge may exist between vertex $u$ and vertex $v$ if and only if the wire segments associated with these vertices are visible neighbors.

**[0070]** The system can then use the updated optimization potentials to select a second wire-segment (step 318). In one embodiment, the system may select an unlocked wire-segment with the highest optimization potential.

**[0071]** Next, the system can return to step 310 and compare the updated local critical area for the second wire-segment and repeat the process steps for a fixed number of iterations and/or until the random yield loss reduces below an acceptable level and/or until the difference between the random yield loss from one iteration to another is less than or equal to a threshold.

## CONCLUSION

**[0072]** The data structures and code described in this detailed description are typically stored on a computer-readable storage medium, which may be any device or medium that can store code and/or data for use by a computer system. This includes, but is not limited to, volatile memory, non-volatile memory, magnetic and optical storage devices such as disk drives, magnetic tape, CDs (compact discs), DVDs (digital versatile discs or digital video discs), or other media capable of storing computer readable media now known or later developed.

**[0073]** Furthermore, the foregoing descriptions of embodiments of the present invention have been presented only for purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be readily apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.

**What Is Claimed Is:**

1. A method to reduce random yield loss, the method comprising:

determining a local critical-area-ratio for a wire segment in a layout;

comparing the local critical-area-ratio with a global critical-area-ratio;

using the result of the comparison to determine a layout optimization; and

applying the layout optimization to the wire segment to obtain an improved layout.

2. The method of claim 1, wherein determining the local critical-area-ratio includes:

determining a weighted open-critical-area for the wire segment;

determining a weighted short-critical-area for the wire segment; and

determining the local critical-area-ratio using the weighted open-critical-area and the weighted short-critical-area.

3. The method of claim 2, wherein determining the weighted open-critical-area includes adjusting the open-critical-area with a factor that is associated with the particle density in metal areas in the design layout.

4. The method of claim 2, wherein determining the weighted short-critical-area includes adjusting the short-critical-area with a factor that is associated with the particle density in empty areas in the design layout.

5. The method of claim 2, further comprising:

determining optimization potentials for a set of wire-segments in the layout, wherein the optimization potentials are determined using weighted open-critical-areas and weighted short-critical-areas associated with the set of wire-segments; and

selecting the wire segment from the set of wire-segments using the optimization potentials.

6. The method of claim 5, wherein a candidate wire-segment in the set of wire-segments has a high optimization potential if the open area on one side of the candidate wire-segment is substantially larger than the open area on the other side of the candidate wire-segment.

7. The method of claim 5, wherein a candidate wire-segment in the set of wire-segments has a high optimization potential if the width of the candidate wire-segment is substantially increasable without violating a design rule.

8. The method of claim 5, wherein selecting the wire segment includes selecting a candidate wire-segment with the highest optimization potential.

9. The method of claim 1, wherein applying the layout optimization to the wire segment includes moving the wire segment.

10. The method of claim 1, wherein applying the layout optimization to the wire segment includes increasing the width of the wire segment.

11. A computer-readable storage medium storing instructions that when executed by a computer cause the computer to perform a method to reduce random yield loss, the method comprising:

determining a local critical-area-ratio for a wire segment in a layout;

comparing the local critical-area-ratio with a global critical-area-ratio;

using the result of the comparison to determine a layout optimization; and

applying the layout optimization to the wire segment to obtain an improved layout.

12. The computer-readable storage medium of claim 11, wherein determining the local critical-area-ratio includes:

determining a weighted open-critical-area for the wire segment;

determining a weighted short-critical-area for the wire segment; and

determining the local critical-area-ratio using the weighted open-critical-area and the weighted short-critical-area.

13. The computer-readable storage medium of claim 12, wherein determining the weighted open-critical-area includes adjusting the open-critical-area with a factor that is associated with the particle density in metal areas in the design layout.

14. The computer-readable storage medium of claim 12, wherein determining the weighted short-critical-area includes adjusting the short-critical-area with a factor that is associated with the particle density in empty areas in the design layout.

15. The computer-readable storage medium of claim 12, further comprising:

determining optimization potentials for a set of wire-segments in the layout, wherein the optimization potentials are determined using weighted open-critical-areas and weighted short-critical-areas associated with the set of wire-segments; and

selecting the wire segment from the set of wire-segments using the optimization potentials.

16. The computer-readable storage medium of claim 15, wherein a candidate wire-segment in the set of wire-segments has a high optimization potential if the open area on one side of the candidate wire-segment is substantially larger than the open area on the other side of the candidate wire-segment.

17. The computer-readable storage medium of claim 15, wherein a candidate wire-segment in the set of wire-segments has a high optimization potential if the width of the candidate wire-segment is substantially increasable without violating a design rule.

18. The computer-readable storage medium of claim 15, wherein selecting the wire segment includes selecting a candidate wire-segment with the highest optimization potential.

19. The computer-readable storage medium of claim 11, wherein applying the layout optimization to the wire segment includes moving the wire segment.

20. The computer-readable storage medium of claim 11, wherein applying the layout optimization to the wire segment includes increasing the width of the wire segment.

21. An apparatus to reduce random yield loss, the apparatus comprising:

a first determining mechanism configured to determine a local critical-area-ratio for a wire segment in a layout;

a comparing mechanism configured to compare the local critical-area-ratio with a global critical-area-ratio;

a second determining mechanism configured to use the result of the comparison to determine a layout optimization; and

an applying mechanism configured to apply the layout optimization to the wire segment to obtain an improved layout.

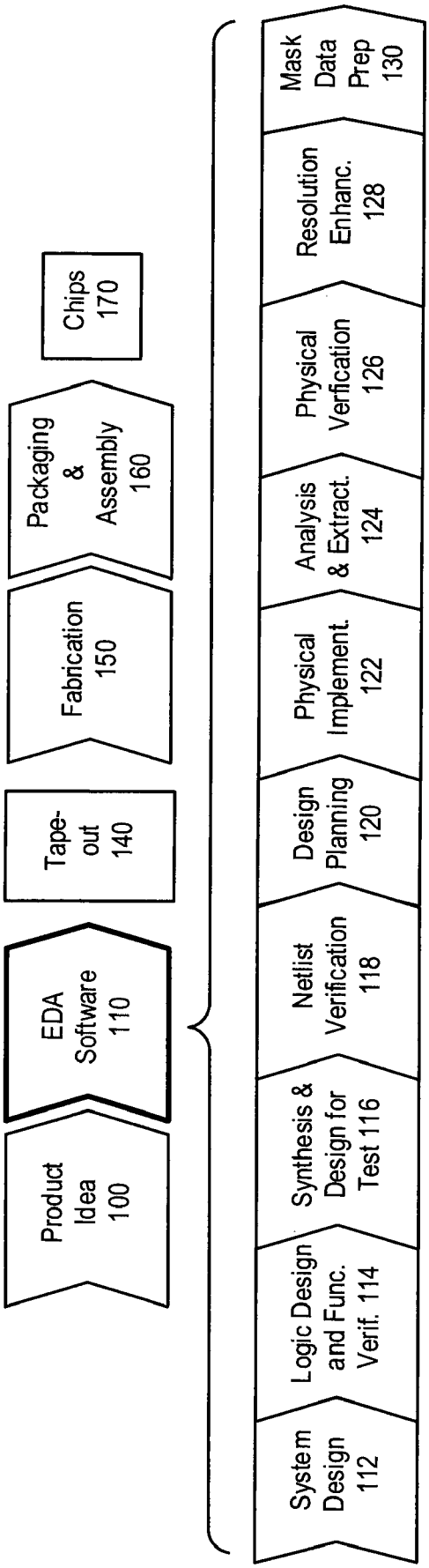
Product Idea 100
EDA Software 110
Tape-out 140
Fabrication 150
Packaging & Assembly 160
Chips 170
System Design 112
Logic Design and Func. Verif. 114
Synthesis & Design for Test 116
Netlist Verification 118
Design Planning 120
Physical Implement. 122
Analysis & Extract. 124
Physical Verfication 126
Resolution Enhanc. 128
Mask Data Prep 130

FIG. 1

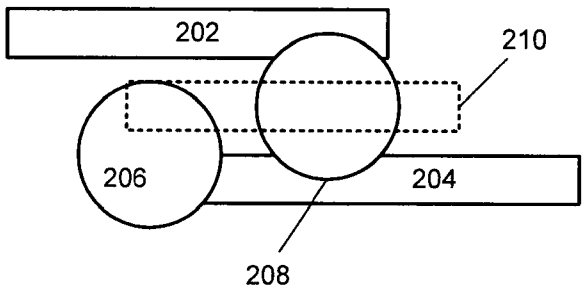


FIG. 2A

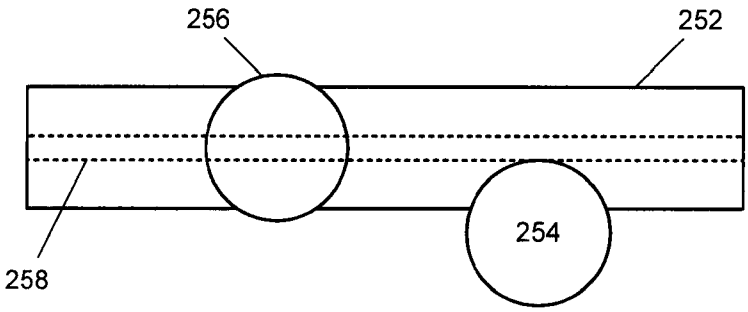


FIG. 2B

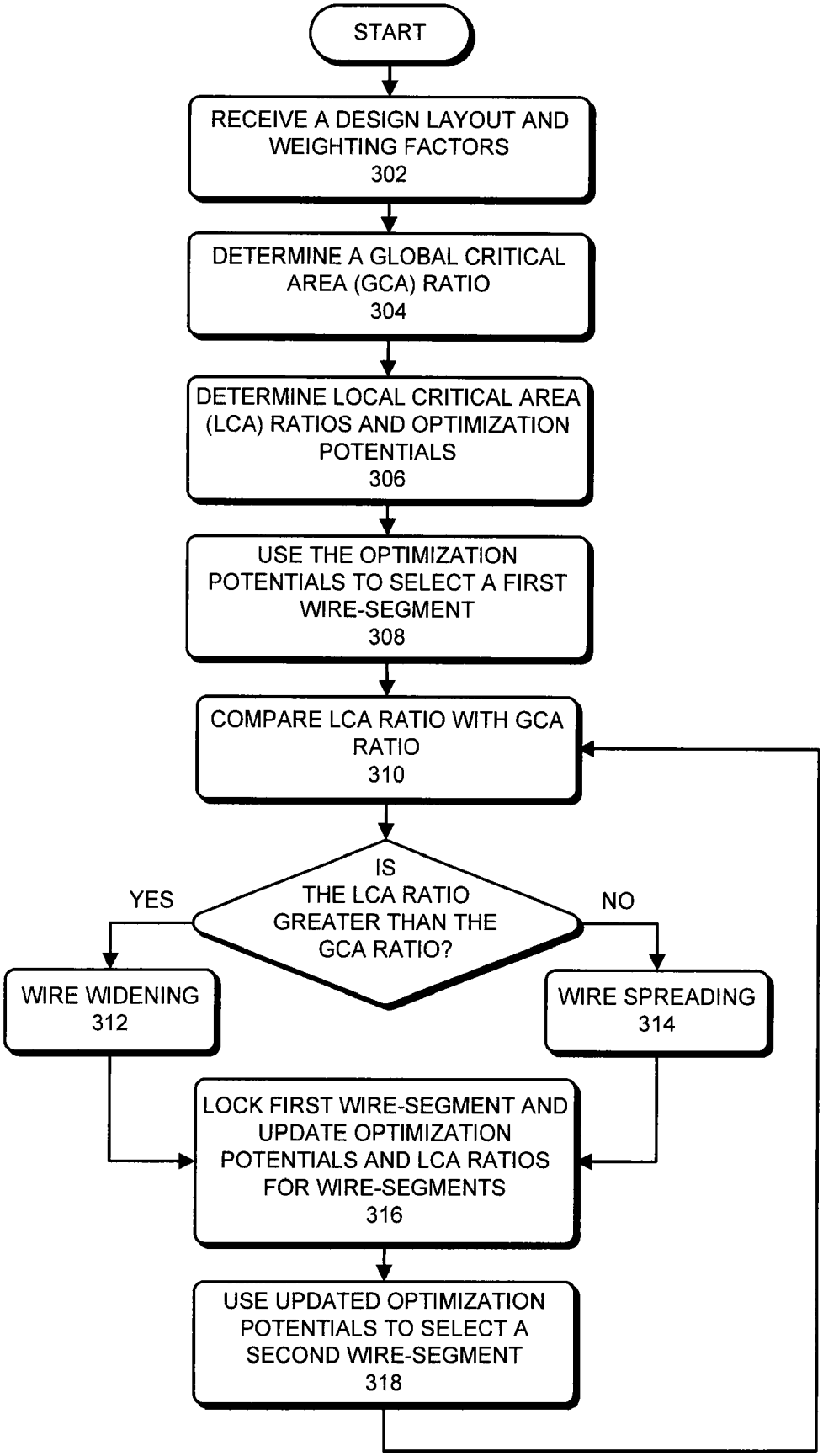
START
RECEIVE A DESIGN LAYOUT AND WEIGHTING FACTORS
302
DETERMINE A GLOBAL CRITICAL AREA (GCA) RATIO
304
DETERMINE LOCAL CRITICAL AREA (LCA) RATIOS AND OPTIMIZATION POTENTIALS
306
USE THE OPTIMIZATION POTENTIALS TO SELECT A FIRST WIRE-SEGMENT
308
COMPARE LCA RATIO WITH GCA RATIO
310
IS THE LCA RATIO GREATER THAN THE GCA RATIO?
YES
NO
WIRE WIDENING
312
WIRE SPREADING
314
LOCK FIRST WIRE-SEGMENT AND UPDATE OPTIMIZATION POTENTIALS AND LCA RATIOS FOR WIRE-SEGMENTS
316
USE UPDATED OPTIMIZATION POTENTIALS TO SELECT A SECOND WIRE-SEGMENT
318

FIG. 3

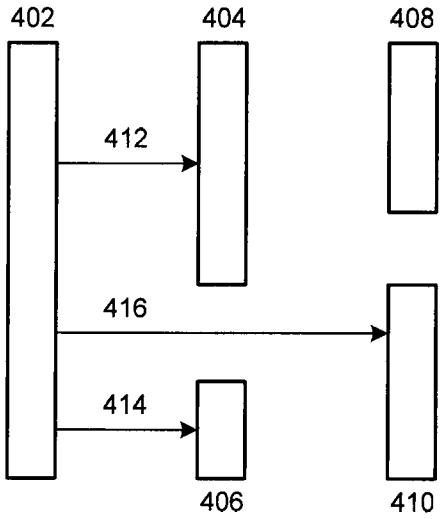


FIG. 4

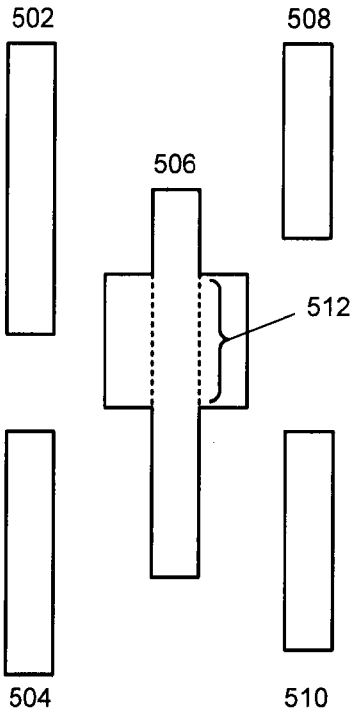


FIG. 5

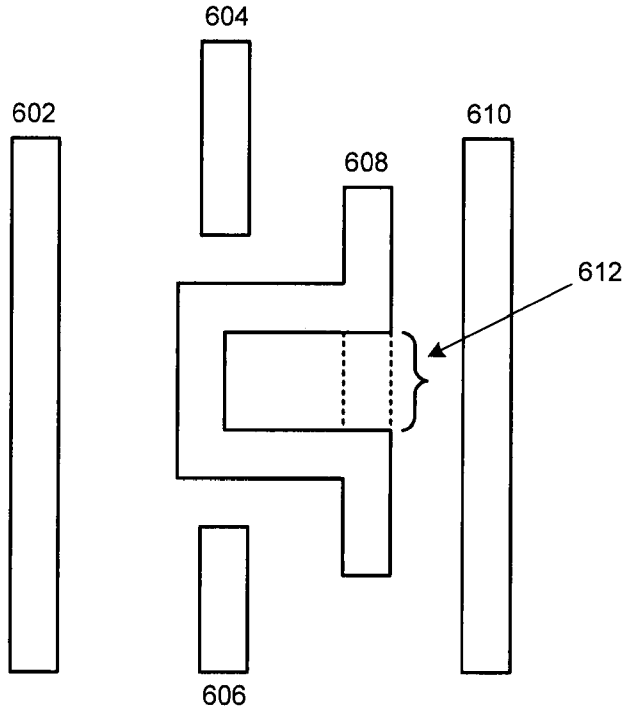


FIG. 6

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/051333

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F17/50

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| P,X | SUBARNA SINHA ET AL: "A New Flexible Algorithm for Random Yield Improvement" QUALITY ELECTRONIC DESIGN, 2007. ISQED '07. 8TH INTERNATIONAL SYM POSIUM ON, IEEE, PI, 26 March 2007 (2007-03-26), pages 795-800, XP031074134 ISBN: 978-0-7695-2795-6 the whole document<br>-----<br>-/-- | 1-21 |

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 24 June 2008 | 30/06/2008 |

| Name and mailing address of the ISA/ | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2<br>NL - 2280 HV Rijswijk<br>Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,<br>Fax: (+31-70) 340-3016 | Alonso Nogueiro, L |

# INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/051333

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | JIN-TAI YAN ET AL: "Timing-Constrained Yield-Driven Wiring Reconstruction for Critical Area Minimization" VLSI DESIGN, 2007. HELD JOINTLY WITH 6TH INTERNATIONAL CONFERENCE ON E MBEDDED SYSTEMS., 20TH INTERNATIONAL CONFERENCE ON, IEEE, PI, 1 January 2007 (2007-01-01), pages 899-906, XP031044516 ISBN: 978-0-7695-2762-8 the whole document | 1-21 |
| A | US 2006/095877 A1 (SU QING [US] ET AL) 4 May 2006 (2006-05-04) paragraph [0085] - paragraph [0095] | 1-21 |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2008/051333

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 2006095877 A1 | 04-05-2006 | US 2007192751 A1 | 16-08-2007 |