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(54) Title: ROBUST ESD CELL

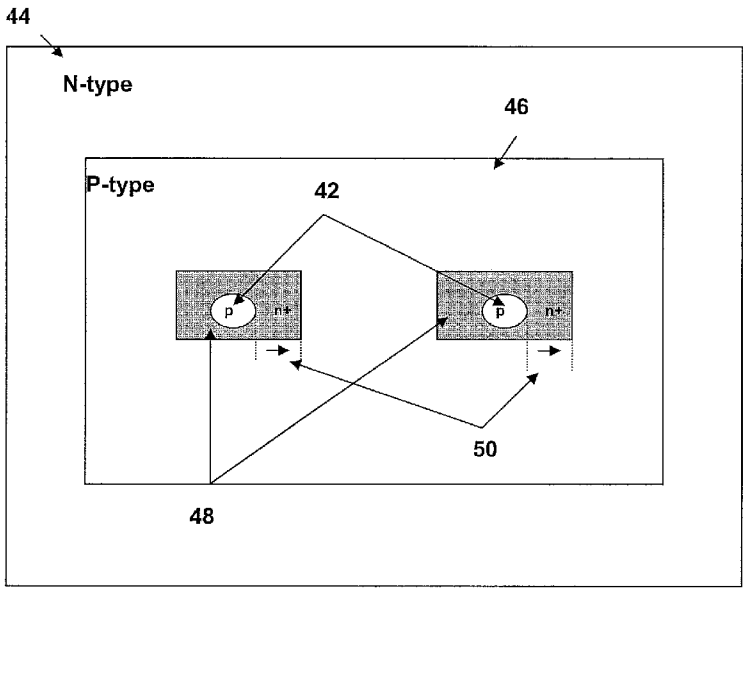

FIG. 3

(57) Abstract: An electric discharge device includes a bipolar transistor configuration comprising a base (46), an emitter (48), and a collector (44). At least one pinched resistor (50) is formed in a region comprising both the base and emitter so as to produce a pinched resistive area that develops a voltage once the bipolar transistor experiences junction breakdown.

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ROBUST ESD CELL

PRIORITY INFORMATION

The present application claims priority to U.S. Utility Application No. 11/697,814, filed on April 9, 2007, which is incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

The invention relates to the field of ESD cells, in particular to an ESD cell having a pinched resistive area.

FIG. 1 is a cross-sectional view of a conventional bipolar transistor-based ESD protection structure 10. Conventional bipolar transistor-based ESD protection structure 10 includes a P-type substrate 12, an N-type collector region 14, a P-type base region 16 (e.g., a P-type Si--Ge base region) and an N-type polysilicon emitter 18. The conventional bipolar transistor-based ESD protection structure 10 also includes electrical isolation regions 20 and 22. A metal base contact 24 makes contact with the P-type base region 16 via polysilicon line 26. A metal emitter contact 28 is in contact with the N-type polysilicon emitter 18, while a metal collector contact 30 is in contact with the N-type collector region 14. The metal base contact 24, the metal emitter contact 28 and the metal collector contact 30 each extends through dielectric layer 32.

Electrical schematics illustrating this conventional bipolar transistor-based ESD protection structure 10 arranged in a grounded base bipolar transistor-based ESD protection device and a Zener Triggered bipolar transistor-based ESD protection device are provided in FIGS. 2A and 2B, respectively.

SUMMARY OF THE INVENTION

According to one aspect of the invention, there is provided an electric discharge device (ESD). The ESD includes a bipolar transistor configuration comprising a base, an emitter, and a collector. At least one pinched resistor is formed in a region comprising both the base and emitter so as to produce a pinched resistive area that develops a voltage once the bipolar transistor experiences junction breakdown.

According to another aspect of the invention, there is provided a method of forming an electric discharge device. The method includes providing a bipolar transistor configuration comprising a base, an emitter, and a collector. Also, the method includes forming at least one pinched resistor in a region comprising both the base and emitter so as to produce a pinched resistive area that develops a voltage once the bipolar transistor experiences junction breakdown.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a conventional ESD device;

FIGs. 2A-2B are circuit diagrams representing conventional ESD devices;

FIG. 3 is a schematic diagram illustrating a top view of the inventive ESD device;

FIG. 4 is a schematic diagram illustrating a top view of another of the inventive ESD device; and

FIG. 5 is a circuit diagram representing the inventive ESD device.

DETAILED DESCRIPTION OF THE INVENTION

The invention involves the use of a pinched resistive area that develops a voltage once junction breakdown occurs.

FIG. 3 shows the inventive ESD device 40 having a pinched resistive area 50. The ESD 40 includes a N-type collector region 44, a P-type base region 46, and N+-type emitter regions 48. Note the ESD device 40 resembles that of a bipolar transistor based ESD device. In other embodiments, the ESD device 40 can include a P-type material collector, a N-type base, and P+-type emitter.

The invention includes a pinched resistive region 50 formed under the emitter regions 48 and the exposed P-type materials comprising the hole 42 and base region 46. A hole 42 is formed in an area comprising the emitter regions 48 leaving an exposed region of the base region 46. The materials inside the hole 42 is connected to the emitter region 48 using an interconnect, such as Al or the like. The collector 44 is connected to a respective node to be protected and the hole 42 and the emitter regions 48 can be connected to ground. Another way also is the hole 42 and the emitter regions 48 can be connected to a node to be protected and the collector 44 can be connected to a positive supply.

In this embodiment, the hole 42 is circular shaped however in other embodiments the shape can vary depending on how much resistance is needed and materials used to form the hole 42, thus one can control the resistive value of the ESD device 40.

The pinched resistive region 50 develops a voltage once junction breakdown occurs. If the voltage that is generated across the pinched resistive region 50 is of sufficient magnitude, it will forward bias the pn junction between the base region 46 and

emitter regions 48, which creates a normal bipolar transistor action so as to allow current to flow only thru the pinched resistive region. The excess current is pumped into the collector region 44. Note the ESD device 40 resembles a bipolar transistor. The result of such a configuration is reduced surface power density and faster turn-on of the ESD device 40 which yields higher reliability and higher ESD rating.

FIG. 4 shows the top view of the inventive ESD device 51. The ESD device 51 includes a collector region 52 which is n-type. The collector region includes a base region 54 that includes emitter regions 58. Each of the emitter regions 58 includes a hole 60 which produces pinched resistive regions similar to pinched resistive region 50, as shown in FIG. 3. In other embodiments, the number of emitter regions 58 can vary depending on the size of base region 54. As more pinched resistive regions are formed on a base-emitter region the more uniform the injection of the protection device become. In this embodiment, the hole 60 is circular shaped however in other embodiments the shape can vary depending on how much resistance is needed and materials used to form the base region 54, thus one can control the resistive value of the ESD device 51.

FIG. 5 shows a circuit representation of the inventive ESD device 70. The ESD device 70 includes a bipolar transistor 72 and a pinched resistor 74. The bipolar transistor includes a collector 76, an emitter 78, and a base 80. The base 80 of the transistor 72 is coupled to the pinched resistor 74. The pinched resistor 74 is also coupled to the emitter 78 of the bipolar transistor 72. Note the emitter 78 can be coupled to ground and the collector 76 can be coupled to a voltage source.

The pinched resistor 74 develops a voltage once junction breakdown occurs. If the voltage that is generated across the pinched resistor 74 is of sufficient magnitude, it

will forward bias the pn junction between the base 80 and emitter 78, which creates a normal bipolar transistor action. The excess current is pumped into the collector 78.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. An electric discharge device (ESD) comprising:

a bipolar transistor configuration comprising a base, an emitter, and a collector; and

at least one pinched resistor that is formed in a region comprising both said base and emitter so as to produce a pinched resistive area that develops a voltage once said bipolar transistor experiences junction breakdown so as to allow current to flow only thru said pinched resistive region.

2. The ESD of claim 1, wherein said pinched resistor is formed using at least one circular shape opening on said emitter.

3. The ESD of claim 1, wherein said pinched resistor is formed using a plurality of circular shape openings on said emitter.

4. The ESD of claim 1, wherein said voltage forward a pn junction formed by said base and emitter.

5. The ESD of claim 3, wherein said circular shape openings comprise the same materials said base.

6. The ESD of claim 1, wherein said collector comprises N-type materials.

7. The ESD of claim 6, wherein said base comprises P-type materials.

8. The ESD of claim 7, wherein said emitter comprises N+-type materials.

9. The ESD of claim 1, wherein said collector comprises P-type materials.

10. The ESD of claim 9, wherein said base comprises N-type materials.

11. The ESD of claim 10, wherein said emitter comprises P+-type materials.

12. A method of forming an electric discharge device (ESD) comprising:

providing a bipolar transistor configuration comprising a base, an emitter, and a collector; and

forming at least one pinched resistor in a region comprising both said base and emitter so as to produce a pinched resistive area that develops a voltage once said bipolar transistor experiences junction breakdown.

13. The method of claim 12, wherein said pinched resistor is formed using at least one circular shape opening on said emitter.

14. The method of claim 12, wherein said pinched resistor is formed using a plurality of circular shape openings on said emitter.

15. The method of claim 12, wherein said voltage forward a pn junction formed by said base and emitter.

16. The method of claim 14, wherein said circular shape openings comprise the same materials said base.

17. The method of claim 1, wherein said collector comprises N-type materials.

18. The method of claim 17, wherein said base comprises P-type materials.

19. The method of claim 18, wherein said emitter comprise N+-type materials.

20. The method of claim 12, wherein said collector comprises P-type materials.

21. The method of claim 20, wherein said base comprises N-type materials.

22. The method of claim 21, wherein said emitter comprises P+-type materials.

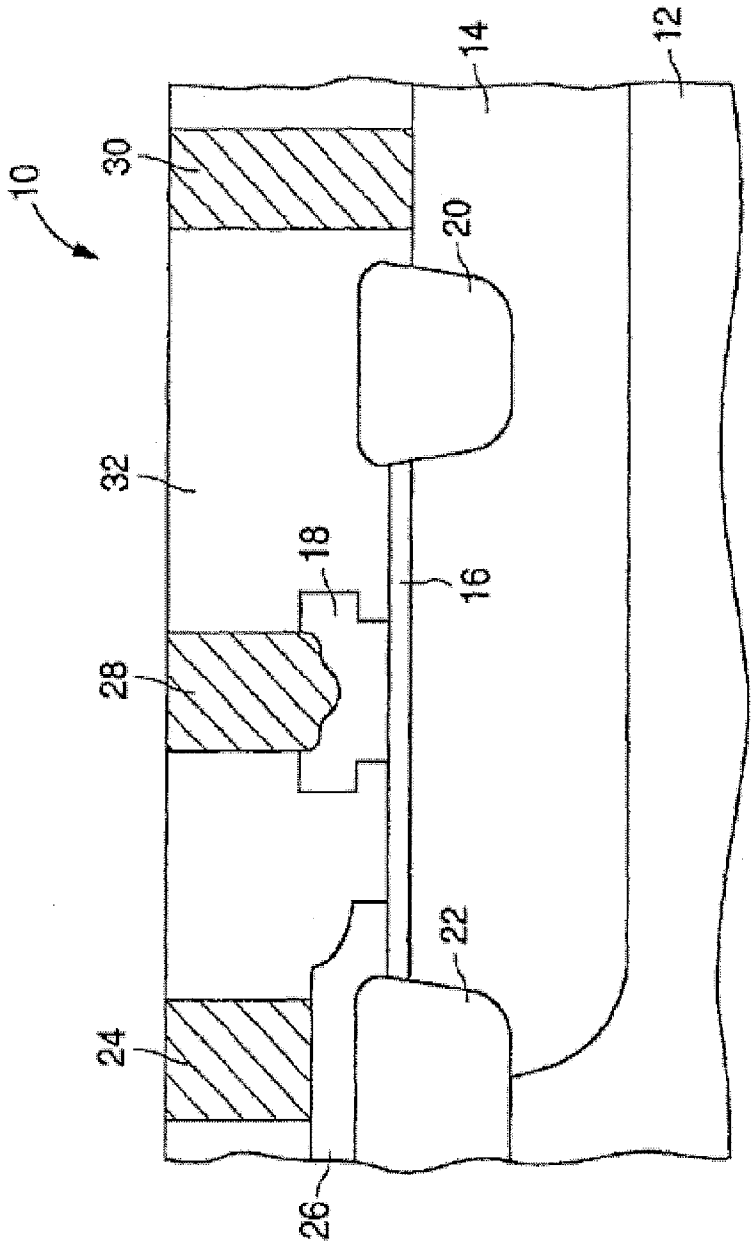

FIG. 1
(PRIOR ART)

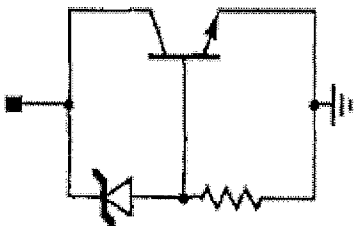

FIG. 2B
(PRIOR ART)

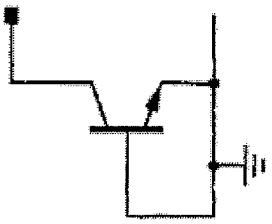

FIG. 2A
(PRIOR ART)

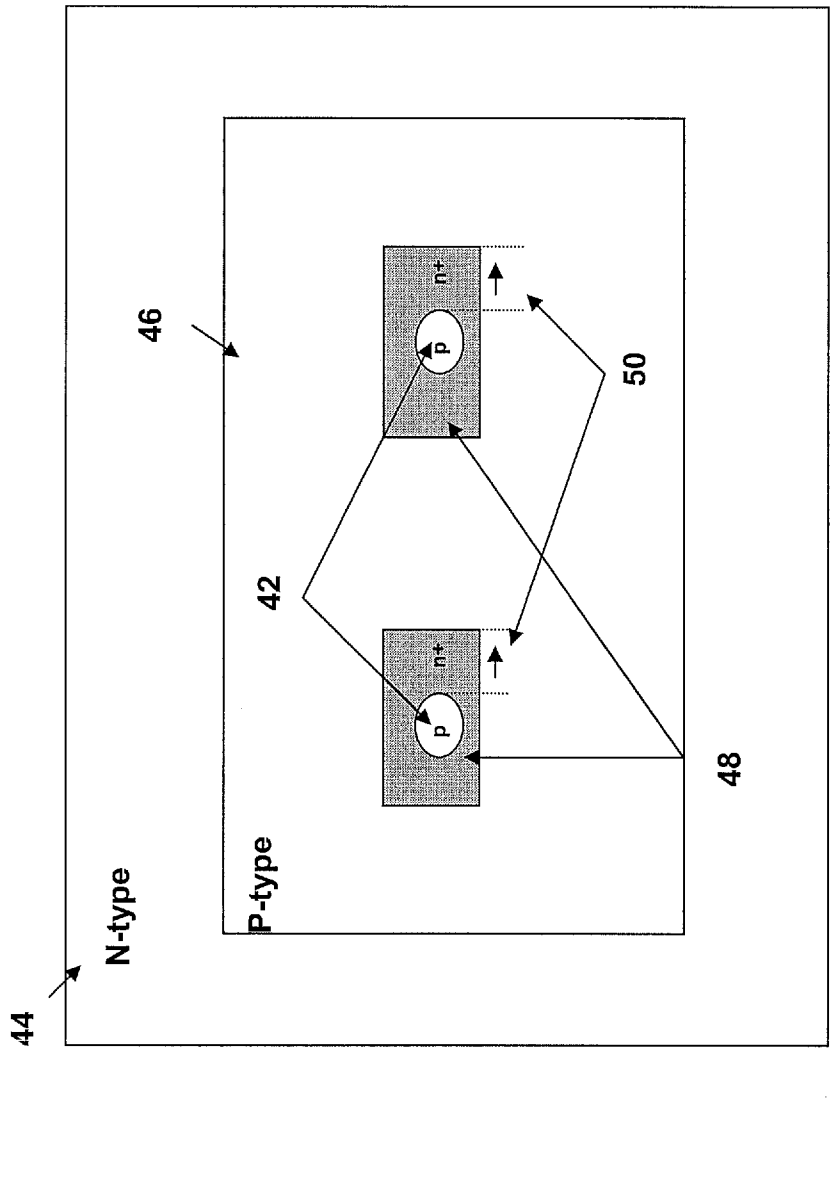

FIG. 3

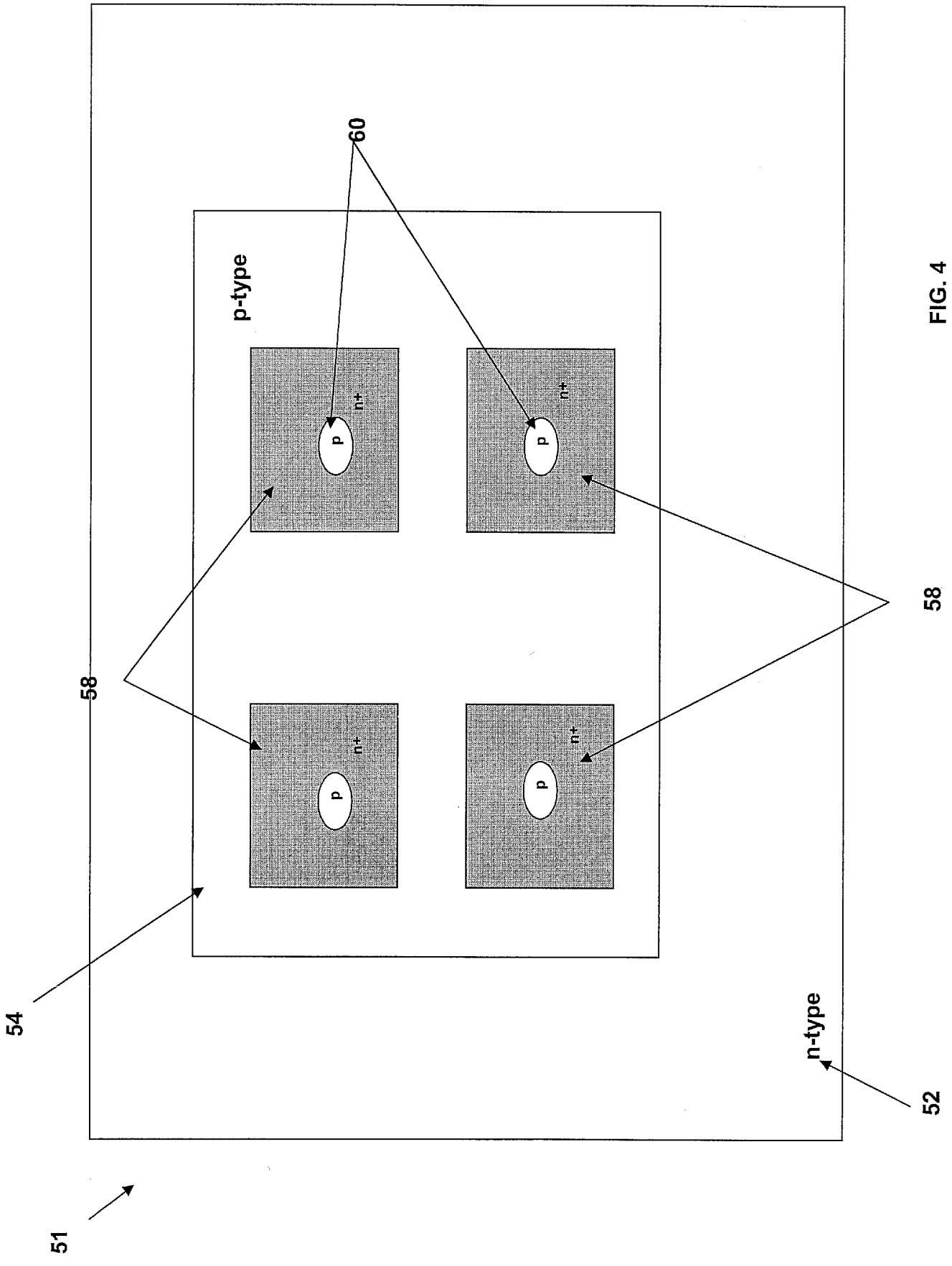

FIG. 4

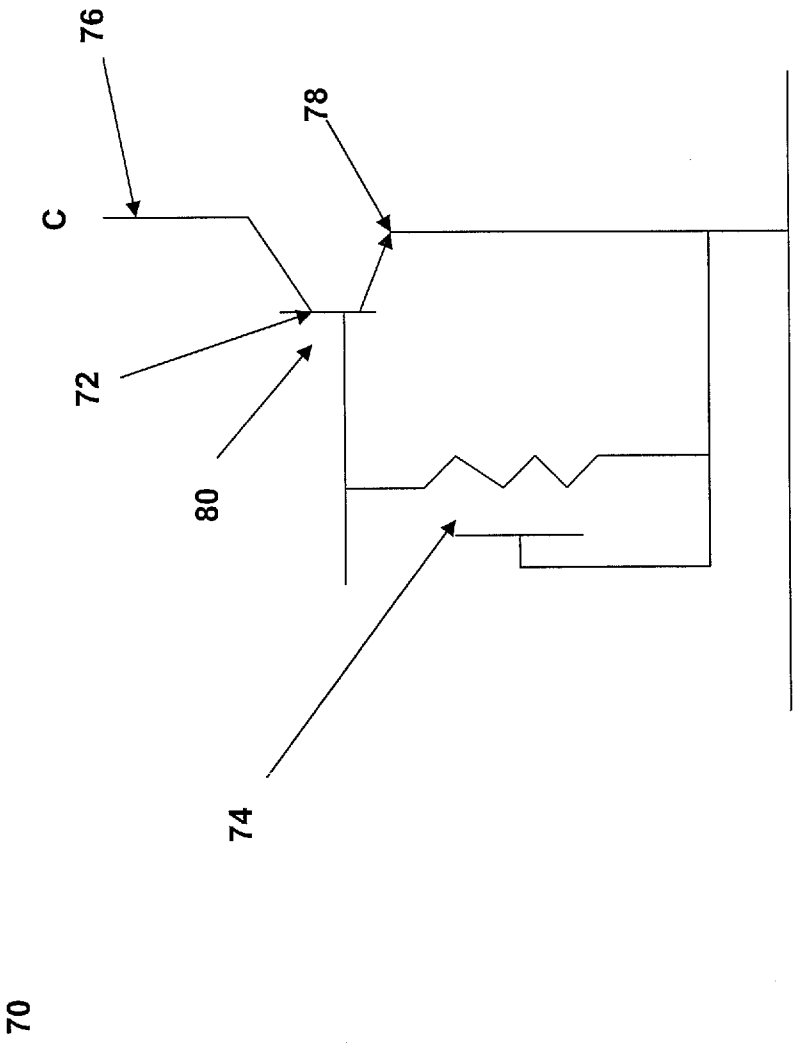

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2008/059538

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/329 H01L21/331 H01L29/73 H01L29/732 H01L29/861
ADD. H01L29/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 22 06 353 A1 (MOTOROLA INC [US]) 26 October 1972 (1972-10-26) the whole document	1-22
X	JP 2005 235844 A (FUJI ELEC DEVICE TECH CO LTD) 2 September 2005 (2005-09-02) paragraphs [0003] - [0009]; figures 5,7	1-22
X	JP 58 199563 A (SANYO ELECTRIC CO; TOKYO SANYO ELECTRIC CO) 19 November 1983 (1983-11-19) * English abstract and figures *	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 June 2008	07/07/2008

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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