(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 January 2009 (22.01.2009)

PCT

(10) International Publication Number
WO 2009/010476 A1

(51) International Patent Classification:
H02M 3/158 (2006.01)

(21) International Application Number:
PCT/EP2008/059127

(22) International Filing Date: 11 July 2008 (11.07.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2007/0509 13 July 2007 (13.07.2007) IE

(71) Applicant *(for all designated States except US)*: **POWERVATION LIMITED** [IE/IE]; Block 1, International Science Centre, National Technolog Park, Castletroy, Limerick (IE).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **RINNE, Karl** [DE/IE]; Ballysallagh, Kinsalebeg, Youghal, Cork (IE). **RUSSELL, Antoin** [IE/IE]; "Rocklands", Coolreiry, Castleconnell, Limerick (IE).

(74) Agent: **HANNA, MOORE & CURLEY**; 13 Lower Lad Lane, Dublin D2 (IE).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,

[Continued on next page]

(54) Title: A POWER CONVERTER

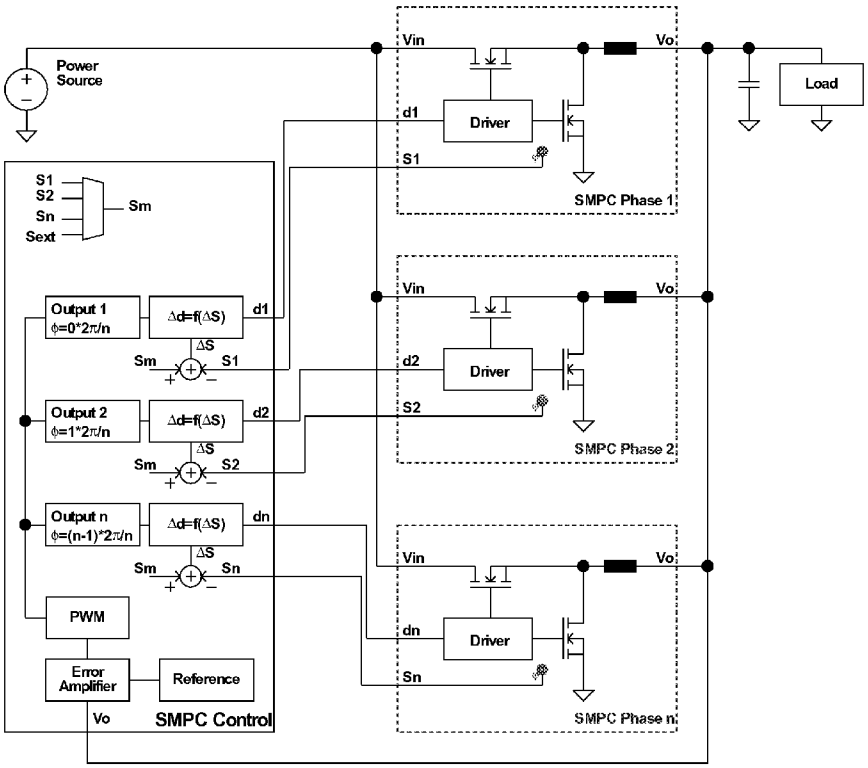

Fig. 1

(57) Abstract: The present invention relates to power converters of the type known generally as switch mode power converters (SMPCs). In particular, the present invention addresses the problem of reducing thermal stress across the phases of a multi phase converter. Specifically, a method of controlling a multi-phase switch mode power arrangement is provided. The mult-phase arrangement comprises a plurality of phases configured to deliver DC power to a common load. The method comprises the steps of: determining the thermal stress of each phase and controlling the share of DC power provided by the individual phases in an effort to equalise the thermal stress across the individual phases.

WO 2009/010476 A1

FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

A Power Converter

Introduction

The invention relates to power converters, particularly switch mode power converters (SMPCs).

In order to function, electronic components, circuits and systems require electrical power. This power is taken from a power source (AC mains, battery, solar panel), conditioned by a power converter, and delivered to a load. Power converters can be implemented in either a linear fashion, or in switch-mode technology. Switch-mode power converters (SMPCs) are becoming increasingly popular because of their inherently high power conversion efficiency. SMPCs are most fundamental components in electronic systems, and commonly determine their ergonomics as well as overall usefulness. The present application is directed to SMPC's which convert a DC voltage to a DC voltage and are referred to generically as DC-DC converters.

In many applications, such as processors and other complex digital circuits, DC-DC converters need to supply large currents. For a number of reasons (e.g. availability of power handling components, component dimensions, reliability, transient performance) it is common practice to provide the power to the circuit from a plurality of switch mode circuits having their outputs connected in parallel to provide power to a common load. Each switching circuit is said to supply a phase. The phases may be provided with a common controller or individual controllers or indeed a combination of the two. In aby event, it will be appreciated that the output phases are in parallel such that the phases feed a common load, and each of the phases contributes to the overall output current supplied to the load circuitry. The most typical implementation is that of a multi-phase buck converter, although other arrangements and topologies are also known. Each of the phases typically consists of active switches and an inductor.

It is important that the individual phases share the work of supplying current to the load so as average out component stresses, and thereby maximize system reliability.

Thus in a typical arrangement, one of the design goals is that each of the SMPC phases contributes a defined ratio of the total output current. Most typically, SMPC designers attempt to have the SMPC phases to contribute the same amount of output current ("current sharing"). A number of techniques are available in order to achieve a degree of current sharing, including both passive current sharing, and active current sharing. Passive current sharing relies on matching of drive signals and power handling components, and achieves current share imbalances of around 10%. Active current share schemes actively measure phase currents, and actively adapt the drive signals such that current share imbalances are minimised. Imbalances of 3% or less are achievable. It is also known to include safety features to switch off individual phases where operating conditions exceed their safe window of operation, for example in the event of overheating or component failure.

The present application seeks to improve upon the reliability of these arrangements.

Summary

Although the prior art methods seek to maximise reliability by trying to ensure that each phase provides its share of the load current, in reality the thermal stress of each phase is determined by more factors than just the output current provided by the phase. Due to electrical and mechanical system limitations and mismatches, each phase in a real system experiences different thermal paths and thermal impedances. As a consequence, the thermal stress arising in each phase may be very different notwithstanding that the phases may share the output current equally. As an example, in a system with fan-assisted forced air convection, the phase experiencing the highest air velocity and most air turbulence may be significantly cooler than the phase located furthest away from the fan. In a real system, the differences in thermal hotspot temperatures may reach values of 20°C, and sometimes more.

The random failure rate of an electronic system is governed by the Arrhenius' relationship. Assuming typical activation energy coefficients, Arrhenius' relationship means that the failure rate of an electronic device or system doubles with about every

10°C increase in its hotspot temperature. Using above numerical example, in a multi-phase SMPC, the hottest phase operating at a temperature of 20°C above the hotspot temperature of the coolest phase will have an expected failure rate four times higher than coolest phase notwithstanding that each phase may be providing equal current to the load. Accordingly, system failure rates will be higher than expected.

Accordingly, the present application addresses this problem by seeking to adjust the load sharing nature of individual phases with reference to their thermal stresses.

Accordingly, in a first embodiment there is provided a switch mode power converter for conditioning and delivering power to a load in a plurality of phases, and a controller, wherein the controller modifies phase outputs according to thermal stresses of the phases.

In one embodiment, the controller dynamically modifies the phase outputs according to sensed temperature.

In another embodiment, the power converter comprises temperature sensors linked with the controller.

In a further embodiment, the sensors are located at hot spots.

In one embodiment, the controller modifies the phase outputs so that induced thermal stress in a phase is an equal proportionate stress relative to the phase's maximum thermal capability.

In another embodiment, the controller operates to equalise thermal stress between phases.

In a further embodiment, the controller performs closed-loop control of the phase duty cycles.

In one embodiment, the controller dynamically elects a thermal stress signal as a master stress signal, and the converter comprises a modulator to modify duty cycles of the phases by amounts determined by differences between thermal stress of a phase the master thermal stress.

In another embodiment, the modulator comprises an integrating error amplifier. These and other embodiments will become apparent from the detailed description and claims which follow.

Detailed Description of the Invention

The invention will be more clearly understood from the following description of an embodiment thereof, given by way of example only with reference to the accompanying drawings in which:-

Fig. 1 is a block diagram of an exemplary multi-phase SMPC of the invention.

The invention provides a switch mode power arrangement for delivering DC power to a load which includes a stress share scheme which distributes thermal stress of individual phases across common phases. It will be appreciated that each of these phases may be controlled by individual controllers or a single controller may control multiple phases or any combination of these. Similarly, there may be one master controller and several slave controllers or a variety of different control configurations.

A temperature (thermal stress) measurement is carried out at a suitable location in each phase (typically close to the thermal hotspot). In this respect, the hotspot in a phase is generally a switching transistor(s). The temperature may be measured directly, for example by means of a sensor such as a thermistor or similar device. Alternatively, a device parameter in the phase circuit may be monitored to provide an indirect measurement of the thermal stress, e.g. by detecting changes in on-resistance or gate voltages in a switching transistor.

In one exemplary arrangement, the temperature is reported back to a central SMPC controller. The SMPC controller modifies the phase drive signals in a suitable fashion in order to distribute the thermal stress between phases in a defined manner. Each phase then provides a portion of the output current such that the induced thermal stress is an equal proportionate stress relative to the phase's maximum thermal capability so that in a typical application, the thermal stress between phases may be equalised. Compared to state of the art multi-phase SMPC employing passive or active current sharing, the invention substantially increases the overall reliability of the SMPC by reducing the peak temperature stress.

Referring to Fig. 1, the output of a multi-phase DC-DC SMPC supplies a DC voltage to a load. Here, the multi-phase SMPC is a synchronous buck converter utilising *n* phases. The n-phase buck converter itself is fed by a power source (which may be a battery, ac-dc converter, or similar). The n-phase buck converter is controlled by a SMPC controller. Each phase of the SMPC consists of a pair of switches and an inductor. Phase currents are filtered by one or more common output capacitors. The output voltage *Vo* is well regulated and predominantly DC, with a small high frequency ripple corresponding to the switching frequency.

Regulation of the output voltage is achieved through closed-loop control by the SMPC controller by means of controlling the required duty cycle *d*. The SMPC controller senses the output voltage *Vo*, compares it to a reference value, amplifies and compensates the error signal, and modifies the duty cycle *d*. Duty cycle *d* is fed to the driver of each phase. Those skilled in the art will be aware of the benefits of phase-shifting the drive signals by a certain phase angle. Thus in a phase shifted converter, the first phase output *d1* will be driven without phase shifting (ϕ=0) with all subsequent phase outputs *dk* (*d2-dn*) be driven with a phase delay of ϕ=k*2π/*n* relative to the preceding phase output.

The thermal stress of each of the phases is sensed, and reported back to the SMPC controller (signals *S1-Sn*). Various methods for temperature measurement may be used. The temperature of the phase is taken at or near the phase's hotspot temperature.

In one arrangement, the SMPC controller dynamically elects one of the thermal stress signals through a multiplexer to become the master thermal stress signal *Sm*. In an alternative embodiment, the SMPC controller averages all thermal stress signals *S1-Sn*, and produces an averages *Sm*.

The stress master signal *Sm* is distributed to the phase control module. The relationship between a change in duty cycle, and a change in output current per phase is either known, or may be approximated. In turn, the relationship between output current per phase and thermal stress per phase can be determined. It will be appreciated that both relationships but particularly the latter, may be highly non-linear. Nevertheless, a relationship between a change in duty cycle per phase and a change in thermal stress of this phase can be determined or estimated.

In the exemplary circuit shown, each output of the SMPC controller has an independent modulator modifying the duty cycle Δd by an amount determined by the difference of the thermal stress of the module to the stress master signal. Using suitable techniques (such as an integrating error amplifier) the difference between module thermal stress and master thermal stress may be minimised.

Thus, as will be clear from the exemplary embodiment, the invention leads to a superior stress share scheme, through reduced peak temperatures leading to improved SMPC system reliability through reduced random temperature-induced failure rates.

It may be necessary to limit Δd that each stress error amplifier may cause in order to improve system behaviour during abnormal situations. In the event of a fault situation, the stress signals *Sk* of the known faulty phase may be excluded from becoming the master signal. In complex systems employing multiple SMPC controllers, stress signals may be distributed to some or all SMPC controllers using suitable analogue or digital buses.

Although, the present application has been described with reference to a control schema in which the phase outputs are controlled with respect to thermal stress, it will be appreciated that other stresses, for example voltage stress, may be experienced by the individual phases. Accordingly, whilst the above application has been described with reference to control based on thermal stresses, it will be appreciated that this schema may readily be modified to account for the measurement and control of additional stresses. In such a modified control schema, the different stresses experienced by a phase may be applied as control inputs in addition to the thermal stress in a weighted fashion so that the control system seeks to equalise each of the measured stresses across the phases. It will be appreciated that in such a scenario, whilst the control algorithm will be attempting to equalise the thermals stresses across the loads, that attempts to equalise other stresses may mean that the thermal stresses are not equalised across the loads despite the efforts of the controller.

The invention is not limited to the embodiments described but may be varied in construction and detail. For example, the controller may modify the phase outputs in a less dynamic manner, once per start-up for example or after a period when normal operating temperatures have been achieved. Moreover, it will be appreciated generally, that adjustment for different thermal stresses may by virtue of the time contstants involved be slower than adjustments for output voltage changes. Also, the controller may rely on expected or modelled thermal stresses rather than sensed temperature. Similarly, whilst the embodiment has been described in terms of an overall arrangement, it will be appreciated that individual phases, controllers and modulators may be provided as individual items, either in discrete or integrated circuit form, for assembly into an overall arrangement and that the scope of protection extends to these individual items and is not limited to the overall arrangement.

Claims

1. A method of controlling a multi-phase switch mode power arrangement, comprising a plurality of phases configured to deliver DC power to a common load, the method comprising the steps of: determining the thermal stress of each phase and controlling the share of DC power provided by the individual phases in an effort to equalise the thermal stress across the individual phases.

2. A method according to claim 1, wherein the thermal stress of each phase is determined by a co-located temperature sensor.

3. A method according to claim 2, wherein the individual temperature sensors are positioned to measure the temperature of the switching elements of the phases.

4. A method as claimed in any preceding claim, wherein the controller modifies the phase outputs so that induced thermal stress in a phase is an equal proportionate stress relative to the phase's maximum thermal capability.

5. A method as claimed in any preceding claim, wherein the controller controls the share of DC power by performing closed-loop control of the phase duty cycles of the individual phases.

6. A method as claimed in any preceding claim wherein the thermal stress of one phase is dynamically elected as a master thermal stress, and the duty cycles of the individual phases are adjusted by amounts determined by differences between their individual thermal stress and that of the master thermal stress.

7. A switch mode power arrangement for delivering DC power to a load, the arrangement having a plurality of phases sharing the supply of power to the load, wherein the arrangement is configured in response to the determined thermal stresses of individual phases to adjust the share of power provided by the individual phases in an effort to equalise the thermal stresses across the plurality of phases..

8. A switch mode power arrangement as claimed in claim 7, wherein the arrangement dynamically adjusts the share of power provided by individual phases according to the sensed temperature of each phase.

9. A switch mode power arrangement as claimed in claim 7, wherein each phase comprises a controller and a temperature sensor linked with the controller.

10. A switch mode power arrangement as claimed in claim 9, wherein the sensors are located at hot spots.

11. A switch mode power arrangement as claimed in any one of claims 7 to 10, wherein the arrangement is configured to modify the phase outputs so that induced thermal stress in a phase is an equal proportionate stress relative to the phase's maximum thermal capability.

12. A switch mode power arrangement as claimed in any one of claims 7 to 11, wherein the arrangement is configured to perform closed-loop control of the phase duty cycles.

13. A switch mode power arrangement as claimed in any one of claims 7 to 12, further comprising a primary controller providing a duty cycle signal to each phase.

14. A switch mode power arrangement according to claim 13, wherein a temperature controller configured to receive a sensed temperature signal from each phase.

15. A switch mode power arrangement according to claim 14, wherein the temperature controller is configured to dynamically elect a thermal stress

signal from the received sensed signals as a master stress signal.

16. A switch mode power arrangement according to claim 14, wherein the temperature controller is configured to average the received sensed signals to provide a master stress signal.

17. A switch mode power arrangement according to claim 15 or 16, further comprising at least one modulator for modifying the duty cycle of a phase by an amount determined by the differences between the thermal stress of the phase and the master thermal stress signal.

18. A switch mode power arrangement according to claim 17, wherein each phase has an associated modulator.

19. A switch mode power arrangement according to claim 17, wherein a single modulator adjusts the duty cycle of all phases.

20. A switch mode power converter as claimed in claim 18 or 19, wherein the modulator comprises an integrating error amplifier.

21. A switch mode power arrangement according to anyone of claim 14 to 20, wherein the primary controller and the temperature controller are the same controller.

22. A modulator for switching at least one switching device in a phase of a switch mode multi-phase power arrangement for delivering DC power to a load, wherein the modulator is adapted to receive a communicated duty cycle signal and a communicated thermal stress signal, and whereby the modulator is

responsive to a
a sensed temperature and is adapted to adjust the received duty cycle in response to the difference between the received thermal stress signal and the sensed temperature to provide the adjusted duty cycle to the at least one switching device.

23. A device providing a a phase of a switch mode multi-phase power arrangement comprising:
a modulator in accordance with claim 22,
at least one switching device,
a temperature sensor for sensing temperature in the device to provide the sensed temperature,.

24. A device according to claim 23, wherein the device is configured to communicate the sensed temperature to a central controller.

25. A controller for providing at least one duty cycle signal to individual phases in a multiple phase arrangement, wherein the controller is configured to receive a sensed temperature signal from each phase.

26. A controller according to claim 24, wherein the controller determines a master temperature signal from the plurality of sensed temperature signals.

27. A controller according to claim 24, wherein the controller determines a master temperature signal equating to the average of plurality of sensed temperature signals.

28. A controller according to claim 24, wherein the controller determines a master temperature signal equal to the average of the minimum and maximum sensed temperature signals.

29. A controller according to anyone of claims 25 to 27, wherein the controller adjusts the duty cycle provided to individual phases in response to the

difference between the sensed temperature signal of the phase and the master temperature signal.

30. A controller according to anyone of claims 25 to 27, wherein the controller provides the master temperature signal to each phase.

31. A switch mode power converter substantially as described herein with reference to and\or as shown in the drawing.

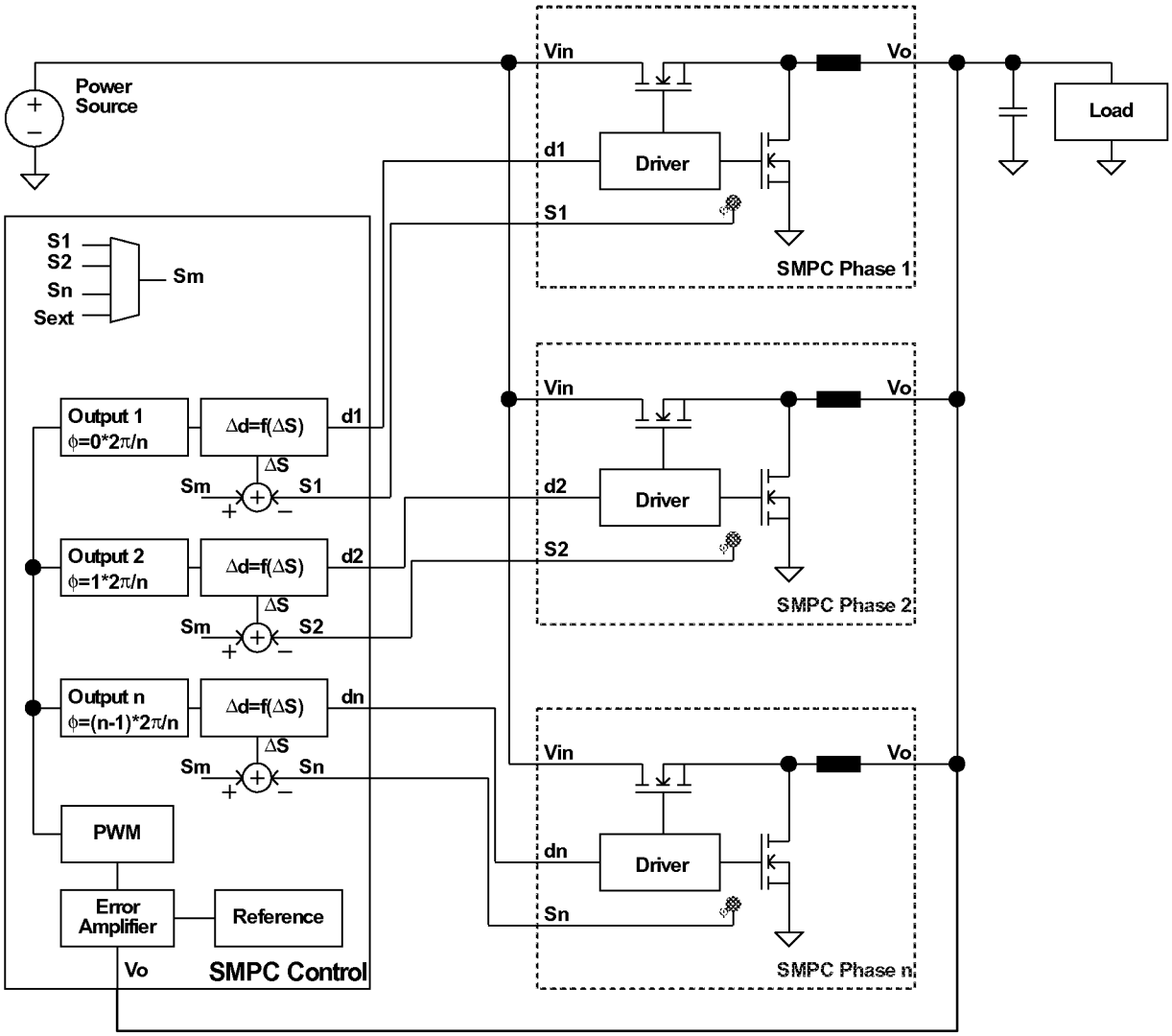
Power Source
Vin
Vo
Load
d1
Driver
S1
SMPC Phase 1
S1
S2
Sn
Sext
Sm
Output 1
ϕ=0*2π/n
Δd=f(ΔS)
d1
ΔS
Sm
S1
Vin
Vo
d2
Driver
S2
SMPC Phase 2
Output 2
ϕ=1*2π/n
Δd=f(ΔS)
d2
ΔS
Sm
S2
Output n
ϕ=(n-1)*2π/n
Δd=f(ΔS)
dn
ΔS
Sm
Sn
Vin
Vo
dn
Driver
Sn
SMPC Phase n
PWM
Error Amplifier
Reference
Vo
SMPC Control

Fig. 1

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2008/059127

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/158

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/044458 A1 (ELBANHAWY ALAN [US]) 18 April 2002 (2002-04-18) the whole document	1-31
X	WO 2007/066676 A (TOYOTA MOTOR CO LTD [JP]; MANABE KOTA [JP]; SHIGE MASAHIRO [JP]) 14 June 2007 (2007-06-14) the whole document	1-31

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
3 October 2008	20/10/2008
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer Imbernon, Lisa

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2008/059127

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002044458 A1	18-04-2002	NONE	
WO 2007066676 A	14-06-2007	JP 2007159315 A	21-06-2007