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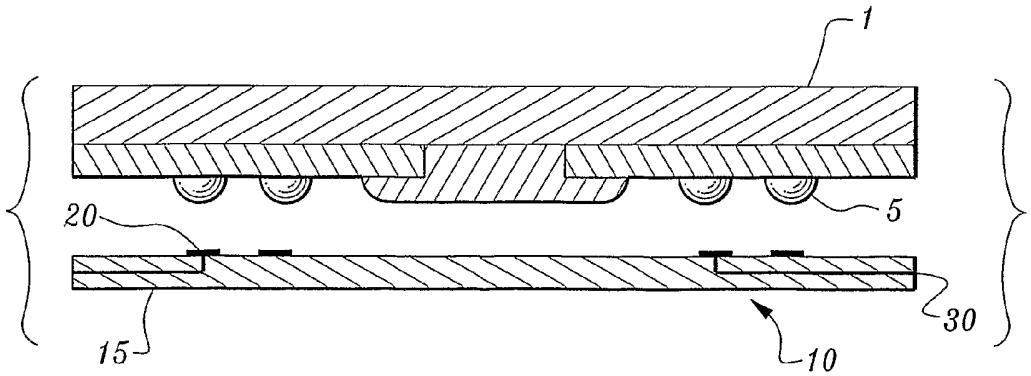
(54) Title: STACKABLE LAYERS CONTAINING BALL GRID ARRAY PACKAGES



(57) Abstract: Layers (35) suitable for stacking in three dimensional, multi-layer modules are formed by interconnecting a ball grid array electronic package (1) to an interposer layer (10) which routes electronic signals to an access plane (45). The layers (35) are under filled and may be bonded together to form a stack (40) of layers (35). The leads (30) on the access plane (45) are interconnected among layers (35) to form a high-density electronic package.

WO 2005/018000 A1

STACKABLE LAYERS CONTAINING BALL GRID ARRAY PACKAGES

REFERENCE TO RELATED APPLICATIONS

This application is related to U.S. Patent Application Serial No. 10/360,244, filed February 7, 2003, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the dense packaging of electronic circuitry and specifically to the stacking of ball grid array (BGA) integrated circuit packages. The invention is also suitable for the stacking of fine ball grid array (FBGA) integrated circuit packages, micro-ball grid array packages and for bump-bonded bare die to form stackable layers which can be combined to form multi-layer electronic modules.

Description of the Background Art

The electronics industry continues to seek smaller, denser electronic packaging. An important advance in this regard has been the use of three-dimensional packaging techniques using stacked bare or packaged integrated circuit die.

Most of the background art disclosures describe methods of stacking multiple unpackaged IC chips. Oguchi et al., U.S. Pat. No. 5,332,922, Miyano et al., U.S. Pat. No. 5,440,171, and Choi et al., U.S. Pat. No. 5,677,569, disclose methods of stacking IC chips within a single package. Jeong et al., U.S. Pat. No. 5,744,827, discloses a new type of custom chip packaging which permits stacking, but which does not allow the use of off-the-shelf packaged IC's. Burns, U.S. Pat. No. 5,484,959, shows a method of stacking TSOP packages which requires multiple leadframes attached above and below each TSOP and a system of vertical bus-bar interconnections, but which does not conveniently allow an expansion of the number of vertically interconnecting leads.

The assignee of this application, Irvine Sensors Corporation, has been a leader in developing high-density packaging of IC chips, for use in focal plane modules and for use in a variety of computer functions such as electronic memory. Examples of Irvine Sensors Corp.'s high-density electronic packaging are disclosed in U. S. Patent Nos. 4,672,737, to Carson, et al.; 5,551,629, to Carson et al.; 5,688,721, to Johnson; 5,347,428 to Carson, et al.; and 6,028,352 to Eide, all of which are fully incorporated herein.

The present invention relates to the stacking of layers containing integrated circuit chips (ICs), thereby obtaining high-density electronic circuitry. In general, the goal of the present invention is to combine high circuit density with reasonable cost. A unique aspect of this invention is that it provides a low cost method of stacking commercially available IC's in BGA packages while allowing the independent routing of several non-common I/O (input/output) signals from upper-level layers to lower layers or to the bottom of the stack. Cost reduction is accomplished by utilizing relatively low cost interposer boards to reroute leads to an access plane and by the ability to stack pre-packaged and pre-tested off-the-shelf BGA packages.

None of the background art addresses the need for compact, dense memory stacks that take advantage of the high speed and small outline of a BGA package that are both low cost and highly reliable. It is therefore an object of the invention to provide a stackable layer formed from a BGA package that can be assembled at a relatively low cost and which is structurally and thermally sound. It is a further object of the invention to provide a stack of BGA layers that can provide high electronic density in a very small volume and which is compatible with a conventional BGA footprint on a printed circuit board. It is yet a further object of the invention to provide a low-cost method for manufacturing a stackable layer incorporating a BGA package and a method for manufacturing a stack of such layers.

SUMMARY OF THE INVENTION

The present invention provides stackable layers which may be interconnected to form a high-density electronic module. This application further discloses a stack of layers electrically interconnected in the vertical direction, suitable for mounting onto a PCB (printed circuit board) or other electronic device. This application further discloses a method for starting with standard BGA packages and manufacturing a stacked IC-containing package using interposer interconnections which are routed in the vertical direction along one or more access planes.

The invention generally consists of BGA packaged die that are electrically interconnected to conductive traces on an interposer board formed from a dielectric material. The interposer board serves to reroute electronic signals from the BGA to the periphery, or access edge, of the interposer. The interposer may have a single layer or multiple layers of conductive traces much like conventional printed circuit board technology.

The BGA package is solder-reflowed to the interposer and under-filled with an epoxy to form a stackable layer. The formed individual layers may then be aligned and bonded to form a multi-layer structure which includes at least one access plane. The conductive traces that terminate at the access edges are lapped and exposed, then rerouted to the desired locations to allow the interconnection of several non-common signals (e.g., chip enable and/or data lines) from an upper layer to a lower layer of a stack of layers.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are a perspective view of ball grid array integrated circuit chip package illustrating, respectively, the top of the package and the ball grid array on the underside thereof;

FIG. 2 plan view of an interposer board with exemplar conductive traces, access leads and solder ball pads formed thereon;

FIG. 3 is a front sectional view of a ball grid array package and interposer board showing the conductive traces, solder balls and solder ball pads;

FIG. 4 is a side sectional view of a ball grid array package and interposer board after the elements have been soldered together and under-filled, creating a stackable layer;

FIG. 5 is a side sectional view of a stack of layers that have been under-filled and bonded and connected a bottom interposer board;

FIG. 6 shows a side view of stack of layers illustrating an access plane with access leads exposed after lapping;

FIG. 7 shows a side view of stack of layers illustrating an access plane with access lead interconnections between access leads on different layers.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the figures where like numerals designate like elements among the several views, FIGS. 1A and 1B show the top and underside, respectively, of a conventional ball grid array (BGA) packaged memory device 1 which includes solder balls 5 for electrical communication of signals and power into and out of the BGA package. Conventional BGA memory packages in fine grid array or micro grid array are readily available from a variety of commercial sources such as MICRON TECHNOLOGIES, INC. or SAMSUNG CORP.

FIG. 2 illustrates an interposer board 10 made of a dielectric material such as BT Resin from Mitsubishi and includes conductive traces 15. Conductive traces 15 include solder ball pads 20 for the receiving of solder balls 5. Conductive traces lead to and terminate at an access edge 25 on the interposer board to form access leads 30.

Conductive traces made of copper or other conductive material are formed on the interposer board in a manner similar to that used in printed circuit board manufacturing. The conductive traces are patterned on the interposer board using conventional photolithography techniques so as to form solder ball pads 20 for the receiving and electrical connection of solder balls 5. The interposer board may include a single layer of conductive traces 15 or, in an alternative embodiment, multiple layers of conductive traces (not shown).

To assemble the device, solder balls 5 of BGA package 1 are aligned and electrically connected to solder ball pads 20 as is shown in FIG. 3. An alternative embodiment includes the use of fine grid BGA packages or even bare die that include ball bonds or that are adapted to be received by the solder ball pads. The BGA package and interposer board are then reflow-soldered using conventional reflow solder techniques. While the solder balls will self-align with the solder ball pads during solder reflow, reflow process controls are critical during soldering, particularly when utilizing fine pitch ball grid array packages. Solder reflow process controls such as those set forth in "MICRON TECHNOLOGY INC. Technical Note TN-00-11 SMT BGA Assembly Design Recommendations" provide guidance for BGA reflow solder processes.

Upon completion of the reflow process, a stackable BGA layer 35 is formed as is illustrated in FIG. 4. The layer is then preferably under-filled with a suitable under-fill

material 36 such as EPOTEK U-300 to provide structural stability and to minimize temperature-related stresses due to CTE mismatch of the interposer board and BGA package. It is preferable to provide sufficient under-fill so as to extend slightly beyond the edge of the BGA package and interposer board as the under-fill eliminates voids along the access edge 25 which will be utilized as discussed further below.

Turning now to FIG. 5, multiple layers 35 may be bonded together using a suitable adhesive or epoxy 37 such as EPOTEK 353 to form a three-dimensional stack 40 of layers 35, forming at least one access plane 45.

Mechanical assembly of multiple layers consists generally of aligning two or more layers 35 in a suitable fixture and bonding together using the appropriate adhesive. After the adhesive has cured, the sides of stack 40 that include access leads 30, i.e., access plane 45, are ground and lapped to expose the access leads as is illustrated in FIG. 6.

FIG. 7 shows how access leads 30 may be rerouted between layers as desired by using conventional photolithography and plating techniques to create conductive interconnecting traces 50. Alternatively, the entire access plane 45 may be metalized or coated with conductive material and the desired access leads isolated or interconnected by selectively removing conductive material using laser ablation, saw-cutting, etching or similar process. It is important that access plane be very planar with no voids to ensure the integrity of the layer interconnects. The stack is preferably encapsulated with a suitable encapsulant to protect interconnecting traces 50.

In this manner a high capacity, multi-layer module is provided that is low cost and which is readily received into existing BGA footprints.

From the foregoing description, it will be apparent the apparatus and method disclosed in this application will provide the significant functional benefits summarized in the introductory portion of the specification.

The following claims are intended not only to cover the specific embodiments disclosed, but also to cover the inventive concepts explained herein with the maximum breadth and comprehensiveness permitted by the prior art.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. Therefore, it must be understood that the illustrated embodiment has been set forth only for the purposes of example and that it should not be taken as limiting the invention as defined by the following claims. For example, notwithstanding the fact the elements of a claim are set forth below in a certain combination, it must be expressly understood that the invention includes other combinations of fewer, more or different elements, which are disclosed above even though not claimed in such combinations.

The words used in this specification to describe the invention and its various embodiments are to be understood not only in the sense of their commonly defined meanings, but to include by special definition in this specification structure, material or acts beyond the scope of the commonly defined meanings. Thus, if an element can be understood in the context of this specification as including more than one meaning, then its use in a claim must be understood as being generic to all possible meanings supported by the specification and by the word itself.

The definitions of the words or elements of the following claims are, therefore, defined in this specification to include not only the combination of elements which are literally set forth, but all equivalent structure, material or acts for performing substantially the same function in substantially the same way to obtain substantially the same result. In this sense it is therefore contemplated that an equivalent substitution of two or more elements may be made for any one of the elements in the claims below or that a single element may be substituted for two or more elements in a claim. Although elements may be described above as acting in certain combinations and even initially claimed as such, it is to be expressly understood that one or more elements from a claimed combination can in some cases be excised from the combination and that the claimed combination may be directed to a sub-combination or variation of a sub-combination.

Insubstantial changes from the claimed subject matter as viewed by a person with ordinary skill in the art, now known or later devised, are expressly contemplated as being equivalently within the scope of the claims. Therefore, obvious substitutions now or later known to one with ordinary skill in the art are defined to be within the scope of the defined elements.

The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptually equivalent, what can be obviously substituted and also what essentially incorporates the essential idea of the invention.

5

CLAIMS

I claim:

1. A stackable layer comprising:
a package containing at least one integrated circuit chip and including at least one terminal on the chip, an interposer board including at least one access edge, means for electrically rerouting the terminals from the chip to the access edge of the interposer board to form at least one access lead.

2. The layer of claim 1 wherein the means for electrically rerouting the at least one terminal from the chip to the access edge include at least one conductive trace in electrical connection with the at least one terminal of the chip.

3. The layer of claim 1 wherein the package is a ball grid array package.

4. The layer of claim 1 wherein the package and interposer board are under-filled after electrical connection.

5. The layer of claim 1 wherein the package is a bare integrated circuit die which includes at least one terminal and adapted so as to be in electrical connection with the means for electrically rerouting the at least one terminal of the bare integrated circuit die to the at least one access edge of the interposer board.

6. A stack of at least two of the layers of claim 1 wherein at least one of the access leads of one of the at least two layers is in electrical communications with at least one of the access leads of another of the at least two layers.

7. A method for providing a stackable layer comprising:
providing a package containing at least one integrated circuit chip that includes at least one terminal on the chip, providing an interposer board with at least one conductive trace thereon routed to an access edge to form at least one access lead and adapted for interconnection with the at least one terminal, interconnecting the at least one terminal with the at least one conductive trace, under-filling the interconnected package

and interposer board to form a stackable layer.

8. The method of claim 7 wherein at least two of the layers are bonded together so as to form at least one access plane, exposing the at least one access lead of each layer and electrically interconnecting each of the at lease one access leads

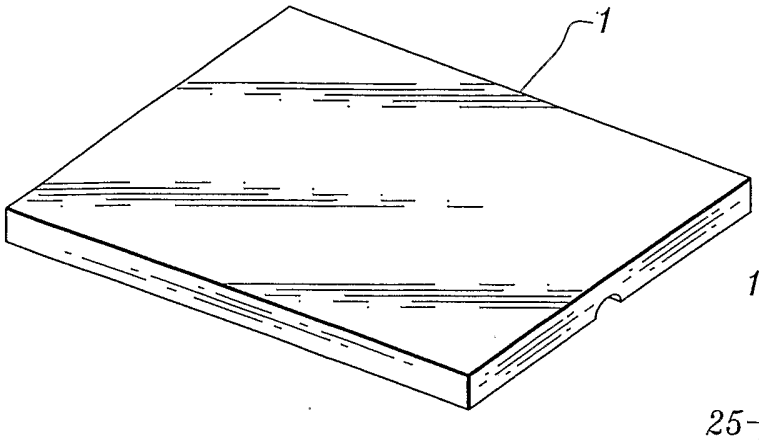


Fig. 1A

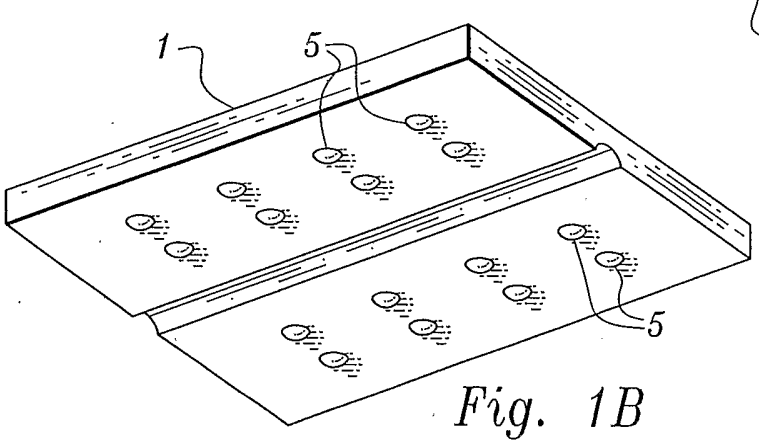


Fig. 1B

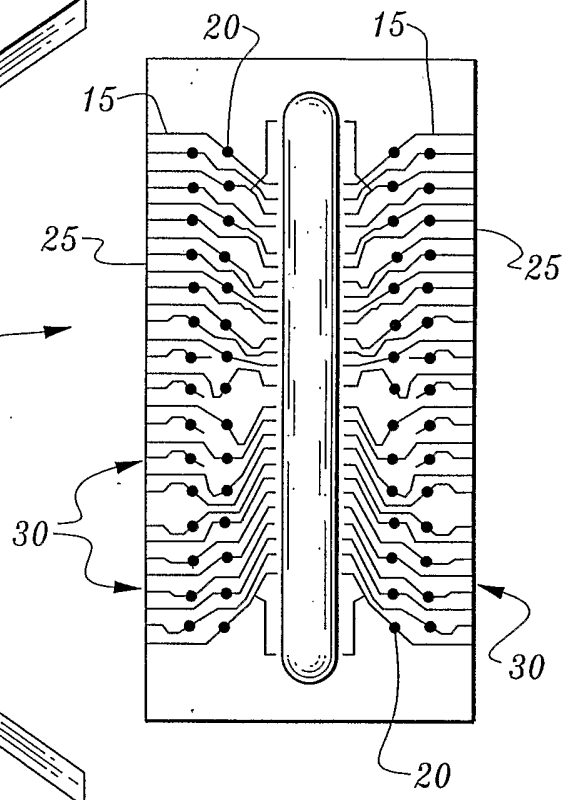


Fig. 2

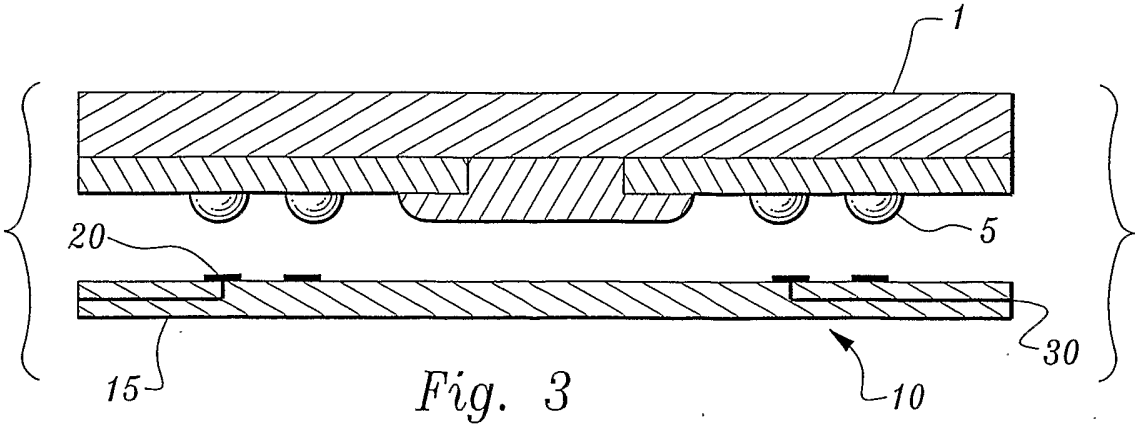


Fig. 3

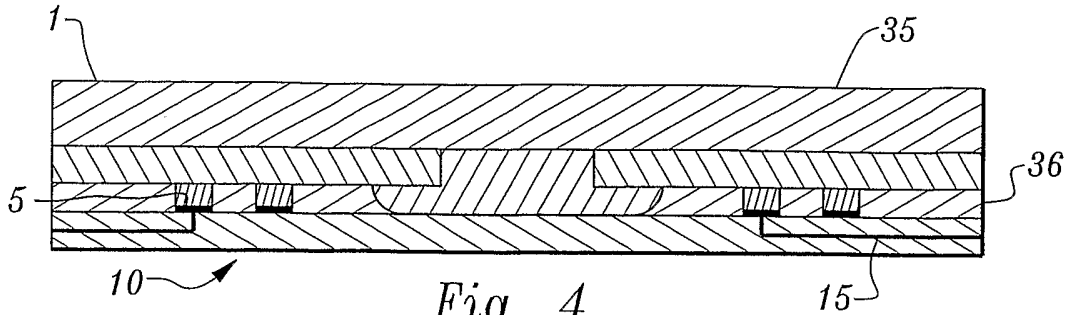


Fig. 4

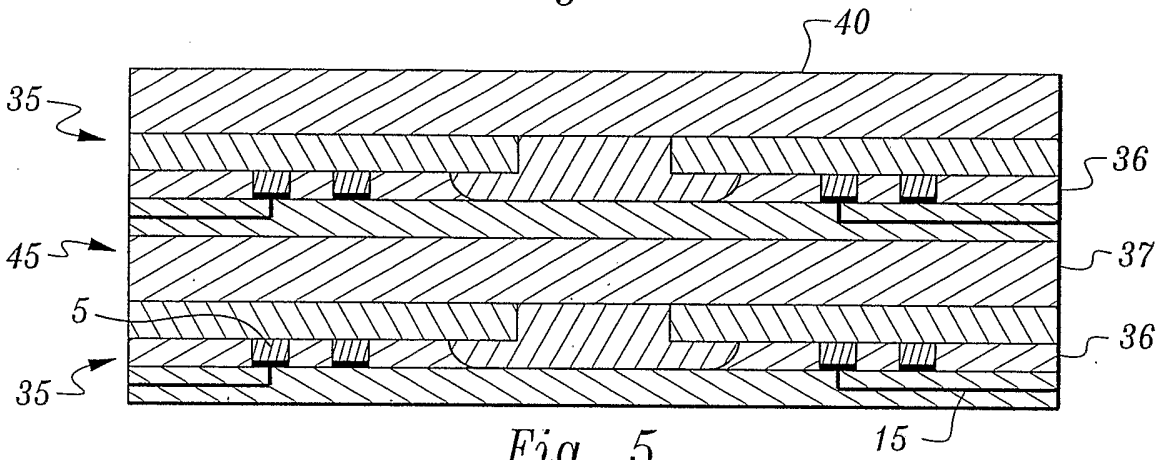


Fig. 5

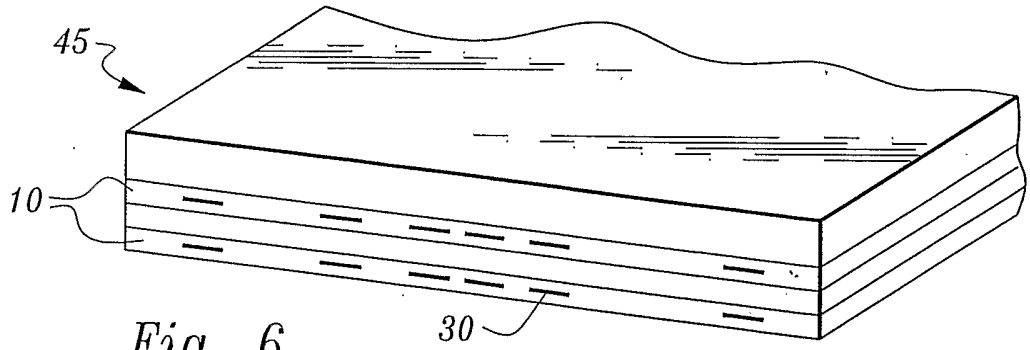


Fig. 6

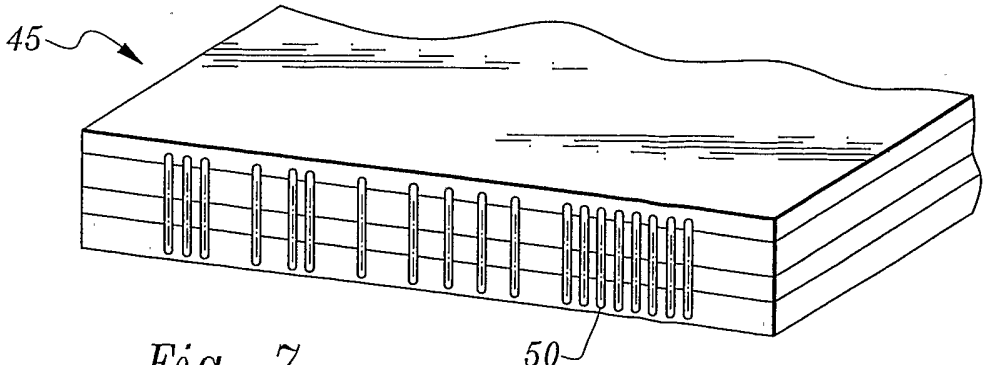


Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/24706

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 23/48, 23/52, 29/40, 21/44, 21/48, 21/50
US CL :257/777, 778; 438/108, 109
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/777, 778; 438/108, 109

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: flip chip, interposer, interconnect, BGA

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,271,598 B1 (VINDASIUS et al) 07 August 2001 (07.08.2001), Figures 3B, 5B, 9, 18.	1-8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
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