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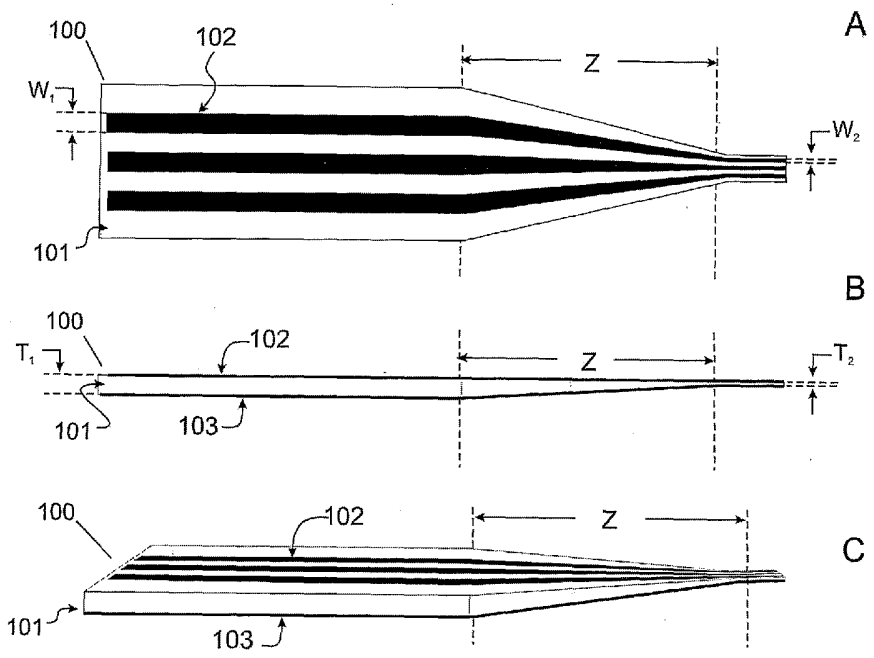
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[Continued on next page]

(54) Title: TAPERED DIELECTRIC AND CONDUCTOR STRUCTURES AND APPLICATIONS THEREOF



(57) Abstract: Disclosed are tapered dielectric and conductor structures which provide controlled impedance interconnection while signal conductor lines transition from finer pitches to coarser pitches thereby obviating electrical discontinuities generally associated with changes of circuit contact pitch. Also disclosed are methods for the construction of the devices and applications therefore.

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Tapered Dielectric and Conductor Structures and Applications Thereof

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from, and hereby incorporates by reference, U.S. Provisional Application No. 60/519,545, filed November 12, 2003 and entitled: "Memory Package and Structures Created There From"

FIELD OF THE INVENTION

[0002] The present invention relates to the field of high speed electronic interconnections and the packaging of semiconductor integrated circuits for use therewith.

BACKGROUND

[0003] The overall performance of high speed electronic systems operating in the multi-gigabit per second range is ultimately dependant on the signal integrity of the transmitted data. The first steps in controlling signal integrity are made in the design of the circuit. Choices made in terms of circuit layout, the materials used and the general architecture of the complete assembly will all have impact on the quality of the transmitted electronic signal. One of the major concerns in maintaining signal integrity is to assure that the signal encounters as few parasitic effects and electrical discontinuities as possible. One solution would be to have all signals in an electronic system be made by means of coaxial cable connections to provide and maintain a fully shielded conductor path having unvarying characteristic impedance through its entire path. However, this solution is impractical and too expensive for most electronic products. In place of coaxial cables, microstrip and stripline interconnection paths are constructed to control the impedance and provide a measure of

shielding. While these solutions have worked well for the industry for some years, as the electronics industry transitions into the gigahertz frequency due to the continuing advance of semiconductors processing, the old methods must be either replaced with new ones or the old methods must be modified to accommodate the changes needed. This is especially true as signals from the IC chip start out at a very fine pitch (i.e. circuit or contact width and spacing) and must from there graduate to the coarser pitches required for next level assembly. These transitions are normally characterized by junctions that are abrupt as the signal moves from one part of the interconnection chain to the next and, depending on the speed of the signal, these transitions can have profound effects on the signal integrity, manifest in the form of reflections and ringing in the circuit. Thus as circuit speeds climb, there is need for new approaches to design of interconnections from the chip through the interconnection chain, which will provide relief from those current design features and elements that degrade circuit performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present invention is best illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings and in which like reference numerals refer to similar elements and in which:

Figure 1 A-C shows top (i.e. conductor circuit side), cross sectional and perspective views of a cable embodiment;

Figure 2 A & B provides first and second side views (i.e. conductor circuit side and ground side) of a probe card embodiment;

Figure 3 A, B & C provides circuit side and cross sectional views of a strip of IC packages embodiment with enlarged areas of detail provided for clarity;

Figure 4 provides a cross sectional view of an embodiment comprising strips of IC packages mounted to opposite sides of a section of next level interconnection substrate and illustrating, with dotted lines, a prospective flow of the signal; and

Figure 5 A & B provides cross sectional views of embodiments that provide access to more than one layer of circuits within a structure.

DETAILED DESCRIPTION

[0005] Disclosed herein are innovative structures for controlling the quality of an electronic signal that must transition from a fine pitch to a coarser, more useful pitch. An example is the pitch transition from IC chip to terminations on an IC package. Another example is pitch transition required from IC chip to an IC test system. The objective is accomplished by creating interconnection paths that simultaneously taper insulating substrate and signal line to effectively produce the desired characteristic impedance in the signal line in a manner that is unchanging as the signal transitions from a fine pitch to a coarser pitch. This structure is useful for a wide variety of applications from test and measurement to electronic system structures such as switches and routers to IC packages for a range of chips and applications from CPU chips to memory chips as well as for circuit structures that are used to interconnect them.

[0006] The embodiments herein disclosed address the limitations of current circumstances relative to the design and manufacturing practices employed in the fabrication of electronic device and system interconnections and the present inability of those design and manufacturing practices to address adequately and fully the needs for improved electronic signal integrity as it transitions from fine pitch to course pitch and back to fine pitch as required. Thus, a first objective of the present disclosure is to describe structures which provide uniform controlled impedance from one electronic device or element to another electronic device or element while the signal transitions from a fine pitch to a course pitch and back. It is a second objective of the disclosure to describe applications of the structures described in specific product embodiments where significant benefit or improvements in product performance can be gained. It is a third objective of this disclosure to describe prospective methods for the construction of tapered dielectric and tapered trace structures that provide a uniform characteristic impedance as traces transition from fine to coarse pitch.

[0007] The present embodiments offer novel alternative approaches to addressing and meeting the stated objective and solving the problems associated with current design approaches. The conceptual structures comprise the use of any of a number of alternative embodiments of controlled impedance signal distribution structures from one device or element to a second device or element while the pitch (i.e. width and spacing) of the conductor is reduced or enlarged.

[0008] In Figure 1 A, B and C is shown an embodiment that accomplishes the objective of maintaining uniform characteristic impedance by simultaneously tapering, or incrementally stepping, both trace and dielectric in a common region. In Figure 1A a top view of a circuit section 100 having a insulating dielectric base 101, which is desirably uniform in terms of its electrical properties (e.g., dielectric constant and loss tangent) and has conductors 102 disposed on its surface. The individual circuit traces have different widths, W_1 and W_2, , at their distal ends, with the width of the traces being reduced as the circuit traces transition through a tapering zone Z. The width of dielectric is shown being also reduced in the illustration but this is not a requirement. Continuing, Figure 1B shows a cross sectional view of 1B wherein the circuit traces 102 are disposed on the first surface and a ground layer 103 resides on the side opposite the circuit traces separated by an insulating dielectric material 101. The dielectric material is shown having two different thicknesses T_1 and T_2, at the distal ends and a zone Z that is tapered in the same region where the insulating dielectric material is tapered to create the effect of uniform characteristic impedance as the circuit trace width and pitch is reduced. Figure 1C provides a perspective view of the circuit section and the elements of structure in a more clarified form. While this represents a preferred embodiment, the objectives can be also be accomplished by keeping the dielectric thickness constant and, in lieu of tapering the dielectric, having the ground metal layer become more physically diffuse with expanding open area to incrementally control capacitance as the circuit width expands. (i.e. having more or greater openings in the metal

ground as the circuit on the opposite side transitions from lesser to greater width) The objective could likewise be accomplished by having the dielectric become more diffuse (e.g. a filigree or sieve-like perforated metal of expanding percentage of open or free space area) to create a gradient dielectric constant in the material that trends from the relative dielectric constant value of the material toward a value of 1.

[0009] Such tapered structures could be created by molding of the dielectric followed by the creation of the conductor traces or, alternatively the dielectric material could be molded over the circuits on a second material. Another alternative manufacturing method is to form the taper structure by deposition of the dielectric, such as by means of multiple layers of prefabricated or multiple layers of sequentially screen printed dielectric materials or by means of ink jet printing thin layers of dielectric materials onto a metal base to create the desired dielectric taper topography for the circuits.

[0010] Figure 2 A provides an illustration of a first side of an embodiment useful for high speed testing, such as a high speed probe card 200. In the figure, circuit traces, having straight and tapered portions along their length 202, are disposed on a dielectric material 201, which has an aperture in the center 204 for accessing a device under test. The outer portion of the circular probe card, zone N, has a constant dielectric thickness and trace width in this area is also constant. Both circuit width and dielectric thickness diminish in zone Z to provide uniform characteristic impedance along their length. Figure 2B provides a view of the reverse side of the probe card revealing a full ground layer with a central aperture 204.

[0011] Figure 3 A & B provide circuit side and cross sectional views of a multi-chip package strip embodiment, such as might be used in a memory module application. Figure 3C provides an enlarged view of an alternative structure and method of interconnection to the IC die. While the structure is shown as a multi-chip structure, it is clear that a single individual IC die could also be packaged with the attributes of those IC die within the packaged strip as shown.

[0012] Figure 3A provides a circuit side view of a packaged strip 300, having IC chips 305 (shown in phantom outline as they are located on the back side) in any practical number. The strip is comprised of an insulating base material 301 that has disposed on its surface parallel circuit traces 302 for critical signal transmission and discrete terminations 303, used for connection to power, ground and non critical signal terminations on a next level assembly (the next level assembly is not shown in this figure). The ends of the strip package 309 are used for termination to the next level assembly. An enlarged view of the terminations with encapsulant 304 removed reveals wires 306 bonded to both bond pads 307 on the chip 305 and the tapered ends of the circuit traces 302A.

[0013] Figure 3B provides a cross section view of Figure 3A wherein the packaged strip 300 is shown on edge to provide more detail. The insulating dielectric base material 301 has circuits 302 disposed on one side and a ground layer 303 on the second side. IC chips 305 are bonded to the base material with its circuits and ground plane by means of an adhesive 308 and interconnections between the chip 305 and the circuits 302 is accomplished by wire bonds 306 and then protected with an encapsulant 304. An enlarged view of a section of the assembly provides greater detail for clarity and shows a section of the material that is tapered 301A beneath the tapered traces.

[0014] While the structures are shown with wire bonds being made to two rows of bond pads, the structure is not so limited and could also be created using a single bond pad in the center or at the edges of the IC chip. For a center bond pad structure as illustrated in Figure 3C, a common lead 310 could be down bonded or soldered to the central bond 311 pad and be unbroken. Moreover, the tapering structure could also fan away from a peripherally leaded device in a manner similar to current BGA or QFP IC packages.

[0015] Figure 4 illustrates a partial view of module embodiment 400 wherein package strips 300 are mounted to an interconnecting substrate 401 having interconnection vias, such as a memory module, as partially shown. In the figure, a memory controller/buffer chip 404

is interconnected to the interconnecting substrate 401 with solder balls 402 or other suitable interconnecting connecting medium. Solder balls or other interconnecting medium are also used to interconnect the package strips 300 to the interconnecting substrate 401. Additional lapped interconnections 403 are made between the packaging strip and the interconnecting substrate at the ends 409 by a suitable method such as soldering or by use of a conductive adhesive. In the figure is also shown a prospective routing path for the critical or high speed signals represented by the dotted line arrows 409. While not shown in the drawing, it is evident that the strip packages could be stacked to increase memory density as well as speed if the I/O terminations for non-critical signals were moved to the gap between the chips while the ends are connected to a bus that controls their passage from different layers of packaged strips.

[0016] Figure 5 A and B illustrate other embodiments wherein more than one layer of tapered circuits (taper of circuit widths not shown) are stacked to increase local contact density. In Figure 5A is shown an embodiment of a multilayer circuit structure having tapered dielectric 500A. In the figure, layers of insulation material 501 are interleaved with conductor signal layers 502 and ground layers 503. The insulation tapers to a reduced thickness in zone Z and the signals egress from the substrate to be accessed for interconnection to mating elements in a stair step fashion at the ends 504A and 504C which are accessed on the same side of the structure.

[0017] In Figure 5B is shown another embodiment of a multilayer circuit structure having tapered dielectric 500B. In the figure, layers of insulation material 501 are interleaved with conductor signal layers 502 and ground layers 503. The insulation tapers to a reduced thickness in the zone Z and the signals egress from the substrate to be accessed for interconnection to mating elements in a stair step fashion at the ends 504B and 504C which are accessed on opposite sides of the structure.

[0018] While the structures in Figure 5 indicate only two conductor signal lines routed in a straight line, it is clear based on the other structures disclosed in this document that many signal lines and many physical configurations (e.g. round, rectangular, triangular, etc.) and that many different step configurations accessing different conductors at different layers are possible. It is also possible within the embodiments shown to integrate, when desired or advantageous, various active and passive electronic elements to enhance or further improve the performance of a system employing the invention. Finally, it is clear that the benefits of the tapered conductor and dielectric and like structures which provide a consistent value of characteristic impedance as signal lines transition from wide to narrow are suitable as interconnection substrates for the assembly of components.

[0019] Although the invention has been described briefly with reference to specific exemplary embodiments thereof, it will be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An electronic interconnection structure to provide a controlled characteristic impedance for signal conductors that converge from a coarser pitch to a finer pitch comprising:
a first dielectric layer having a tapered thickness;
a first signal conductor disposed on a first surface of the first dielectric layer and having a tapered width; and
a first conductive grounding layer disposed on a surface of the first dielectric layer opposite the first surface.

2. The electronic interconnection structure of Claim 1 wherein the first signal conductor is tapered to a progressively narrower width over a region of the first dielectric layer that tapers to a progressively narrower thickness to provide a substantially uniform characteristic impedance along the length of the first signal conductor.

3. The electronic interconnection structure of Claim 1 further comprising a second dielectric layer having a tapered thickness and having a first surface disposed adjacent the first surface of the first dielectric layer to sandwich the first signal conductor therebetween.

4. The electronic interconnection structure of claim 1 further comprising a second grounding layer disposed on a second surface of the second dielectric layer, the second surface of the second dielectric layer being opposite the first surface of the second dielectric layer.

5. The electronic interconnection structure of claim 4 further comprising:
a third dielectric layer having a tapered thickness and having a first surface disposed

adjacent the second surface of the second dielectric layer to sandwich the second grounding layer therebetween; and

a second signal conductor having a tapered width and disposed on a surface of the third dielectric layer opposite the first surface of the third dielectric layer.

6. The electronic interconnection structure of claim 5 wherein each of the first and second signal conductors is exposed at both ends of the electronic interconnection structure..

7. An integrated circuit packaging assembly comprising:

a first integrated circuit die;

a dielectric substrate having at least one region of tapered dielectric material;

a tapered signal conductor disposed on the dielectric substrate and extending, across the region of tapered dielectric material, from a narrow-pitch termination at the first integrated circuit die to a coarser pitch termination.

8. The integrated circuit packaging assembly of claim 7 further comprising a package housing, and wherein the coarser pitch termination is disposed adjacent an outer surface of the package housing.

9. The integrated circuit packaging assembly of claim 7 wherein the tapered signal conductor exhibits a substantially uniform characteristic impedance over its length.

10. The integrated circuit package assembly of Claim 7 wherein the assembly comprises a strip of interconnected integrated circuit devices, the integrated circuit devices including the first integrated circuit die.

11. The integrated circuit package assembly of Claim 7 wherein the assembly comprises a strip of interconnected integrated circuit memory devices, the integrated circuit memory

devices including the first integrated circuit die.

12. The integrated circuit package assembly of claim 7 wherein at least one of the tapered signal conductor and the region of tapered dielectric material is stepwise tapered.

13. A method of manufacturing a substrate for a controlled-impedance electronic interconnection structure that provides substantially uniform controlled characteristic impedance for circuits, the method comprising selective layering of dielectric material by dispensing to create a dielectric having a tapered topography.

14. The method of claim 13 wherein dispensing to create a dielectric having a tapered topography comprises dispensing the dielectric material with an ink jet.

15. A method of manufacturing a substrate for a controlled-impedance electronic interconnection structure that provides a substantially uniform characteristic impedance for circuits, the method comprising sequentially stenciling layers of dielectric material to create a dielectric having a tapered topography.

16. A controlled impedance test structure comprising:
a dielectric substrate having at least one area of tapered dielectric; and
at least one tapered signal conductor disposed on the tapered dielectric, wherein said dielectric substrate and at least one tapered signal conductor constitute a test connection that extends between a narrow-pitch termination and a coarser-pitch termination and exhibits substantially uniform characteristic impedance from the narrow-pitch termination to the coarser-pitch termination.

17. The test structure of Claim 16 where the test structure is a probe card.

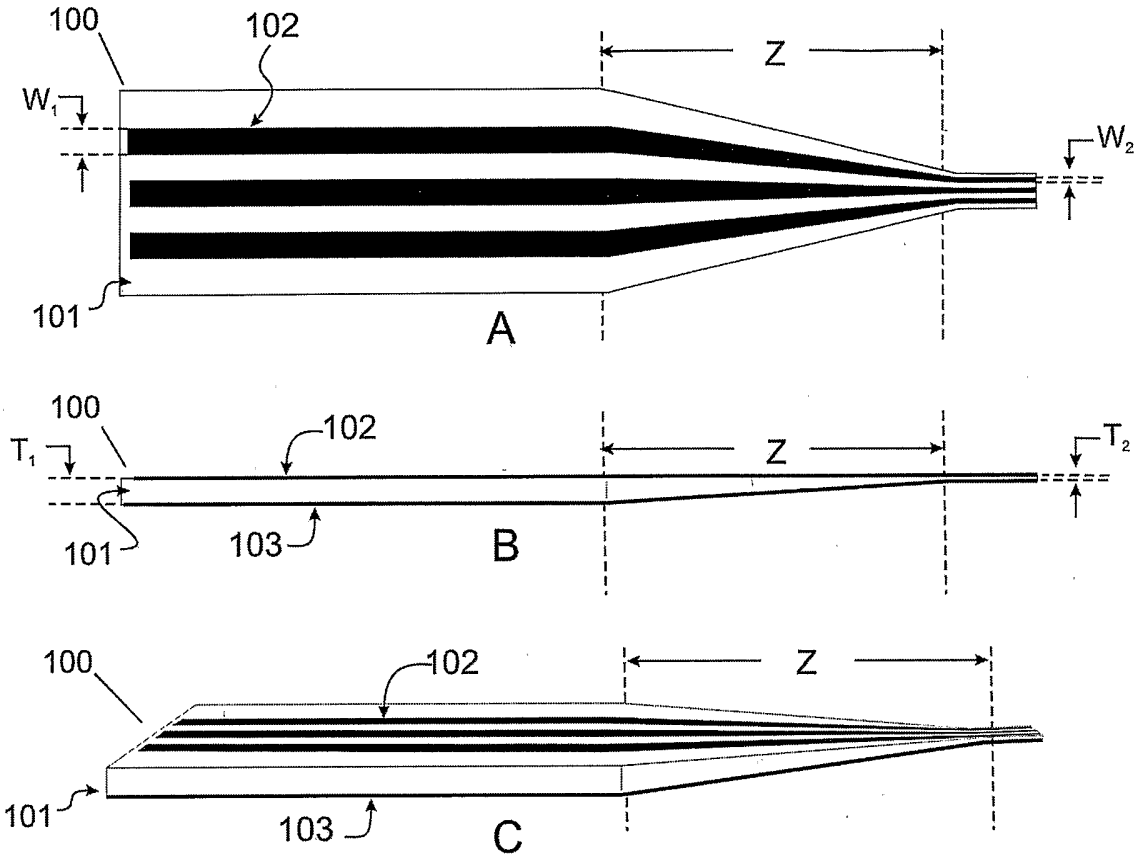


Figure 1

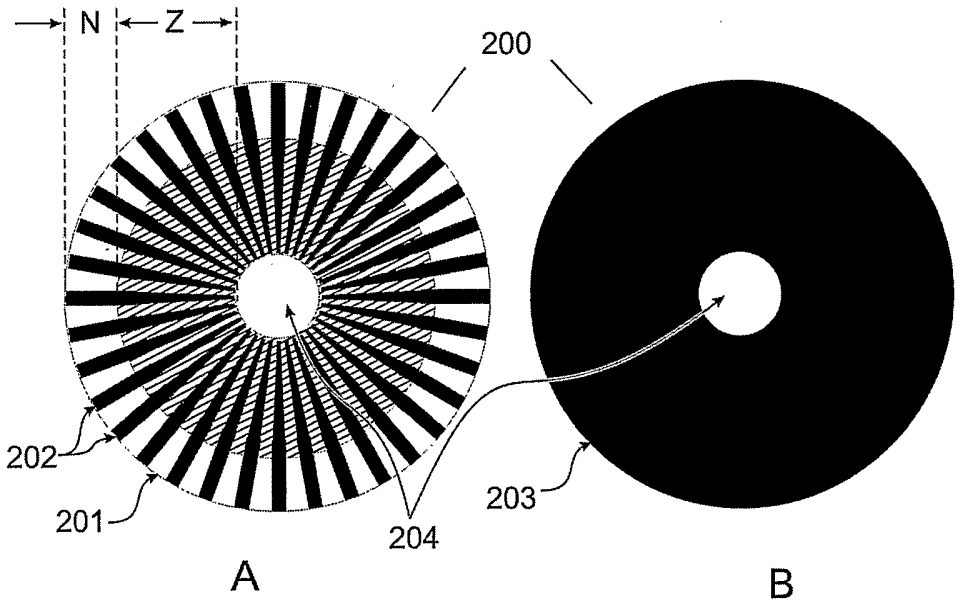


Figure 2

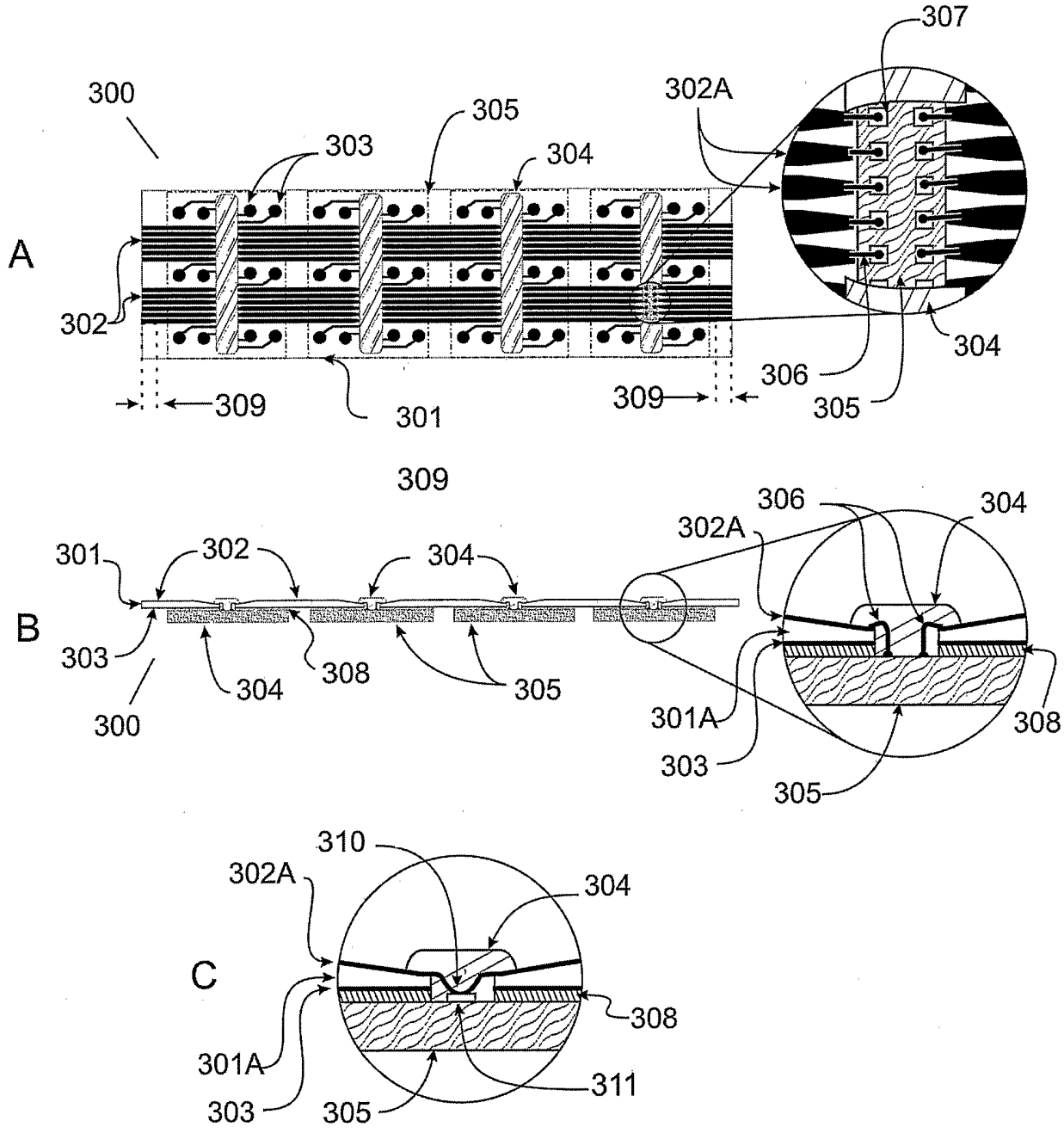

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Figure 3

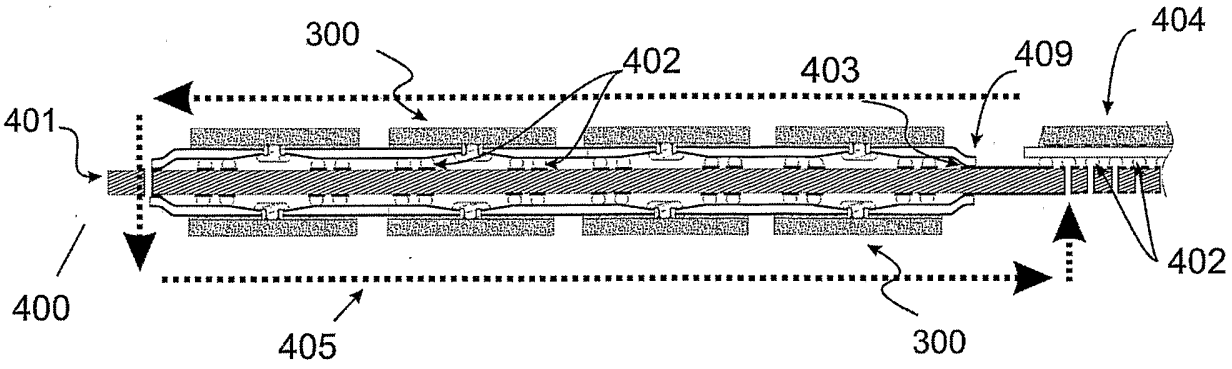


Figure 4

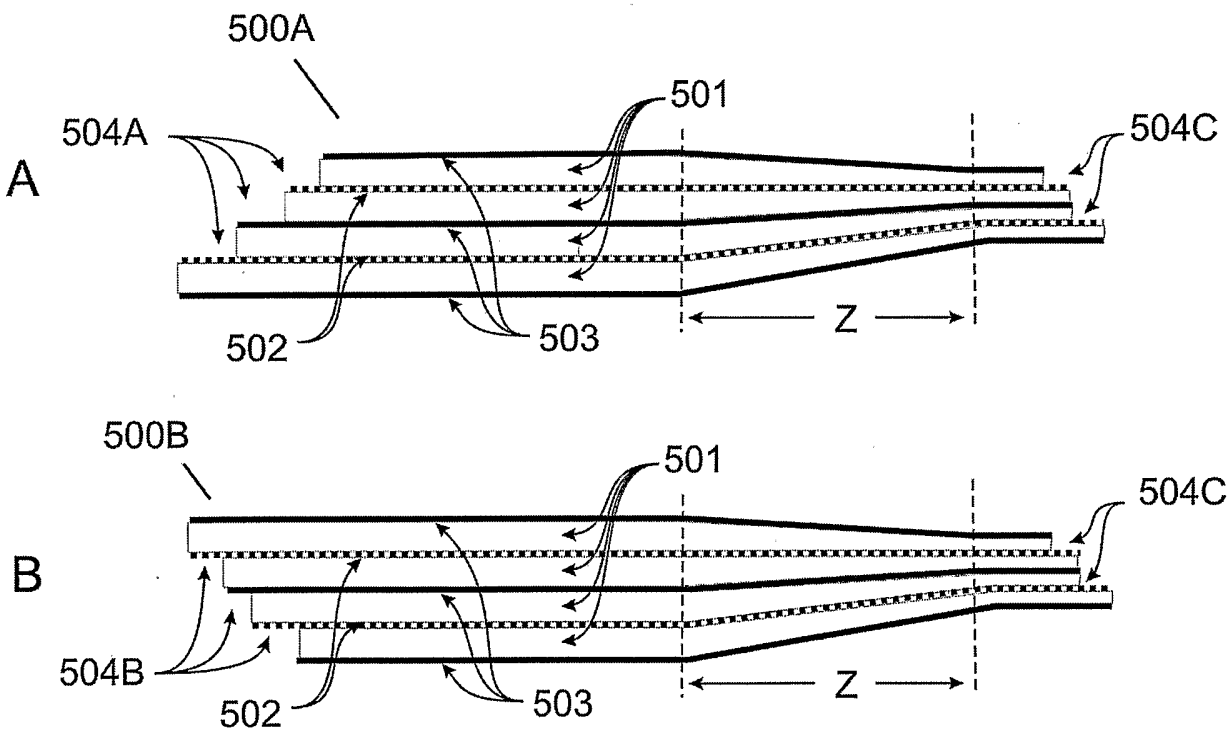


Figure 5