United States Patent [19]

Perkins, III

[11] **3,854,586**

[45] **Dec. 17, 1974**

[54] **AUTOMATIC GRADER FOR SORTING OBJECTS ACCORDING TO BRIGHTNESS AND COLOR TONES**

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[73] Assignee: **AMF Incorporated,** White Plains, N.Y.

[22] Filed: **May 15, 1973**

[21] Appl. No.: **360,570**

[52] **U.S. Cl.** **209/111.6,** 209/115, 356/221, 356/229, 356/178, 356/191

[51] **Int. Cl.** **B07c 5/342**

[58] **Field of Search** ..... 356/51, 221, 222, 229, 356/176, 177, 178, 179, 191, 186, 195; 209/111.6, 111.7, 111.5; 250/223 R, 226

[56] **References Cited**

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3,744,919	7/1973	Babb	356/186
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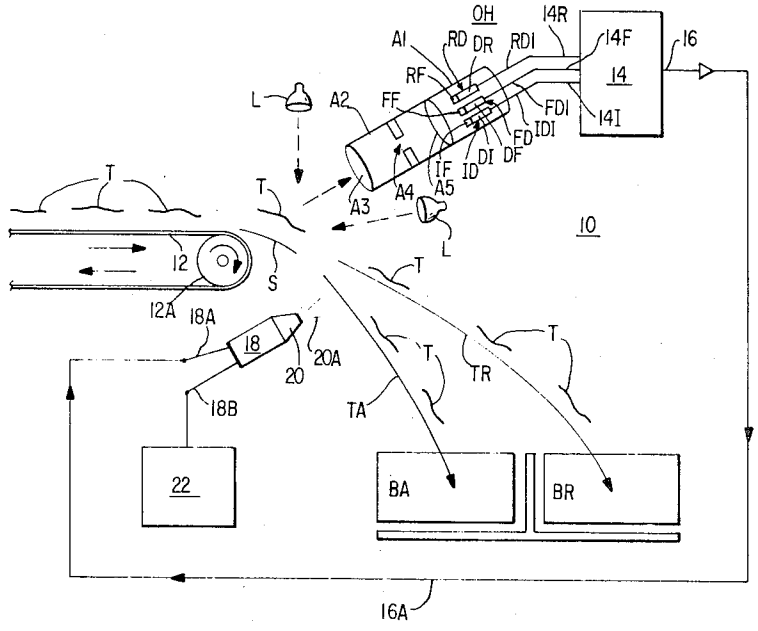
Primary Examiner—Allen N. Knowles

Attorney, Agent, or Firm—George W. Price; Charles J. Worth

[57] **ABSTRACT**

A system and apparatus for grading and sorting tobacco leaves and other objects according to brightness and two color tones are provided. The tobacco leaves or objects are caused to traverse a background plate of known color and both are impinged by polychromatic light. The light reflected therefrom in three distinct spectral bands is detected and analyzed according to a predetermined mathematical relationship to compare the brightness and two color tones of the said leaves or objects to standards which are selectively dialed in to the apparatus. Logic circuitry is provided to constrain acceptance or rejection of the leaves or objects by the system in response to a determination that at least one of the characteristics of brightness and two color tones exceeds a predetermined deviation from the preset standards. One of the spectral bands is chosen to provide uniform reflectivity from the series of leaves or objects being sorted to normalize the size of the various objects to that of the background surface.

82 Claims, 46 Drawing Figures



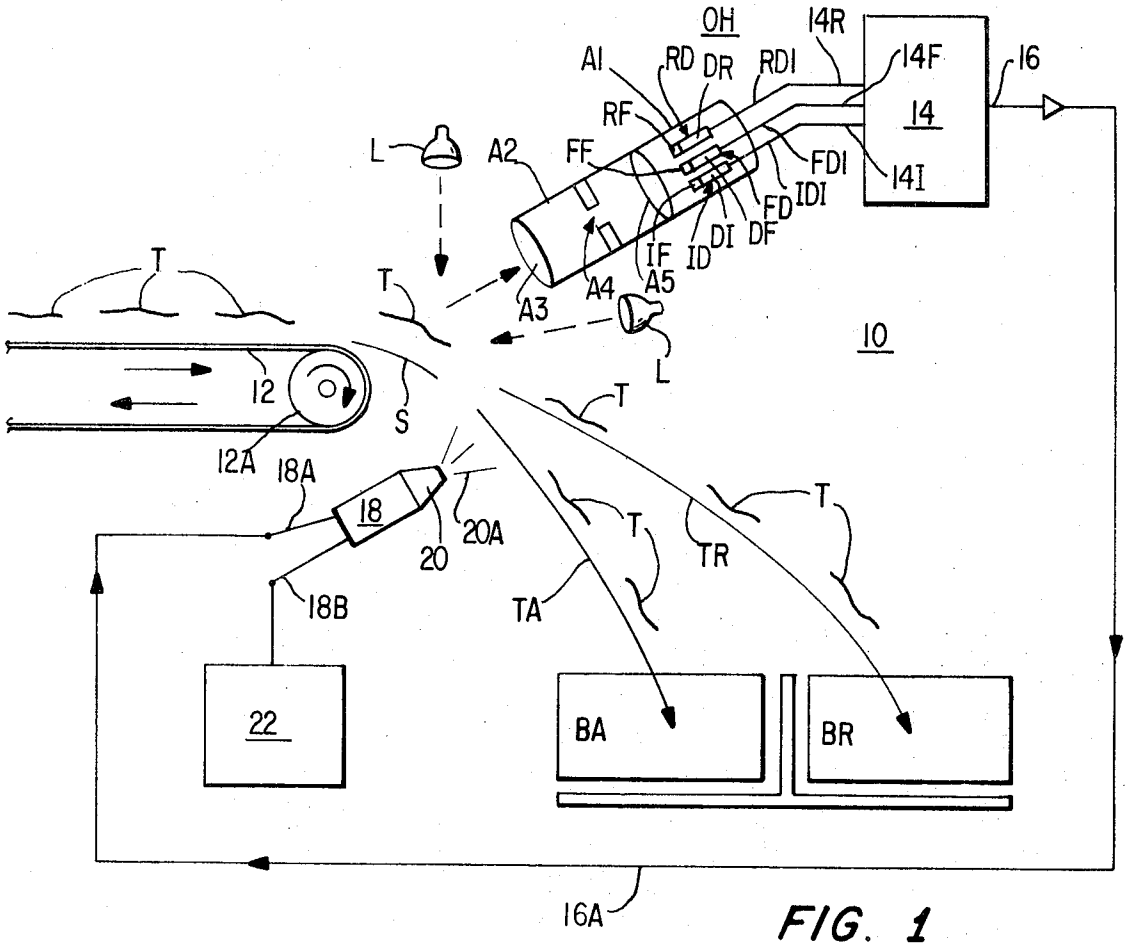

OH
14R
AI
RD
DR
RDI
14F
16
RF
14
L
A2
FF
FDI
14I
FD
IDI
DI
DF
IF
ID
A5
A4
A3
T
10
12
S
L
12A
18A
18
20
20A
TA
TR
18B
22
BA
BR
16A

FIG. 1

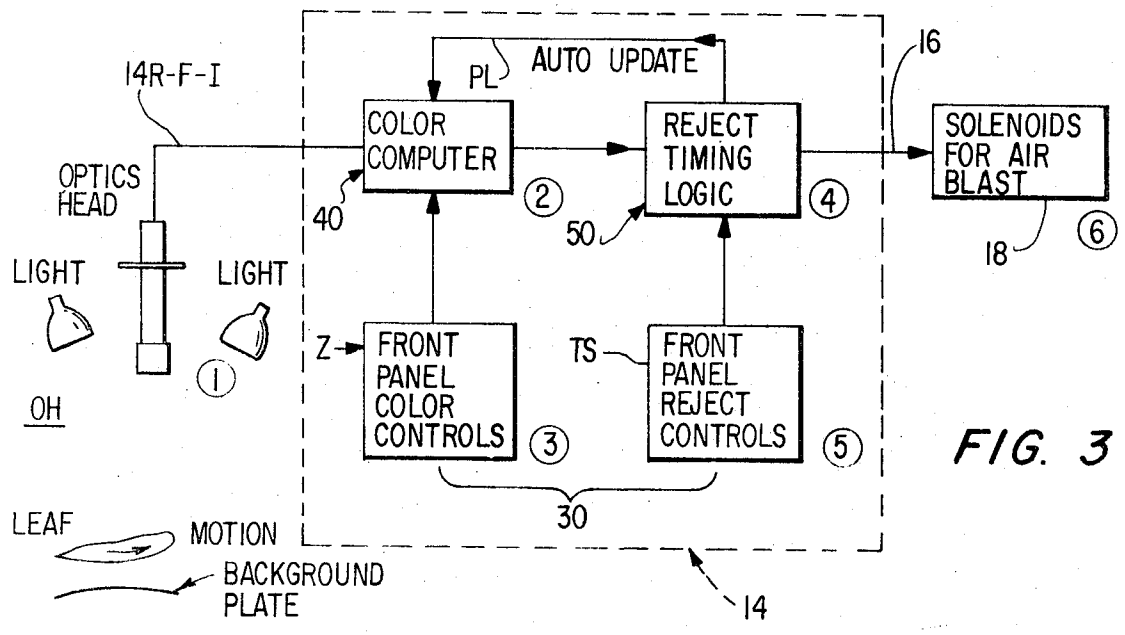
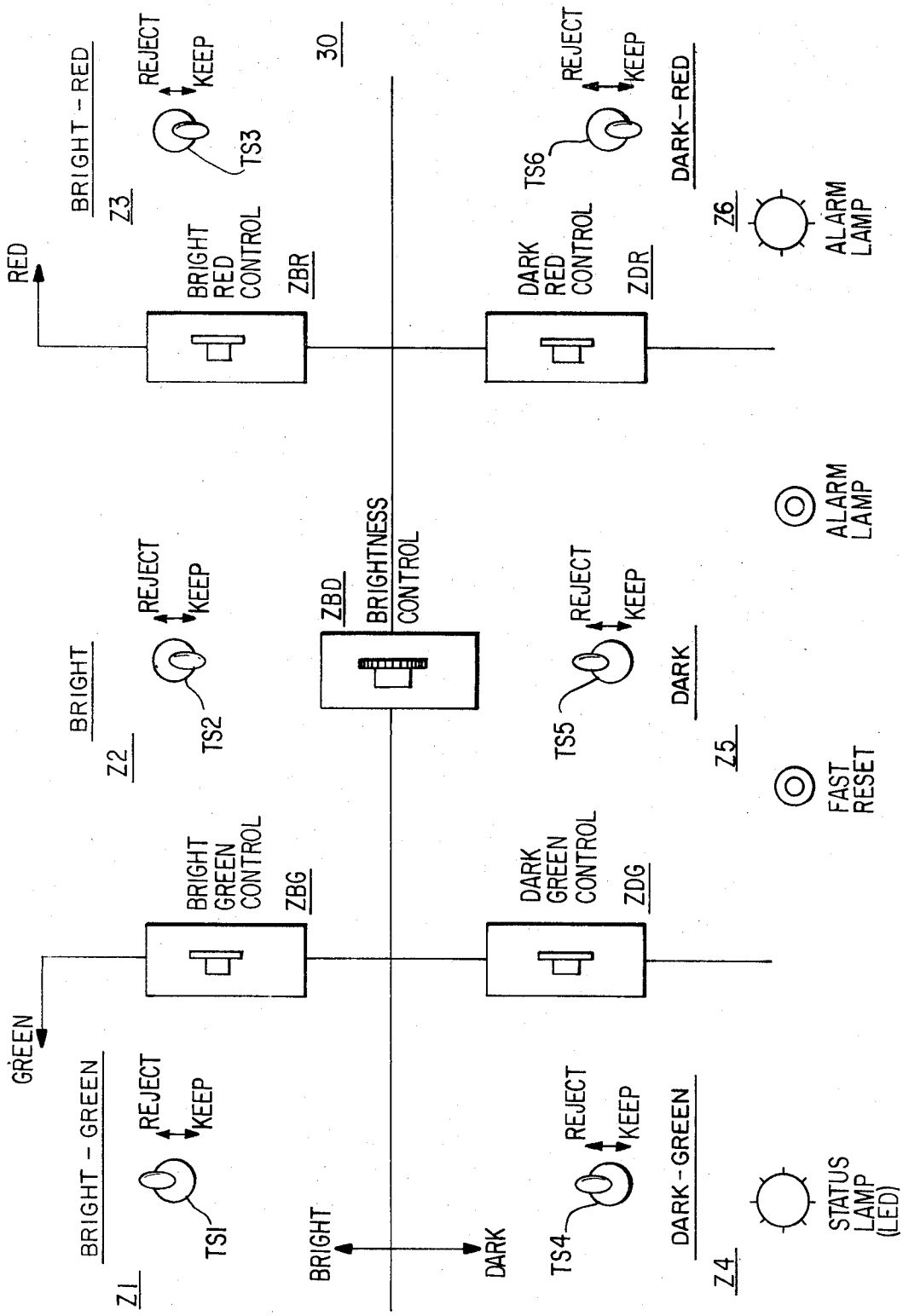

14R-F-I
PL
AUTO UPDATE
16
COLOR COMPUTER
REJECT TIMING LOGIC
SOLENOIDS FOR AIR BLAST
OPTICS HEAD
40
2
50
4
18
6
LIGHT
LIGHT
1
Z
FRONT PANEL COLOR CONTROLS
3
TS
FRONT PANEL REJECT CONTROLS
5
OH
30
LEAF
MOTION
BACKGROUND PLATE
14

FIG. 3

FIG. 2


FRONT PANEL
BRIGHT - GREEN
Z1
REJECT
KEEP
TS1
GREEN
BRIGHT
Z2
REJECT
KEEP
TS2
BRIGHT GREEN CONTROL
ZBG
BRIGHT - RED
Z3
REJECT
KEEP
TS3
RED
BRIGHT RED CONTROL
ZBR
30
ZBD
BRIGHTNESS CONTROL
BRIGHT
DARK
TS4
REJECT
KEEP
DARK - GREEN
Z4
STATUS LAMP (LED)
TS5
REJECT
KEEP
DARK
Z5
FAST RESET
DARK GREEN CONTROL
ZDG
TS6
REJECT
KEEP
DARK - RED
Z6
ALARM LAMP
DARK RED CONTROL
ZDR
ALARM LAMP

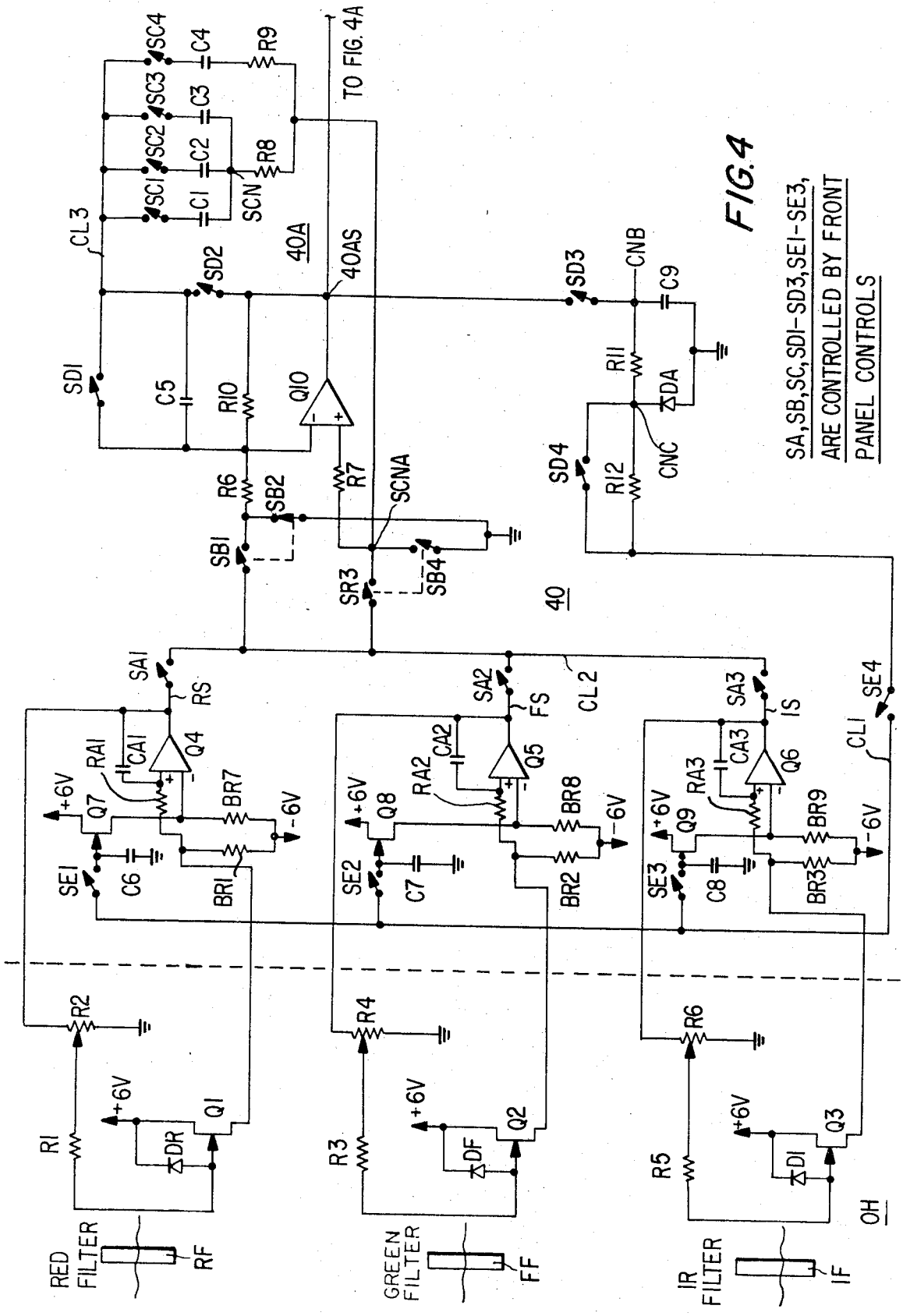

TO FIG. 4A
SC4
SC3
SC2
SC1
C4
C3
C2
C1
R9
R8
SCN
CL3
SD2
40A
40AS
SD3
CNB
C9
SDI
C5
RIO
QIO
RII
DA
CNC
SD4
RI2
R6
SB2
R7
SCNA
SBI
SB4
SR3
40
SA,SB,SC,SDI-SD3,SEI-SE3,
ARE CONTROLLED BY FRONT
PANEL CONTROLS
SAI
RS
SA2
FS
SA3
IS
CL2
SE4
CLI
RAI
CAI
Q4
RA2
CA2
Q5
RA3
CA3
Q6
+6V
Q7
Q8
Q9
BR7
BR8
BR9
-6V
SEI
SE2
SE3
C6
C7
C8
BRI
BR2
BR3
R2
R4
R6
RI
R3
R5
DR
DF
DI
Q1
Q2
Q3
OH
RED
FILTER
RF
GREEN
FILTER
FF
IR
FILTER
IF

FIG. 4

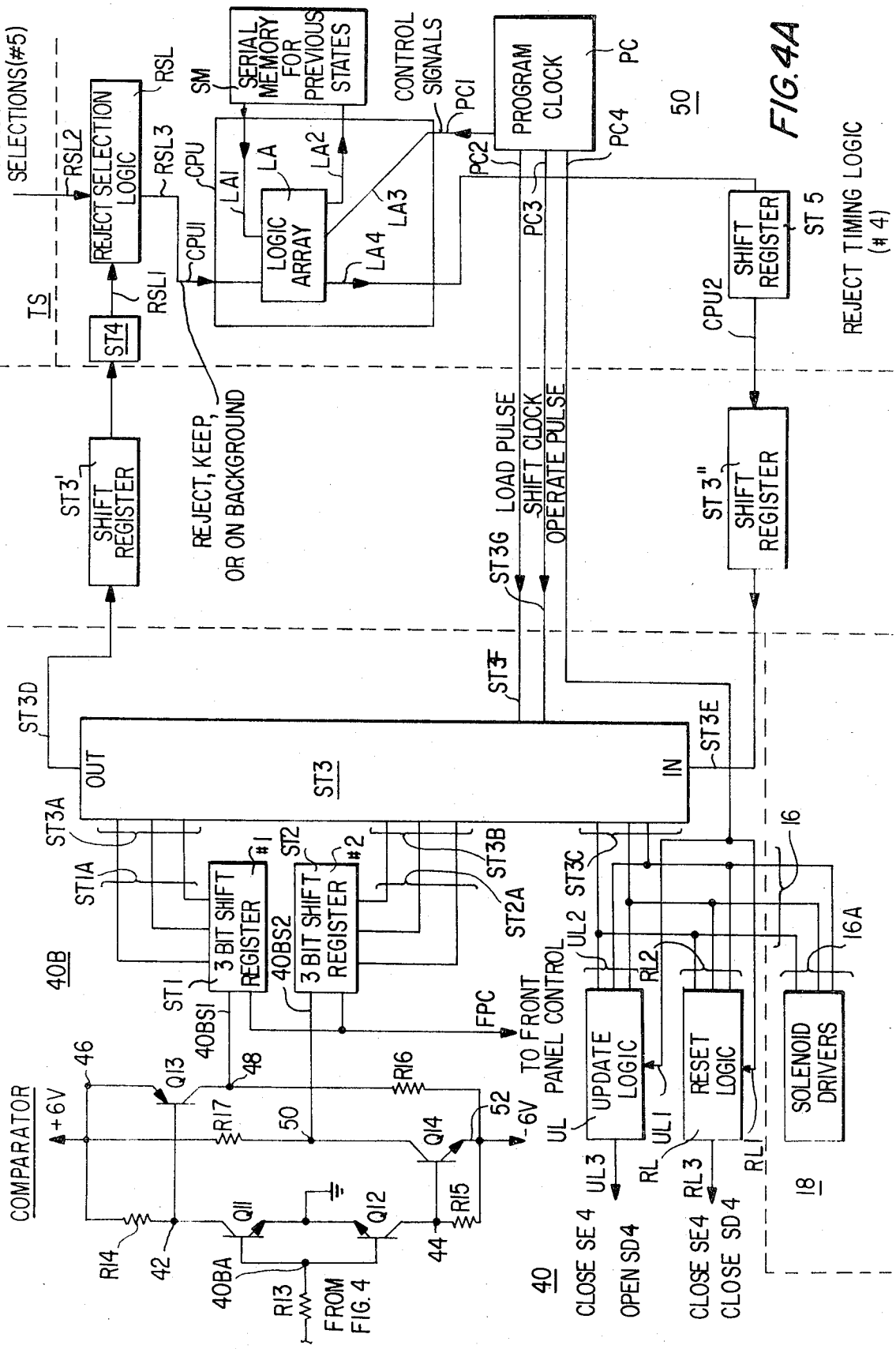
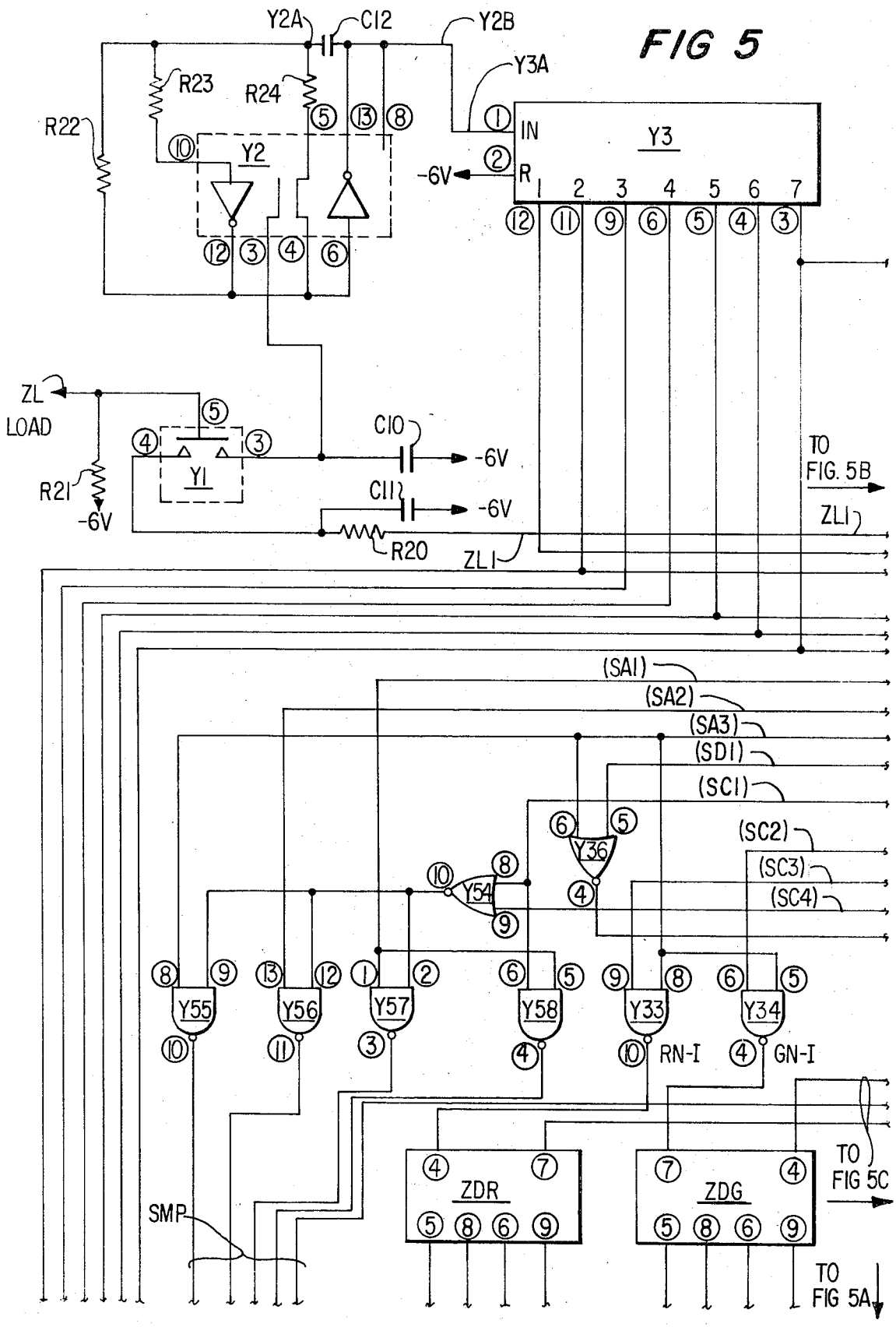

FRONT PANEL REJECT SELECTIONS(#5)
TS
ST4
REJECT SELECTION LOGIC
RSL2
RSL3
RSL
RSL1
CPU
CPUI
LAI
LA
LA2
LA3
LA4
LOGIC ARRAY
SM
SERIAL MEMORY FOR PREVIOUS STATES
CONTROL SIGNALS
PCI
PC2
PC3
PC4
PROGRAM CLOCK
PC
50
ST 5
SHIFT REGISTER
CPU2
REJECT TIMING LOGIC (# 4)
ST3'
SHIFT REGISTER
REJECT, KEEP, OR ON BACKGROUND
ST3G
LOAD PULSE
SHIFT CLOCK
OPERATE PULSE
ST 3"
SHIFT REGISTER
ST3F
ST3D
ST3E
OUT
ST3
IN
ST3A
ST1A
40B
3 BIT SHIFT REGISTER
#1
ST2
#2
3 BIT SHIFT REGISTER
40BS2
ST3B
ST2A
ST3C
UL2
16
16A
ST1
40BS1
FPC
TO FRONT PANEL CONTROL
UL
UPDATE LOGIC
RL2
RESET LOGIC
SOLENOID DRIVERS
COMPARATOR
+6V
46
Q13
48
RI6
RI7
50
Q14
52
-6V
ULI
RL
RLI
UL3
RL3
18
RI4
42
Q11
Q12
RI5
44
40BA
RI3
FROM FIG. 4
40
CLOSE SE 4
OPEN SD4
CLOSE SE4
CLOSE SD 4

FIG. 4A

FIG 5


Y2A
C12
Y2B
Y3A
R23
R24
R22
Y2
IN
R
Y3
-6V
ZL
LOAD
R21
-6V
Y1
C10
-6V
C11
-6V
R20
ZL1
TO FIG. 5B
ZL1
(SA1)
(SA2)
(SA3)
(SD1)
(SC1)
(SC2)
(SC3)
(SC4)
Y36
Y54
Y55
Y56
Y57
Y58
Y33
Y34
RN-I
GN-I
SMP
ZDR
ZDG
TO FIG 5C
TO FIG 5A

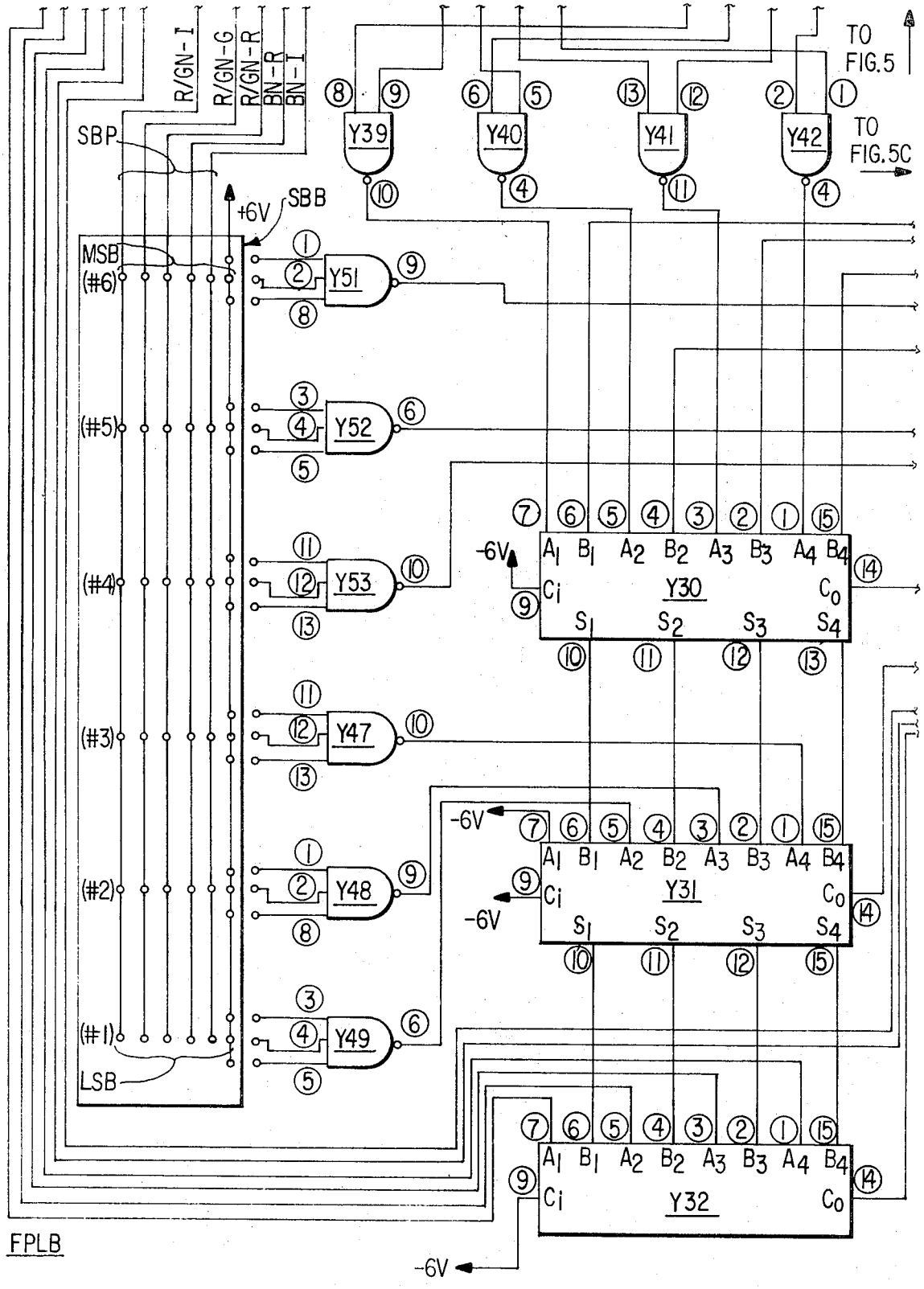

R/GN-I
R/GN-G
R/GN-R
BN-R
BN-I
SBP
SBB
+6V
MSB
(#6)
(#5)
(#4)
(#3)
(#2)
(#1)
LSB
Y39
Y40
Y41
Y42
Y51
Y52
Y53
Y47
Y48
Y49
Y30
Y31
Y32
A1 B1 A2 B2 A3 B3 A4 B4
Ci
Co
S1 S2 S3 S4
-6V
TO FIG.5
TO FIG.5C
FPLB

FIG. 5A

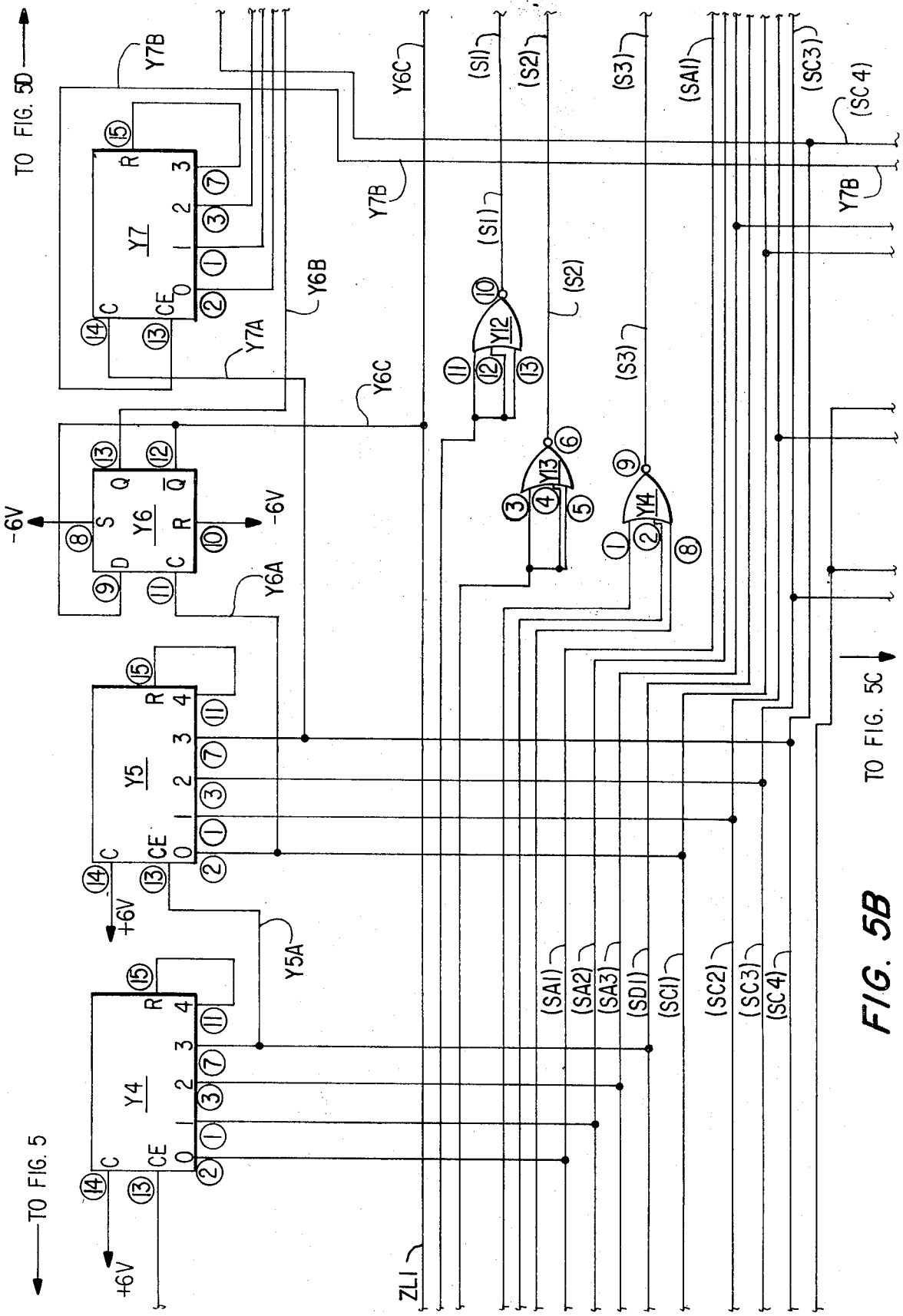

TO FIG. 5D
TO FIG. 5
TO FIG. 5C
Y7
Y6
Y5
Y4
Y12
Y13
Y14
Y7B
Y6C
Y6B
Y7A
Y6A
Y5A
-6V
+6V
(S1)
(S2)
(S3)
(SA1)
(SA2)
(SA3)
(SD1)
(SC1)
(SC2)
(SC3)
(SC4)
ZLI

FIG. 5B

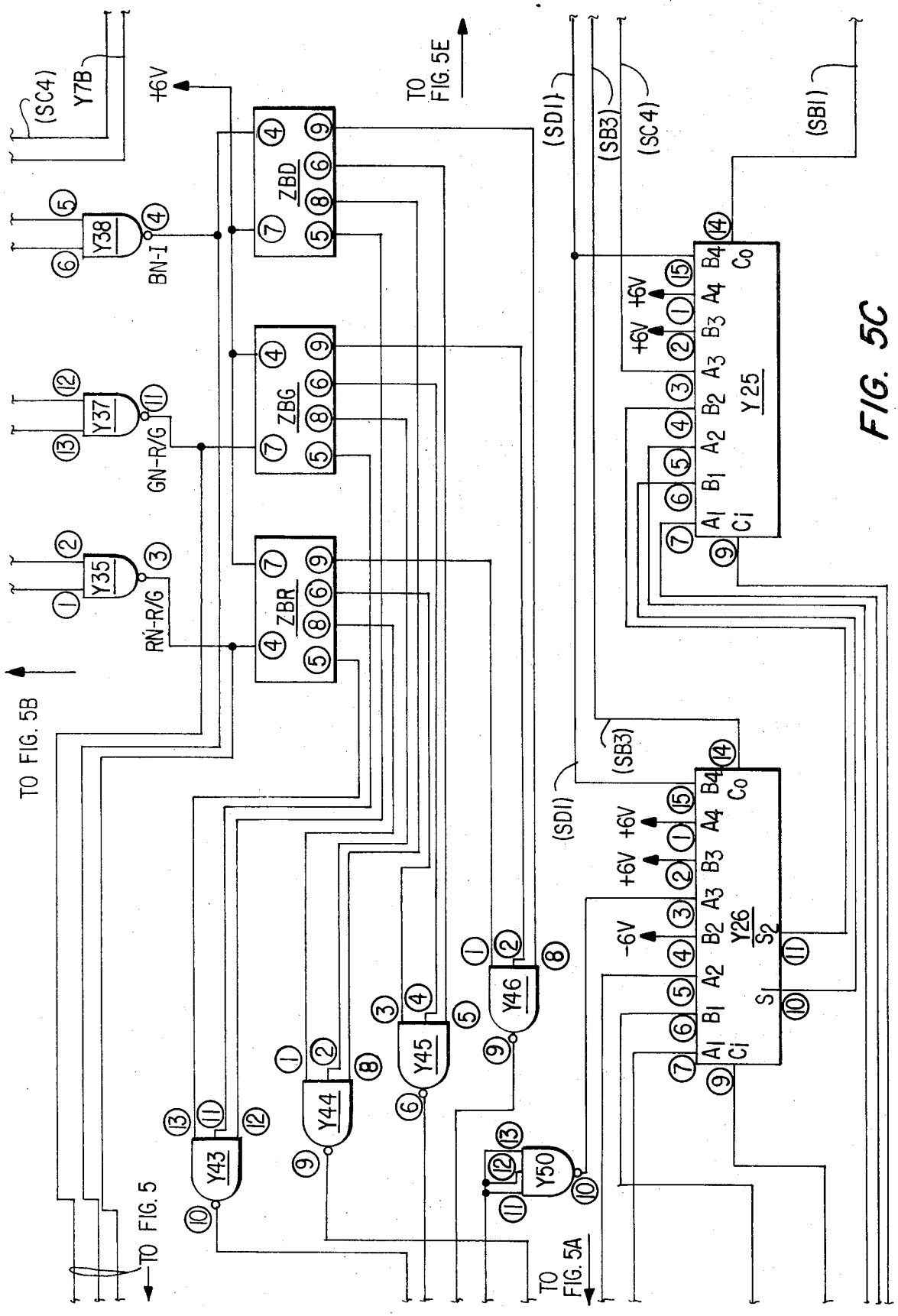
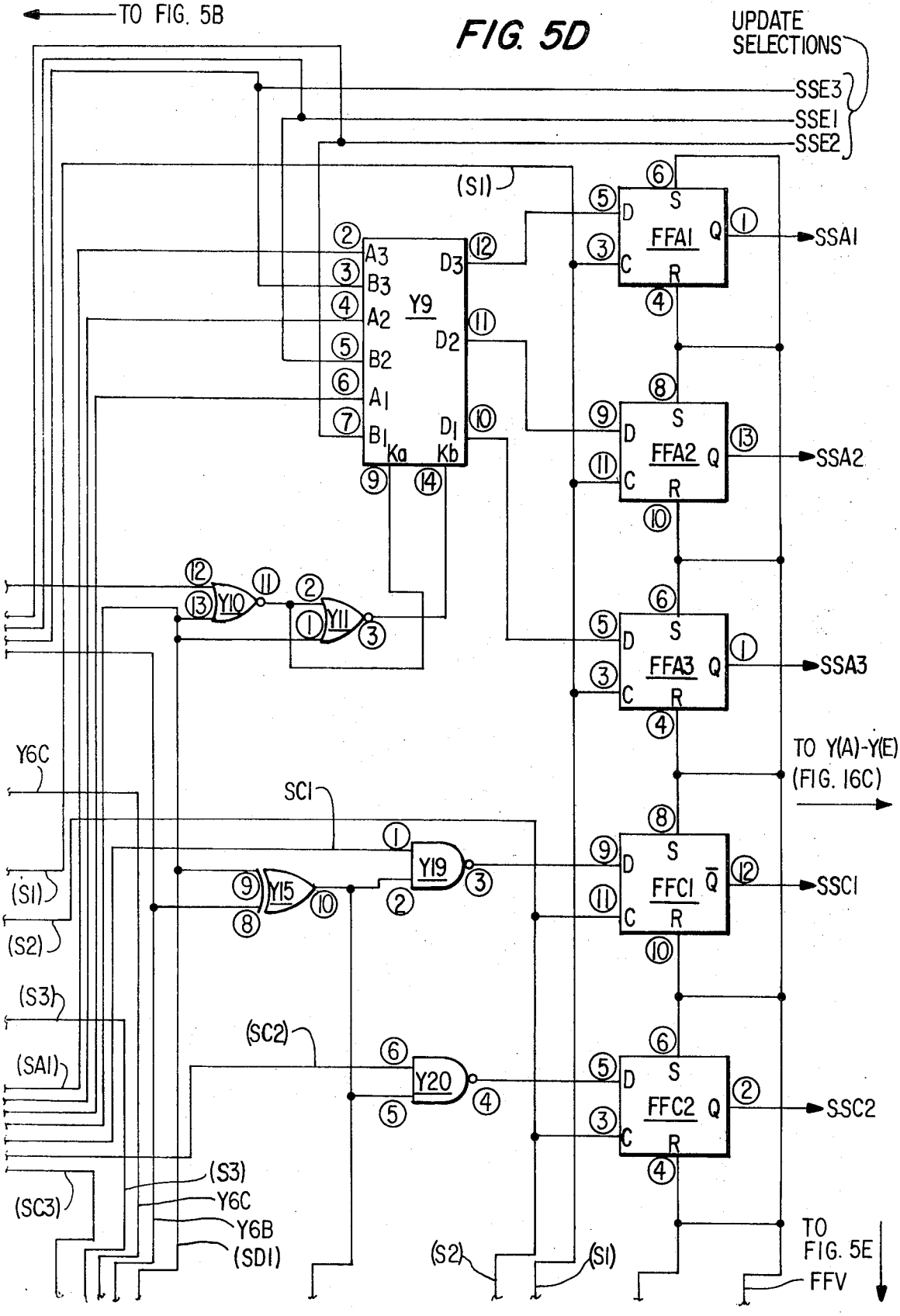

(SC4)
Y7B
+6V
TO FIG. 5E
(SDI)
(SB3)
(SC4)
(SBI)
Y38
BN-I
ZBD
Y37
GN-R/G
ZBG
Y35
RN-R/G
ZBR
TO FIG. 5B
Y25
Y26
S2
S1
Y46
Y45
Y44
Y43
Y50
-6V
TO FIG. 5
TO FIG. 5A

FIG. 5C

FIG. 5D


TO FIG. 5B
UPDATE SELECTIONS
SSE3
SSE1
SSE2
(S1)
A3
B3
A2
B2
A1
B1
D3
D2
D1
Ka
Kb
Y9
FFA1
FFA2
FFA3
FFC1
FFC2
S
D
C
R
Q
SSA1
SSA2
SSA3
SSC1
SSC2
Y10
Y11
Y19
Y15
Y20
Y6C
SC1
(S1)
(S2)
(S3)
(SA1)
(SC2)
(SC3)
(S3)
Y6C
Y6B
(SD1)
(S2)
(S1)
TO Y(A)-Y(E) (FIG. 16C)
TO FIG. 5E
FFV

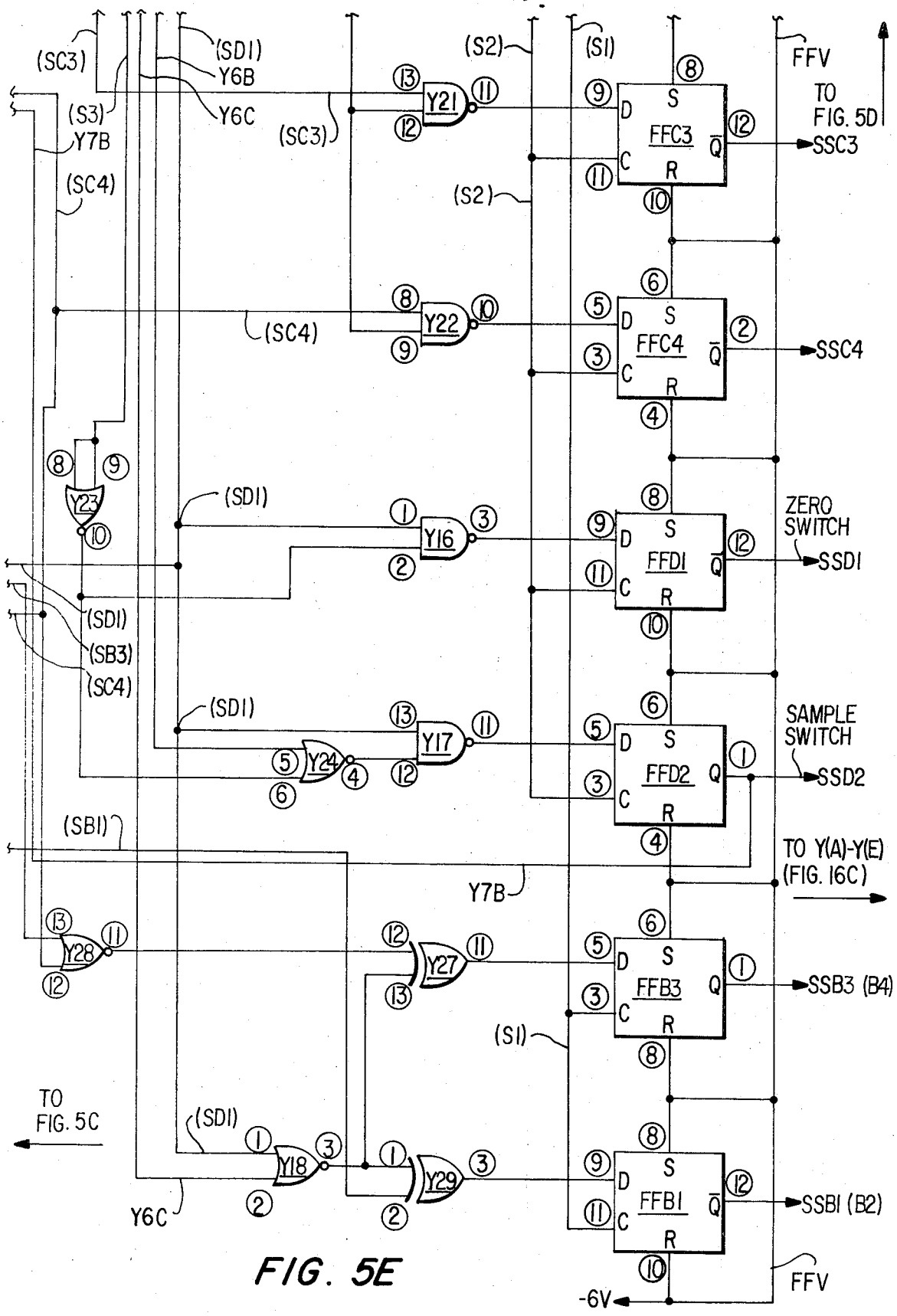

(SC3)
(SD1)
Y6B
Y6C
(S3)
Y7B
(SC4)
(SC3)
(S2)
(S1)
FFV
TO FIG. 5D
Y21
FFC3
SSC3
(S2)
Y22
(SC4)
FFC4
SSC4
Y23
(SD1)
Y16
FFD1
ZERO SWITCH
SSD1
(SD1)
(SB3)
(SC4)
(SD1)
Y17
Y24
FFD2
SAMPLE SWITCH
SSD2
(SB1)
TO Y(A)-Y(E) (FIG. 16C)
Y7B
Y28
Y27
FFB3
SSB3 (B4)
(S1)
TO FIG. 5C
(SD1)
Y18
Y29
FFB1
SSB1 (B2)
Y6C
-6V
FFV

FIG. 5E

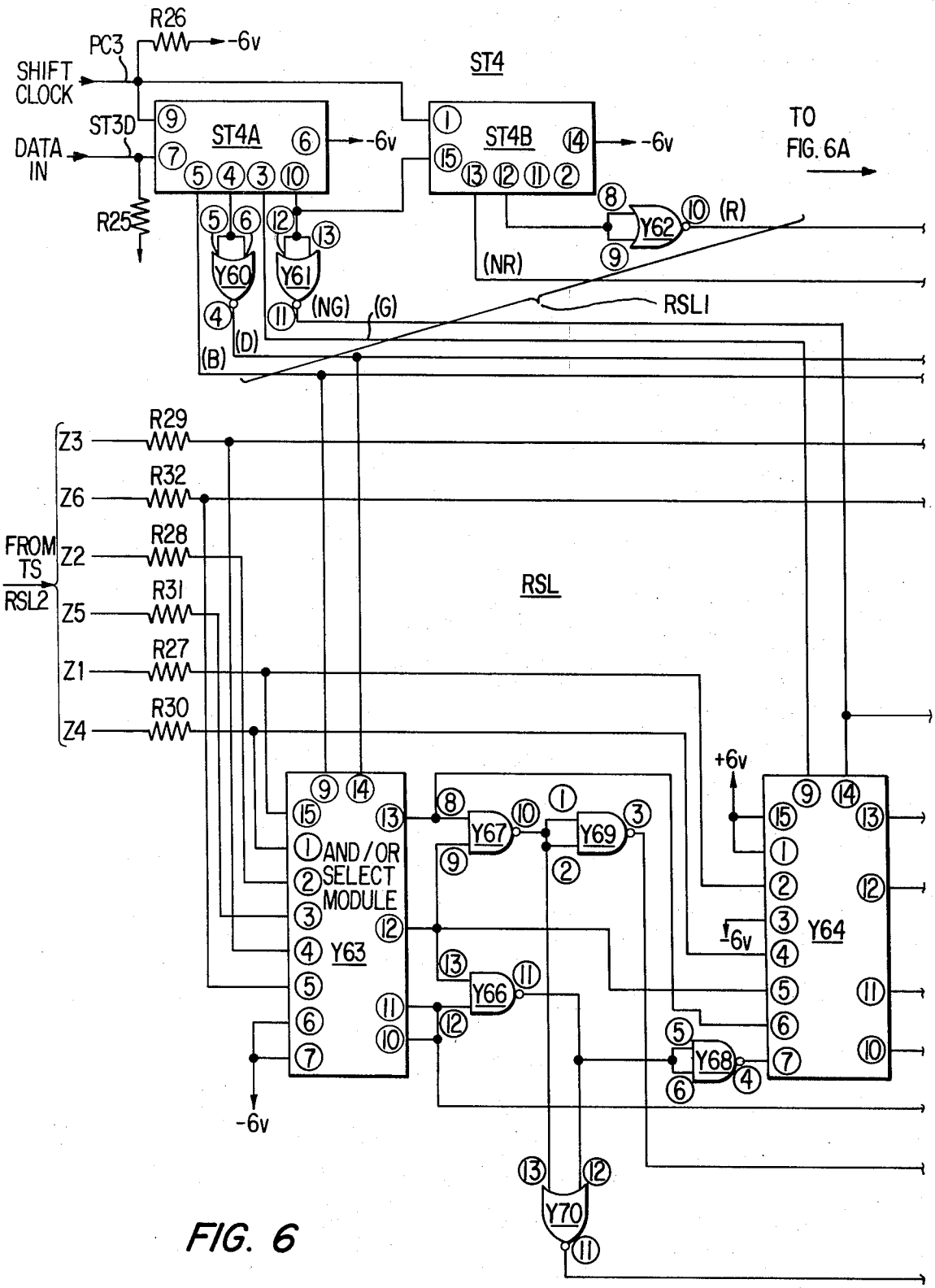

R26
PC3
-6v
SHIFT CLOCK
ST4
ST3D
DATA IN
ST4A
ST4B
-6v
TO FIG. 6A
R25
Y60
Y61
Y62
(R)
(NR)
(NG)
(G)
(D)
(B)
RSLI
R29
Z3
R32
Z6
FROM TS
RSL2
R28
Z2
R31
Z5
R27
Z1
R30
Z4
RSL
+6v
AND/OR SELECT MODULE
Y63
Y64
Y67
Y69
Y66
Y68
Y70

FIG. 6

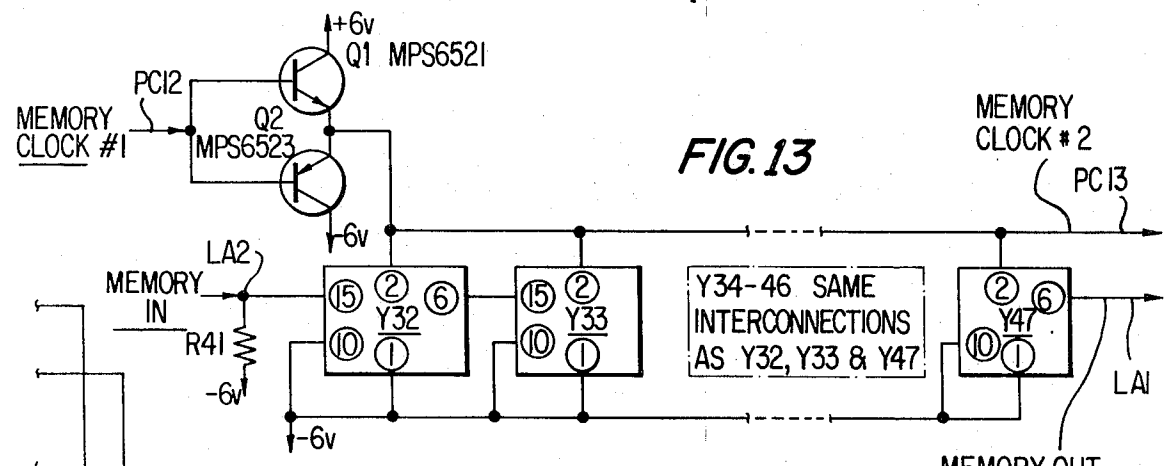
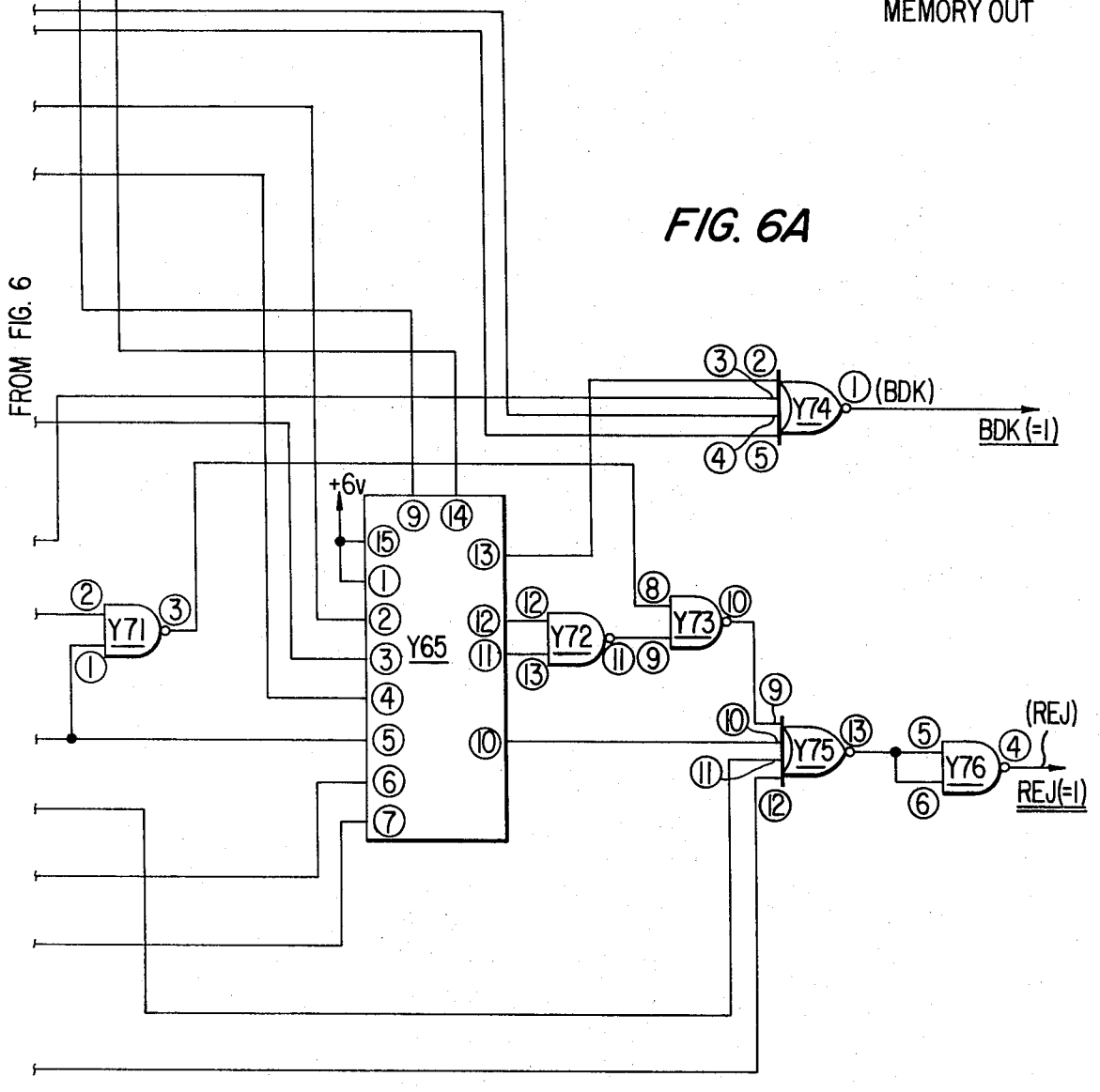

+6v
Q1 MPS6521
PCI2
MEMORY CLOCK #1
Q2 MPS6523
-6v
MEMORY CLOCK # 2
PC13
LA2
MEMORY IN
R41
-6v
Y32
Y33
Y34-46 SAME INTERCONNECTIONS AS Y32, Y33 & Y47
Y47
LAI
-6v
MEMORY OUT

FIG. 13

FIG. 6A


FROM FIG. 6
Y74
(BDK)
BDK (=1)
+6v
Y71
Y65
Y72
Y73
Y75
Y76
(REJ)
REJ(=1)

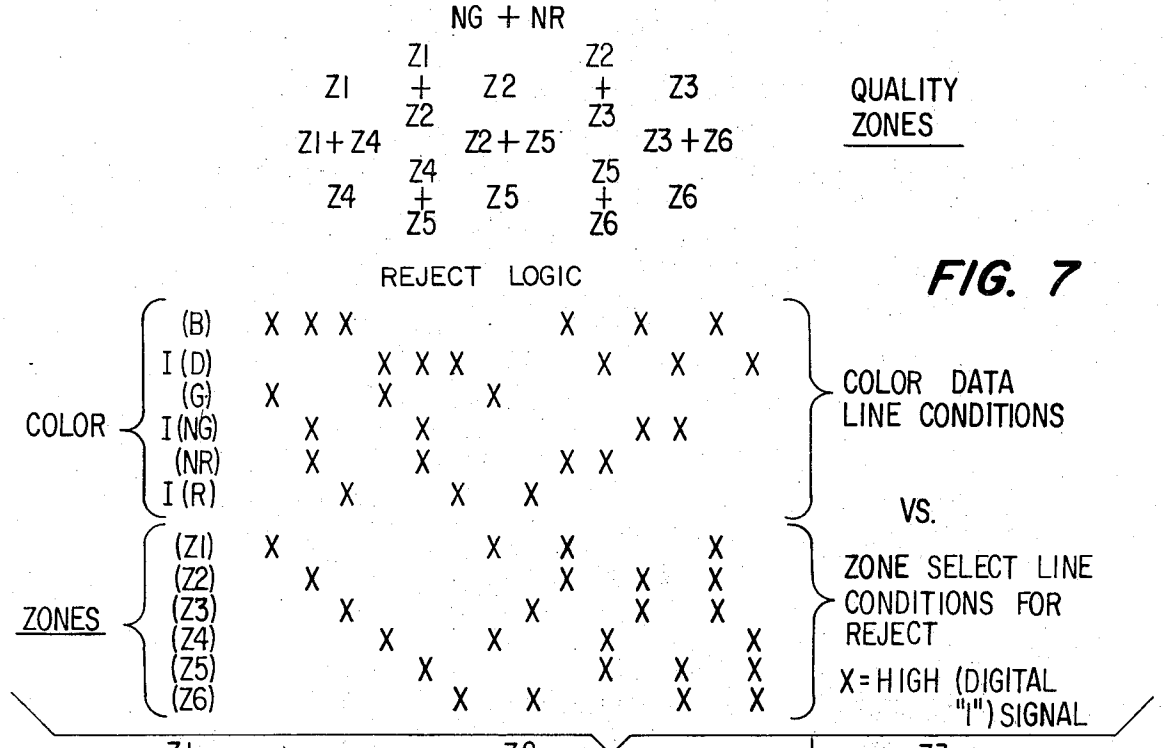


FIG. 7

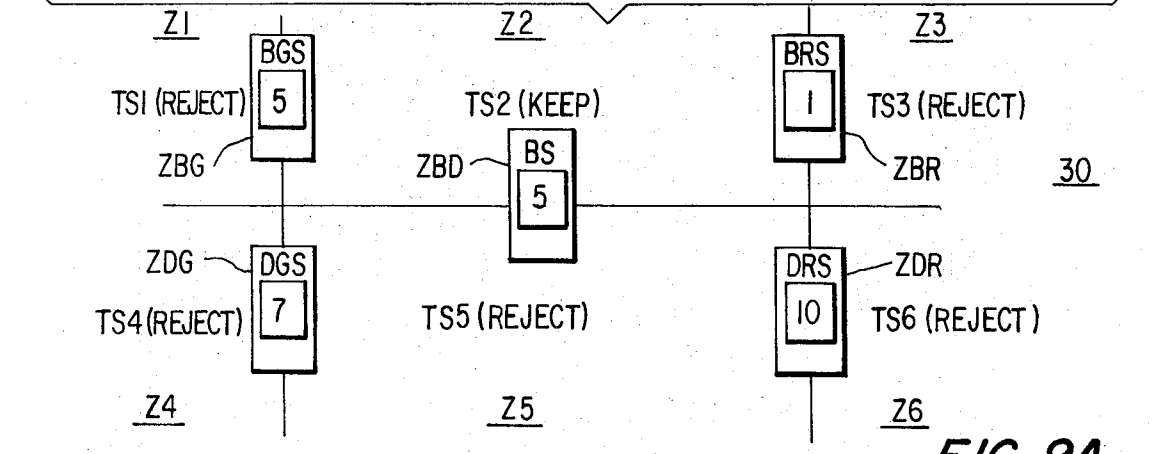


FIG. 9A

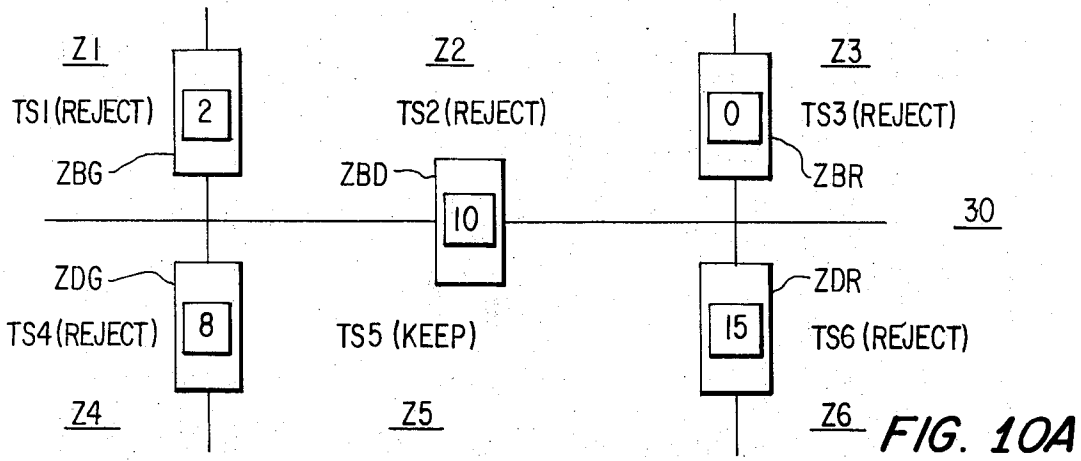


FIG. 10A

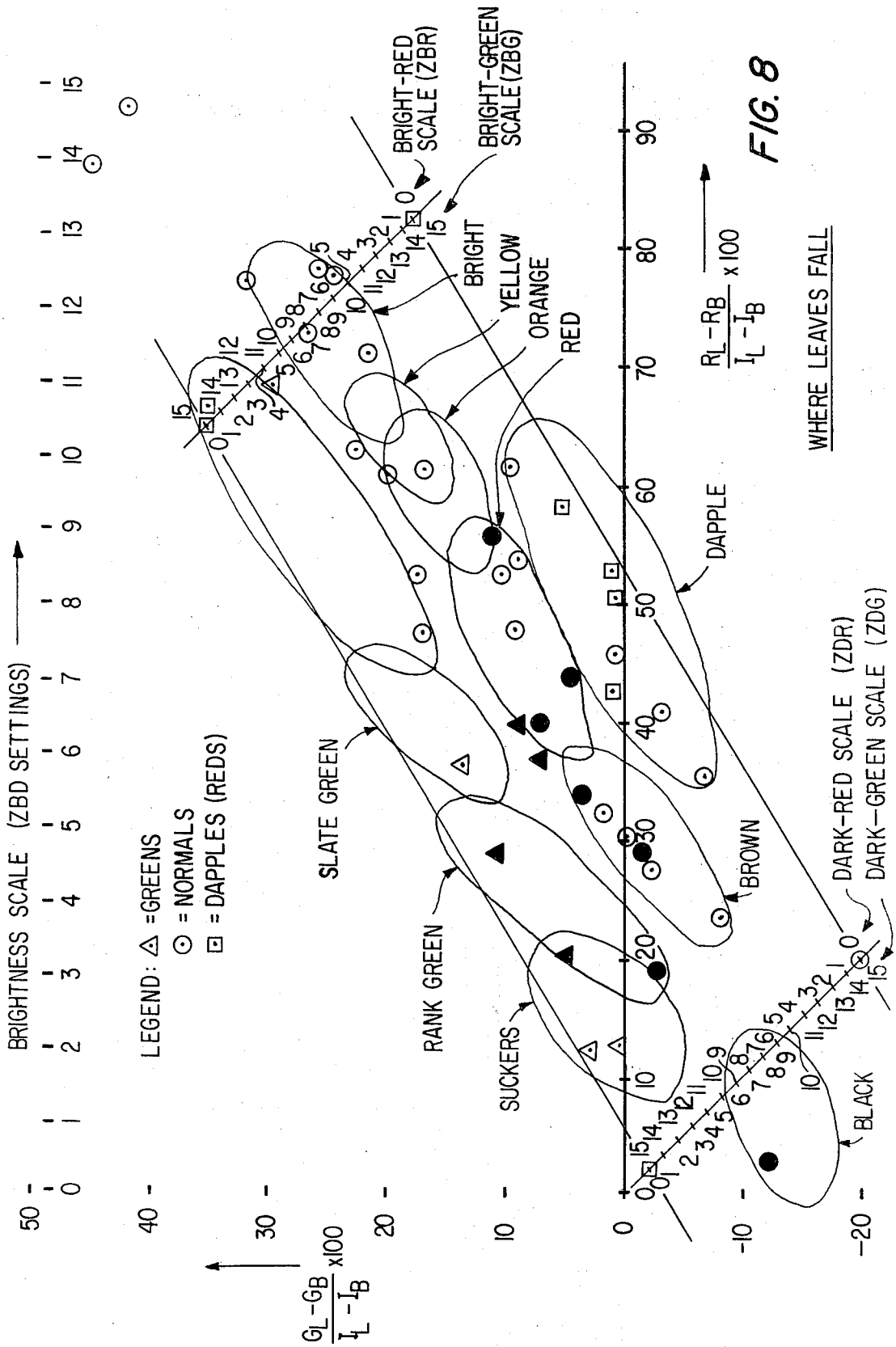

BRIGHTNESS SCALE (ZBD SETTINGS)
LEGEND: △ =GREENS
⊙ = NORMALS
⊡ = DAPPLES (REDS)
BRIGHT-RED SCALE (ZBR)
BRIGHT-GREEN SCALE (ZBG)
BRIGHT
YELLOW
ORANGE
RED
SLATE GREEN
RANK GREEN
SUCKERS
DAPPLE
BROWN
BLACK
DARK-RED SCALE (ZDR)
DARK-GREEN SCALE (ZDG)
WHERE LEAVES FALL
$\frac{G_L - G_B}{I_L - I_B} \times 100$
$\frac{R_L - R_B}{I_L - I_B} \times 100$

FIG. 8

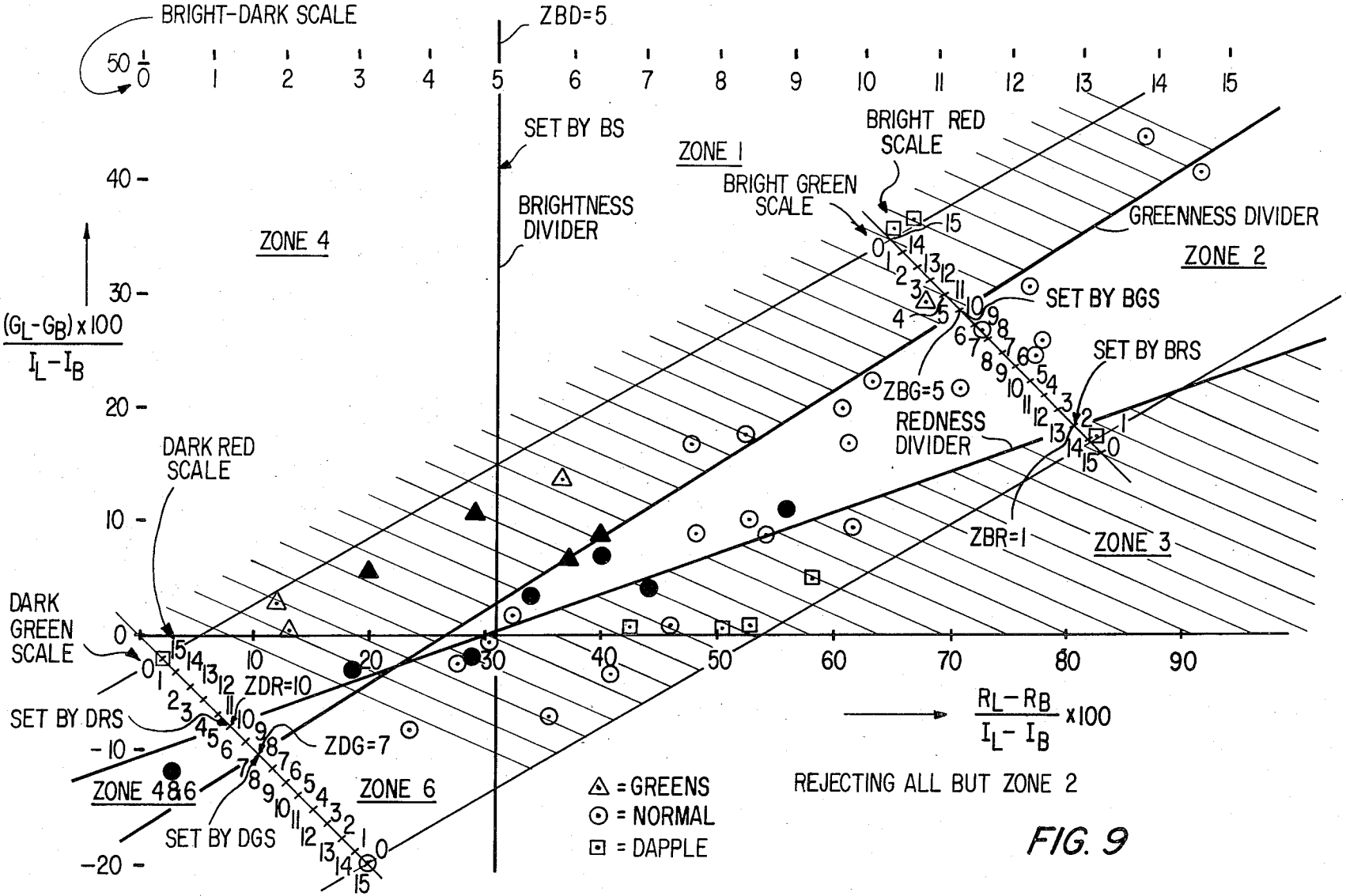

BRIGHT-DARK SCALE
ZBD=5
SET BY BS
BRIGHTNESS DIVIDER
ZONE 1
BRIGHT RED SCALE
BRIGHT GREEN SCALE
GREENNESS DIVIDER
ZONE 2
ZONE 4
SET BY BGS
SET BY BRS
ZBG=5
REDNESS DIVIDER
ZBR=1
ZONE 3
DARK RED SCALE
DARK GREEN SCALE
SET BY DRS
ZDR=10
ZDG=7
ZONE 4&6
ZONE 6
SET BY DGS
(GL-GB) x100 / IL-IB
RL-RB / IL-IB x100
△ = GREENS
⊙ = NORMAL
⊡ = DAPPLE
REJECTING ALL BUT ZONE 2

FIG. 9

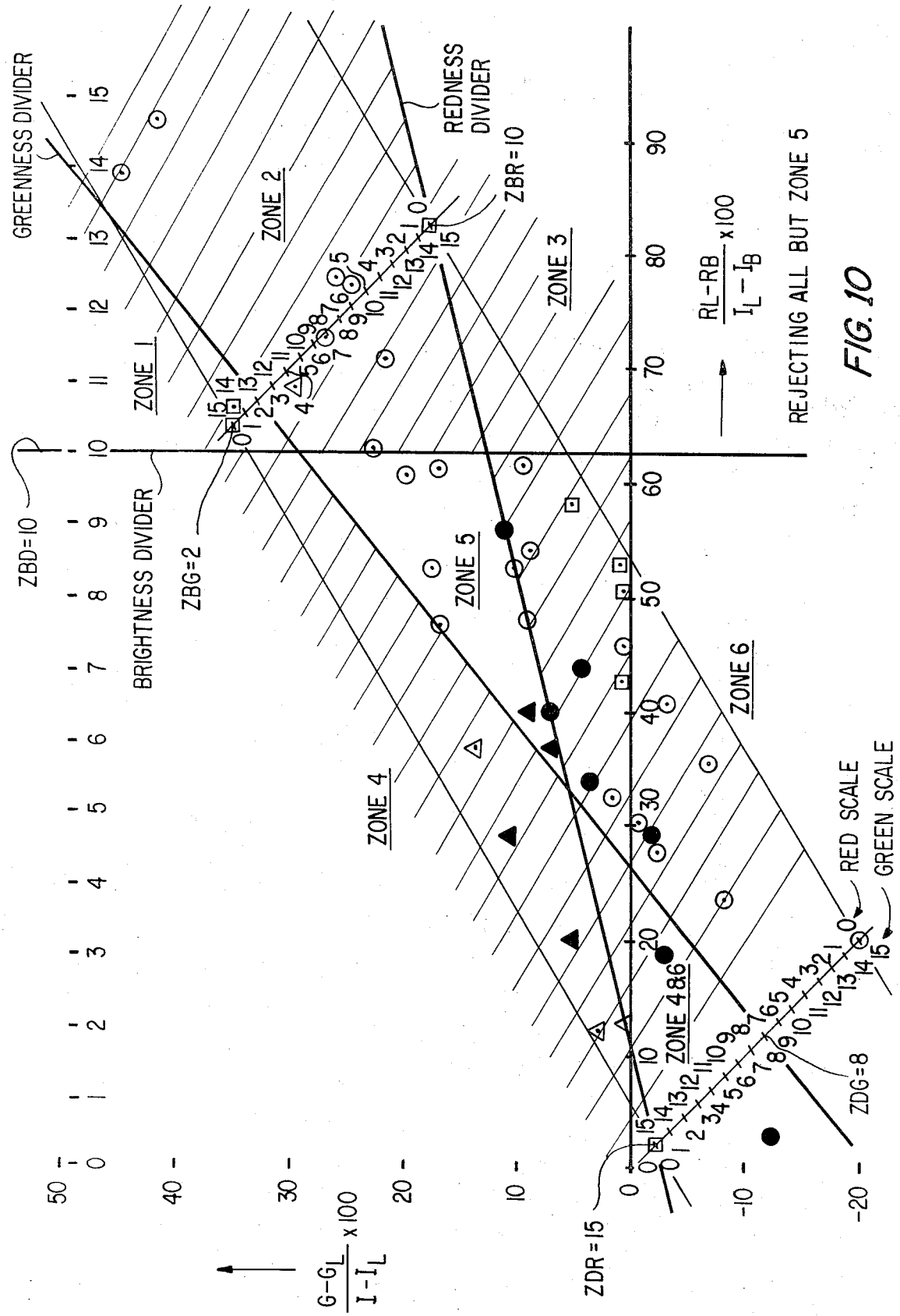

GREENNESS DIVIDER
REDNESS DIVIDER
BRIGHTNESS DIVIDER
ZONE 1
ZONE 2
ZONE 3
ZONE 4
ZONE 5
ZONE 6
ZONE 4&6
ZBD=10
ZBG=2
ZBR=10
ZDR=15
ZDG=8
RED SCALE
GREEN SCALE
REJECTING ALL BUT ZONE 5
$\frac{G-G_L}{I-I_L} \times 100$
$\frac{RL-RB}{I_L-I_B} \times 100$

FIG. 10

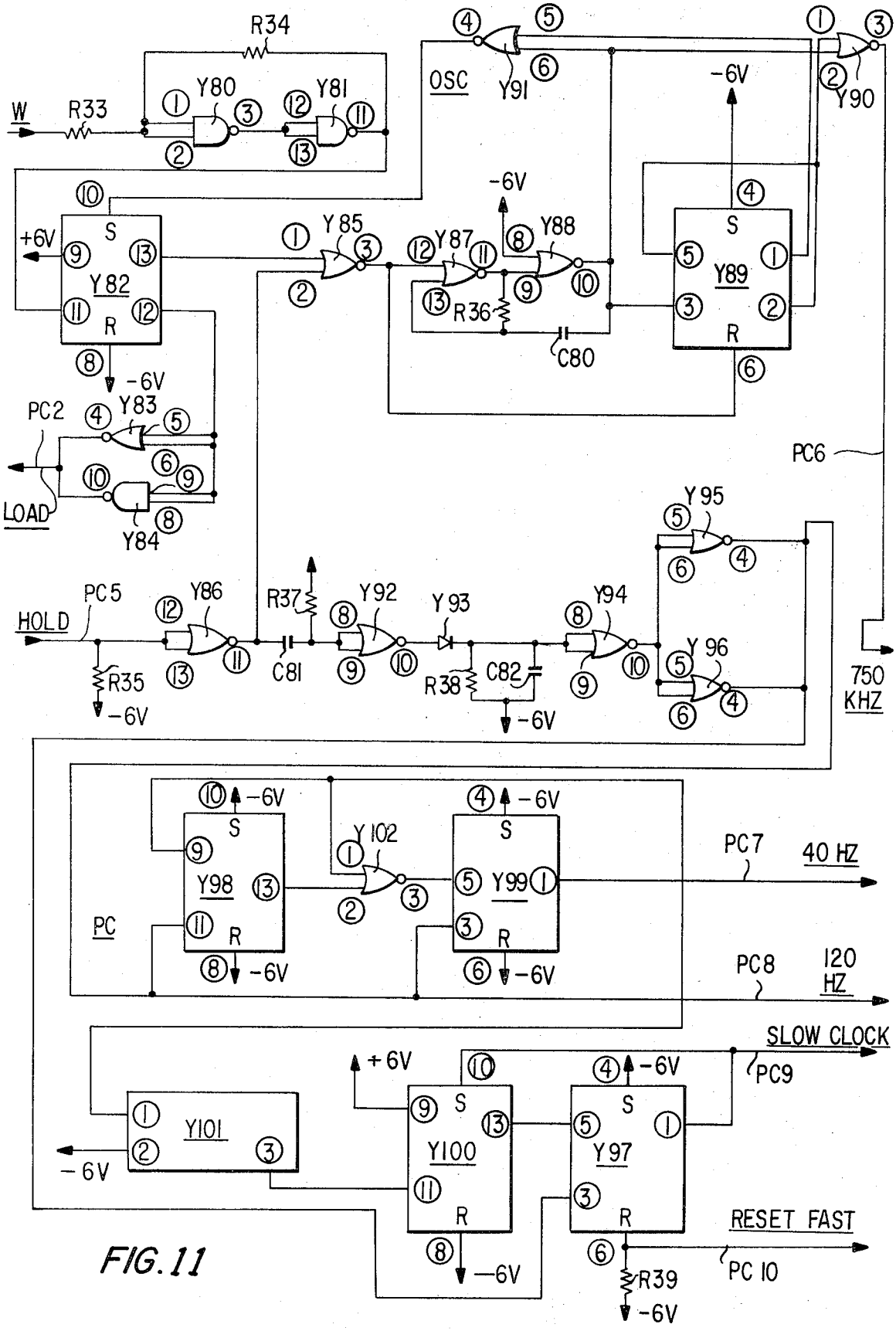

R34
W
R33
Y80
Y81
OSC
Y91
Y90
-6V
+6V
S
Y82
R
Y85
Y87
Y88
R36
C80
Y89
PC2
Y83
LOAD
Y84
PC6
Y95
PC5
HOLD
Y86
R37
C81
Y92
Y93
R38
C82
Y94
Y96
R35
750
KHZ
Y98
PC
Y102
Y99
PC7
40 HZ
PC8
120
HZ
SLOW CLOCK
PC9
Y101
Y100
Y97
RESET FAST
PC 10
R39

FIG. 11

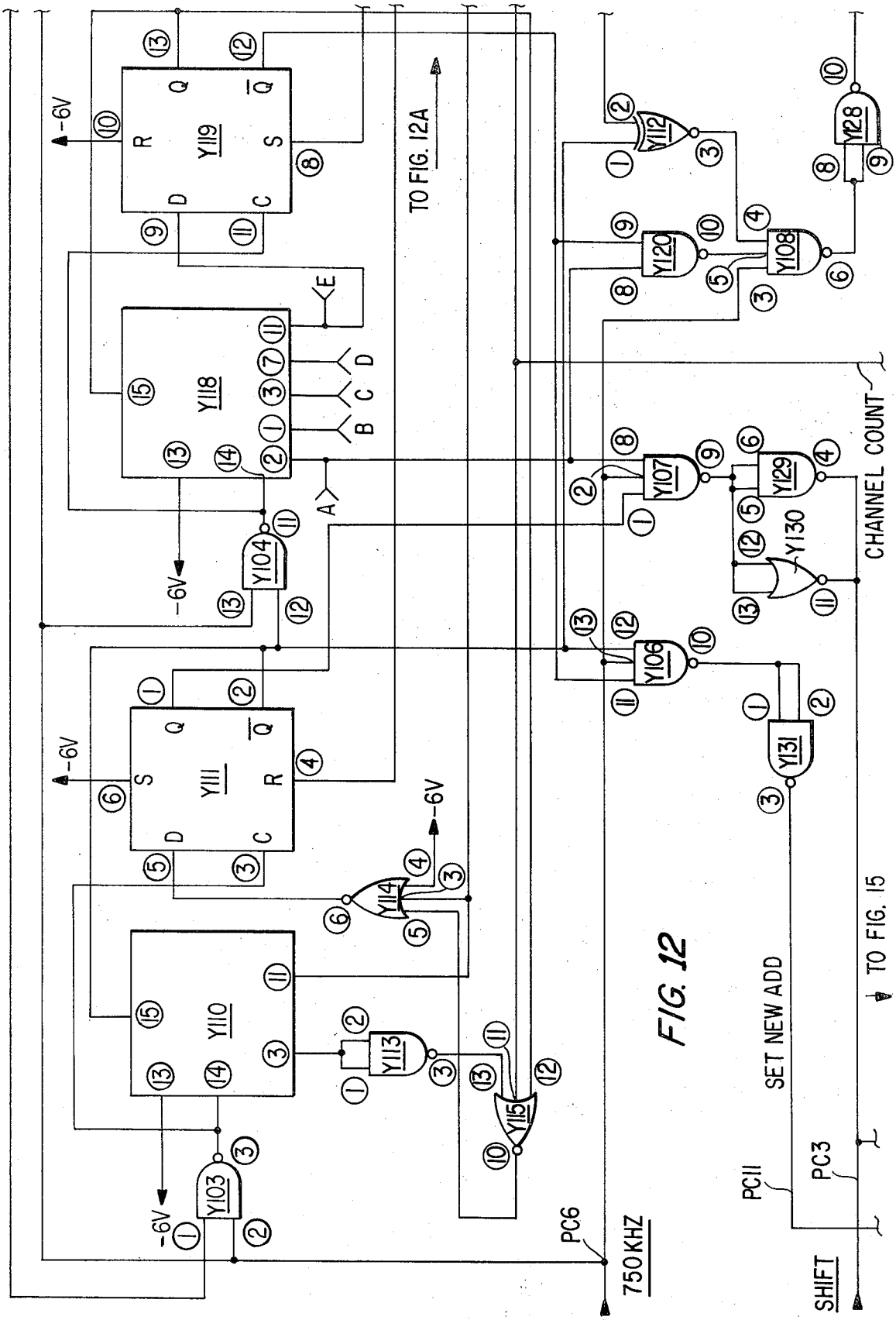

-6V
Y119
R
S
D
C
Q
$\overline{Q}$
TO FIG. 12A
E
Y118
A
B
C
D
Y104
Y111
Y110
Y103
Y114
Y113
Y115
Y112
Y120
Y108
Y128
Y107
Y129
Y130
Y106
Y131
CHANNEL COUNT
SET NEW ADD
PC11
PC3
SHIFT
PC6
750 KHZ
TO FIG. 15

FIG. 12

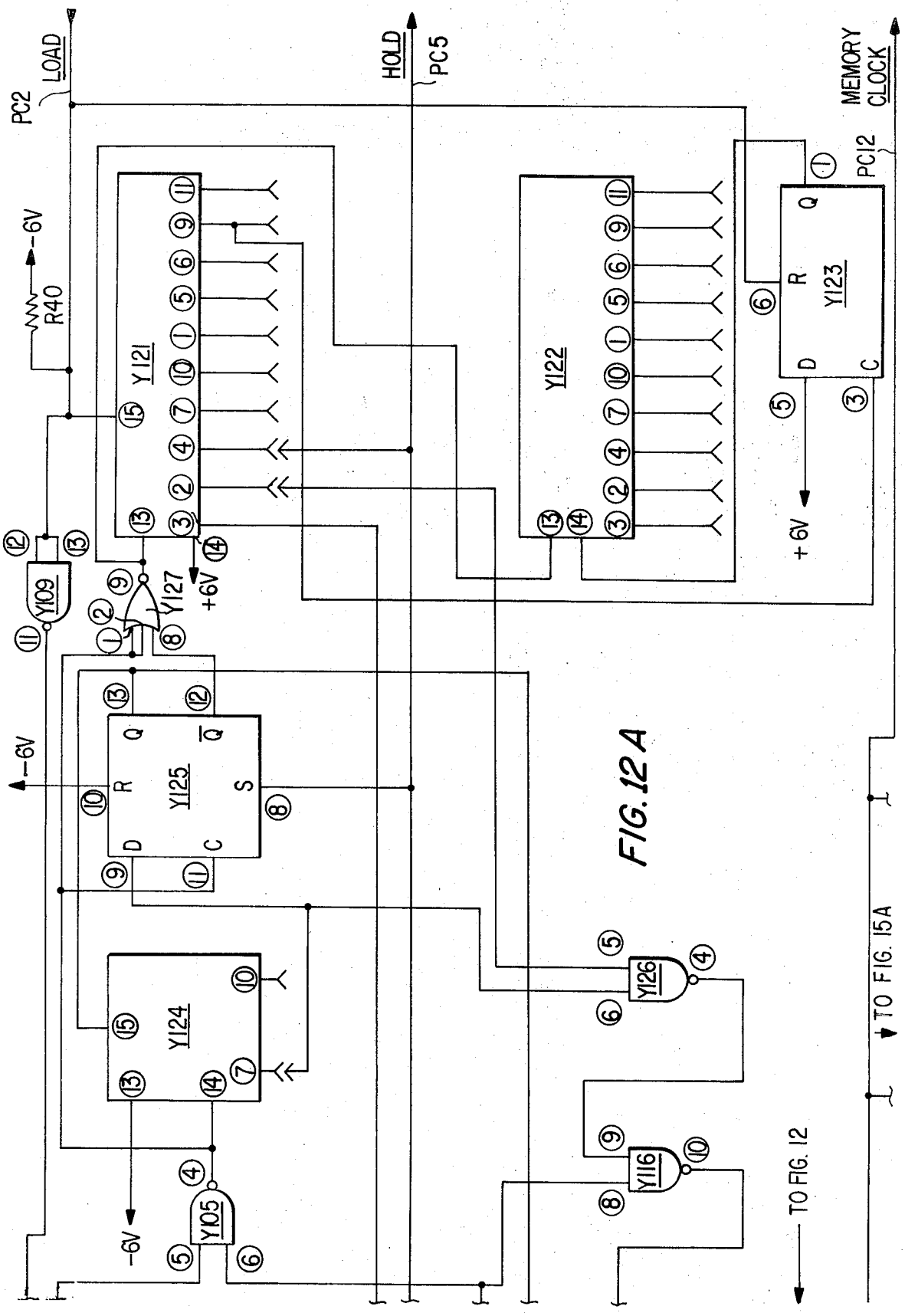

LOAD
PC2
HOLD
PC5
MEMORY CLOCK
PC12
-6V
R40
Y121
Y122
Y123
Y109
Y127
+6V
Y125
Y124
Y126
Y116
Y105
TO FIG. 15A
TO FIG. 12

FIG. 12A

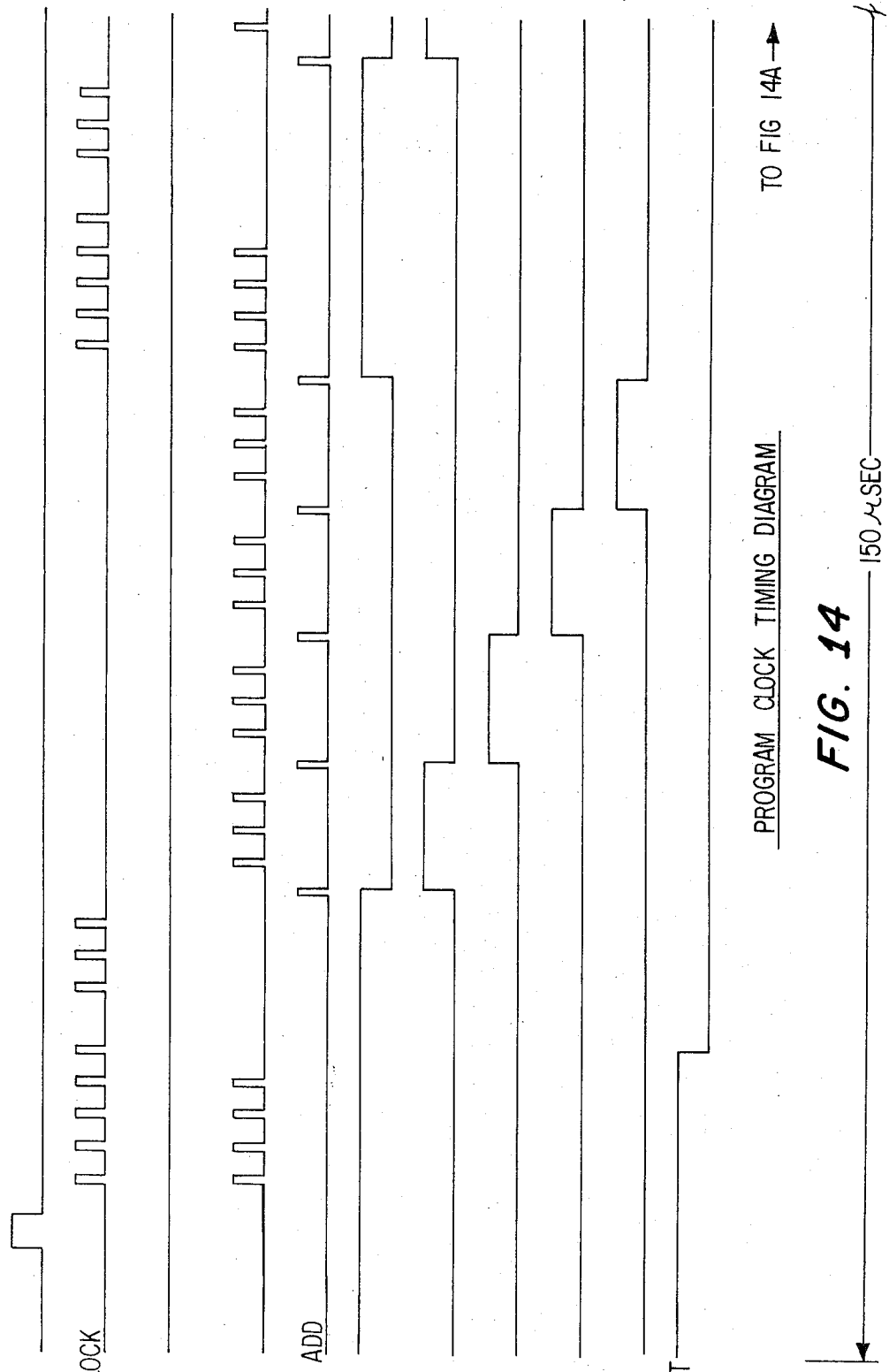

LOAD
SHIFT CLOCK
120 HZ
MEMORY CLOCK
SET NEW ADD
"A"
"B"
"C"
"D"
"E"
ACC. RESET
PROGRAM CLOCK TIMING DIAGRAM
TO FIG 14A
150 μSEC

FIG. 14

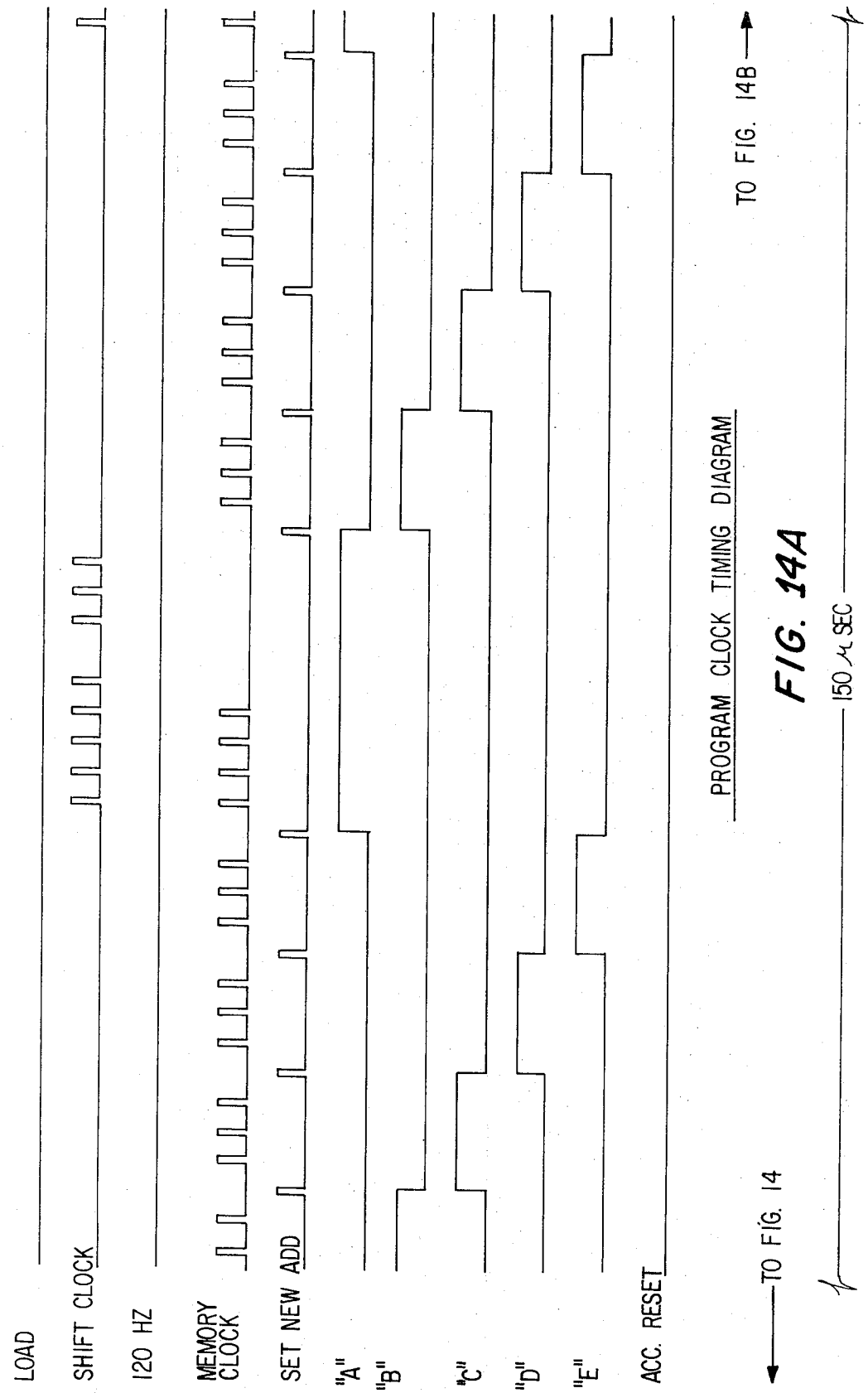

LOAD
SHIFT CLOCK
120 HZ
MEMORY CLOCK
SET NEW ADD
"A"
"B"
"C"
"D"
"E"
ACC. RESET
TO FIG. 14
TO FIG. 14B
PROGRAM CLOCK TIMING DIAGRAM
150 μ SEC

FIG. 14A

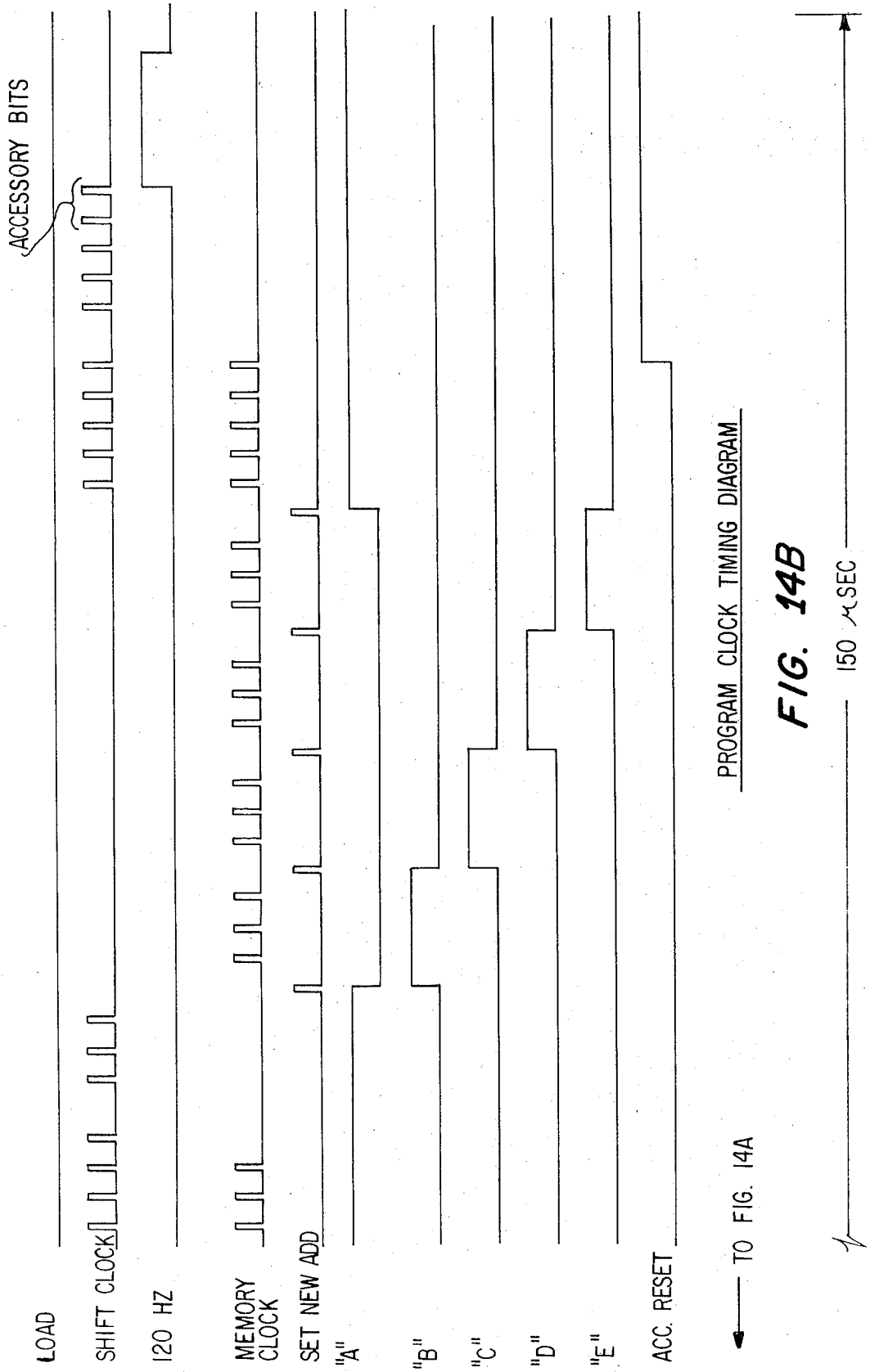

ACCESSORY BITS
LOAD
SHIFT CLOCK
120 HZ
MEMORY CLOCK
SET NEW ADD
"A"
"B"
"C"
"D"
"E"
ACC. RESET
TO FIG. 14A
PROGRAM CLOCK TIMING DIAGRAM
150 μSEC

FIG. 14B

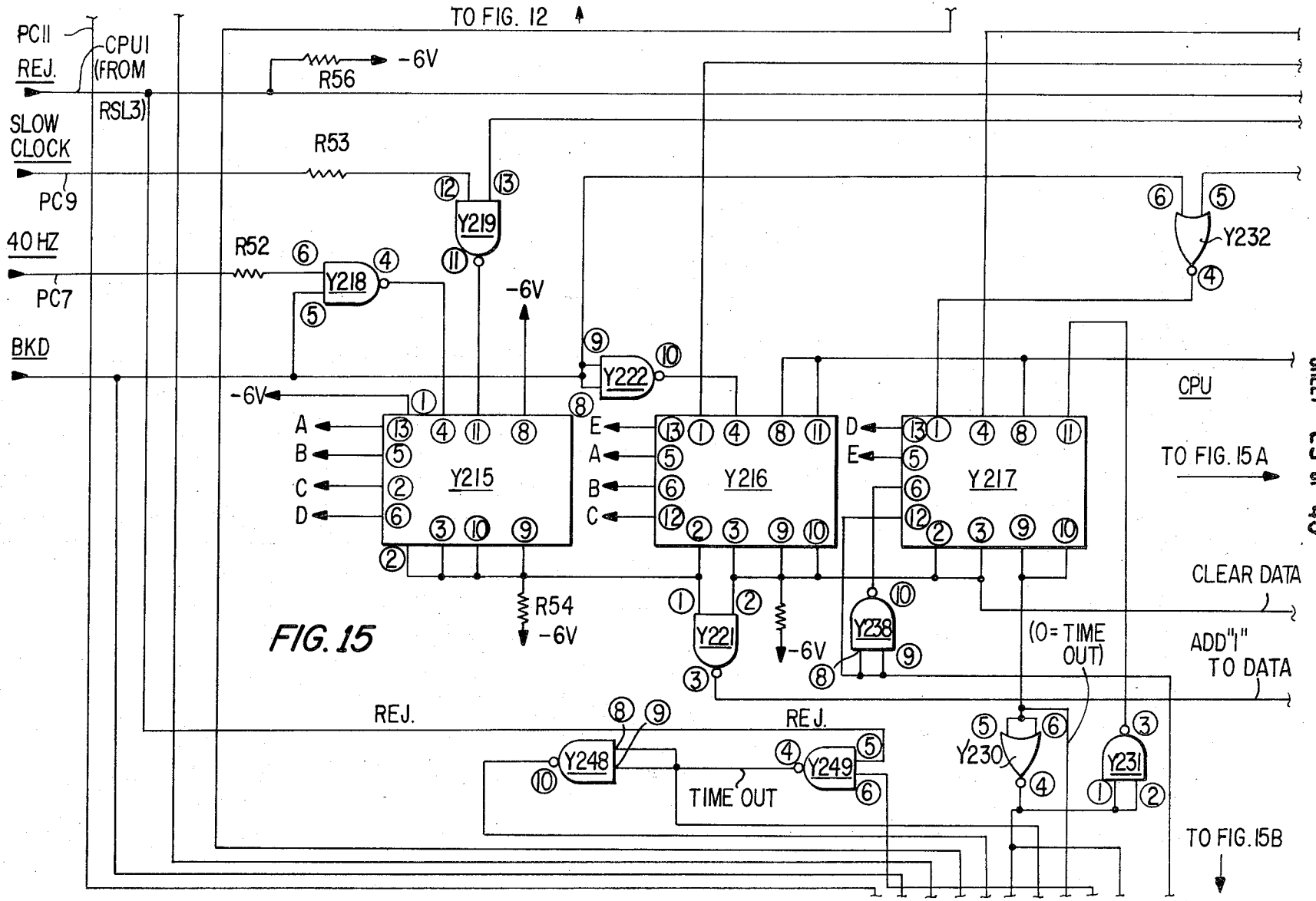

TO FIG. 12
PCII
REJ.
CPUI (FROM RSL3)
SLOW CLOCK
PC9
40 HZ
PC7
BKD
R56
-6V
R53
R52
Y218
Y219
Y222
Y232
-6V
-6V
A
B
C
D
Y215
E
A
B
C
Y216
D
E
Y217
CPU
TO FIG. 15A
CLEAR DATA
ADD "1" TO DATA
(0 = TIME OUT)
R54
-6V
Y221
-6V
Y238
REJ.
REJ.
Y248
Y249
TIME OUT
Y230
Y231
TO FIG. 15B

FIG. 15

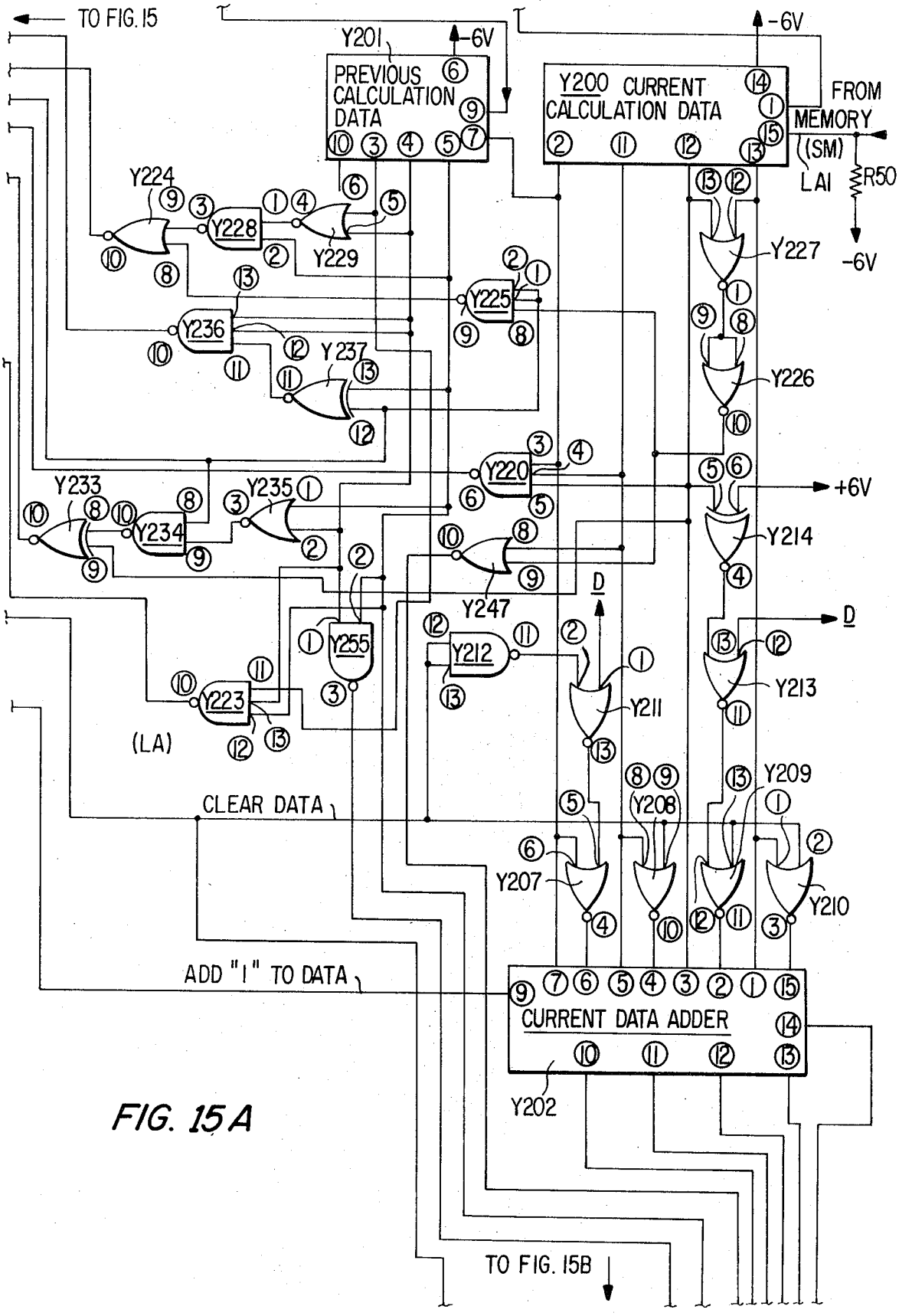

TO FIG. 15
Y201
-6V
PREVIOUS CALCULATION DATA
Y200 CURRENT CALCULATION DATA
-6V
FROM MEMORY
(SM)
LAI
R50
-6V
Y224
Y228
Y229
Y225
Y227
Y236
Y237
Y226
Y220
+6V
Y233
Y235
Y234
Y214
Y247
D
D
Y255
Y212
Y213
Y223
Y211
(LA)
Y209
Y208
CLEAR DATA
Y207
Y210
ADD "1" TO DATA
CURRENT DATA ADDER
Y202
TO FIG. 15B

FIG. 15A

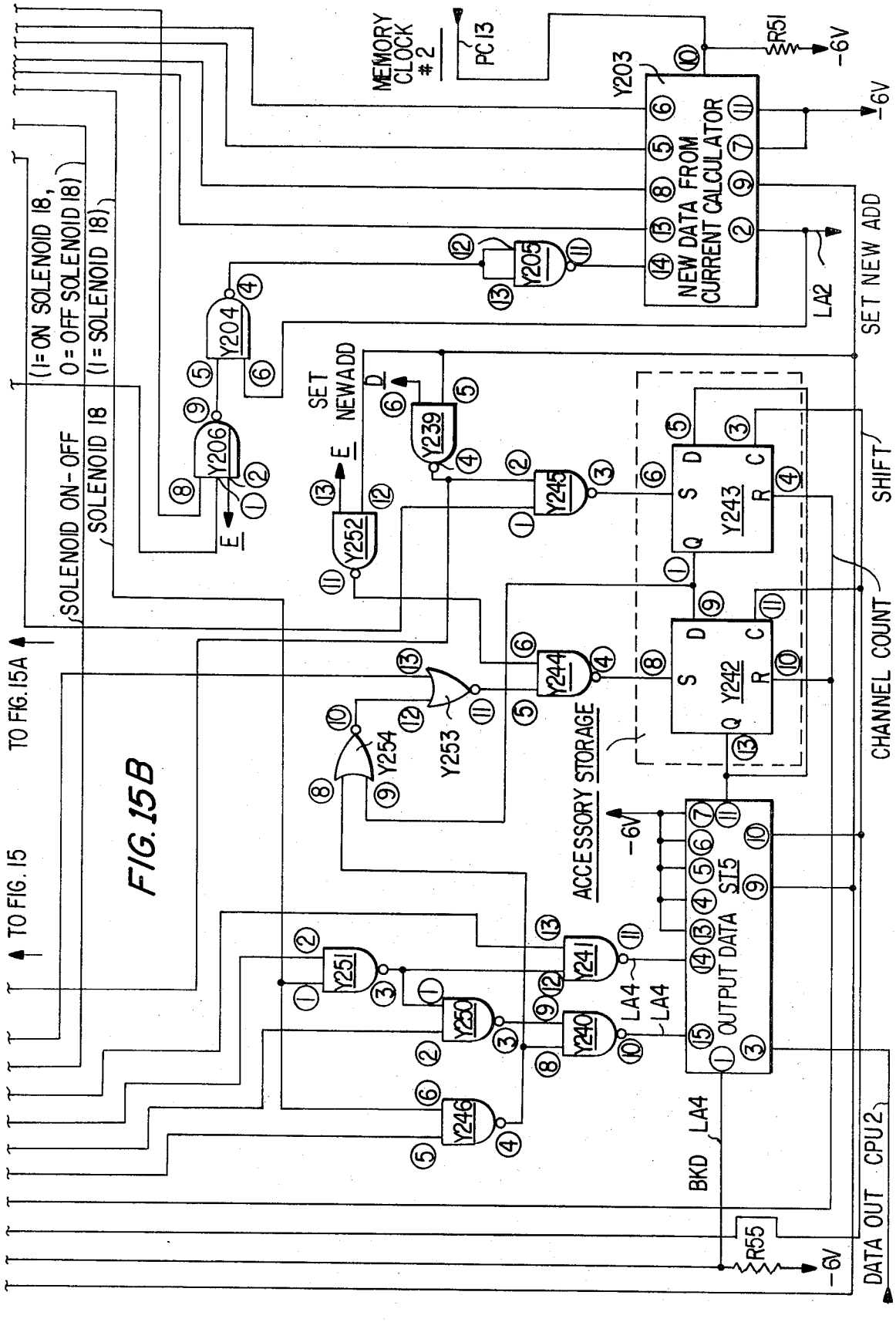

MEMORY CLOCK #2
PC13
Y203
NEW DATA FROM CURRENT CALCULATOR
R51
-6V
+6V
LA2
SET NEW ADD
Y205
Y204
Y206
SET NEWADD
E
D
Y239
Y252
Y245
Y243
Y242
SHIFT
CHANNEL COUNT
Y244
Y253
Y254
ACCESSORY STORAGE
Y251
Y250
Y246
Y241
Y240
LA4
OUTPUT DATA ST5
BKD LA4
R55
DATA OUT CPU2
(1= ON SOLENOID 18, 0 = OFF SOLENOID 18)
(1 = SOLENOID 18)
SOLENOID ON-OFF SOLENOID 18
TO FIG. 15A
TO FIG. 15

FIG. 15B

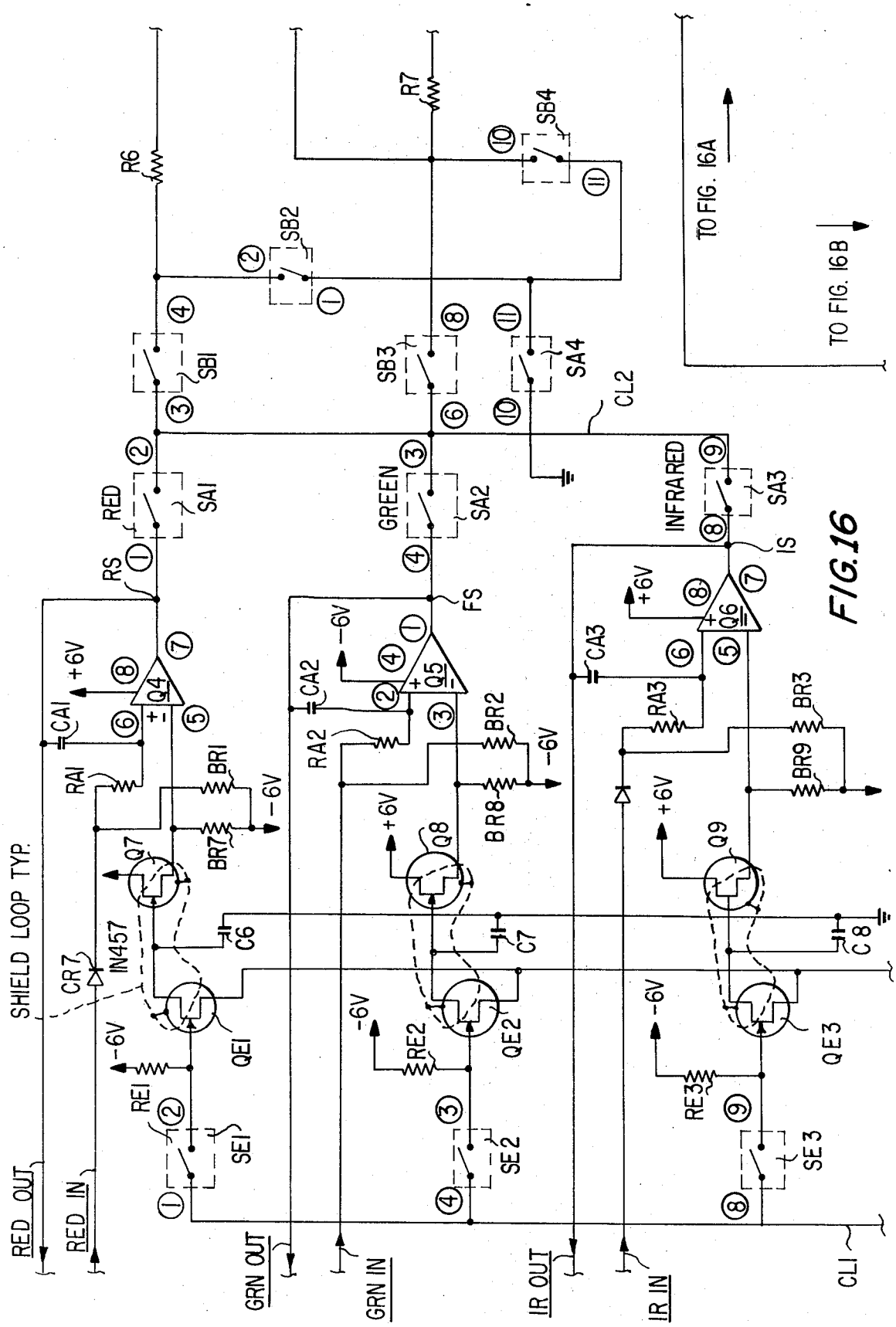

TO FIG. 16A
TO FIG. 16B
R6
R7
SB1
SB2
SB3
SB4
SA1
SA2
SA3
SA4
RED
GREEN
INFRARED
RS
FS
IS
CL2
Q4
Q5
Q6
Q7
Q8
Q9
+6V
-6V
CA1
CA2
CA3
RA1
RA2
RA3
BR1
BR2
BR3
BR7
BR8
BR9
C6
C7
C8
CR7
IN457
QE1
QE2
QE3
RE1
RE2
RE3
SE1
SE2
SE3
SHIELD LOOP TYP.
RED OUT
RED IN
GRN OUT
GRN IN
IR OUT
IR IN
CLI

FIG. 16

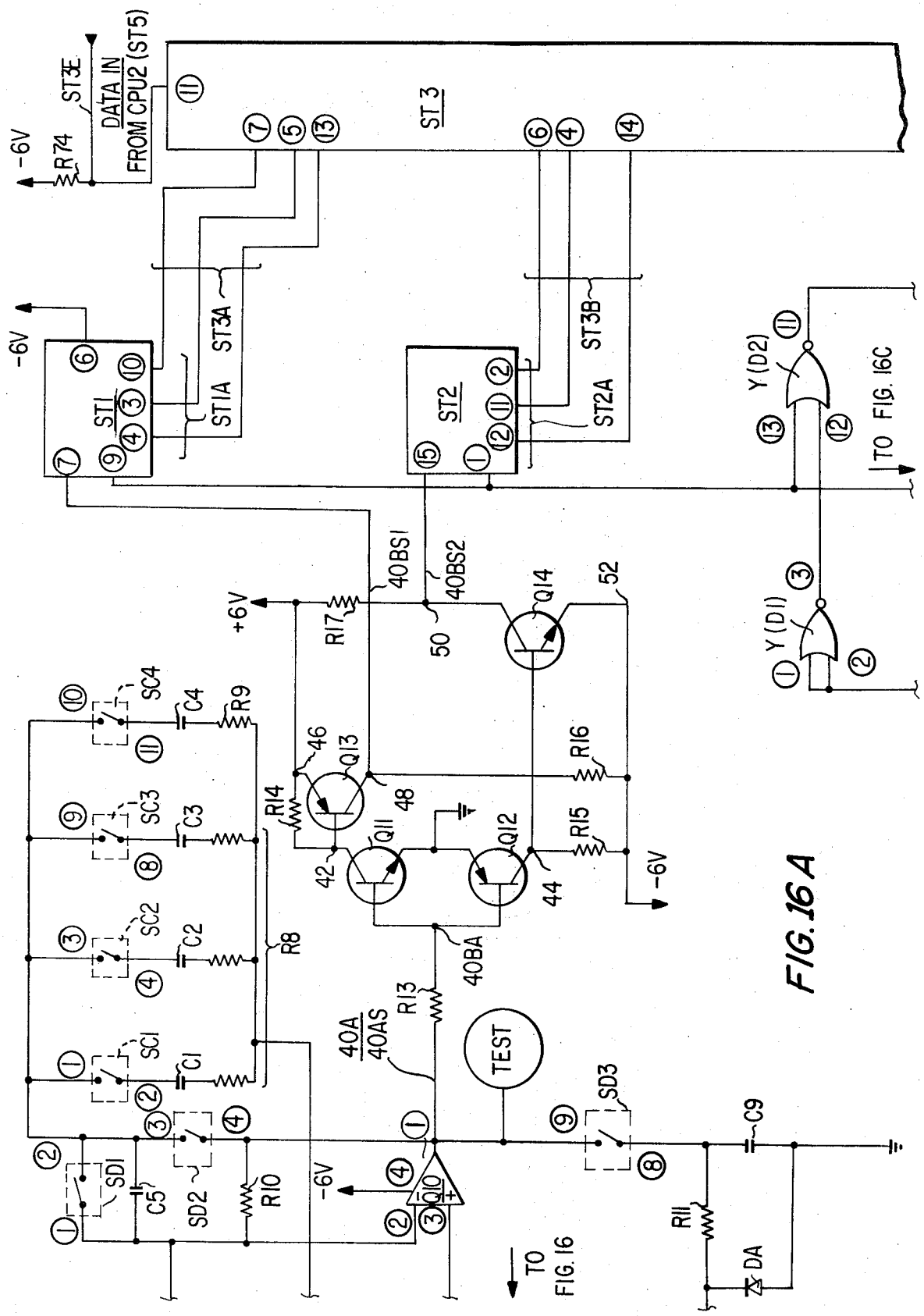

ST3E
DATA IN
FROM CPU2 (ST5)
-6V
R74
ST 3
ST1
ST2
ST1A
ST3A
ST2A
ST3B
Y(D2)
TO FIG. 16C
Y(D1)
+6V
R17
40BS1
40BS2
50
52
Q14
46
Q13
R16
R14
48
Q11
Q12
R15
42
44
40BA
R13
40A
40AS
TEST
SC4
C4
R9
SC3
C3
SC2
C2
R8
SC1
C1
SD1
C5
SD2
R10
Q10
SD3
C9
R11
DA
TO FIG. 16

FIG. 16A

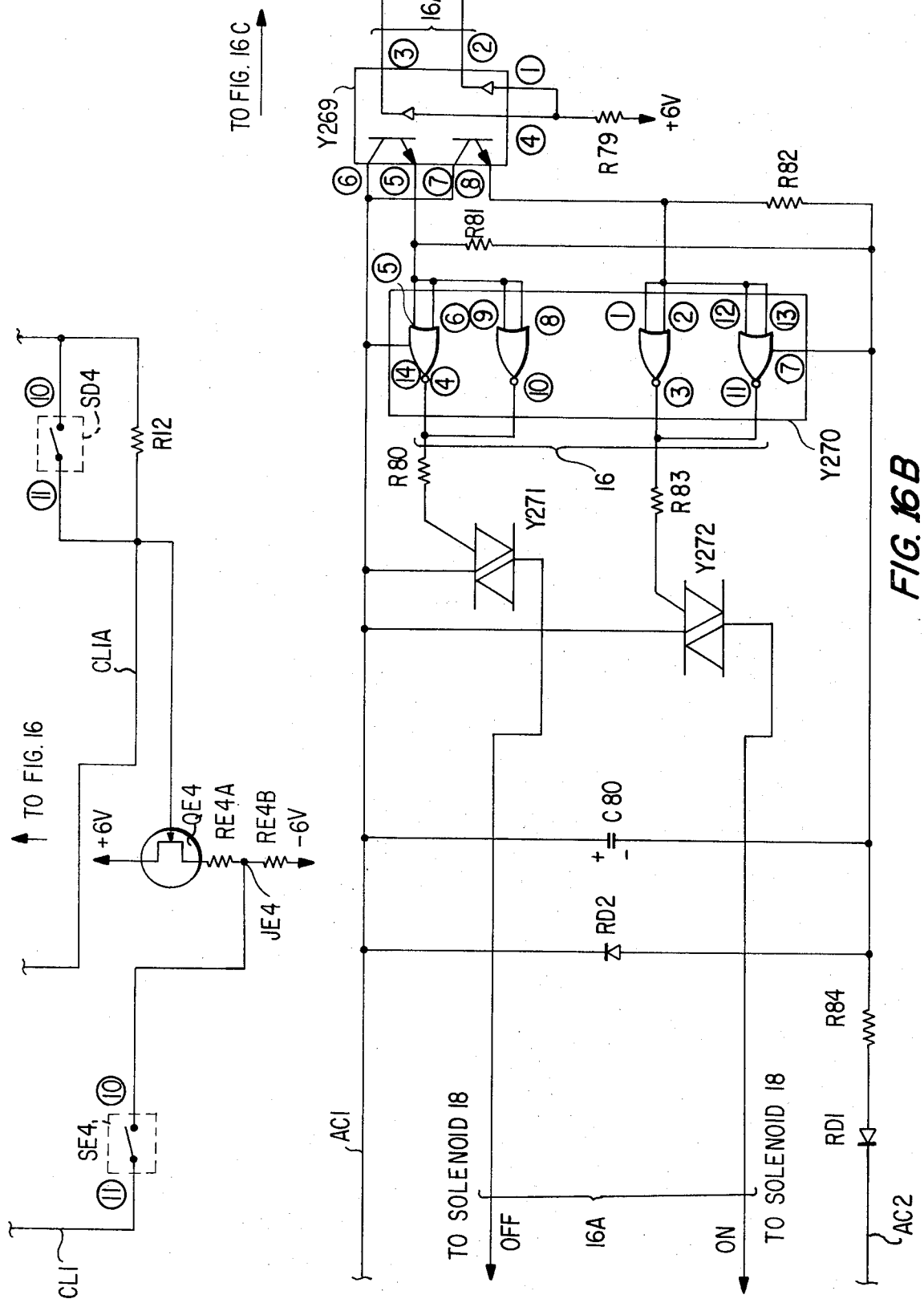

TO FIG. 16C
16A
Y269
+6V
R79
R82
R81
R80
16
R83
Y270
Y271
Y272
C80
RD2
AC1
TO SOLENOID 18
OFF
16A
ON
TO SOLENOID 18
R84
RD1
AC2
TO FIG. 16
CL1A
+6V
QE4
RE4A
RE4B
-6V
JE4
SE4
CL1
SD4
R12

FIG. 16B

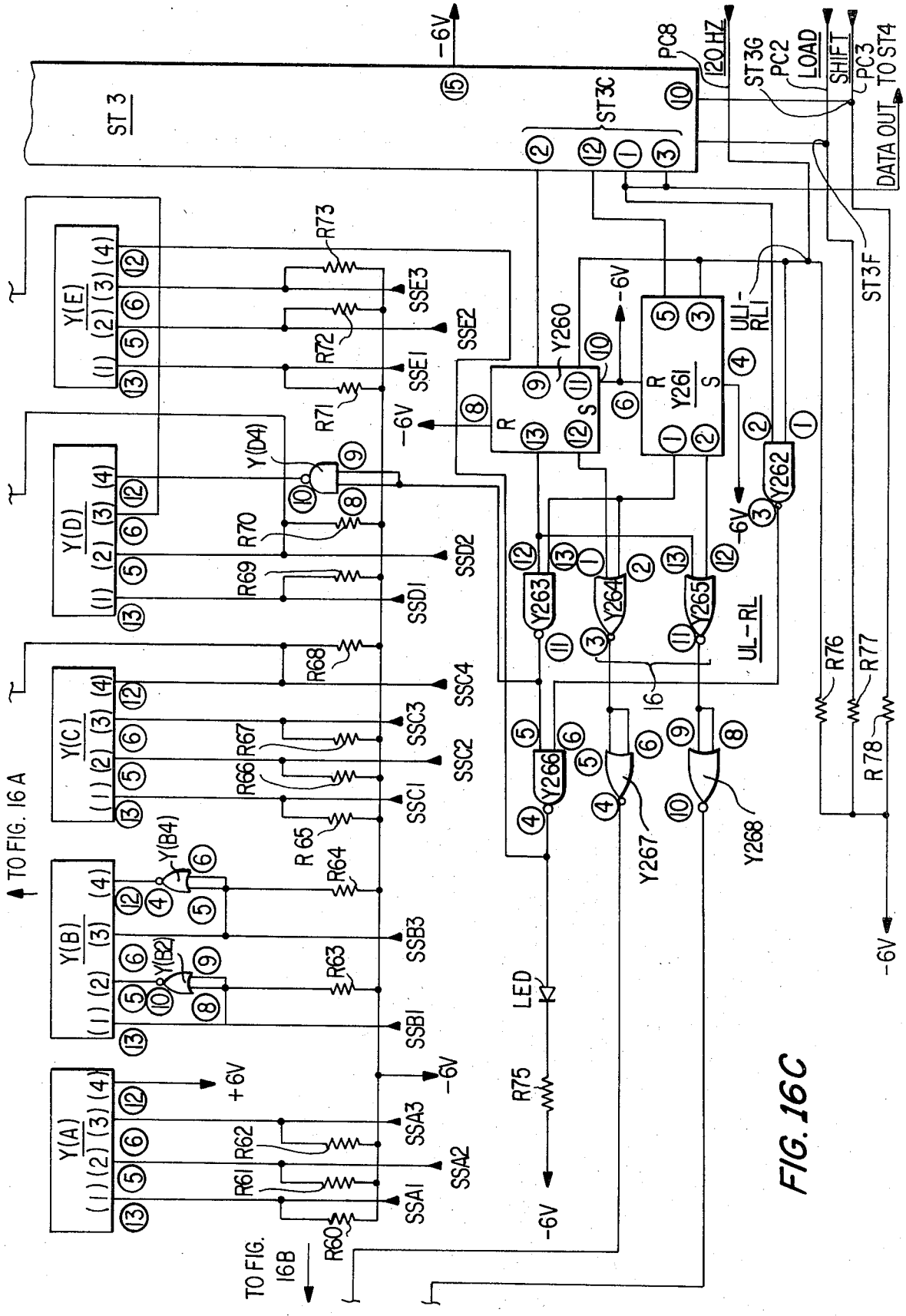

ST 3
-6V
PC8
120 HZ
ST3G
PC2
LOAD
SHIFT
PC3
TO ST4
DATA OUT
ST3C
ST3F
Y(E)
Y(D)
Y(C)
Y(B)
Y(A)
R73
R72
R71
R70
R69
R68
R67
R66
R65
R64
R63
R62
R61
R60
SSE3
SSE2
SSE1
SSD2
SSD1
SSC4
SSC3
SSC2
SSC1
SSB3
SSB1
SSA3
SSA2
SSA1
Y(D4)
Y(B4)
Y(B2)
+6V
Y260
Y261
Y262
Y263
Y264
Y265
Y266
Y267
Y268
ULI-RLI
UL-RL
I6
LED
R75
R76
R77
R 78
TO FIG. I6A
TO FIG. I6B

FIG. 16C

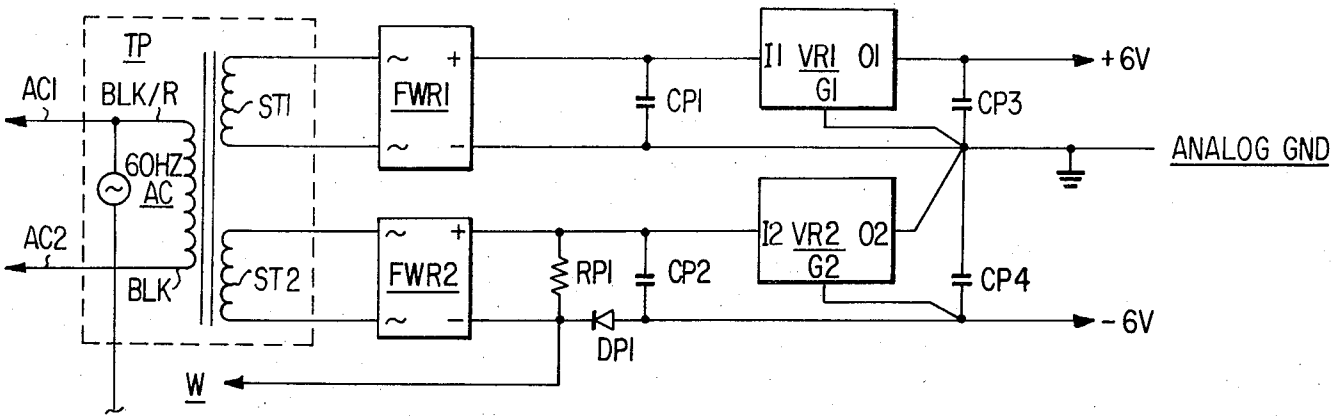
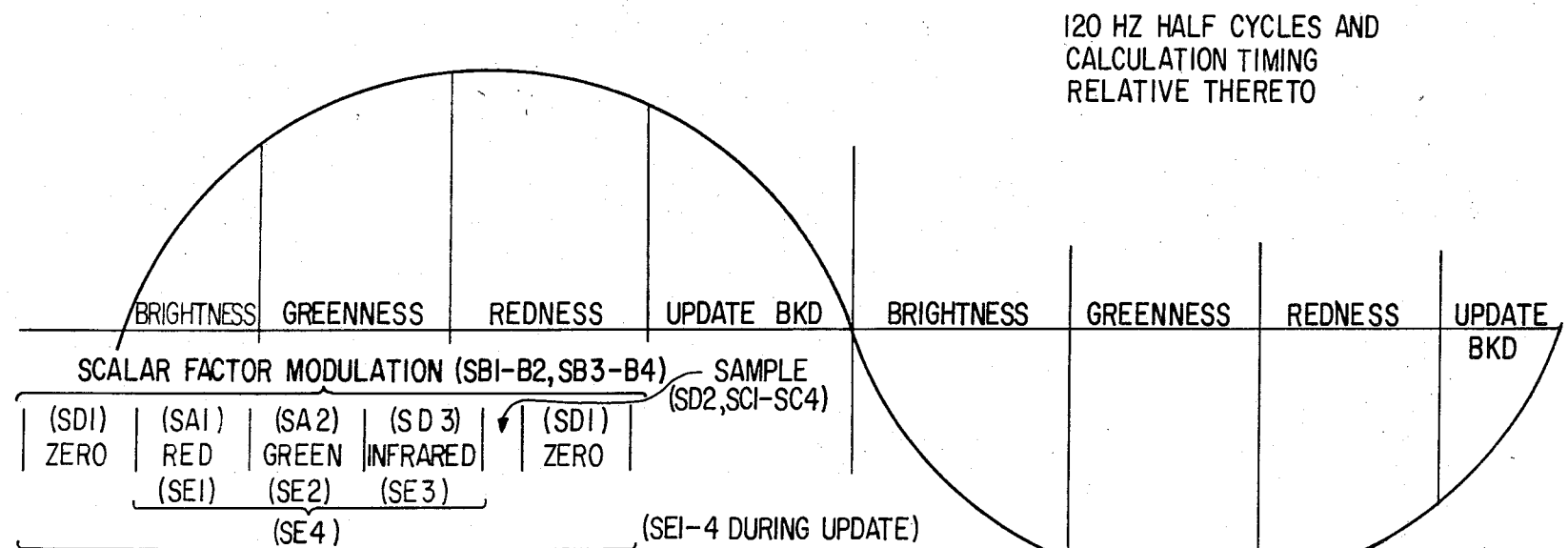


FIG. 17



TYPICAL SUBDIVISION OF BRIGHTNESS, GREENNESS, REDNESS AND UPDATE BACKGROUND CALCULATIONS EFFECTED BY THE PROGRAM CLOCK PC, FRONT PANEL LOGIC BOARD FPLB; AND CENTRAL PROCESSOR CPU.

FIG. 20

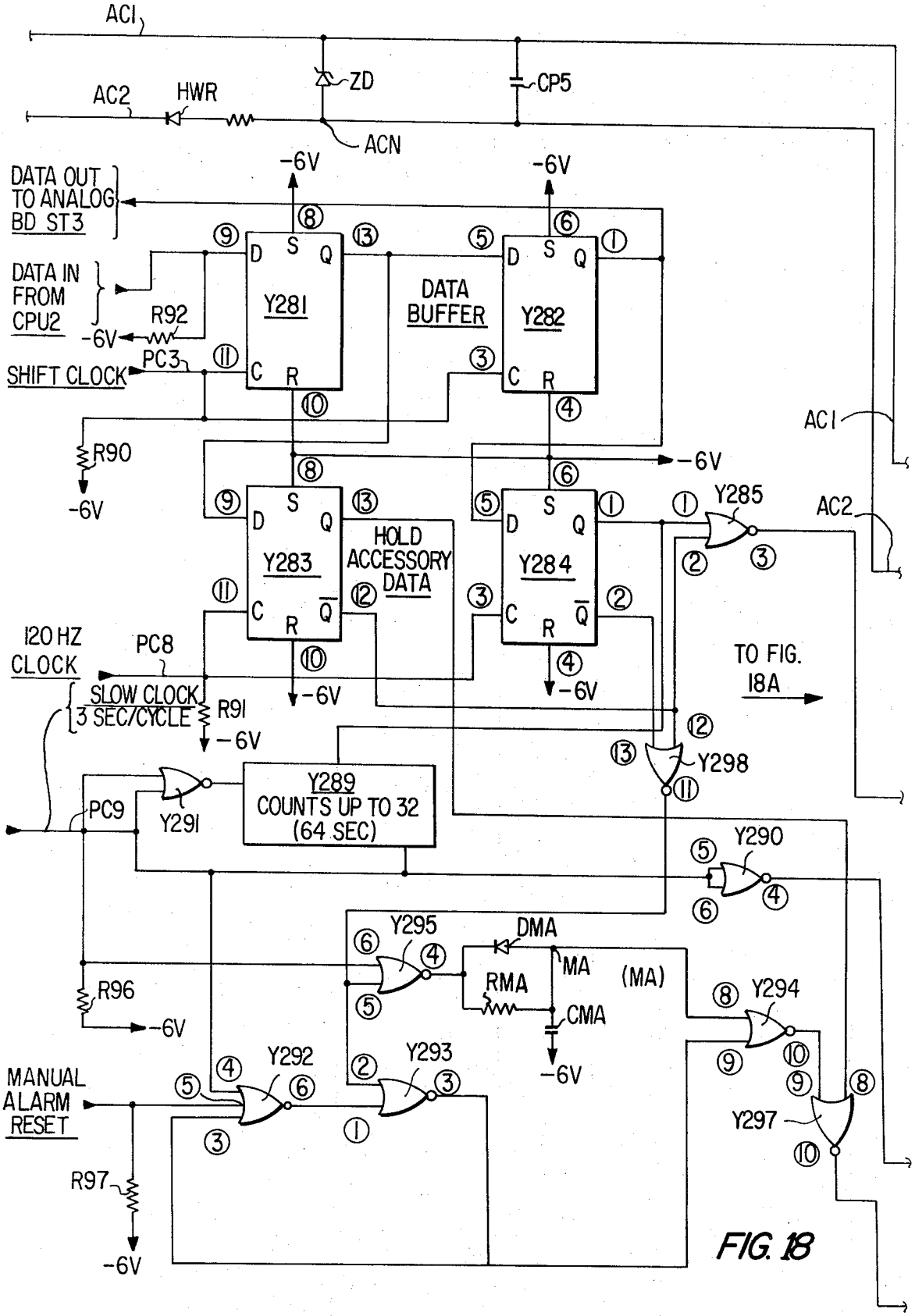

AC1
AC2
HWR
ZD
CP5
ACN
-6V
DATA OUT TO ANALOG BD ST3
DATA IN FROM CPU2
R92
SHIFT CLOCK
PC3
Y281
DATA BUFFER
Y282
R90
AC1
Y283
HOLD ACCESSORY DATA
Y284
Y285
AC2
120 HZ CLOCK
PC8
SLOW CLOCK 3 SEC/CYCLE
R91
TO FIG. 18A
Y298
Y289 COUNTS UP TO 32 (64 SEC)
PC9
Y291
Y290
Y295
DMA
RMA
MA
(MA)
CMA
R96
Y294
Y292
Y293
MANUAL ALARM RESET
Y297
R97

FIG. 18

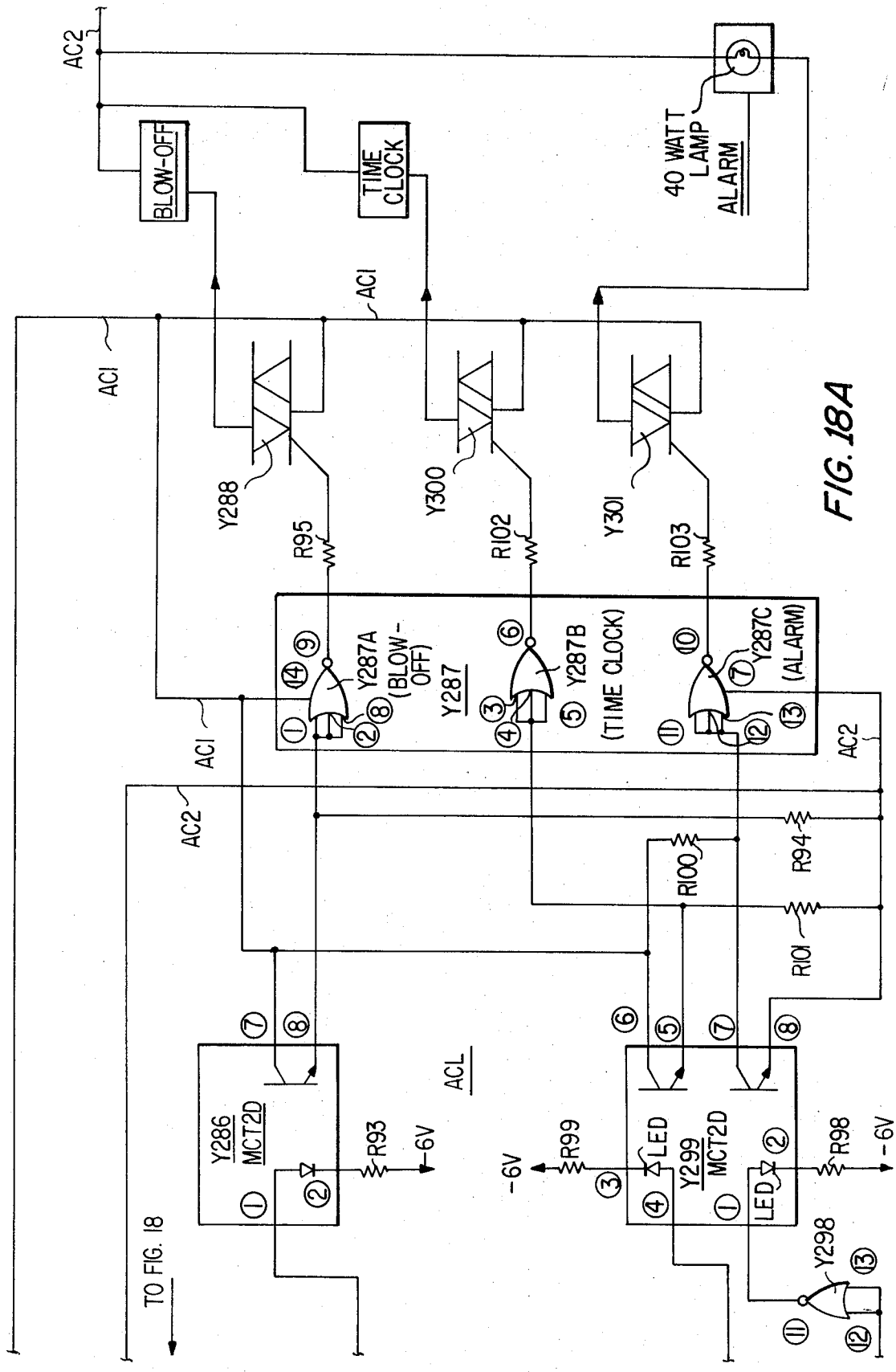

AC2
BLOW-OFF
TIME CLOCK
40 WATT LAMP ALARM
AC1
Y288
Y300
Y301
R95
R102
R103
Y287A (BLOW-OFF)
Y287
Y287B (TIME CLOCK)
Y287C (ALARM)
R100
R94
R101
Y286 MCT2D
R93
-6V
ACL
R99
LED
Y299 MCT2D
R98
Y298
TO FIG. 18

FIG. 18A

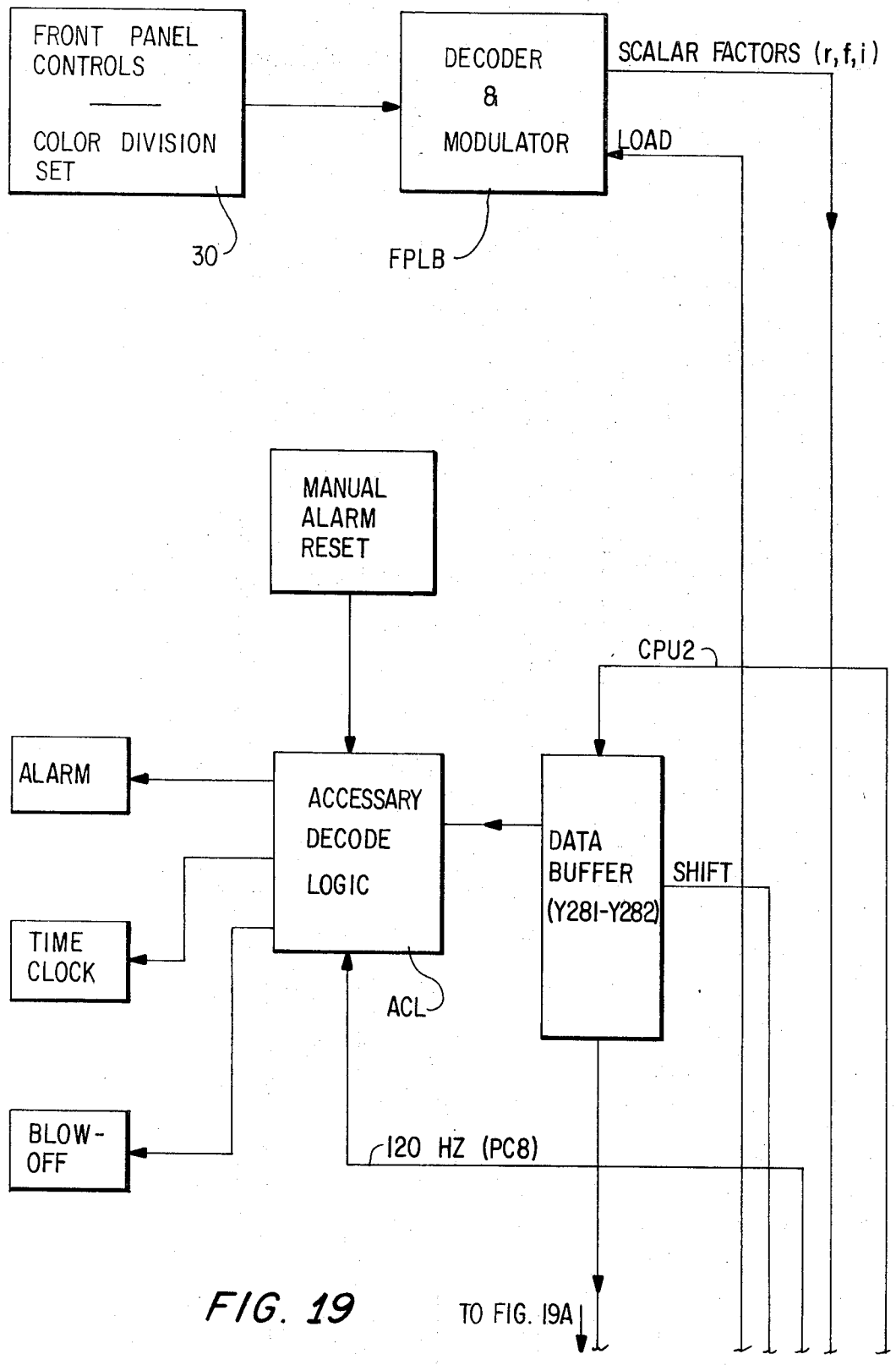

FRONT PANEL CONTROLS
COLOR DIVISION SET
30
DECODER & MODULATOR
FPLB
SCALAR FACTORS (r,f,i)
LOAD
MANUAL ALARM RESET
CPU2
ALARM
ACCESSARY DECODE LOGIC
ACL
DATA BUFFER (Y281-Y282)
SHIFT
TIME CLOCK
BLOW-OFF
120 HZ (PC8)
TO FIG. 19A

FIG. 19

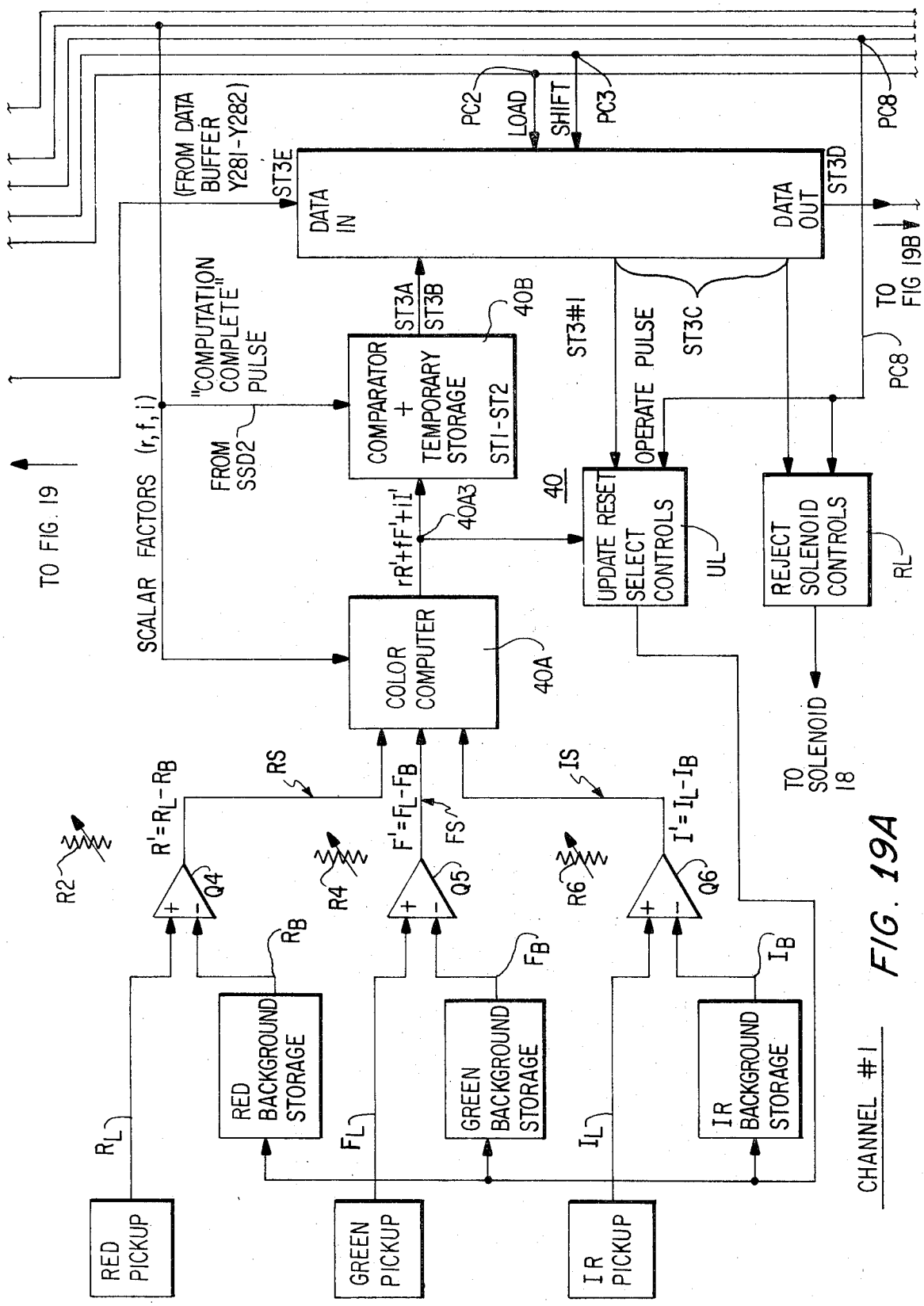

TO FIG. 19
SCALAR FACTORS (r,f,i)
(FROM DATA BUFFER Y281-Y282)
"COMPUTATION COMPLETE" PULSE
FROM SSD2
PC2
LOAD
SHIFT
PC3
PC8
ST3E
DATA IN
DATA OUT
ST3D
ST3A
ST3B
40B
COMPARATOR + TEMPORARY STORAGE
ST1-ST2
ST3#1
ST3C
OPERATE PULSE
TO FIG 19B
PC8
rR'+fF'+iI'
40A3
40
UPDATE RESET SELECT CONTROLS
UL
REJECT SOLENOID CONTROLS
RL
COLOR COMPUTER
40A
TO SOLENOID 18
RS
IS
R'=RL-RB
F'=FL-FB
FS
I'=IL-IB
R2
R4
R6
Q4
Q5
Q6
RB
FB
IB
RED BACKGROUND STORAGE
GREEN BACKGROUND STORAGE
IR BACKGROUND STORAGE
RL
FL
IL
RED PICKUP
GREEN PICKUP
IR PICKUP
CHANNEL #1

FIG. 19A

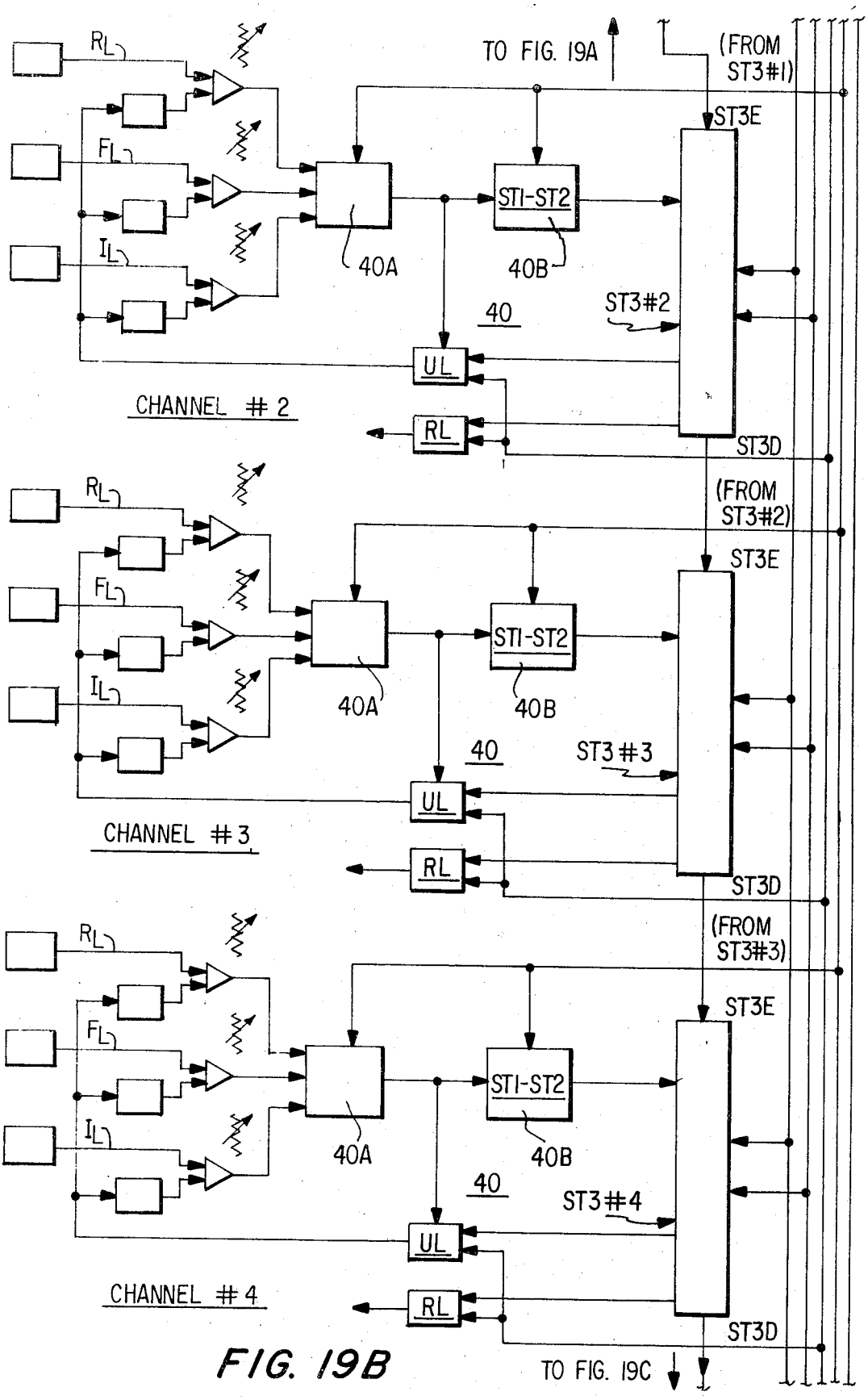

RL
FL
IL
40A
STI-ST2
40B
40
UL
RL
CHANNEL # 2
TO FIG. 19A
(FROM ST3#1)
ST3E
ST3#2
ST3D
(FROM ST3#2)
ST3#3
CHANNEL # 3
(FROM ST3#3)
ST3#4
CHANNEL # 4
TO FIG. 19C

FIG. 19B

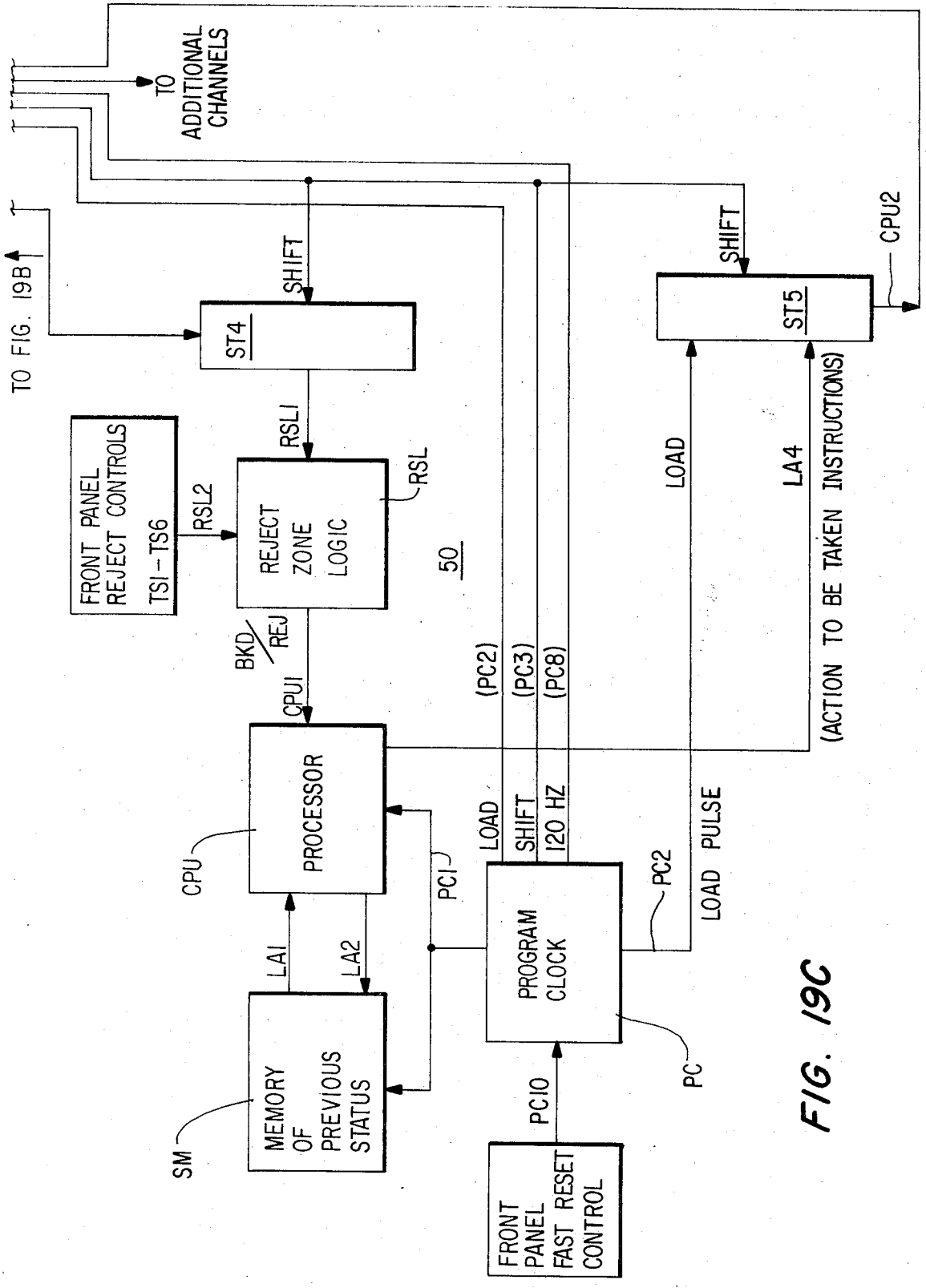

TO ADDITIONAL CHANNELS
TO FIG. 19B
ST4
SHIFT
RSL1
RSL
FRONT PANEL REJECT CONTROLS
TS1 - TS6
RSL2
REJECT ZONE LOGIC
50
BKD/REJ
CPU1
(PC2)
(PC3)
(PC8)
SHIFT
ST5
CPU2
LOAD
LA4
(ACTION TO BE TAKEN INSTRUCTIONS)
PROCESSOR
CPU
LOAD
SHIFT
120 HZ
PC1
PC2
LOAD PULSE
LA1
LA2
PROGRAM CLOCK
PC
MEMORY OF PREVIOUS STATUS
SM
PC10
FRONT PANEL FAST RESET CONTROL

FIG. 19C

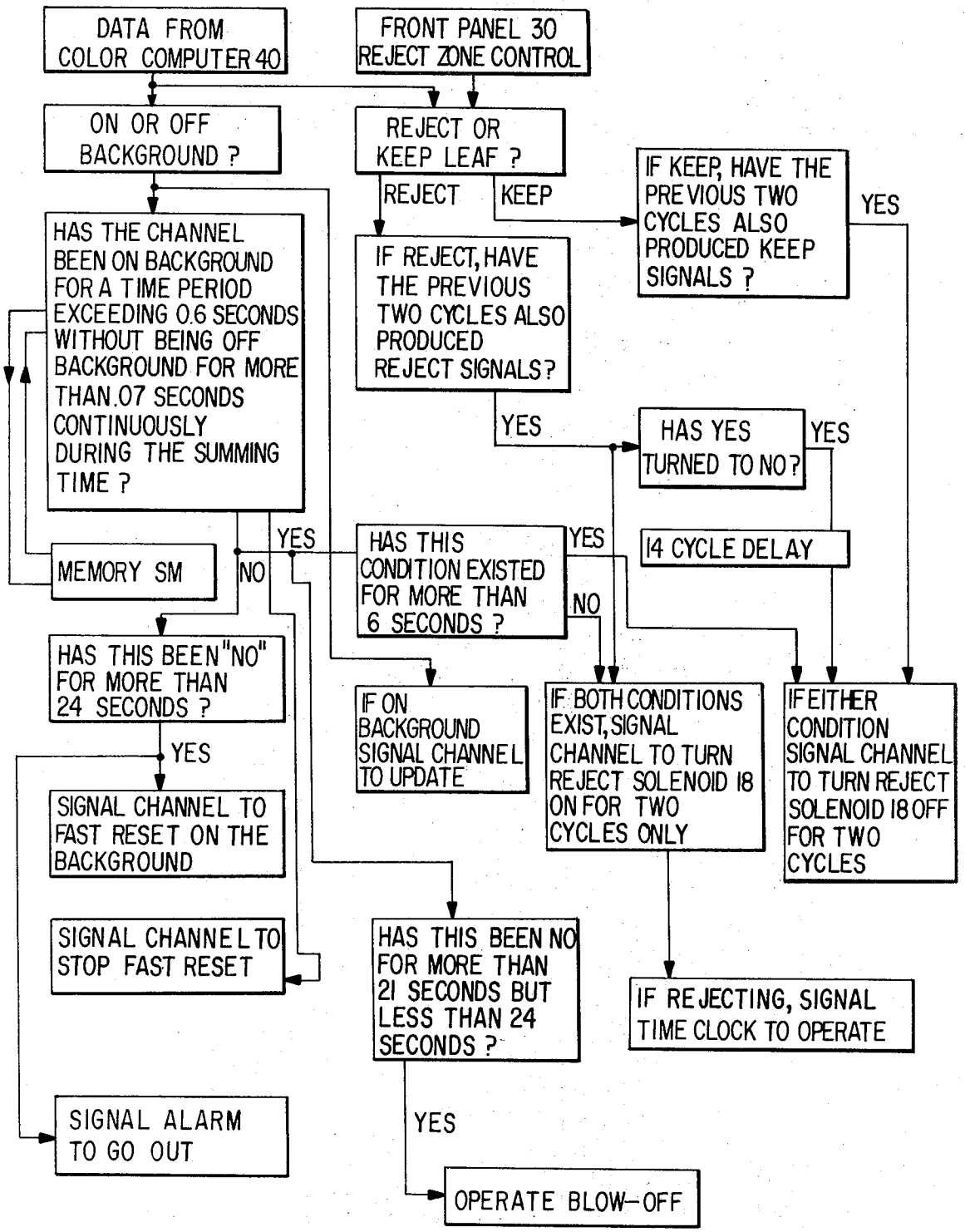

DATA FROM COLOR COMPUTER 40
FRONT PANEL 30 REJECT ZONE CONTROL
ON OR OFF BACKGROUND ?
REJECT OR KEEP LEAF ?
REJECT
KEEP
IF KEEP, HAVE THE PREVIOUS TWO CYCLES ALSO PRODUCED KEEP SIGNALS ?
YES
HAS THE CHANNEL BEEN ON BACKGROUND FOR A TIME PERIOD EXCEEDING 0.6 SECONDS WITHOUT BEING OFF BACKGROUND FOR MORE THAN .07 SECONDS CONTINUOUSLY DURING THE SUMMING TIME ?
IF REJECT, HAVE THE PREVIOUS TWO CYCLES ALSO PRODUCED REJECT SIGNALS?
YES
HAS YES TURNED TO NO?
YES
MEMORY SM
YES
NO
HAS THIS CONDITION EXISTED FOR MORE THAN 6 SECONDS ?
YES
NO
14 CYCLE DELAY
HAS THIS BEEN "NO" FOR MORE THAN 24 SECONDS ?
IF ON BACKGROUND SIGNAL CHANNEL TO UPDATE
IF BOTH CONDITIONS EXIST, SIGNAL CHANNEL TO TURN REJECT SOLENOID 18 ON FOR TWO CYCLES ONLY
IF EITHER CONDITION SIGNAL CHANNEL TO TURN REJECT SOLENOID 18 OFF FOR TWO CYCLES
YES
SIGNAL CHANNEL TO FAST RESET ON THE BACKGROUND
SIGNAL CHANNEL TO STOP FAST RESET
HAS THIS BEEN NO FOR MORE THAN 21 SECONDS BUT LESS THAN 24 SECONDS ?
IF REJECTING, SIGNAL TIME CLOCK TO OPERATE
SIGNAL ALARM TO GO OUT
YES
OPERATE BLOW-OFF

FIG. 21

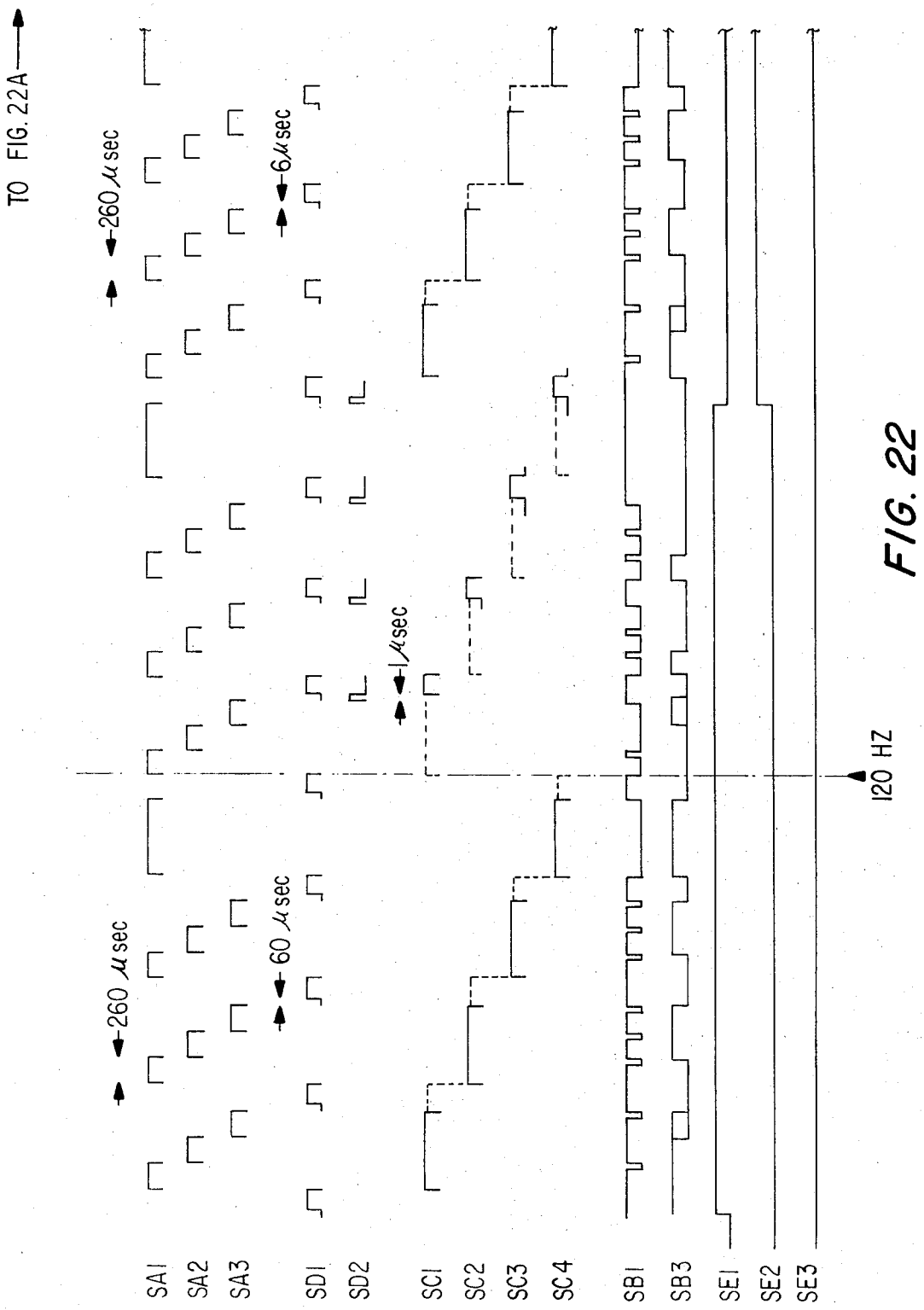

TO FIG. 22A
260 μsec
6 μsec
260 μsec
60 μsec
1 μsec
120 HZ
SA1
SA2
SA3
SD1
SD2
SC1
SC2
SC3
SC4
SB1
SB3
SE1
SE2
SE3

FIG. 22

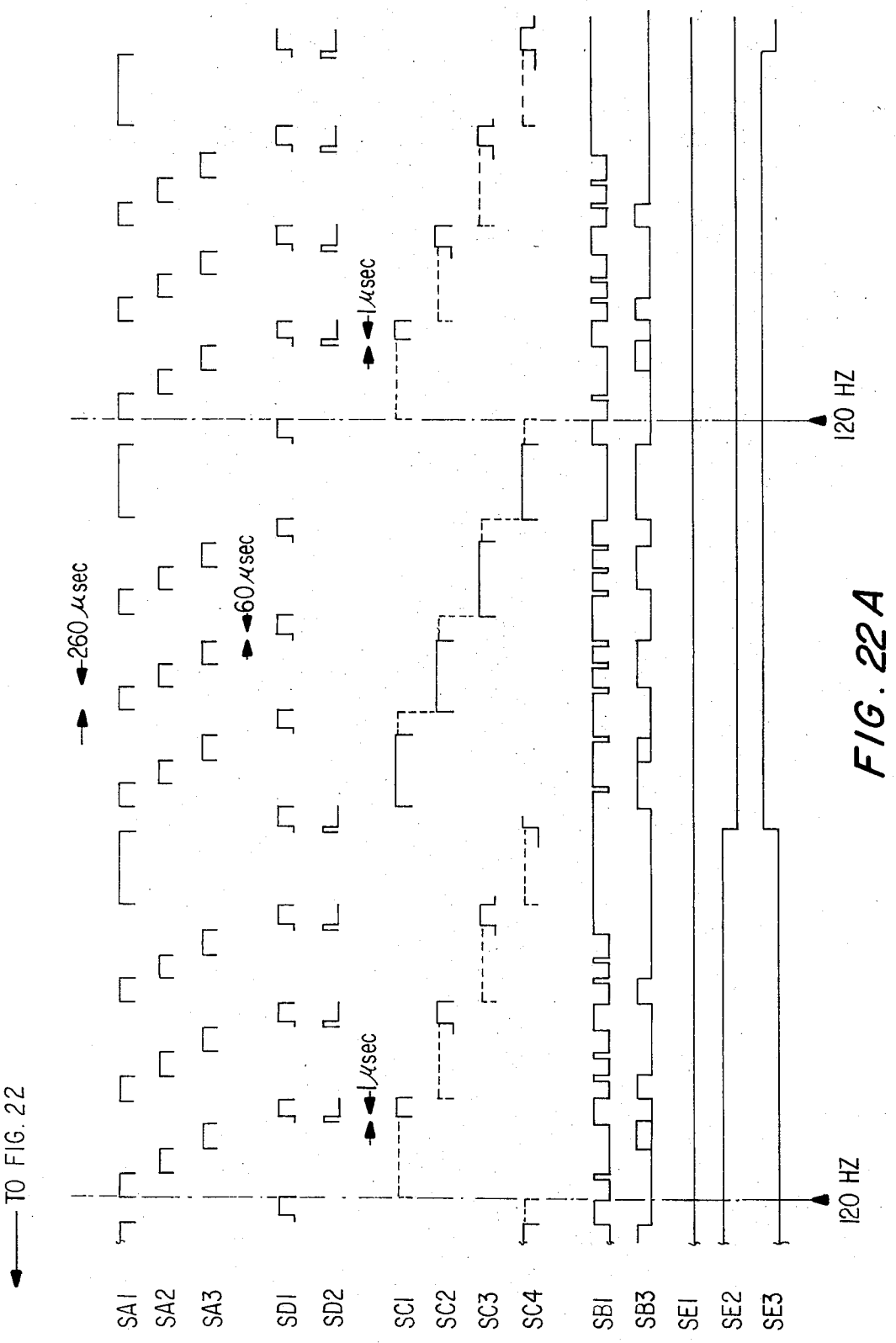

TO FIG. 22
SA1
SA2
SA3
SD1
SD2
SC1
SC2
SC3
SC4
SB1
SB3
SE1
SE2
SE3
260 μsec
60 μsec
1 μsec
1 μsec
120 HZ
120 HZ

FIG. 22A

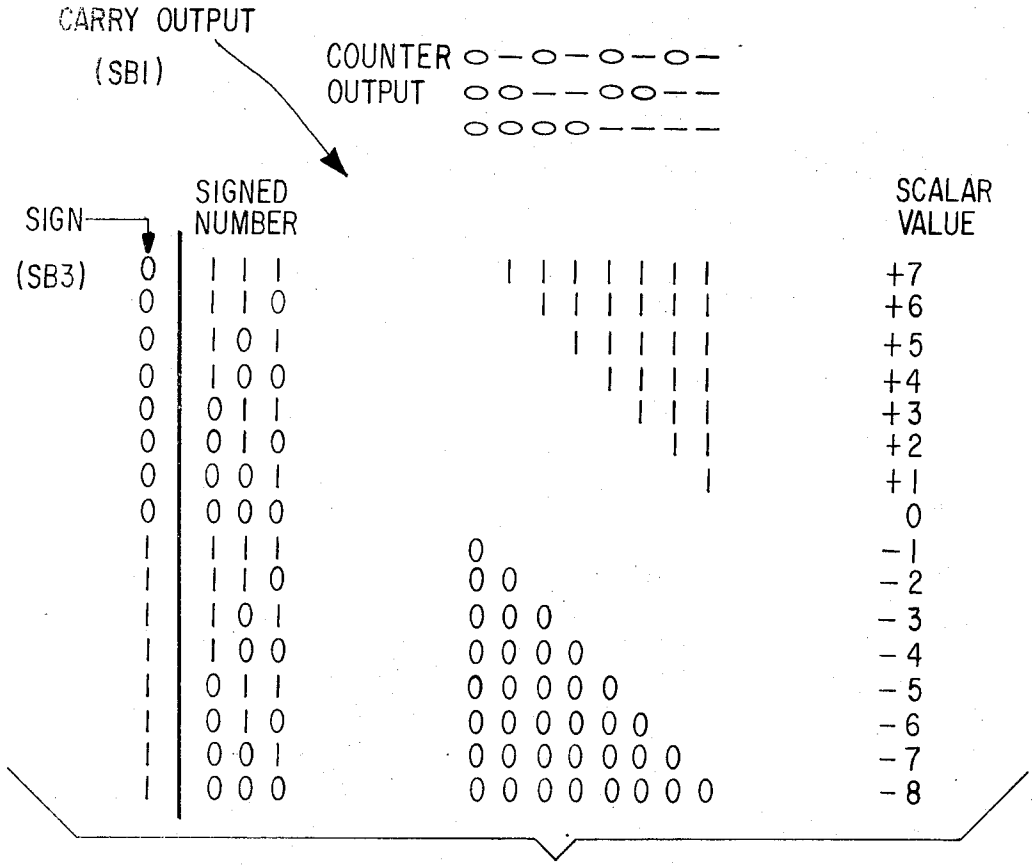

CARRY OUTPUT
(SBI)
COUNTER OUTPUT
SIGN
(SB3)
SIGNED NUMBER
SCALAR VALUE
+7
+6
+5
+4
+3
+2
+1
0
-1
-2
-3
-4
-5
-6
-7
-8

FIG. 23

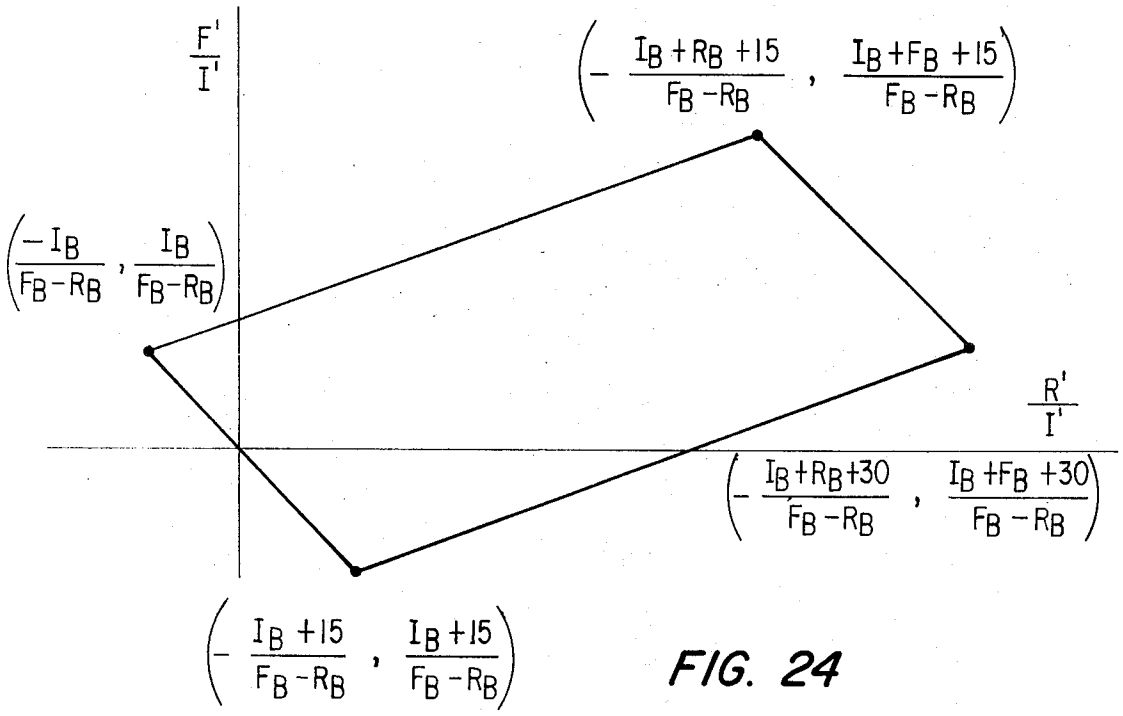

F'/I'
R'/I'
(-IB/(FB-RB), IB/(FB-RB))
(-(IB+RB+15)/(FB-RB), (IB+FB+15)/(FB-RB))
(-(IB+RB+30)/(FB-RB), (IB+FB+30)/(FB-RB))
(-(IB+15)/(FB-RB), (IB+15)/(FB-RB))

FIG. 24

AUTOMATIC GRADER FOR SORTING OBJECTS ACCORDING TO BRIGHTNESS AND COLOR TONES

This invention relates to automatic graders and more particularly to systems and apparatus for automatically grading tobacco leaves and the like according to color.

In the past and at the present time, it is a normal practice to grade tobacco by manual methods, i.e., by visual inspection of each leaf to determine given grades of tobacco leaves.

Furthermore, should a leaf be too green for present processing, such as a green sucker, manual inspection is also presently used to remove these leaves from further processing as undesirable grades.

As a result, accurate duplication of tobacco grades is very difficult to achieve at the present time. This is due to the difference of opinion which exists among manual sorters who must use their own judgment in determining the grade of a given tobacco leaf. The eye of the observer is the standard rather than an actual grade reference.

It is, therefore, an object of the present invention to provide a new and novel automatic grader which can readily duplicate grades of tobacco leaves and the like according to color regardless of the size or condition of the leaves.

It is another object of the present invention to provide a means of rapidly grading tobacco leaves and the like without the need for manual inspection of each leaf.

It is another object of the present invention to provide a new and novel automatic grading system and apparatus which operates to grade tobacco leaves and the like by comparing the color of a given leaf with a background color standard over which the given leaf must pass during the sorting and grading process to which it is being subjected.

Still another object of the present invention is to provide a new and novel automatic grader utilizing a color comparison system which may be embodied in a transducer arrangement for adapting existing manual sorting equipment to fully automatic sorting and grading equipment.

Still another object of the present invention is to provide a new and novel automatic grader system and apparatus utilizing an unique combination of three color detection and resulting detected color signal strength to provide selective grading of tobacco leaves and the like for both brightness of color and redness and greenness of leaf.

Yet another object of the invention is to provide a new and novel automatic tobacco sorting and grading system and apparatus which may be operated as a series of machines or devices performing a like series of sorting and selecting functions such that all of the leaves in a given batch of tobacco being graded will be separated into desired categories.

These and other objects of the present invention will become more fully apparent with reference to the following specification and drawings which relate to a preferred embodiment of the invention.

In the drawings:

FIG. **1** is a general schematic of the present invention including the basic physical details of a preferred optical system for same;

FIG. **2** is a schematic of the front control panel of the present invention;

FIG. **3** is a general block diagram of the control circuit of the present invention;

FIGS. **4** and **4A** together comprise a more detailed block diagram and schematic of the control circuit of the present invention;

FIGS. **5**, **5A**, **5B**, **5C**, **5D** and **5E** together comprise a detailed schematic of the front panel switch and coding logic of the present invention;

FIGS. **6** and **6A** together comprise a detailed schematic of the reject selection logic of the present invention;

FIG. **7** is a combind schematic of the possible color zones and combinations derived from the front control panel and an associated reject logic table illustrating color data line conditions vs. zone select line conditions for selective reject of various leaf colors;

FIG. **8** is a graphic portrayal of colors of tobacco leaves relative to the ordinates of red and green reflectivity in the present invention;

FIGS. **9** and **9A** illustrate one example of color zones selected for reject and the corresponding front panel switch settings, respectively;

FIGS. **10** and **10A** illustrate another example of color zones selected for reject and the corresponding front panel switch settings, respectively;

FIG. **11** is a block diagram of a portion of the program clock logic of the present invention;

FIGS. **12** and **12A** together comprise a block diagram of another portion of the program clock logic of the present invention;

FIG. **13** is a block diagram of the serial memory of the present invention;

FIGS. **14**, **14A** and **14B** together comprise a timing diagram of the program clock signals of the present invention;

FIGS. **15**, **15A** and **15B** together comprise a schematic of the central process unit logic of the present invention;

FIGS. **16**, **16A**, **16B** and **16C** together comprise a more detailed schematic of the color computer color input logic and circuitry of the present invention, more generally shown in FIGS. **4** and **4A**;

FIG. **17** is a diagram of a power supply for the present invention;

FIGS. **18** and **18A** together comprise a schematic of data buffer and accessory control logic of the present invention;

FIGS. **19**, **19A**, **19B** and **19C** together comprise a block diagram of a four-channel embodiment of the present invention;

FIG. **20** is a diagram illustrating the color calculation timing of the present invention;

FIG. **21** is a flow diagram of the operating program of the present invention;

FIGS. **22** and **22A** taken together comprise a timing diagram of the color input, color computing, scalar value and update control means of the present invention;

FIG. **23** is a tabular illustraton of the logical generation of positive and negative scalar values of the present invention; and

FIG. **24** is a graphic illustration of the analysis and related parameters for same performed by the present invention.

REFLECTIVITY OF TOBACCO LEAVES AND BACKGROUND STANDARDS

It has been ascertained that for properly cured tobacco leaves, there is a predictable difference between the reflectivity of green light and red light, the red reflectivity being on the order of 20 percent greater than the green, depending upon the type of tobacco and its curing process.

This predictable difference will be varied by the greenness of the leaf being monitored, thereby providing parameters that are determinative of the acceptability of a tobacco leaf according to its degree of greenness or redness, regardless of its acceptance in a given color grade based on its relative brightness.

Either the red reflectivity or the green reflectivity (or a combination thereof) of a given leaf can be utilized to effect automatic grading on the basis of relative brighness of the leaf to a background color standard.

The purpose of a standard color background is twofold. First, the optical means used to detect the reflectivity of the various colors is calibrated against this background; and second, in the event that a tobacco leaf passing over the standard background does not completely fill the field of view of the optics, the visible portion of the background will present a known factor which can be compensated for in a computational means associated with the optical means.

Calibration is required since such components as photodetectors, light sources, and related components are subject to drift in their various response characteristics and require periodic recalibration to prevent errors.

In regard to the size of the leaves relative to the field of view of the optical means, tobacco leaves are not always large enough to fill the field of view of a given optical means and the resulting color reflection sensed by that optical means is a combination of the reflectivities of the leaf and the standrd background. However, if the color of the background is a known standard or reference, that portion of the response attributed to the plate can be compensated for to reveal the true color of the leaf being analyzed, provided that a measure of the relative contribution, to the response, of the leaf and the background can be determined.

It is a known factor of tobacco leaves that they consistently absorb the shorter wavelengths and reflect the longer wavelengths (about 80 percent reflection at 1000nM) regardless of the visual color differences of individual leaves.

Hence, it is possible to generate signals via the chosen optical means that are a measure of the size of the tobacco leaves by using a color filter to detect either the infrared or the ultraviolet light reflected from the leaf and use this as a calibration signal for the visual color measurements provided that the color of the background plate is sufficiently different from that of the leaves in one of the regions of the spectrum.

There are two parameters which are sufficient to define the visual color differences of tobacco leaves, namely, brightness-darkness (or gray scale) and greenness-redness. In practice, it has been established that a deep red filter centered at 670 nM to 700 nM in combination with an orange, yellow or green filter is sufficient to make such measurements of visual color difference. The sum of the outputs of two filter-photodetector combinations determines the brightness of the leaf and the difference of these two outputs determines the greenness-redness thereof.

It has also been established that it is advantageous to have the color of the background reference close enough in the visual region to that of the leaves being sorted such that the contribution of the background reference to the total generated signal is minimized. For example, using the colors red and green for detection and infrared for calibration is compatible with blue, green, brown, red or purple background references or a gray background reference having a reflectivity in the range of 20 to 30 percent for wavelengths from 600 nM to 1000 nM, the unit "nM" conventionally designating nanometers.

THEORY

The mathematical relationships of the several color reflectivities from the background reference and tobacco leaves taking the proportionate size of the leaf and optical field of view into account, are as follows:

Definitions

a = proportion of field of view covered by tobacco leaf;

R = red reflectivity signal in percent;

F = green reflectivity signal in percent;

I = near infrared relfectivity signal in percent; and

L and B are subscripts which denote leaf and background, respectively.

The foregoing quantities are basically interrelated as follows:

$$R = aR_L + (1 - a)\,R_B$$
$$F = aF_L + (1 - a)\,F_B$$
$$I = aI_L + (1 - a)\,I_B$$

In the system of the present invention the three known reflectivity signals from the background reference (R_B, F_B and I_B) are stored in order that these can be subtracted from the resultant reflectivities R, F and I, as follows:

$$(R - R_B) = a(R_L - R_B)$$
$$(F - F_B) = a(F_L - F_B)$$
$$(I - I_B) = a(I_L - L_B)$$

Accordingly when $a = 0$ (i.e., no leaf is present in the optical field of view of the present invention), all of these quantities are equal to zero. Also, as a result, any linear combination of these signals will be zero when $a = 0$.

To remove the effect of a, the size of the leaf relative to the field of view on the background reference, the relatively constant infrared signal component ($I_L - I_B$) is used as a standard, by using the well known ratio tecnhique.

Two ratios may be computed from this standard as follows:

$$a(R_L - R_B)/a(I_L - I_B) = R_L - R_B/I_L - I_B$$

and

$$a(F_L - F_B)/a(I_L - I_B) = F_L - F_B/I_L - I_B$$

To compute the color of a leaf, the following function is calculated in which the quantity m is a scalar factor either positive or negative:

$$\text{Color} = R_L - R_B/I_L - I_B + m(F_L - F_B/I_L - I_B)$$

By manipulation, the foregoing relationship can be expressed as:

$$\text{color} = R_L + mF_L/I_L - I_B - R_B + mF_B/I_L - I_B$$

Now, since $(I_L - I_B)$ and $R_B + mF_B)$ are known constants, all of there components being known, these quantities can be removed by multiplication and subtraction leaving the quantity $R_L + mF_L$ as the unknown to be determined as a measure of leaf color.

If this general unknown is compared to a predetermined quantity C to determine its relative magnitude, then the dividing line between acceptable or unacceptable tobacco leaves in the grading process and system of the present invention can be expressed as the equation:

$$R_L + mF_L + C = 0$$

In the present invention this dividing line is also expressed as:

$$R_L + mF_L/I_L + I_B - R_B + mF_B/I_L - I_B + b = 0$$

By manipulation, the following expression is derived:

$$R_L + mF_L - [R_B + mF_B + b(I_L - I_B)] = 0$$

where b is a scalar factor chosen such that

$$C = -[R_B + mF_B + b\ (I_L - I_B)]$$

Multiplying last-derived dividing line equation by the leaf size factor a, results in:

$$a\ (R_L + mF_L) - a\ [R_B + mF_B + b\ (I_L - I_B)] = 0$$

which, when expanded and rewritten, is as follows:

$$a\ (R_L - R_B) - m\ [a\ (F_L - F_B)] - b\ [a(I_L - I_B)] = 0$$

Therefore any appropriate acceptability dividing lines for the leaves under test can be established and the relative color of the leaves to these established dividing lines determined from a linear combination of the available optically generated signals $(R_L - R_B)$, $(F_L - F_B)$ and $I_L - I_B)$, the resultant signals of the combined reflectivities from the background reference and leaves for each of the chosen colors.

In the actual practice of the invention the above equation is not made equal to zero, but to a small quantity $\pm d$. Thus a determination is made to see if the weighted sum of the colors is greater than $+d$ or less than $-d$. Exactly how small "d" is determines the gain of the system.

The equation $r(R_L - R_B) + f(F_L - F_B) + i\ (I_L - I_B) = \pm d$ can be described as two parallel planes in $(R_L - R_B)$, $(F_L - F_B)$, and $(I_L - I_B)$ space, that are displaced from the origin by $\pm d$, a small quantity. Hence it can be seen that in the general case where R_L, F_L and I_L are all variables, the three color system can accomplish separation of different colored objects by using planes at various angles and tilts. However in the case of tobacco leaves where I_L is relatively constant, it is more convenient to think in terms of two dimensions, with I_L a calibrating signal.

BACKGROUND OF THE INVENTION

By utilizing two color response, sorting of leaves for relative brightness, greenness and/or redness can be achieved. However, in such a two color process the dappled (red) and green leaves cannot be sorted at the same time since the color of the background reference is the determining point of division for acceptable and unacceptable leaves.

Accordingly, the need for a "neutral" background reference and a means whereby the red and green divisions of acceptability could be achieved to permit automatic separation of leaves on both sides of a desired range of normality or acceptability is clearly present.

If such a capability were available in color sorting equipment, then the need for a wide range of background references and the maintenance and storage thereof would be obviated.

SUMMARY OF THE INVENTION

By using three colors for generating response signals in the color sorting equipment of the present invention, one of these colors can be utilized to measure the size of the leaf or other object being graded in the field of view of the optical means utilized to detect the several color reflections from the background reference and a leaf or object being tested when it is positioned over that reference in the field of view of the said optical means.

A bias signal can then be developed from the third color response signal that can be used to electronically alter the appearance of the background relative to the leaf, thereby permitting the use of a neutral (single) selected background reference and electronic controls such as dials or the like for establishing desired bright-/dark and green/red divisions of acceptability for the objects under test.

Basically, a light is provided which impinges upon a background reference plate over which tobacco leaves are projected by a conveyor in a ballistic path which carries the leaves through the field of view of an optics head having red, green and infrared sensing means thereon to generate signals representative of the reflected light in these selected spectral regions or wavelengths.

A control panel and associated logic module are provided to permit the latitude of acceptable and unacceptable colors of the leaves (or other objects being graded by color) to be selectively adjusted as desired, and provide commensurate control signals to the color computer to constrain it to either accept or reject the leaves being analyzed according to the control panel settings.

The color computer solves the equations discussed under Theory in the general discussion of Reflectivity Of Tobacco Leaves And Background Standards herein so that the divisions between acceptable and unacceptable leaves are determined and then compared to the colors of individual leaves to either constrain an accept or reject condition on each leaf.

The computer also stores the color of the background reference upon command from a reject timing logic means that determines when and if a leaf should be rejected in response to computer output signals indicating the results of comparison of actual leaf colors with the desired accept — reject settings of the control panel. This reject timing logic means also determines when the background reference is in view of the optics head so that this reference color can be stored in the computer and that storage can be updated for current calculations.

Subject to the results determined by the color computer and associated logic, a solenoid actuated air jet is provided adjacent the ballistic path of the leaves to cause unacceptable leaves to change their ballistic paths and arrive at a reject bin or other predetermined destination apart from the acceptable leaves.

Three accessary functions are also provided by the associated logic. The first is a clock that is controlled to determine how long the color grader has been grading. The second is a side blower for the background plate to clean it of obstructions and dust; and the third is an alarm light to indicate when the background is properly stored in memory when it has been necessary to recalibrate while in operation.

THE BASIC SYSTEM AND APPARATUS

With the foregoing consideration of reflectivity established, the basic system and apparatus of the present invention can best be described by reference to FIG. **1,** where the grading means **10** of the present invention is schematically illustrated.

Tobacco leaves T are fed sequentially over a background color standard (platen) S by means of an endless belt conveyor **12** driven by a pulley drive **12A** (or by other suitable conveyor means).

Mounted above the color standard S is a light source comprising a plurality of lamps L, three detector means, namely, a red light detector RD and a green light detector FD and an infrared or near infrared detector ID, which, in a preferred embodiment comprise photodiodes DR, DF and DI with red, green and infrared filters RF, FF and IF optically coupling them, respectively, with the light from the lends **A5.** These filters may have suitable light gathering optics associated therewith if desired.

The optical system OH comprises a housing **A1** with an enlarged telescope tube **A2** extending therefrom. An objective lens **A3** is mounted in the front of the telescope tube **A2** facing the obverse surface of the background reference S and focuses reflected light. from the latter through an apertured plate **A4,** defining the field of view of the optical system OH.

A field lens **A5** is positioned in the telescope tube **A2,** and directs the green, red and infrared light into the housing **A1.**

The detector means RD, FD and ID are connected via signal leads **RD1, FD1** and **ID1,** respectively, to signal inputs **14R, 14F,** and **14I** of a control circuit **14,** the latter generating a control signal at a control output **16,** which signal is conveyed through output lead **16A** to the control terminal **18A** of a pneumatic reject mechanism **18.**

The pneumatic reject mechanism **18** includes a solenoid controlled air jet **20** which directs stream of air **20A** against the underside of selected ones of the tobacco leaves T, namely, undesired or rejected ones of the leaves T to contstrain upon the latter a trajectory TR which, when leaving the background standard S, is predictably different from the trajectory TA taken by acceptable ones of the leaves T which are of the grade desired.

The trajectories TA and TR carry the leaves T into a pair of receiving bins BA and BR, or conveyor belts, respectively for acceptable and rejected ones of the leaves T.

As further shown in FIG. **1,** the pneumatic reject mechanism has a pressure input **18B** which is connected to a pneumatic source **22** to provide the pressurized air for the jet **20.**

The light source L is positioned to illuminate the background reference S and any leaf T thereon and cause reflection of that light back to the optical system OH.

In basic operation, which will be hereinafter more fully described, those leaves T which are within the color limit set within to control circuit **14** are permitted to fall from the background reference S and assume the acceptable trajectory TA into the acceptable grade bin BA.

When a leaf T is of a color external of the preset limit, this difference is detected by the detectors RD, FD and ID and a resulting control signal is generated in the control circuit **14,** and thence transmitted through the control output **16,** control lead **16A** and input terminal **18A** to energize the pneumatic reject mechanism **18** before that particular leaf T leaves the platen shaped background reference S.

Accordingly, an upwardly directed stream of air **20A** is emitted from the jet **20** and lifts the rejected (undesirable) leaf T to constrain it into the reject trajectory TR and into the reject bin BR, effecting a selective grading of the tobacco leaves T.

As will be hereinafter more fully described, the duration of the airstream **20A** is timed such that it will not interfere with the trajectory of the next successive leaf T unless the latter is not within the preset color limits for acceptable leaves.

The color filters RF, FF and IF are centered, respectively, at 540nM(green), 670nM(red) and 900nM (infrared) in a preferred embodiment of the invention.

THE CONTROL PANEL

Referring now to FIG. **2,** a control panel **30** for selecting the division between acceptable and unacceptable leaves is shown as divided into six quality zones by a BRIGHT-DARK divider line with a transverse GREEN line and a transverse RED line thereacross.

These quality zones are labelled as follows:

BRIGHT (Not Red — Not Green)	Z2
DARK (Not Red — Not Green)	Z5
BRIGHT-RED	Z3
DARK-RED	Z6
BRIGHT-GREEN	Z1
DARK-GREEN	Z4

In each zone is a toggle switch TS which has a REJECT position and a KEEP position. As will be more fully described hereinafter, the KEEP position constrains the color sorter **10** to accept leaves qualifying for a correlated quality zone and the reject position constrains a rejection of leaves qualifying for that zone.

From the previous discussion of the theory of three-color sorting it can be readily seen that the color function to be calculated by the control circuit **14** (FIG. **1**) is of the form $rR + fF + iI$, where R, F and I are the red, green and infrared color signals and r, f and i are scalar factors which are to be established depending upon the desired division between quality zones, such that the toggle switches TS can be thrown to constrain predetermined acceptance and rejection of leaves by the sorter **10.**

When the color function is zero, then the only thing in the field of view of the optics OH is the background

reference S. If this color function is positive or negative then there is an object (leaf) in the field of view that is below or above the preset color, i.e., in the various BRIGHT or DARK quality zones, respectively, with these zones being defined by predetermined selection of the scalar factors *r*, *f* and *i*.

Thus, the BRIGHT-DARK, GREEN and RED lines on the control panel **30** simulate a graph of relative color qualities which graph will be more fully defined hereinafter with reference to FIGS. **8, 9** and **10.** When dividing lines between the various color zones are established, the control panel **30** via the toggle switches TS, determines which quality zones (ranges) of colors in a given leaf will be accepted or rejected by the sorter **10.**

The quality zones Z1–Z6 are established prior to sorting by means of five (**5**) scalar factor thumbwheel switches ZBD, ZBG, ZDG, ZBR and ZDR which select the division lines between the various color zones.

The scalar factor switch ZBD sets the division between the BRIGHT and DARK zones; the scalar factor switches ZBG and ZDG in the BRIGHT-GREEN and DARK-GREEN zones set the accept-reject tolerance to light and dark green leaves, i.e., tilt the BRIGHT-DARK and GREEN division lines relative to one another, mathematically, to enlarge or reduce the range of greens in a given one of the "green" zones as well as setting the degree of greenness accepted; and the scalar factor switches ZBR and ZDR in the BRIGHT-RED and DARK-RED zones set the accept-reject tolerance to light and dark red leaves, i.e., tilt the BRIGHT-DARK and RED division lines relative to one another, mathematically, to enlarge or reduce the range of reds in a given one of the "red" zones as well as determine the degree of redness acceptable.

Each of the scalar factor switches comprise, for example, sixteen-position thumbwheel switches which impose input constraints on compatible logic circuitry, the latter controlling the relative durations of the red, green and infrared signals R, F and I in a given sensing cycle such that when these signals are integrated, the resulting magnitudes will be proportionately modified or modulated by the desired scalar factors to provide color parameters for comparison with the preset quality zone divisions by a color computer **40,** see FIG. **3.**

The accept-reject function of the sorter **10** is controlled by the correlation between the comparison of a leaf color parameter as being above or below the desired division line in magnitude (i.e. a positive or negative comparison) and the positions of the toggle switches TS, which, referring to FIG. **3,** are shown as controlling an accept-reject logic module **50,** the latter serving to update the quality division line data in the color computer module **40** through a programming lead PL.

Referring to FIG. **4A,** the optics head OH is shown as including the red, green and infrared filters RF, FF and IF with the photodiodes or phototransistors DR, DF and DI respectively associated therewith, together with field effect transistors **Q1, Q2** and **Q3** connected, respectively, with their control terminals connected at the respective anodes of the said diodes and with another electrode in common connection with a positive bias, for example **+6V,** and the cathode of the said diodes. The other electrodes of the said transistors **Q1, Q2** and **Q3** are connected, respectively, to the positive inputs of operational amplifiers **Q4, Q5,** and **Q6** in the color computer **40** via coupling resistors **RA1, RA2** and **RA3,** respectively, as well as through biasing resistors **BR1, BR2** and **BR3** to a source of negative bias, shown for example, as **−6V.**

The anodes of the photodiodes DR, DF and DI are respectively connected through load resistors **R1, R3** and **R5** to the variable taps of trimming resistors **R2, R4** and **R6** which serve to adjust the response characteristics of the said photodiodes to the incident filtered light impinging thereon through the respective filters RF, FF and IF.

The trimming resistors **R2, R4** and **R6** have one end thereof connected to ground and their opposite ends connected, respectively, to the outputs RS, FS and IS of the operational amplifiers **Q4, Q5** and **Q6.** The designations RS, FS and IS indicate that the red signal (R), green signal (F) and infrared signal (I) of the function to be solved by the color computer **40** appear at these respective outputs of the operational amplifiers **Q4, Q5** and **Q6.**

The trimming resistors **R2, R4** and **R6** thus provide a means for adjusting the amplitudes of the color signal outputs RS, FS and IS of the operational amplifiers **Q4, Q5** and **Q6.** In practice **R2, R4,** and **R6** are adjusted so that a voltage swing of six volts will result when the reflectance signal is made to change from **100%** to **0%.** This calibrates each color detector and insures uniform grading from one head to another.

The positive inputs of the operational amplifiers **Q4, Q5,** and **Q6** are respectively connected to the junction of **CA1** and **RA1, CA2** and **RA2,** and **CA3** and **RA3.** These resistor-capacitor combinations limit the bandwidth of the photo detectors to that required to track the leaves as they pass under the heads; this extra feedback also maintains the output impedance of **Q4, Q5,** and **Q6** at a low value.

RA1, RA2, and **RA3** are respectively connected to the negative bias source (−6V) through bias resistors **BR1, BR2** and **BR3** and are further respectively connected to one of the electrodes of field effect transistors **Q7, Q8** and **Q9.** The other of the electrodes of these transistors **Q7, Q8** and **Q9** are connected to the source of positive bias (+6V) which in the preferred embodiment of the invention is symmetrical with the negative bias (−6V).

The control electrodes of the transistors **Q7, Q8** and **Q9** are respectively connected to ground through reference capacitors **C6, C7** and **C8** and selectively, through switch means **SE1, SE2** and **SE3,** respectively, to a common circuit lead **CL1** on the opposite sides of the said switch means.

This interconnection of the operational amplifiers **Q4, Q5** and **Q6** with the photodiodes DR, DF and DI results in the maintenance of a constant voltage at the junctions between the anodes of the said photodiodes and their respectively associated load resistors **R1, R3** and **R5,** whereby the voltages at the outputs RS, FS and IS correspond to the respective amounts of filtered light impinging upon the said diodes.

Further, the power dissipated in the field effect transistors **Q1, Q2** and **Q3** is maintained constant, thereby keeping the voltage constant across the respectively associated photodiodes DR, DF and DI, whereby linearity is maintained over a wide range of magnitudes of light incident upon the said photodiodes and "thermal memory" effects are avoided.

The red, green and infrared signal outputs RS, FS and IS are connected, respectively, through selectively actuated switch means SA1, SA2 and SA3 to a second common circuit lead CL2 which serves as a common input to an integrator circuit 40A including an operational amplifier Q10 having input resistors R6 and R7 connected at one end, respectively, with the negative and positive inputs of the said amplifier Q10.

The other end of the negative terminal load resistor R6 is selectively connected to the second common lead CL2 or to the ground by means of a ganged pair of switch means SB1 and SB2, respectively, operating to assume opposite open and closed states one from the other.

The other end of the positive terminal load resistor R7 is selectively connected to the second common lead CL2 or to the ground by means of a ganged pair of switch means SB3 and SB4, respectively, operating to assume opposite open and closed states one from the other.

The negative input terminal of the integrator amplifier Q10 is directly connected through a feedback resistor R10 to the amplifier output 40AS, that feedback resistor R10 being selectively by-passed through the integration capacitor C5 via a selectively actuated switch means SD2 in series between amplifier output 40AS and one side of the said capacitor C5, that side of the capacitor C5 being directly connected to a third common circuit lead CL3.

The other side of the said capacitor C5 is connected to the negative input terminal of the integrator amplifier Q10 and a selectively activated switch means SD1 is connected across the said capacitor C5 to connect the said negative input terminal either directly to the third common circuit lead CL3 or through the said capacitor C5 to the said third common circuit lead CL3.

The selective switch means SD2 serves to directly connect the amplifier output 40AS to the said third common circuit lead CL3 in its closed state.

First, second and third storage capacitors C1, C2, and C3 are connected on one side to a common node SCN and on the other sides thereof, respectively, through selectively activated storage control switch means SC1, SC2 and SC3 to the third common circuit lead CL3. The common node SCN is connected through a reference resistor R8 to the common connection SCNA between the positive terminal input resistor R7 and the ganged switch pair SB3, SB4 which serve, respectively, to selectively connect one side of the said reference resistor R8 to either the second common circuit lead CL2 or to ground.

A fourth storage capacitor C4 is selectively connected to the third circuit lead CL3 through a fourth storage control switch means SC4 on one side thereof and on the other side thereof through a reference resistance R9 and the common connection SCNA to either the second common circuit lead CL2 or ground via the said ganged switch pair SB3, SB4.

The integrator amplifier ouput 40AS is further connected through a selectively activated switch means SD3 to a circuit node CNB, the latter being connected to ground through a capacitor C9 to form a sample and hold circuit and to another circuit node CNC through a resistor R11, the latter circuit node being connected to ground through the reverse direction of a clamping diode DA.

The node CNC is connected to the first common circuit lead CL1 either directly through a selectively activated switch means SD4 or through a reference resistor R12, the latter being selectively shunted by the said switch means SD4 to implement the FAST RESET function of the color grader as will be more fully described hereinafter.

A final connection of the output 40AS of the integrator amplifier Q10 is through a coupling resistor R13 to the input 40BA of a comparator circuit 40B.

The comparator circuit 40B comprises an input stage having two NPN transistors Q11 and Q12 with their bases commonly connected to the comparator input 40BA; their emitters commonly connected to ground; and their collectors 42 and 44 connected, respectively, directly to the bases of output transistors Q13 and Q14.

The first output transistor Q13 is of the PNP type while the second output transistor Q14 is of the NPN type.

The collector 42 of the first input transistor Q11 and the base of the first output transistor Q13 are connected through a coupling resistor R14 to the emitter 46 of the first output transistor Q13 and the source of positive bias (+6V).

The collector 44 of the second input transistor Q12 and the base of the second output transistor Q14 are connected through resistor R15 to the source of negative bias (−6V) and the collector 48 of the first output transistor Q13 is connected through a resistor R16 to the source of negative bias (−6V), with the said collector 48 comprising a positive comparison output 40BS1 of the comparator 40B.

The collector 50 of the second output transistor Q14 comprises a negative comparison output 40BS2 of the comparator 40B and is connected through a biasing resistor R17 to a positive bias source which for example, is shown as +6V. The emitter 52 of the second output transistor Q14 is directly connected to a source of negative bias, symmetrical with the positive bias, which is shown, therefore as −6V.

The comparator outputs 40BS1 and 40BS2 comprise the data inputs of first and second 3-bit shift registers ST1 and ST2 which store, respectively, the positive and negative signals on the comparator outputs 40BS1 and 40BS2. Each of these shift registers has a central clock to be hereinafter more fully described.

The 3-bit outputs ST1A and ST2A of the first and second shift registers ST1 and ST2 drive 3-bit data inputs ST3A and ST3B, respectively, of an 8-bit shift register ST3, the latter having a 3-bit control output ST3C, a serial data output ST3D, a serial data input ST3E, a load pulse input ST3F and a shift clock input ST3G.

The serial data output terminal ST3D is connected through a data transfer register ST4 to the first data input RSL1 of a reject selection logic module RSL, the latter having a second data input RSL2 from the six toggle switches TS on the front control panel 30 and an output terminal RSL3 which drives the main data input CPU1 of a central processing input CPU.

The central processing unit or computer CPU includes a logic array LA into which the main data input CPU1 feeds. The logic array LA also includes in and out terminals LA1 and LA2, respectively, which effect recirculation of data into and out of a serial memory SM which stores the state of the logic array LA subsequent to the receipt of data from the reject selection

logic module RSL. A clock input LA3 is provided the logic array LA from the output PC1 of a program clock PC. The data output terminal LA4 of the logic array LA comprises the output CPU2 of the computer CPU and is connected through an output data transfer register ST5 to the serial data input ST3E of the 8-bit shift register ST3.

The program clock PC has a load pulse output PC2 directly connected to the load pulse control input ST3F of the 8-bit shift register ST3; a shift clock output PC3 directly connected to the shift clock control input ST3G of the 8-bit shift register ST3; and an operate pulse output PC4 directly connected to the control inputs UL1 and RL1 of an update logic module UL and a reject logic module RL, respectively.

The update logic module UL and the reject logic module RL have 3-bit data input terminals UL2 and RL2, respectively, connected to the 3-bit control output ST3C of the 8-bit shift register ST3 and further include respective control outputs UL3 and RL3.

The 3-bit control outputs ST3C of the 8-bit shift register ST3 comprise the general control output 16 of the general control circuit 14 and are connected directly to the input leads 16A of the solenoid driver circuit 18.

FRONT PANEL LOGIC BOARD FOR CODING THUMBWHEEL SWITCHES ZBG, ZDG, ZBD, ZBR AND ZDR

Referring to FIG. 5, a preferred embodiment of logic board FPLB for encoding the quality zone setting thumbwheel switches ZBG, ZDG, ZBD, ZBR and ZDR on the front control panel 30 and generating the resulting sequencing signals for the control switches SA1—SA3, SC1—SC4, SD1, SD2, SB3 (SB4), SB1 (SB2), and SE1—SE4 will now be described.

In all of the following descriptions all modular components are commercially available types and are listed in Appendix I. Further, all commercially available modules are presented in the drawings with conventional terminal pin numbers such that when interconnected as shown and described will result in the performance of the functions to be defined hereinafter.

The load pulse from the output PC2 of the program clock PC (see FIG. 4B), is applied to the clock input terminal ZL of the control panel board FPLB and thence into the No. 5 terminal of a sample and hold type phase comparator Y1 (CD4016AE module of RCA), the latter having its No. 3 terminal connected with the No. 3 terminal of a voltage controlled oscillator Y2 (CD4007AE of RCA) as well as through a coupling capacitor C10 to the source of negative bias (−6V), and its No. 4 terminal connected to a circuit lead ZL1 through a resistor R20 and the negative bias source (−6V) through a coupling capacitor C11. The load pulse input ZL is connected to the negative bias source (−6V) through a resistor R21.

The No. 4, No. 6 and No. 12 terminals of the oscillator Y2 are connected through a resistor R22 to a node Y2A, the latter being connected to the No. 10 and No. 5 terminals of the oscillator Y2 through resistors R23 and R24, respectively. The node Y2A is connected through a coupling capacitor C12 to the oscillator output Y2B, the latter being directly connected to the No. 8 and No. 13 terminals of the oscillator Y2 and to the No. 1 terminal comprising an input Y3A of a seven-bit counter circuit Y3 (CD4024AE module of RCA).

The No. 2 terminal of the seven-bit counter Y3 is connected to the source of negative bias (−6V). The No. 12, No. 11, No. 9, No. 6, No. 5, No. 4 and No. 3 terminals of the counter Y3 correspond to the 1st through seventh bits, in that order, counted by Y3, with the carry signal from the counter Y3 exiting at its No. 3 terminal, the latter being connected to the No. 13 terminal of a five-bit counter Y4 (CD4022AE module of RCA), the No. 14 terminal of the counter Y4 being connected to the source of positive bias (+6V).

The 7-bit counter Y3 subdivides each of the color computation periods by controlling the sequencing of the various switches in the input circuit A and color computer 40 as will be hereinafter more fully described.

The count of 4 counter Y4 has its No. 2, No. 1, No. 3, No. 7 and No. 11 terminals corresponding to the first through fifth counts (0, 1, 2, 3, 4) in that order, with the No. 11 terminal connected to the No. 15 terminal to reset the counter Y4 and the No. 7 terminal of the latter is connected to the input Y5A (No. 13 terminal) of a second count of four counter Y5 (CD4022AE module of RCA), the latter having its No. 14 terminal pin connected to the source of positive bias (+6V).

The first count of 4 counter Y4 serves to sequence the selector switch means SA1, SA2 and SA3 and SD1 in the color computer 40 while the second count of 4 counter serves to sequence the storage selector or sampling switch means SC1, SC2, SC3 and SC4 in the color computer 40.

As in the first count of 4 counter Y4, the No. 2, No. 1, No. 3, No. 7 and No. 11 terminals of the second counter Y5 correspond to the first through fifth counts (0, 1, 2, 3, 4), in that order, with the No. 11 terminal connected to the No. 15 terminal to reset the said counter Y5.

The No. 2 terminal of the second count of 4 counter Y5 is connected to the input Y6A (No. 11 terminal) of phase counting flip-flop Y6 (CD4013AE module of RCA) and, the No. 7 terminal of the second 5-bit counter Y5 is connected to the input Y7A (No, 14 terminal) of a count of 3 update switch selection counter Y7 (CD4022AE module of RCA).

The phase counting flip-flop Y6 has its No. 8 and No. 10 terminals connected to the source of negative bias (−6V), its No. 13 terminal providing a first half cycle signal output Y6B and its No. 9 and No. 12 terminals providing a second half cycle signal output Y6C. These two outputs Y6B and Y6C serve as control inputs for sequencing the storage sampling switches SC1, SC2, SC3, SC4, the zero switch SD1, the main sampling switch SD2 and the selector switches SB3 (SB4) and SB1 (SB2) which control the scalar factor values in the color computations as will be more fully described hereinafter.

The count of 3 counter Y7, designated also as the update selection counter, ultimately controls the sequencing of the update selector switches SE1, SE2 and SE3 to thereby control the application of updated background reference voltages to the reference capacitors C1, C2 and C3 in the optics input circuitry A previously described in FIG. 4. This sequencing is correlated with the sequencing of the color selector switches SA1, SA2 and SA3 and the sample switch SD2 as will become more readily apparent hereinafter.

The No. 13 terminal of the counter Y7 is connected to the control output SSD2 of the sample switch SD2 by a lead Y7B.

The No. 2, No. 1, No. 3 and No. 7 terminals of the (update selection) counter Y7 correspond to the first through fourth counts (0, 1, 2, 3) in that order, of the said counter Y7, with the No. 7 terminal connected to the No. 15 terminal to reset the said counter.

The No. 2 terminal of the update selection counter Y7 comprises the control output SSE3 for the update switch SE3; the No. 1 terminal comprises the control output SSE1 for the update switch SE1; and the No. 3 terminal comprises the control output SSE2 for the update switch SE2.

The No. 2, No. 1 and No. 3 terminals of the update selection counter Y7 are connected, respectively, to the No. 3, No. 5 and No. 7 terminals of a color switch selector Y9 (CD4019AE logic module of RCA) to serve as part of the sequencing data for the color switches SA1, SA2 and SA3 as correlated with the update switches SE1 — SE3.

The No. 2, No. 4 and No. 6 terminal pins of the color switch selector Y9 are directly connected with the No. 2, No. 1 and No. 3 terminals, respectively, of the first counter Y4 to provide the primary sequencing information for the color switches SA1, SA2 and SA3 through the leads containing the switch designations in parantheses, (SA1), (SA2), etc. The No. 7 terminal of the said counter Y4 is connected through the lead (SD1) to the No. 13 terminal of a NOR gate Y10 (CD4001AE module of RCA) the output thereof comprising a No. 11 terminal which drives the No. 2 terminal of a like NOR gate Y11 as well as the No. 9 terminal of the color switch selector Y9.

The No. 12 terminal comprising the other input of the NOR gate Y10 is driven through the lead (SC4) from the No. 7 terminal of the second counter Y5.

The No. 1 terminal comprising the other input of the NOR gate Y11 is driven through the lead (SD1) from the No. 3 terminal of the first counter Y4 and the output (No. 3 terminal) of the NOR gate Y11 drives the No. 14 terminal of the color switch selector Y9.

Thus, the switches in the SA, SC, SD and SE series are seen to be interrelated in their respective sequences.

The control terminals, SSA1— SSA3, SSC1 — SSC4, SSD1, SSD2, SSB3 and $\overline{\text{SSB1}}$ for the various sequenced switches are selectively gated ON or OFF by flip-flops (CD4013AE modules of RCA) as follows:

1. SSA1 is the NO. 1 terminal of a flip-flop FFA1;
2. SSA2 is the No. 13 terminal of a flip-flop FFA2;
3. l SSA3 is the No. 1 terminal of a flip-flop FFA3;
4. SSC1 is the No. 12 terminal of a flip-flop FFC1;
5. SSC2 is the No. 2 terminal of a flip-flop FFC2;
6. SSC3 is the No. 12 terminal of a flip-flop FFC3;
7. SSC4 is the No. 2 terminal of a flip-flop FFC4;
8. SSD1 is the No. 12 terminal of a flip-flop FFD1;
9. SSD2 is the No. 1 terminal of a flip-flop FFD2;
10. SSB3 (B4) is the No. 1 terminal of a flip-flop FFB3; and
11. $\overline{\text{SSB1}}$ (B2) is the No. 12 terminal of a flip-flop FFB1.

The counters Y3, Y4, Y5, Y6 and Y7 comprise a sequence control clock for the selector switches SA1 — SA3, SC1 — SC4, SD2, SB1 (B2), SB3 (B4) and SE1 — SE3.

In order to complete the controlling input connections to the control terminals (like designations with the prefix S) of these switches, with the exception of the terminals SSE3 — SSE4 driven directly from the update selection counter Y7, signal lines (S1), (S2), (S3), (SA1), (SA2), (SA3), (SD1), (SC1), (SC2), (SC3), (SC4), Y6C and Y6B are provided by either direct or combined connections of the outputs of the counters Y3, Y4, Y5 and Y6 as follows:

1. The control line (S1) commences at the output (No. 10 terminal) of a NOR gate Y12 (CD4025 AE module of RCA) connected as an inverter by a common connection of its No. 11, No. 12 and No. 13 terminals to the No. 12 terminal (No. 1 bit) of the 7-bit counter Y3;
2. The control line (S2) commences at the output (No. 6 terminal) of a NOR gate Y13 (CD4025AE module of RCA) connected as an inverter by a common connection of its No. 3, No. 4 and No. 5 terminals to the No. 11 terminal (No. 2 bit) of the 7-bit counter Y3;
3. The control line (S3) commences at the output (No. 9 terminal) of a NOR gate Y14 (CD4025AE module of RCA) having its No. 1, No. 2 and No. 8 input terminals connected, respectively, to the No. 5 (No. 5 bit), No. 4 (No. 6 bit) and No. 3 (No. 7 bit) terminals, respectively, of the 7-bit counter Y3;
4. The control lines (SA1) – (SA3) have previously been defined as extending from the No. 2, No. 1, No. 3 terminals (No. 0, No. 1 and No. 2 counts) of the first counter Y4 to the No. 2, No. 4 and No. 6 terminals, respectively of the color selector module Y9;
5. The control line (SD1) commences at the No. 7 terminal (No. 3 count) of the first counter Y4 and extends to the No. 13 terminal of the NOR gate Y10 and ultimately drives the No. 9 terminal of the color selector Y9; and
6. The control lines (SC1), (SC2), (SC3), (SC4) originate at the No. 2, No. 1, No. 3 and No. 7 terminals (No. 0, No. 1, No. 2 and No. 3 counts) of the second counter Y5, which sequences the calculations being performed in the color computer 40, and extend to various inputs and gates associated with the sequenced switch controlling flip-flops FFA1-A3, FFC1-C4 FFD1-D2, FFB1 and FFB 3 as will now be described.

The control line (SD1) is connected to the No. 1 terminal of the NOR gate Y11; the No. 9 terminal of an EXCLUSIVE OR gate Y15 (CD4030 AE module of RCA); the No. 1 terminal of a NAND gate Y16 (CD4011 AE module of RCA); the No. 13 terminal of a like NAND gate Y17; and the No. 1 terminal of a NOR GATE Y18 (CD4001 AE module of RCA). Thus, the control line (SD1) carries sequencing signals for all of the switch control flip-flops FFA1 – A3, FFC1 – C4, FFD1 – D2, FFB1 and FFB3 as will become more fully apparent hereinafter.

As previously disclosed, the calculations are performed once in each half cycle in the color computer 40 to compensate for ripple and for offset in the integrator amplifier Q10 (FIG. 4). Accordingly, part of the required sequencing signals involve the generation of a 1st half cycle and second half cycle pulse from the

phase counter Y6 on the control lines Y6B and Y6C, respectively.

The other input to the EXCLUSIVE OR gate Y15 is the control line Y6B connected to the No. 8 terminal of the said gate Y15, the output (No. 10 terminal) thereof being commonly connected to the No. 2, No. 5, No. 12 and No. 9 terminals (inputs) of NAND gates Y19, Y20, Y21 and Y22, respectively. The control lines (SC1), (SC2), (SC3) and (SC4), respectively, drive the remaining inputs (No. 1, No. 6, No. 13 and No. 8 terminals) respectively, of the said NAND gates Y19, Y20, Y21, and Y22 (all of which are CD4011 AE modules of RCA).

The outputs (No. 3, No. 4, No. 11 and No. 10 terminals) of the respective NAND gates Y19 – Y22 drive, respectively, the input terminals No. 9, No. 5, No. 9 and N0. 5 of the switch controlling flip-flops FFC1, FFC2, FFC3 and FFC4.

The control line S2 is commonly connected to the other input terminals No. 11, No. 3, No. 11 and No. 3 of the said flip-flops FFC1, FFC2, FFC3 and FFC4, respectively, as well as to the input terminals No. 11 and No. 3 of the control flip-flops FFD1 and FFD2, respectively.

The remaining control flip-flops FFA1, FFA2, FFA3, FFB3 and FFB1 have terminals No. 3, No. 11, No. 3, No. 3 and No. 11, respectively, connected in common to the control line (S1).

The control line (S3) is connected to the No. 8 and No. 9 terminals of a NOR gate Y23 (CD4001 AE module of RCA) which is thus wired as an inverter with its No. 10 terminal (output) constituting a control line ($\overline{S3}$).

The control flip-flop FFD1 (for the zero switch SD1) has the control line (S2) driving one input (No. 11 terminal) and the output (No. 3 terminal) of the NAND gate Y16 driving another imput (No. 9 terminal). The No. 1 and No. 2 terminals (inputs) of the NAND gate Y16 are driven by the control lines (SD1) and ($\overline{S3}$), respectively.

The control flip-flop FFD2 (for the sample switch SD2) has the control line (S2) driving one input (No. 3 terminal) and the output (No. 11 terminal) of the NAND gate Y17 driving another input (No. 5 terminal).

The NAND gate Y17 is driven at one input (No. 13 terminal) by the control line (SD1) and at its other input (No. 12 terminal) by the output (No. 4 terminal) of a NOR gate Y24 (CD4001 AE module of RCA), the latter being driven at one input (No. 5 terminal) by the first half cycle control line Y6B and at the other input (No. 6 terminal) by the control line ($\overline{S3}$). The input Y7B (No. 13 terminal) of the update selection counter Y7 is connected to the sample switch control output SSD2 (No. 1 terminal) of the control flip-flop FFD2 to correlate the updating function with the sampling function in the color computer 40.

Additional control lines (SB1) 8nd (SB3) for the ganged control switches SB1 – SB2 and SB3 – SB4, respectively, originate from the carry-out (No. 14 terminals) terminals of 4-bit adders Y25 and Y26, respectively (CD4008 AE modules of RCA).

The control flip-flop FFB2 has one input (No. 3 terminal) driven by the control line (S1) and another input (No. 5 terminal) driven by the output (No. 11 terminal) of an EXCLUSIVE OR gate Y27 (CD4030 AE module of RCA), the latter having two inputs (No. 12 and No. 13 terminals) driven, respectively, by the output (No. 11 terminal) of a NOR gate Y28 (CD4001 AE module of RCA) and the output (No. 3 terminal) of the NOR gate Y18. Thus, the control lines Y6C and (SD1) influence the flip-flop FFB3 via the NOR gate Y18 and the control lines (SC4) and (SB3) influence the flip-flop FFB3 via the NOR gate Y28 since these latter control lines are connected, respectively, to the inputs (No. 12 and No. 13 terminals) of the said NOR gate Y28.

The control flip-flop FFB2 has one input (No. 11 terminal) driven by the control line (S1) and another input (No. 9 terminal) driven by the output (No. 3 terminal) of an EXCLUSIVE OR gate Y29 (CD4030 AE module of RCA), the latter having two inputs (No. 1 and No. 2 terminals) driven, respectively, by the output (No. 3 terminal) of the NOR gate Y18 and the control line (SB1). Thus, the control flip-flop FFB1 is influenced by the control lines (SD1) and Y6C via the NOR gate Y18 and EXCLUSIVE OR gate Y29, as well as by the control line (SB1) via the EXCLUSIVE OR gate Y29 and the control line (S1) by direct connection at the No. 11 terminal of the control flip-flop FFB1.

In the sequencing operation, the EXCLUSIVE OR gates Y27 and Y29 serve to reverse the logic between the first and second half cycles to permit the dual calculation in the color computer 40 to be more fully described in reference to the operation of FIG. 4.

To complete the logic interconnection of the several control flip-flops, all of the set and reset terminals thereof are connected to a common lead FFV which is connected to the source of negative bias (−6V).

The set and reset and output terminal Nos. of each of the said flip-flops are as follows:

Output Designation

Control Flip-Flop	Output Terminal No.	Set Terminal No.	Reset Terminal No.
FFA1	SSA1 (No. 1)	6	4
FFA2	SSA2 (No. 13)	8	10
FFA3	SSA3 (No. 1)	6	4
FFC1	SSC1 (No. 12)	8	10
FFC2	SSC2 (No. 2)	6	4
FFC3	SSC3 (No. 12)	8	10
FFC4	SSC4 (No. 2)	6	4
FFD1	SSD1 (No. 12)	8	10
FFD2	SSD2 (No. 1)	6	4
FFB3	SSB3 (B4) (No. 1)	6	4
FFB1	SSB1 (B2) (No. 12)	8	10

The front panel quality zone selector switches ZDR, ZDG, ZBR, ZBG and ZBD (Interswitch BB239/s Hexadecimal Switches with two commons) are all driven through suitable logic circuitry from the control lines (SA1–A3), (SD1), (SC1–C4) and in turn, drive the group of adders including the adders Y25 and Y26 to determine the sign and magnitude of the various scalar multipliers previously set forth in the Theory discussion.

There are five adders, manely Y25, Y26, Y30, Y31 and Y32 (all comprising CD4008AE modules of RCA) which are additionally driven by the outputs of the 7-bit counter Y3 such that the periods of closure of the color switch means SB1, SB2, SB3 and SB4 will be as required for the three scalar factors involved in each color calculation.

The quality zone switch inputs are as follows:

The dark-red zone switch ZDR has its No. 7 terminal connected in common with the No. 4 terminal of the bright-red zone switch ZBR, the No. 7 terminal of the latter being connected in common with the source of positive bias (+6V) together with the No. 4 terminal of the bright-green zone switch ZBG and the No. 7 terminal of the bright-dark zone switch ZBD.

The No. 4 terminal of the dark-green zone switch ZDG is connected in common with the No. 7 terminal of the bright-green zone switch ZBG.

The No. 4 terminal of the dark-red switch ZDR is driven from the output (No. 10 terminal) of a NAND gate Y33 (CD4011AE module of RCA), the latter having its inputs (No. 8 and No. 9 terminals) driven by the control lines (SA3) and (SC3), respectively.

The dark-green zone switch ZDG has its No. 7 terminal driven by the output (No. 4 terminal) of the like NAND gate Y34, the latter having its inputs (No. 5 and No. 6 terminals) driven by the control lines (SA3) and (SC2), respectively.

The bright-red zone switch ZBR has its No. 4 terminal (as well as the No. 7 terminal of ZDR) driven by the output (No. 3 terminal) of a NAND gate Y35 (CD4011 AE module of RCA), the latter having its inputs (No. 1 and No. 2 terminals) driven by the control line (SC3) and the output (No. 3 terminal) of a NOR gate Y36 (CD4001 AE module of RCA), respectively, the latter having its inputs (No. 5 and No. 6 terminals) driven, respectively, by the control lines (SD1) and (SA3).

The bright-green zone switch ZBG has its No. 7 terminal (as well as the No. 4 terminal of the zone switch ZDG) driven by the otput (No. 11 terminal) of a NAND gate Y37 (CD4011 AE module of RCA), the latter having its inputs (No. 12 and No. 13 terminals) driven by the output (No. 4 terminal) of the NOR gate Y36 and the control line (SC2), respectively. Thus, the zone switch ZBG is driven by the control lines (SA3) or (SD1) via the NOR gate Y36 and the control line (SD2), all routed through the said NAND gate Y37.

The bright-dark zone switch ZBD is driven at its No. 4 terminal by the output (No. 4 terminal) of a NAND gate Y38 having its inputs (No. 5 and No. 6 terminals) driven, respectively, by control lines (SA3) and (SC1), respectively.

All of the zone switches ZDR, ZDG, ZBR, ZBG and ZBD drive inputs of the adder Y30 as follows:

The No. 5 terminal of zone switch ZDR and the No. 5 terminal of zone switch ZDG drive the No. 9 and No. 8 terminals (inputs), respectively, of a NAND gate Y39 (CD4011 AE module of RCA), having its output (No. 10 terminal) connected to the No. 7 terminal of the adder Y30.

The No. 8 terminals of the zone switches ZDR and ZDG drive, respectively, the No. 5 and No. 6 terminals (inputs) of a like NAND gate Y40, having its output (No. 4 terminal) connected to the No. 5 terminal of the adder Y30.

The No. 6 terminals of the zone switches ZDR and ZDG drive, respectively, the No. 13 and No. 12 terminals (inputs) of a like NAND gate Y41 having its output (No. 11 terminal) connected to the No. 3 terminal of the adder Y30.

The No. 9 terminals of the zone switches ZDR and ZDG drive, respectively, the No. 1 and No. 2 terminals of a like NAND gate Y42, having its output (No. 4 terminal) connected to the No. 1 terminal of the adder Y30.

The zone switches ZBR, ZBG and ZBD have their No. 5 terminals driving, respectively, the No. 13, No. 11 and No. 12 terminals (inputs) of a NAND gate Y43 (CD4023 AE module of RCA), having its output (No. 10 terminal) connected to the No. 6 terminal of the adder Y30.

The No. 8 terminals of the zone switches ZBR, ZBG and ZBD drive, respectively, the No. 3, No. 4 and No. 8 terminals of a like NAND gate Y44, having its output (No. 9 terminal) connected to the No. 4 terminal of the adder Y30.

The No. 6 terminals of the zone switches ZBR, ZBG and ZBD drive, respectively, the No. 3, No. 4 and No. 5 terminals (inputs) of a like NAND gate Y45, having its output (No. 6 terminal) connected with the No. 2 terminal of the adder Y30.

The No. 9 terminals of the zone switches ZBR, ZBG and ZBD drive, respectively, the No. 1, No. 2 and No. 8 terminals (inputs) of a like NAND gate Y46, having its output (No. 9 terminal) connected to the No. 15 terminal of the adder Y30.

Since each of the zone switches ZDR, ZDG, ZBR, ZBG and ZBD are sixteen position thumbwheel switches with the positions designated by the numbers zero to fifteen, the four outputs (No. 5, No. 8 No. 6 and No. 9 terminals) from each of said switches carries a binary code designating switch position. Therefore, the combination of these position codes via the NAND logic gates Y39–Y46, drives the adder Y30 to provide the parameters indicating the three divisions between the six quality zones Z1–Z6 as set by the said zone switches. In conjunction with other parameters to be defined, the adder Y30 drives certain inputs on two additional 4-bit adders Y31 and Y26 interconnected to provide a 6-bit scalar multiplier output and the sequencing of the control line (SB3).

This scalar multiplier output of the adders Y31 and Y26, together with other parameters to be defined, drives certain inputs on two additional 4-bit adders Y32 and Y25 to effect the proper sequencing of the control line (SB1).

The No. 9 terminal of the adder Y30 is connected to the source of negative bias (−6V).

The remaining terminals (No. 10, No. 11, No. 12, No. 13 and No. 14) of the adder Y30 comprise the first through fourth and carry-out bits, respectively, of the coded sum output of the adder Y30 and are connected, respectively, with the No. 6, No. 4, No. 2 and No. 15 terminals of the adder Y31 and the No. 6 terminal of the adder Y26.

The coded sum output of the adder Y31 comprises its No. 10, No. 11, No. 12 and No. 13 terminals representing the first through fourth bits, respectively, of the scalar multiplier number for a given red, green or infrared parameter in the color calculations and are respectively connected to the No. 6, No. 4, No. 2 and No. 15 terminals of the adder Y32.

The fifth and sixth bits of the scalar multiplier number appear at the coded outputs comprising the No. 10 and No. 11 terminals, respectively, of the adder Y26 which terminals are respectively connected to the No. 6 and No. 4 terminals of the adder Y25. As previously disclosed the carry-out bit (No. 14 terminal) of the adder Y26 determines the algebraic sign of the scalar multiplier and sequences the control line (SB3); and the carry-out bit (No. 14 terminal) of the adder Y25 sequences the control line (SB1).

The remaining inputs to the adders Y31 and Y26 are as follows:

The carry-out bit (No. 14 terminal) of the adder Y31 drives the No. 9 terminal of the adder Y26.

The No. 1, No. 3 and No. 5 terminals of the adder Y31 are driven by the respective outputs (No. 10, No. 9 and No. 6 terminals) of NAND gates Y47, Y48 and Y49 (CD4023 AE modules of RCA).

The No. 3 terminal of the adder Y26 is driven by the output (No. 10 terminal) of a NAND gate Y50 (CD4023 AE module of RCA) having its No. 11, No. 12 and No. 13 terminals (inputs) connected in common to the output (No. 9 terminal) of a like NAND gate Y51. The No. 5 and No. 7 terminals of the adder Y26 are driven by the respective outputs (No. 6 and No. 10 terminals) of like NAND gates Y52 and Y53.

The No. 7 and No. 9 terminals of the adder Y31 and the No. 4 terminal of the adder Y26 are connected to the source of negative bias (−6V); and the No. 1 and No. 2 terminals of the adder Y26 are connected to the source of positive bias (+6V).

The remaining connections of the 4-bit adders Y32 and Y25 are as follows:

The carry-out bit (No. 14 terminal) of the adder Y32 drives the No. 9 terminal of the adder Y25.

The No. 9 terminal of the adder Y32 is connected to the source of negative bias (−6V); and the No. 1 and No. 2 terminals of the adder Y25 are connected to the source of positive bias (+6V).

The second through seventh bits of the calculation period subdivision counter Y3 (No. 11, No. 9, No. 6, No. 5, No. 4 and No. 3 terminals, respectively) are connected, respectively, to the No. 7 No. 5, No. 3, No. 1 terminals of the adder Y25.

Scalar bias parameters SBP for determining the range and starting points of the control switches ZDR through ZBD thereof for driving the adders Y31 and Y26 are as follows:

1. R/GN-I: redness or greenness, infrared mode.
2. R/GN-G: redness or greenness, green mode.
3. R/GN-R: redness or greenness, red mode.
4. BN-R: brightness, red mode.
5. BN-I: brightness, infrared mode.

When the values for the bias parameters SBP have been determined as will be described hereinafter, the values are hard-wired into scalar bias circuit board SBB which serves as an interface between certain control line logic and the inputs of the NAND gates Y47–Y49 and Y51–Y53 driving the adders Y31 and Y26.

The scaler multiplier board has five inputs designated as the scalar bias parameters SBP, the said inputs corresponding to R/GN-I, R/GN-G, R/GN-R, BN-R and BN-I, respectively, with a sixth input connected to the source of positive bias (−6V) as shown.

The number of hard-wired terminals are for 6-bit parameters SBP with the most significant bit MSB determining the algebraic sign of the particular wired parameter SBP. The position of the least significant bits LSB is also indicated on the scalar bias board SBB.

The input terminal numbers for the NAND gates Y47–Y49 and Y51–Y53 for connection with the scalar bias board SBB are as follows:

NAND Gate	Input Terminal Nos.
Y47	No. 11, No. 12, No. 13
Y48	No. 1, No. 2, No. 8
Y49	No. 3, No. 4, No. 5
Y51	No. 1, No. 2, No. 8
Y52	No. 3, No. 4, No. 5
Y53	No. 11, No. 12, No. 13

From the foregoing table and from the drawing it can be seen that several of the foregoing gates can be provided in a single CD4023 AE module (IC chip) with the designated terminals connected to provide multiple NAND gate functions therethrough. This is also the case for like designated NAND, NOR and other gates of like commercial designation in the description of FIG. 5 and other Figures. The gates are individually shown and described to better show the interplay of the logic in controlling the various sequencing or clocking functions involved.

The scalar bias parameters SBP are generated as follows:

1. R/GN-I: the control lines (SC1) and (SC4) drive the inputs (No. 8 and No. 9 terminals, respectively) of a NOR gate Y54 (CD4001 AE module of RCA), the output (No. 10 terminal) of the latter driving one input (No. 9 terminal) of a NAND gate Y55 (CD4011 AE module of RCA). The other input (No. 8 terminal) of the NAND gate Y55 is driven by the control line (SA3) and the output (No. 10 terminal) of the NAND gate Y55 controls the parameter R/GN-I.

2. R/GN-G: the control line (SA2) drives one input (No. 13 terminal) of a like NAND gate Y56 having its other input (No. 12 terminal) connected to the output (No. 10 terminal) of the NOR gate Y54. Thus the output (No. 11 terminal) of the NAND gate Y56 controls the parameter R/GN-G.

3. R/GN-R: the control line (SA1) drives one input (No. 1 terminal) of a like NAND gate Y57 having its other input (No. 2 terminal) driven by the output (No. 10 terminal) of the NOR gate Y54. Thus, the output (No. 3 terminal) of the NAND gate Y57 controls the parameter R/GN-R.

4. BN-R: the control line (SA1) drives one input (No. 5 terminal) and the control line (SC1) drives the other input (No. 6 terminal) of a like NAND gate Y58, the output (No. 4 terminal) thereof controls the parameter BN-R.

5. BN-I: this parameter is signaled by the output (No. 4 terminal) of a like NAND gate Y38, previously described, and control is derived from the control lines (SA3) and (SC1) previously defined as the inputs to the NAND gate Y38.

Thus, because of the parenthetical designations of the control lines (SA1), (SA2), (SA3), (SC1) and (SC4) corresponding to the control switch means bearing like primary designations, the scalar bias parameters SBP are clearly controlled by the color selection means SA1, SA2, SA3 (red, green, infrared, respectively) and the first and last of the storage control means SC1 and SC4, respectively, which also control the switches in the color computer 40 (see FIGS. 4A and 4B).

All of the thumbwheel switches ZDR, ZDG, ZBR, ZBG and ZBD are of the hexadecimal 1248 code and compliment type with two (2) commons and wheel po-

sitions 0 – 15 such as the BB239/S modules of Inter Switch.

THE REJECT SELECTION LOGIC RSL

Referring now to FIG. 6, the shift register ST4 providing the data input between the register ST3 and the reject selection logic RSL is shown as having a SHIFT CLOCK input driving the No. 9 terminal of a first 8-bit shift register ST4A and the No. 1 terminal of a second 8-bit shift register ST4B (both comprising a CD4015 AE module of RCA) and a DATA IN terminal (RSL1) receiving the data from the output ST3D of the shift register ST3, as generally described previously in reference to FIGS. 4A and 4B, driving the No. 7 terminal of the first register ST4A.

The No. 7 and No. 9 terminals of the first register ST4A are connected to the source of negative bias (−6V) through resistors R25 and R26, respectively, while the No. 6 terminal of the first register ST4A and the No. 14 terminal of the second register ST4B are directly connected to the said source of negative bias (−6V).

The No. 10 terminal of the first register ST4A drives the No. 15 terminal of the second register ST4B and the resulting interaction of the two said registers results in six (6) bits of information which relate to the color of the objects detected by the comparator 40B of the color computer 40 in the following manner:

B ≡ Bright
D ≡ Dark
G = Green
NG ≡ Not Green
NR ≡ Not Red
R ≡ Red

The foregoing symbols in parentheses designate corresponding data lines on which representative data bits appear to indicate the presence or absence of that given color characteristic of the objects (leaves) detected.

The BRIGHT data line (B) originates at the No. 5 terminal of the first register ST4A.

The DARK data line (D) originates at the output (No. 4 terminal) of a NOR gate Y60 (CD4001 AE module of RCA) connected as an inverter by connecting both its inputs (No. 5 and No. 6 terminals) to the No. 4 terminal of the first register ST4A.

The GREEN data line (G) originates at the No. 3 terminal of the first register ST4A.

The NOT GREEN data line (NG) originates at the output (No. 11 terminal) of a NOR gate Y51 (CD4001 AE module of RCA) connected as an inverter by having both its inputs (No. 12 and No. 13 terminals) connected with the No. 10 terminal of the first register ST4A.

The NOT RED data line (NR) originates at the No. 13 terminal of the second register ST4B.

The RED data line (R) originates at the output (No. 10 terminal) of a NOR gate Y62 (CD4001 AE module of RCA) connected as an inverter by having both its inputs (No. 8 and No. 9 terminals) connected with the No. 12 terminal of the second register ST4B.

If all of the said color data lines are driven low, this indicates that the comparator has detected only the background reference with no leaves present over its surface.

All other combinations of signals on the said color data lines indicate the relative brightness, greenness and/or redness of a leaf to the quality zone dividing lines set on the front control panel FPC.

Thus, the color data lines (B), (D), (G), (NG). (NR) and (R) comprise the first input RSL1 of the reject selection logic circuit RSL.

The selected quality zone data from the toggle switches TS in each of the quality zones Z1–Z6 (on the front control panel FPC) is received on the second data input RSL2, the latter comprising six corresponding zone select lines (Z1), (Z2), (Z3), (Z4), (Z5) and (Z6) which drive the reject selection logic circuit RSL through in-line protection resistors R27, R28, R29, R30, R31 and R32, respectively.

The color data lines and the zone select lines selectively drive three interconnected AND/OR SELECT modules Y63, Y64 and Y65 (CD4019 AE modules of RCA) as follows:

Color Data Line	AND/OR SELECT MODULE	TERMINAL NUMBER
(B)	Y63	9
(D)	Y63	14
(G)	Y64	9
(NG)	Y64	14
(NG)	Y65	3
(NR)	Y65	14
(R)	Y65	9
Zone Select Line		
(Z1)	Y63	15
(Z2)	Y63	2
(Z3)	Y63	4
(Z4)	Y63	1
(Z5)	Y63	3
(Z6)	Y63	5
(Z1)	Y64	2
(Z4)	Y64	4
(Z3)	Y65	2
(Z6)	Y65	4

The remaining terminals of the first AND/OR SELECT module Y63 are connected as follows:

The No. 6 and No. 7 terminals are connected to the source of negative bias (−6V);

The No. 11 terminal is connected to an input (No. 6 terminal) of the third AND/OR SELECT module Y65 and to one input (No. 12 terminal) of a NAND gate Y66 (CD4011 AE module of RCA);

The No. 12 terminal is connected to an input (No. 5 terminal) of the second AND/OR SELECT module Y64, to the other input (No. 13 terminal) of the NAND gate Y66 and to one input (No. 9 terminal) of a like NAND gate Y67; and

The No. 13 terminal is connected to an input (No. 6 terminal) of the second AND/OR SELECT module Y64 and to the other input (No. 8 terminal) of the NAND gate Y67.

The NAND gates Y66 and Y67 drive like NAND gates Y68 and Y69, respectively, and together drive a NOR gate Y70 (CD4001 AE module of RCA) as follows:

The output (No. 10 terminal) of the NAND gate Y67 drives both inputs (No. 1 and No. 2 terminals) of the NAND gate Y69 and one input (No. 13 terminal) of the NOR gate Y70; and

The output (No. 11 terminal) of the NAND gate Y66 drives both inputs (No. 5 and No. 6 terminals) of the NAND gate Y68 and the other input (No. 12 terminal) of the NOR gate Y70.

The remaining terminals of the second AND/OR SELECT module Y64 are connected as follows:

The No. 15 and No. 1 terminals are connected to the sources of positive bias (+6V) and the No. 3 terminal to the source of negative bias (−6V);

The No. 7 terminal is connected to the output (No. 4 terminal) of the NAND gate Y68;

The No. 10 terminal is connected to one input (No. 11 terminal) of NOR gate Y75 (CD4002 AE module of RCA);

The No. 11 and No. 12 terminals are connected to the respective inputs (No. 1 and No. 2 terminals) of a NAND gate Y71 (CD4011 AE module of RCA); and

The No. 13 terminal is connected to one input (No. 3 terminal) of a NOR gate Y74 (CD4002 AE module of RCA).

The remaining terminals of the third AND/OR SELECT module Y65 are connected as follows:

The No. 15 and No. 1 terminals are connected to the source of positive bias (+6V);

The No. 5 terminal is connected to the No. 11 terminal of the second AND/OR SELECT module Y64;

The No. 7 terminal is connected to the output (No. 3 terminal) of the NAND gate Y69;

The No. 10 terminal is connected to an input (No. 10 terminal) of the NOR gate Y75;

The No. 11 and No. 12 terminals are connected to respective inputs (No. 13 and No. 12 terminals) of a NAND gate Y72 (CD4011 AE module of RCA); and

The No. 13 terminal is connected to an input (No. 2 terminal) of the NOR gate Y74.

The remaining inputs to the NOR gate Y74 are connected as follows:

The No. 4 terminal is connected to the color data line (D); and

The No. 5 terminal is connected to the color data line (B).

The remaining inputs to the NOR gate Y75 are connected as follows:

The No. 9 terminal is connected to the output (No. 10 terminal) of a NAND gate Y73 (CD4011 AE module of RCA) having one of its inputs (No. 9 terminal) connected to the output (No. 11 terminal) of the NAND gate Y72 and the other of its inputs (No. 8 terminal) connected to the output (No. 3 terminal) of the NAND gate Y71; and

The No. 12 terminal connected to the output (No. 11 terminal) of the NOR gate Y70.

The output (No. 1 terminal) of the NOR gate Y74 is the background data line comprising a part of the output RSL3 of the reject selection logic RSL which drives the input CPU1 of the central processor CPU.

The output (No. 13 terminal) of the NOR gate Y75 drives both inputs (No. 5 and No. 6 terminals) of a NAND gate Y76 (CD4011 AE module of RCA), the output (No. 4 terminal) of the latter being the reject data line (REJ) comprising the other part of the output RSL3 of the reject selection logic RSL which drives the input CPU1 of the central processor CPU.

A high or digital "1" condition on the background data line (BKD) indicates to the processor CPU that the color sorter is detecting only background.

A high or digital 1 condition on the reject data line (REJ) indicates to the processor CPU that a given leaf being detected is to be rejected.

The quality zones Z1–Z6, color data lines (B), (D), (G), (NG), (NR) and (R) and the zone select lines (Z1)–(Z6) are logically interrelated as shown in FIG. 7.

The reject logic is set up to selectively reject zones Z1–Z6 individually or the zone pairs Z1 and Z4, Z1 and Z2, Z2 and Z3, Z3 and Z6, Z5 and Z6, and Z4 and Z5, or triplets Z1, Z2 and Z3 and Z4, Z5 and Z6. The Z2 and Z5 combination is not provided for as it is infrequently used.

The presence of an "X" in the REJECT LOGIC table of FIG. 7 indicates a high (digital 1) condition of a given color data or zone select line.

If all of the color data lines are low (digital "0") then there is no leaf present over the background. Other high-low conditions of the various color data lines indicate the particular leaf color detected.

The high and low conditions of the zone control lines are determined by the "reject" and "keep" positions respectively, of the zone select switches TS on the front control panel FPC.

CONTROLS EFFECTED BY FRONT CONTROL PANEL 30, LOGIC BOARD FPLB AND REJECT SELECT LOGIC RSL

Referring first to FIG. 2, each of the quality zone switches ZBD, ZBG, ZDG, ZBR and ZDR are sixteen position switches with the positions identified by the numbers 0 to 15, respectively.

The position numbers on the green zone switches ZBG and ZDG complement like position numbers on the red zone switches ZBR and ZDR as will be more clearly shown hereinafter with reference to FIGS. 8, 9, 9A, 10 and 10A.

Referring first to FIG. 8, the area of adjustment of the front control panel 30 is shown for the zone control switches. Note the complimentary scales between the red and green zone control switches ZBG, ZDG and ZBR, ZDR.

In FIG. 8, the various colors of tobacco leaves are portrayed relative to the ordinates of green reflectivity $(G_L - G_B/I_L - I_B) \times 100$ and reflectivity $(R_L - R_B/I_L - I_B) \times 100$.

To effect quality zone selection, reference is first made to FIGS. 9 and 9A, wherein an example is shown wherein all tobacco that is too green (Z1 and Z4), too red (Z3 and Z6) or too dark (Z4, Z5 and Z6) are to be rejected.

By reference to FIG. 9A, the settings of the toggle switches TS1–TS6 and the zone switches ZBD, ZBG, ZBR, etc., are as follows:

Zone No.	TS No.	Zone Switch Position No.
Z1	TS1 = Reject	ZBG = 5
Z2	TS2 = Keep	ZBD = 5
Z3	TS3 = Reject	ZBR = 1
Z4	TS4 = Reject	ZDG = 7
Z5	TS5 = Reject	ZBD = 5
Z6	TS6 = Reject	ZDR = 10

These values on the zone switches set the slopes and relative positions of the brightness, greenness and redness divides lines which serve as the standards for the comparator 40B in the color computer 40 to determine whether a leaf is brighter, greener, redder or viceversa from these established division lines.

The setting of the reject selection switches TS then prescribes which of the leaves falling within the various

zones defined by the given division lines are to be kept or rejected.

With the front control panel thus set, the graphic interrelationship of the zones Z1–Z6 is shown. with zone Z2 the only acceptable zone for the leaves being inspected. As can be seen, only normal leaves are contained in zone Z2.

In FIGS. 10 and 10A, the flexibility of settings in the present invention is illustrated.

With the quality zone switches ZBD, ZBG, ZBR, etc., and the reject select switches TS1–TS6 set as shown in FIG. 10A (representative of the front control panel 30 of FIG. 2), the unhatched portion of FIG. 10 shows that only the leaves having colors falling in a preset zone Z5 are acceptable and all other colors of leaves are rejected. In other words, only leaves that are darker than the brightness division and are not green and not red compared to the greenness and redness dividers, respectively, are acceptable.

Thus, the present invention can isolate leaves of a single color or leaves having a range of colors by proper adjustment of the said zone control and reject selection switches on the front control panel 30.

THE PROGRAM CLOCK PC

The program clock PC will now be described with reference to FIGS. 11 and 12.

The program clock is synchronized to the 120Hz ripple from the power supply of the present invention, hereinafter to be more fully described, by a 120Hz clock input W, see FIG. 11, which drives a pair of NAND gates Y80 and Y81 (CD4011 AE modules of RCA) connected in a Schmitt trigger configuration as follows:

The synchronizing input W is connected through an input resistor R33 to the No. 1 and No. 2 terminals (input) of the NAND gate Y80 and through a resistor R34 to the No. 11 terminal (output) of the NAND gate Y81. The No. 3 terminal (output) of the NAND gate Y80 drives the No. 12 and No. 13 terminals (input) of the NAND gate Y81.

The output (No. 11 terminal) of the NAND gate Y81 is the output of the Schmitt trigger configuration and drives No. N. 11 terminal of a D type flip-flop Y82 (CD4013 AE module of RCA), the latter having its No. 8 terminal connected to the source of negative bias (−6V) and its No. 9 terminal connected to the source of positive bias (+6V).

The No. 12 terminal of the flip-flop Y82 drives the LOAD pulse output PC2 of the program clock PC through the following configuration:

A NOR gate Y83 (CD4001 AE module of RCA) has its inputs (No. 5 and No. 6 terminals) driven by the No. 12 terminal of the flip-flop Y82 and its output (No. 4 terminal) driving the LOAD pulse output PC2.

A NAND gate Y84 (CD4011 AE module of RCA) also drives the LOAD pulse output PC2 through its No. 10 terminal (output) and has its inputs (No. 8 and No. 9 terminals) also driven by the No. 12 terminal of the flip-flop Y82.

The No. 13 terminal (output) of the flip-flop Y82 drives one input (No. 1 terminal) of a NOR gate Y85 (CD4001 AE module of RCA), the other input (No. 2 terminal) of the latter being driven from the HOLD pulse input PC5 of the program clock PC through a like NOR gate Y86 having both its inputs (No. 12 and No. 13 terminals) driven by the HOLD input PC5 and its output (No. 11 terminal) driving the said No. 2 terminal of the NOR gate Y85.

The HOLD terminal PC2 is connected to the source of negative bias (−6V) through a resistor R35.

The NOR gate Y85 drives and controls a 750 KHz oscillator circuit OSC connected in the following configuration to synchronize the said oscillator with the 120Hz input W and to provide for disabling the said oscillator with the appearance of the HOLD pulse at the input PC2 to indicate a "cease calculation" command to the color computer 40 as will be more fully described hereinafter:

The output (No. 3 terminal) of the NOR gate Y85 drives one input (No. 12 terminal) of a NOR gate Y87 (CD4001 AE module of RCA), the latter having its output (No. 11 terminal) driving one input (No. 9 terminal of a like NOR gate Y88, the latter having its other input (No. 8 terminal) connected to the source of negative bias (−6V) and its output (No. 10 terminal) driving the other input (No. 13 terminal of the NOR gate Y87 through a feedback capacitor C80.

The No. 11 terminal of the NOR gate Y87 is connected to its No. 13 terminal through a resistor R36.

The NOR gate Y88 has its output (No. 10 terminal) driving the No. 3 input terminal of a D type flip-flop Y89 (CD4013 AE module of RCA), the latter having its No. 4 terminal connected to the source of negative bias (−6V), its No. 6 terminal driven by the output (No. 3 terminal) of the NOR gate Y85 (and thus controlled by the synchronizing signal W and the HOLD pulse via the NOR gate Y85), its No. 2 terminal (one output) connected to its No. 5 terminal and driving one input (No. 1 terminal) of an output NOR gate Y90 (CD4001 AE module of RCA) and its No. 1 terminal (second output) driving one input (No. 5 terminal) of another like NOR gate Y91.

The other inputs (No. 2 and No. 6 terminals, respectively) of the NOR gates Y90 and Y91 are driven by the output (No. 10 terminal) of the NOR gate Y88.

The output (No. 3 terminal) of the NOR gate Y90 drives the output PC6 of the program clock PC in the provision of a 750KHz clock signal.

The output (No. 4 terminal) of the NOR gate Y91 drives the No. 10 terminal of the flip-flop Y82.

The HOLD pulse input PC5, from the output (No. 11 terminal) of the NOR gate Y86 constrains the generation of a 40Hz clock signal at clock output PC7, a 120 Hz clock signal at clock output PC8 and a SLOW CLOCK signal at clock output PC 9 as follows:

The output (No. 11 terminal) of the NOR gate Y86 drives the inputs (No. 8 and No. 9 terminals) of a like NOR gate Y92 through a coupling capacitor C81, the said inputs of the NOR gate Y92 being connected to the source of negative bias (−6V) through a resistor R37. The output (No. 10 terminal) of the NOR gate Y92, through the forward path of a diode Y93 (IN457), drives the inputs (No. 8 and No. 9 terminals) of a NOR gate Y94 (CD4023 AE module of RCA), the said inputs of the NOR gate Y94 being connected to the source of negative bias through a resistor R38 in parallel with a capacitor C82.

The output (No. 10 terminal) of the NOR gate Y94 drives both inputs (No. 5 and No. 6 terminals) of a like NOR gate Y95 and both inputs (No. 5 and No. 6 terminals) of another NOR gate Y96 (CD4011 AE module of RCA), both outputs (No. 4 terminals) of the said NOr gates Y95 and Y96 directly driving the 120Hz

clock output PC8, the No. 3 terminal (input) of a D type flip-flop Y97 (CD4013 AE module of RCA), and the No. 11 and No. 3 terminals (inputs), respectively, of alike D type flip-flop Y 98 and Y99.

The No. 6 terminal of the flip-flop Y97 is driven by the RESET FAST input terminal PC10 which is in turn controlled by a front panel push button to eliminate "Time-out" wait, and is connected to the source of negative bias (−6V) through a resistor R39. The No. 4 terminal of the flip-flop Y97 is connected to the source of negative bias (−6V).

The No. 1 terminal (output) of the flip-flop Y97 drives the SLOW CLOCK output PC9 and the No. 10 terminal of a like flip-flop Y100; the latter having its No. 8 terminal connected to the source of negative bias (−6V), its No. 9 terminal connected to the source of positive bias (−6V), its No. 13 terminal (output) connected to an input (No. 5 terminal) of the flip-flop Y97 and its No. 11 terminal connected to the input (No. 3 terminal) of a 7-bit counter Y101 (CD4024 AE module of RCA).

The counter Y101 has its No. 2 terminal connected to the source of negative bias (−6V) and its output (No. 1 terminal) driving one input (No. 9 terminal) of the flip-flop Y98 and the No. 1 terminal (input) of a NOR gate Y102 (CD4023 AE module of RCA). The other input (No. 2 terminal) of the NOR gate Y102 is driven by the No. 13 terminal (output) of the flip-flop Y98. The output (No. 3 terminal) of the NOR gate Y102 drives an input (No. 5 terminal) of the flip-flop Y99, the output (No. 1 terminal) of the latter driving the 40Hz clock output PC7.

The No. 8 and No. 10 terminals of the flip-flop Y98 and the No. 4 and No. 6 terminals of the flip-flop Y99 are connected to the source of negative bias (−6V).

The combination Y97, Y100, Y101 comprises a counter circuit as does the combination Y98, Y99, Y102, the latter being synchronized from the former and both counter circuits being synchronized with the HOLD clock signal which is counted down therein to provide the 40Hz and SLOW CLOCK clock signals at the clock outputs PC7 and PC9 respectively.

Referring now to FIG. 12, the balance of the program clock PC is shown in which the 750KHz signal on the clock terminal PC6 drives the No. 2, No. 13 and No. 5 terminals (inputs), respectively, of NAND gates Y103, Y104 and Y105 (CD4011 AE modules of RCA) and the No. 13, No. 2 and No. 3 terminals (inputs), respectively, of NAND gates Y106, Y107 and Y108 (CD4023 AE modules of RCA).

The NAND gate Y103 is responsive to the LOAD pulse signal from the clock terminal PC2, the latter being connected through both inputs No. 12 and No. 13 terminals) of a NAND gate Y109 (CD4011) AE module of RCA) the latter having its output No. 11 terminal) connected to the other input No. 1 terminal) of the said NAND gate Y103.

The output (No. 3 terminal) of the NAND gate Y103 drives an input (No. 14 terminal) of an octal counter Y110 (CD4022 AE module of RCA) and an input (No. 3 terminal) of a D type flip-flop Y111 (CD4013 AE module of RCA).

The No. 2 terminal (one output) of the flip-flop Y111 drives the No. 12 terminal (input) of the NAND gate Y104, the No. 12 terminal (input) of the NAND gate Y106, the No. 15 terminal of the octal counter Y110 and the No. 1 terminal (input) of an EXCLUSIVE OR gate Y112 (CD4030 AE module of RCA). The No. 1 terminal (output) of the flip-flop Y111 drives the No. 1 terminal (input) of the NAND gate Y107.

The No. 6 terminal (set) of the flip-flop Y111 is connected to the source of negative bias (−6V) while the No. 4 terminal (reset) thereof is connected directly to the HOLD pulse output PC5.

The No. 5 terminal of the flip-flop Y111 is driven by the output (No. 6 terminal) of a NOR gate Y114 (CD4025 AE module of RCA).

For the octal counter Y110:

The No. 13 terminal is connected to the source of negative bias;

The No. 3 terminal drives both inputs (No. 1 and No. 2 terminals) of a NAND gate Y113 (CD4011 AE module of RCA); and

The No. 11 terminal drives an input (No. 3 terminal) of the NOR gate Y114, an input (No. 6 terminal) of the NAND gate Y105 and an input (No. 8 terminal) of a like NAND gate Y116, the latter having its output (No. 10 terminal) driving the input (No. 2 terminal) of the EXCLUSIVE OR gate Y112.

An input (No. 5 terminal) of the NOR gate Y114 is driven by the output (No. 10 terminal) of a like NAND gate Y115, the latter having an input (No. 13 terminal) driven by the output (No. 3 terminal) of the NAND gate Y113. The remaining input (No. 4 terminal) of the NOR gate Y114 is connected to the source of negative bias (−6V).

The NAND gate Y104 drives a compute cycle signal generator Y118–Y119, the module Y118 comprising an octal counter (CD4022 AE module of RCA) and the module Y119 comprising a D type flip-flop (CD4013 AE module of RCA). The output (No. 11 terminal) of the NAND gate Y104 drives the input (No. 14 terminal) of the octal counter Y118 and the input (No. 11 terminal) of the flip-flop Y119.

The No. 13 terminal of the octal counter Y118 is connected to the source of negative bias (−6V) and the No. 25 terminal thereof is driven by an output (No. 13 terminal) of the flip-flop Y119, that output terminal also driving the input (No. 12 terminal) of the NOR gate Y115.

The outputs, No. 2, No. 1, No. 3, No. 7 and No. 11 terminals of the octal counter Y118, respectively, carry compute cycle instruction bits A, B, C, D and E which are connected into the central processor CPU as will be more fully described hereinafter.

The No. 2 terminal (A-bit) of the octal counter Y118 also drives an input (No. 8 terminal) of the NAND gate Y107 and an input (No. 8 terminal) of a NAND gate Y120 (CD4023 AE module of RCA); while the No. 11 terminal (E-bit) of the octal counter Y118 drives an input (No. 9 terminal) of the flip-flop Y119.

The other output (No. 12 terminal) of the flip-flop Y119 drives an input (No. 9 terminal) of the NAND gate Y120 and an input No. 11 terminal) of the NAND gate Y106.

The No. 10 terminal (reset) of the flip-flop Y119 is connected to the source of negative bias (−6V) while the No. 8 terminal (set) thereof is driven by an output (No. 3 terminal) of a decade counter Y121 (CD4017 AE module of RCA), which, in a combination of modules Y121, Y122, Y123 comprises counting means for counting off the number of color sorting units slaved to the main or central process controller CPU and the

color computer **40** as will hereinafter be more fully described.

In brief, **Y122** is another decade counter of the same type as **Y121** and **Y123** is a D type flip-flop like **Y119.**

The number of optical channels in each of the slaved color sorting units (i.e., the number of optics units A in each color sorter) is counted off by the combination of modules **Y124, Y125,** the module **Y125** being a D type flip-flop of the same type as flip-flop **Y119** and the module **Y124** being an octal counter of the same type as the octal counter **Y118.**

The channel counter **Y124, Y125** is driven by the output (No. **4** terminal) of the NAND gate **Y105** through the No. **14** terminal (input) of the octal counter **Y124,** the latter having a 4-channel output (No. **7** terminal) and an 8-channel output (No. **10** terminal) and through an input (No. **11** terminal) of the flip-flop **Y125.** In the configuration shown only the **4**-channel output (No. **7** terminal) is connected and it drives an input (No. **9** terminal) of the flip-flop **Y125** and an input (No. **6** terminal) of a NAND gate **Y126** (**CD4011** AE module of RCA), the latter having its other input (No. **5** terminal) connected to an output (No. **2** terminal) of the decade counter **Y121** in the slaved unit counter **Y121, Y122, Y123** and its output (No. **4** terminal) connected to an input (No. **9** terminal) of the NAND gate **Y116.**

The 8-channel output (No. **10** terminal) of the octal counter **Y124** can selectively be connected to the input (No. **6** terminal) of the NAND gate **Y126** depending upon the number of channels involved.

The No. **12** terminal (one output) of the flip-flop **Y125** drives an input (No. **8** terminal) of a NOR gate **Y127** (**CD4025** AE module of RCA) and the No. **13** terminal (other output) of the flip-flop **Y125** drives the No. **15** terminal of the octal counter **Y124** and the input (No. **11** terminal) of the NOR gate **Y115.**

The No. **13** terminal of the octal counter **Y124** and the No. **10** terminal (reset) of the flip-flop **Y125** are both connected to the source of negative bias (−6V).

The No. **8** terminal (set) of the flip-flop **Y125** is connected to the HOLD pulse terminal **PC5** of the program clock PC.

The output (No. **4** terminal) of the NAND gate **Y105,** in addition to driving the input (No. **14** terminal) of the octal counter **Y124,** also drives the No. **1** and No. **2** terminals (inputs) of the NOR gate **Y127,** the output (No. **9** terminal) of the latter driving the inputs (No. **13** terminals) of the decade counters **Y121** and **Y122.**

In the slave unit counter **Y121, Y122, Y123,** the No. **15** terminals of the decade counters **Y121, Y122,** and the No. **6** terminal (reset) of the flip-flop **Y123** are all driven by the LOAD pulse terminal **PC2** of the program clock PC and are connected, together with the said terminal **PC2** through a resistor **R40** to the source of negative bias (−6V). The No. **14** terminal of the decade counter **Y121** is connected to the source of positive bias (+6V) as is the No. **5** terminal of the flip-flop **Y123.**

The No. **4** terminal (output) of the decade counter **Y121** is shown as driving the HOLD pulse terminal **PC5** and the No. **9** terminal (output) thereof is shown as driving the No. **3** terminal (input) of the flip-flop **Y123,** the output (No. **1** terminal) of the latter driving the No. **14** terminal (input) of the decade counter **Y122.**

The remaining outputs of the decade counter **Y121** (No. **7,** No. **10,** No. **1,** No. **5,** No. **6** and No. **11** terminals) and of the decade counter **Y122** (No. **3,** No. **2,** No. **4,** No. **7,** No. **10,** No. **1,** No. **5,** No. **6,** No. **9** and No. **11** terminals) may all be optionally connected with the input (No. **5** terminal) of the NAND gate **Y126,** the HOLD pulse terminal **PC5** and the input (No. **3** terminal) of the flip-flop **Y123** depending upon the number of color sorting units slaved to the central processor CPU and the requisite timing therebetween to correlate the data received from the given number of channels in each slaved unit.

The various signals driving the NAND gate **Y108,** including the output (No. **10** terminal) of the NAND gate **Y120** driving the No. **5** terminal of the NAND gate **Y108,** and the output (No. **3** terminal) of the EXCLUSIVE OR gate **Y112** driving the No. **4** terminal thereof, effect a MEMORY CLOCK No. **1** output **PC12** at the output (No. **10** terminal) of a NAND gate **Y128** (**CD4011** AE module of RCA), the inputs (No. **8** and No. **9** terminals) of the latter both being driven by the output (No. **6** terminal) of the said NAND gate **Y108.**

A SHIFT pulse output **PC3** from the program clock PC is provided as follows:

The output (No. **9** terminal) of the NAND gate **Y107** drives the inputs (No. **5** and No. **6** terminals) of a NAND gate **Y129** (**CD4011** AE module of RCA) and the inputs (No. **12** and No. **13** terminals) of a NOR gate **Y130** (**CD4001** AE module of RCA), the respective outputs (No. **4** and No. **11** terminals, respectively) of the NAND gate **Y129** and NOR gate **Y130** both driving the SHIFT pulse terminal **PC3.**

A SET NEW ADD pulse terminal **PC11** for the program clock PC is provided as follows:

The NAND gate **Y106** has its output (No. **10** terminal) driving both inputs (No. **1** and No. **2** terminals) of a NAND gate **Y131** (**CD4011** AE module of RCA), the output (No. **3** terminal) of the latter driving the SET NEW ADD pulse terminal **PC11.**

THE SERIAL MEMORY SM

Referring to FIG. **13,** the serial memory SM for the central processor CPU is shown as having a MEMORY CLOCK No. **1** input **PC12** which drives a switching stage consisting of two oppositely poled transistors **Q20**(**MPS6521**) and **Q21**(**MPS6523**) having their base terminals driven by the said input **PC12,** their collectors being connected to the positive and negative bias sources (+6V, −6V), respectively and their emmitters connected in common and comprising the MEMORY CLOCK No. **2** output **PC13.**

The MEMORY CLOCK No. **2** output **PC13** drives the No. **2** terminals of each of a plurality of serially connected 64-bit shift registers **Y32** through **Y47,** (**CD4031** AE modules of RCA) shown connected for a maximum of sixteen such shift registers depending upon the number of input channels to be associated with and controlled by the color sorter of the present invention, i.e., 4-channels per shift register for a maximum of 48 channels.

The No. **10** and No. **1** terminals of each of the shift registers **Y32–Y47** are connected to the source of negative bias (−6V), with the No. **6** terminal of each comprising the output to the input (No. **15** terminal) of the

next shift register or to the MEMORY OUT terminal LA1 as required.

The MEMORY IN terminal LA2 drives the input (No. 15 terminal) of the first 64-bit shift register Y32 to bring the required data into the serial memory SM. The MEMORY IN terminal LA2 is connected to the source of negative bias (−6V) through a resistor R41 to complete the serial memory circuit SM.

THE PROGRAM CLOCK PULSES

The various pulses from the program clock PC are functionally defined as follows and are shown in timed relationship with reference to FIG. 14:

LOAD (PC2): this is the first clock pulse in the control sequence which is initiated by the 120Hz pulses W from the power supply (to be more fully described hereinafter); and

instructs each of the shift registers ST3 to load the data in the shift registers ST1 and ST2 (i.e. load the coded data representing the output of the comparator 40B (see FIG. 4B).

SHIFT (PC3): this clock pulse shifts data around the series loop consisting of one or more shift registers ST3, the transfer register ST4, reject selection logic RSL, processor CPU and transfer register ST5 to thereby shift the data from each said shift register ST3, in turn, in to the eject selection logic circuit RSL.

120Hz (PC8): this clock pulse indicates that all computing cycles have been completed for a given piece of loaded data, that the computing has stopped, that all data is back in its correct place; and

that REJECT, UPDATE or FAST RESET actions should take place, as appropriate.

MEMORY CLOCK No. 1 and No. 2 (PC12 and PC13); these clock pulses shift data into and out of the 64-bit shift registers Y132–Y147 in the serial memory SM.

SET NEW ADD (PC11): This clock pulse shifts new memory data into a transfer register (to be more fully described hereinafter) for shifting said data into the memory under control of the MEMORY CLOCK.

A, B, C, D and E (from Y118): these represent five "numbers" which are held in the CPU that indicate the state of each optical channel OH and its associated color computer 40. These clocks select the appropriate action to be taken on old data to correct it into new data for the memory.

ACC RESET: this clock pulse clears the accessory register (to be more fully described hereinafter) for the next compute cycle.

40Hz (PC7): this clock is used to permit selective operations under its control for every third compute cycle.

SLOW CLOCK (PC9): this clock is used to permit selective operations under its control for one compute cycle every (3) seconds.

THE CENTRAL PROCESSING UNIT AND LOGIC ARRAY CPU(LA)

The performance of calculations for generating the operating signals for the accessory signals, reject mechanisms and the like and the final coordination of all of the color and clock data is by the central processing unit CPU and logic array LA which are shown in FIG. 15.

What has been generally described with reference to FIG. 4 as the control signal output PC1 from the program clock PC and the corresponding driven input LA3 of the logic array LA now comprises, in FIG. 15, the REJ (reject) and BKD (background) inputs (CPUL) from the output RSL3 of the front panel logic board FPLB and the shift input PC3, SLOW CLOCK input PC9, 40Hz input PC7, SET NEW ADD input PC11, MEMORY CLOCK No. 1 input PC12 and the A, B, C, D and E status number inputs (PC1 and LA3) from the program clock PC.

The logical manipulation of these various inputs in conjunction with the data from the serial memory SM appearing on the input LA1 controls the operation of the color sorter of the present invention.

The MEMORY CLOCK No. 1 (PC12) drives the No. 1 terminal and No. 9 terminal, respectively, of a CURRENT CALCULATION 8-bit shift register Y200 and a PREVIOUS CALCULATION 8-bit shift register Y201 (CD4015 AE modules of RCA); and the data from the serial memory SM enters the No. 15 terminal of the CURRENT CALCULATION register Y200, the latter terminal being connected through a resistor R50 to the source of negative bias (−6V).

A 4-bit CURRENT CALCULATION data word exits the register Y200 from the No. 2, No. 11, No. 12 and No. 13 terminals thereof, the No. 2 terminal driving the No. 7 terminal of the register Y201.

A 3-bit PREVIOUS CALCULATION data word exits in the register Y201 at the No. 3, No. 4 and No. 5 terminals thereof.

The No. 14 and No. 6 terminals, respectively, of the registers Y200 and Y201 are connected to the source of negative bias (−6V).

The outputs (No. 2, No. 11, No. 12 and No. 13 terminals) of the CURRENT CALCULATION register Y200 are applied to the inputs (No. 7, No. 5, No. 3 and No. 1 terminals, respectively) of a 4-bit adder Y202 (CD 4008 AE module of RCA), the latter having four outputs (No. 10, No. 11, No. 12 and No. 13 terminals) which drive, respectively, four inputs (No. 13, No. 8, No. 5 and No. 6 terminals) of an 8-bit shift register Y203 (CD4021 AE module of RCA) the latter having its No. 10 terminal driven by the MEMORY CLOCK No. 2 (PC13) as one constraint to shift the NEW DATA FROM CURRENT CALCULATION serially into the serial memory SM via the No. 2 terminal thereof which corresponds to the output terminal LA2 of the logic array LA previously described in FIG. 4. The No. 10 terminal is also connected to the source of negative bias (−6V) through a resistor R51, as are the No. 7 and No. 11 terminals.

The No. 2 terminal of the said NEW DATA' register Y203 also drives an input (No. 6 terminal) of a NAND gate Y204 (CD4011 AE module of RCA) which, through its output (No. 4 terminal) drives both inputs (No. 12 and No. 13 terminals) of a like NAND gate Y205, the output (No. 11 terminal) of the latter driving the No. 14 terminal of the NEW DATA' register Y203.

The other input (No. 5 terminal) of the NAND gate Y204 is driven by the output (No. 9 terminal) of a NAND gate Y206 (CD4023 AE module of RCA) the latter having its three inputs (No. 1, No. 2 and No. 8 terminals) driven, respectively, by a CLEAR DATA

line, the E-bit (No. 11 terminal) of the calculation number generator Y118, and the carry-out (No. 14 terminal) of the CURRENT DATA ADDER Y202.

Since the adder Y202 is driven by the CLEAR DATA and D-bit lines through a logic array (to be more fully described hereinafter) and the No. 9 terminal of the said adder Y202 is driven by an ADD "1" TO DATA line, all to effect clearing and handling of the current calculation data by the adder Y202, the general correlation between the said CURRENT DATA ADDER Y202 and the NEW DATA' register Y203 is more apparent.

The No. 9 terminal (input) of the NEW DATA' register Y203 is driven by the SET NEW ADD signal and the No. 7 and No. 11 terminals thereof are connected to the source of negative bias (−6V).

The remaining inputs (No. 6, No. 4, No. 2 and No. 15 terminals) of the CURRENT DATA ADDER Y202 are connected, respectively, with the outputs (No.4, No. 10, No. 11 and No. 3 terminals) of NOR gates Y207, Y208, Y209 and Y210 (CD 4011 AE modules of RCA); these NOR gates having input constraints as follows:

NOR gate Y207 has its No. 6 terminal driven by the No. 2 terminal of the CURRENT CALCULATION DATA register Y200 and its No. 5 terminal driven, as a function of the D-bit output (No. 7 terminal) of the calculation number generator Y118 and the CLEAR DATA signal, all via the output (No. 3 terminal) of a NOR gate Y211 (CD4001 AE module of RCA), the latter having its No. 1 terminal (input) driven by the said D-bit output (No. 11 terminal) of generator Y118 and its No. 2 terminal (input) driven by the No. 11 terminal (output) of a NAND gate Y212 (CD4011 AE module of RCA), the latter having both its inputs (No. 12 and No. 13 terminals) driven by the CLEAR DATA line.

The NOR gates Y208 and Y210 each have one input (No. 9 and No. 2 terminals, respectively) driven by the CLEAR DATA line and another input (No. 8 and No. 1 terminals, respectively) driven by the outputs (No. 11, and No. 13 terminals, respectively) of the CURRENT CALCULATION DATA register Y200.

The NOR gate Y209 is driven at its No. 13 terminal (input) by the CLEAR DATA line and at its No. 12 terminal (input) as a function of the D-bit and No. 12 terminal (output) of the CURRENT CALCULATION DATA register Y202, all via the output (No. 11 terminal) of a NOR gate Y213 (CD4001 AE module of RCA) having its No. 12 terminal (input) driven by the D-bit and its No. 13 terminal (input) driven by the No. 4 terminal (output) of an EXCLUSIVE OR gate Y214 (CD 4030 AE module of RCA), the latter having one input (No. 6 terminal) connected to the source of positive bias (+6V) and another input (No. 5 terminal) driven by the No. 12 terminal (output) of the CURRENT CALCULATION DATA register Y200.

The CLEAR DATA, ADD 1 TO DATA, control signals for each calculation are derived as a function of A-bit through E-bit, SLOW CLOCK (PC9) 40Hz clock (PC7), REJ and BKD signals and data from memory SM in three multiplexing switch means Y215, Y216 and Y217 (CD 4016 AE modules of RCA) by a variety of logic arrays and connections now to be described for the multiplexer Y215:

the No. 1 terminal is connected to the source of negative bias (−6V);

The No. 13, No. 5, No. 12 and No. 6 terminals are driven, respectively, by the A-bit, B-bit, C-bit and D-bit outputs (No. 2, No. 1, No. 3 and No. 7 terminals, respectively) of the calculation number generator Y118;

the No. 4 terminal is driven by the output (No. 4 terminal) of a NAND gate Y218 (CD4011 AE module of RCA), the latter having its No. 5 terminal (input) driven by the BKD signal and its No. 6 terminal (input) driven, through a resistor R52 by the 40Hz clock (PC7);

the No. 11 terminal driven by the output (No. 11 terminal) of a like NAND gate Y219, the latter having its No. 12 terminal (input) driven by the SLOW CLOCK (PC9) via a resistor R53 and its No. 13 terminal (input) driven by the output (No. 6 terminal) of a NAND gate Y220, having inputs (No. 3, No. 4 and No. 5 terminals) respectively connected to three outputs (No. 2, No. 11 and No. 12 terminals) of the CURRENT CALCULATION DATA register Y200;

the No. 8 terminal is connected to the source of negative bias (−6V); and

the No. 2, No. 3, No. 10 and No. 9 terminals (outputs) are connected to the source of negative bias (−6V) through a resistor R54 and drive the input (No. 1 terminal) of a NAND gate Y221 (CD 4011AE module of RCA) in conjunction with the No. 2 terminal of the second multiplexer Y216.

For the second multiplexer Y216:

the No. 13, No. 5, No. 6 and No. 12 terminals are driven, respectively, by the E-bit, A-bit, B-bit and C-bit outputs of the calculation number generator Y118;

the No. 3, No. 9 and No. 10 terminals, in conjunction with two outputs (No. 2 and No. 3 terminals) of the third multiplexer Y217 drive the other input (No. 2 terminal) of the NAND gate Y221, the output (No. 3 terminal) of the latter comprising the ADD 1 TO DATA line driving the No. 9 terminal of the CURRENT DATA ADDER Y202;

The No. 4 terminal is driven by the output (No. 10 terminal) of a NAND gate Y222 (CD 4011 AE module of RCA), the latter having both inputs (No. 8 and No. 9 terminals) driven by the BKD signal;

The No. 8 and No. 11 terminals driven by the output (No. 10 terminal) of a NAND gate Y223 (CD4023 AE module of RCA), the latter having its three inputs (No. 11, No. 13 and No. 12 terminals) driven by three outputs (No. 3, No. 4 and No. 5 terminals, respectively) of the PREVIOUS CALCULATION DATA register Y201; and

the No. 1 terminal driven by the output (No. 10 terminal) of a NOR gate Y224 (CD 4001 AE module of RCA) which receives a combination of inputs functionally related to the outputs of the PREVIOUS CALCULATION DATA register Y201, the CURRENT CALCULATION DATA register Y200 and the REJ signal as follows:

the REJ signal drives two inputs (No. 1 and No. 2 terminals) of a NAND gate Y225 (CD 4023 AE module of RCA), the latter having its output (No. 9 terminal) driving one input (No. 8 terminal) of the NOR gate Y224 and another input (No. 8 terminal) driven by the output (No. 10 terminal) of a NOR gate Y226 (CD4001 AE module of RCA), connected as an inverter, both inputs (No. 8 and No. 9 terminals) of the latter being driven by the output of a like NOR gate Y227 having its inputs (No. 13 and No. 12 terminals)

driven by two output (No. 12 and No. 13 terminals, respectively) of the CURRENT DATA CALCULATION REGISTER Y200;

The No. 5 terminal (output) of the PREVIOUS CALCULATION DATA register Y201 drives one input (No. 2 terminal) of a NAND gate Y228 (CD 4011 AE module of RCA) the latter having its output (No. 3 terminal) driving the other input (No. 9 terminal) of the NOR gate Y224; and

The No. 3 and No. 4 terminals (outputs) of the PREVIOUS CALCULATION DATA register Y201 drive the No. 6 and No. 5 terminals (inputs) respectively of a NOR gate Y229 (CD 4001 AE module of RCA), the output No. 4 terminal) of the latter driving the remaining input No. 1 terminal) of the NAND gate Y228.

For the third multiplexer Y217:

the No. 13 and No. 5 terminals are driven, respectively, by the D-bit and E-bit outputs of the computation number generator Y118;

The No. 8 terminal is driven by the output (No. 10 terminal) of the NAND gate Y223 (same logic as the No. 8 and No. 11 terminals of the second multiplexer Y216);

the No. 9 and No. 10 terminals comprise the O = TIME OUT signal output of a sample and hold latch and drive the No. 11 terminal through two inverters comprising NOR gates Y230 and Y231 (CD4001 AE modules of RCA) the former having both inputs (No. 5 and No. 6 terminals) driven by the said No. 9 and No. 10 terminals and its output (No. 4 terminal) driving both inputs (No. 1 and No. 2 terminals) of the latter, the output (3 terminal) of the latter (Y231) driving the said No. 11 terminal of the third multiplexer Y217;

the No. 1 terminal is driven by the output (No. 4 terminal) of a NOR gate Y232 (CD 4001 AE module of RCA) the latter having one input (No. 6 terminal) driven by the BKD signal and another input (No. 5 terminal) driven by a logic array as a function of the REJ signal, PREVIOUS CALCULATION DATA, and CURRENT CALCULATION DATA, as follows:

the output (No. 10 terminal) of an EXCLUSIVE OR gate Y233 (CD 4030 AE module of RCA) drives the No. 5 terminal of the NOR gate Y232 with the No. 9 (input) terminal of the said EXCLUSIVE OR gate Y233 being driven by the No. 12 terminal (output) of the CURRENT CALCULATION DATA register Y200 and the No. 8 terminal thereof being driven by the No. 10 terminal (output) of a NAND gate Y234 (CD 4011 AE module of RCA), the latter having one input (No. 8 terminal) driven by the REJ signal and one input (No. 9 terminal) driven by the output (No. 3 terminal) of a NOR gate Y235 (CD 4001 AE module of RCA), the latter having its inputs (No. 2 and No. 1 terminals) connected to two outputs (No. 4 and No. 5 terminals, respectively) of the PREVIOUS CALCULATION DATA register Y201;

the No. 4 terminal (of the third multiplexer Y217) is driven by the output (No. 10 terminal) of a NAND gate Y236 (CD 4023 AE module of RCA) as a function of the REJ signal and the PREVIOUS CALCULATION DATA as follows:

the NAND gate Y236 has its No. 12 and No. 13 terminals (inputs) driven by the No. 4 terminal (output) of the PREVIOUS CALCULATION DATA register Y201 and its other input (No. 11 terminal) driven by the output (No. 11 terminal) of an EXCLUSIVE OR gate Y237 (CD 4030 AE module of RCA), the latter having one input (No. 12 terminal) driven by the REJ signal and its other input (No. 13 terminal) driven by the No. 5 terminal (output) of the PREVIOUS CALCULATION DATA register Y201;

the No. 6 terminal (of the third multiplexer Y217) is driven by the output (No. 10 terminal) of a NAND gate Y238 (CD 4011 AE module of RCA) having its inputs (No. 8 and No. 9 terminals) both driven by the output (No. 4 terminal) of a like NAND gate Y239, the inputs (No. 5 and No. 6 terminals) of the latter being driven, respectively, by the SET NEW ADD signal and the D-bit output of the calculation number generator Y118; and

The No. 12 terminal (third multiplexer Y217) is also driven by the output (No. 4 terminal) of the said NAND gate Y239 as a function of the SET NEW ADD signal and D-bit.

Thus, among its other functions, the third multiplexer Y217 comprises a holding register for TIME OUT and FAST RESET information, these functions being determined by a history of previous calculations to determine if something in the color sorter requires attention. This condition is flagged by too many sequential rejections, too long off background and other unduly consistent conditions which indicate the need for a "TIME OUT" and a subsequent recalibration of the device, at which time a FAST RESET is required to recalibrate (store) the background color in the capacitors C6, C7 and C8 via the switch means SE1, SE2, SE3 and SE4 (see FIG. 4).

The computation control for the central processor CPU is effected by the computation control multiplexers Y215, Y216 and Y217, previously described, in conjunction with the program clock signals, REJ (reject) and BKD (background) condition signals, to circulate data in and out of the serial memory SM and control the contents of and operations in the CURRENT CIRCULATION DATA register Y200, the PREVIOUS CALCULATION DATA register Y201, the CURRENT DATA ADDER Y202 and the NEW DATA FROM CURRENT CALCULATION register Y203.

In addition to the data handling and computation functions, these computation control multiplexers Y215–Y217 in conjunction with the PREVIOUS and CURRENT CALCULATION DATA registers, REJ and BKD condition signals SET NEW ADD, CHANNEL COUNT and SHIFT signal, act through an output logic array, to drive the OUTPUT DATA register ST5 and an associated ACCESSORY STORAGE register to drive the serial DATA OUT terminal CPU2 of the central processor CPU.

The OUTPUT DATA register ST5 (CD4021 AE module of RCA) is an 8-bit shift register having its output (No. 3 terminal) driving the DATA OUT terminal CPU2 of the central processor CPU.

Inputs of the OUTPUT DATA register ST5 are driven as follows;

the No. 1 terminal is driven by the BKD condition signal and is connected to the source of negative bias (−6V) through a resistor R55;

the No. 15 terminal is driven by the output (No. 10 terminal) of a NAND gate Y240 (CD4011 AE module of RCA);

the No. 14 terminal is driven by the output (No. 11 terminal) of a like NAND gate Y241;

the No. 13, No. 4, No. 5, No. 6 and No. 7 terminals are connected to the source of negative bias (−6V);

the No. 9 terminal is driven by the SET NEW ADD signal (PC11);

the No. 10 terminal is driven by the SHIFT signal; and

the No. 11 terminal is driven by the output (No. 13 terminal) of the output flip-flop Y242 of the ACCESSORY STORAGE register Y242, Y243.

The ACCESSORY STORAGE register comprises two D type flip-flops Y242 and Y243 (CD4013 AE modules of RCA) interconnected and driven as follows:

For the flip-flop Y242:

the output (No. 13 terminal) drives the input (No. 11 terminal) of the OUTPUT DATA register ST5 as stated above;

the No. 10 terminal (reset) is driven by the CHANNEL COUNT signal from the channel counter Y124, Y125 (Pin 13 of Y125) in the program clock PC;

the No. 11 terminal (one input) is driven by the SHIFT signal (PC3);

the No. 9 terminal (other input) is driven by the output (No. 1 terminal) of the flip-flop Y243; and

the No. 8 terminal (set) is driven by the output (No. 4 terminal) of a NOR gate Y244 (CD4001 AE module of RCA).

For the flip-flop Y243:

the No. 4 terminal (reset) is driven by the CHANNEL COUNT signal;

the No. 3 terminal (one input) is driven by the SHIFT signal (PC3);

the No. 5 terminal (other input) is driven by the output (No. 13 terminal) of the flip-flop Y242; and

the No. 6 terminal (set) is driven by the output (No. 3 terminal) of a NOR gate Y245 (CD4001 AE module of RCA).

The logic arrays driving each of the NAND gates Y240 and Y241 and the NOR gates Y244 and Y245 are as follows:

For the NAND gate Y240:

one input (No. 8 terminal) is driven by the output (No 4 terminal) of a NAND gate Y246 (CD4011 AE module of RCA) the latter having a first input (No. 6 terminal) driven by a SOLENOID 18 (reject solenoid of FIG. 1) signal line extending from the output (No. 10 terminal) of a NOR gate Y247 (CD4001 AE module of RCA), with the inputs (No. 8 and No. 9 terminals) thereof driven, respectively, by the No. 11 terminal of the CURRENT CALCULATION DATA register Y200 and the output of the NOR gate Y226 (No. 10 terminal) and the other input (No. 5 terminal) of the NAND gate Y246 is driven by the output (NO. 10 terminal) of a NAND gate Y248 (CD4011 AE module of RCA) with its inputs (No. 8 and No. 9 terminals) both driven by the output (No. 4 terminal) of a like NAND gate Y249 having one input (No. 5 terminal) driven by the REJ condition signal (the REJ line being connected to the source of negative bias (−6V) through a resistor R56) and another input (No. 6 terminal) driven by a SOLENOID ON-OFF line (No. 5 terminal of the PREVIOUS CALCULATION DATA register Y201); and

another input (No. 9 terminal) driven by a like NAND gate Y250, the latter having one input (No. 2 terminal) driven by the output (No. 4 terminal) of the NOR gate Y230 (inverter) and another input (No. 1 terminal) driven by the output (No. 3 terminal) of a like NAND gate Y251, the latter having one input (No. 1 terminal) driven by the SOLENOID 18 signal line and another input (No. 2 terminal) driven by the output (No. 4 terminal) of the NAND gate Y249 as a function of the REJ and SOLENOID ON-OFF signals.

For the NAND gate Y241:

one input (No. 12 terminal) is driven by the output (No. 3 terminal) of the NAND gate Y251; and

another input (No. 13 terminal) is driven by the TIME OUT SIGNAL line from the No. 9 and No. 10 terminals of the third computation control multiplexer Y217.

For the NOR gate Y244:

one input (No. 6 terminal) is driven by the output (No. 11 terminal) of a NAND gate Y252 (CD4011 AE module of RCA) the latter having one input (No. 13 terminal) driven by the E-bit signal and another input (No. 12 terminal) driven by the SET NEW ADD signal; and

another input (No. 5 terminal) is driven by the output (No. 11 terminal) of a like NOR gate Y253 having a first input (No. 13 terminal) driven by the output (No. 4 terminal) of the NOR gate Y230 (inverter) and a second input (No. 12 terminal) driven by the output (No. 10 terminal) of another like NOR gate Y254, the latter having one input (No. 9 terminal) driven by the output (No. 1 terminal) of the ACCESSORY STORAGE flip-flop Y243 and another input (No. 8 terminal) driven by the output (NO. 4 terminal) of the NAND gate Y246.

For the NOR gate Y245:

one input (No. 2 terminal) is driven by the output (No. 4 terminal) of the NAND gate Y239 as a function of the D-bit and SET NEW ADD signals; and

another input (No. 1 terminal) is driven by the output (No. 3 terminal) of a NAND gate Y255 (DC4011 AE module of RCA) the latter having its No. 1 and No. 2 terminals (inputs) driven, respectively, by the No. 4 and No. 5 terminals (outputs) of the PREVIOUS CALCULATION DATA register Y201.

For the NAND gate Y251, one input (No. 1 terminal) is driven by the output (No. 10 terminal) of Y247 and the other input (No. 2 terminal) is driven by the output (No. 4 terminal) of Y249.

THE ANALOG BOARD IN DETAIL (COLOR COMPUTER 40)

Referring to FIG. 16, the analog board comprising the color computer 40 and its associated update and reset logic will now be described, with like elements to those in FIG. 4 bearing like numerals.

In FIG. 16, the sequencing switch means SA1–A3, SB1–B4, SD1–D4 and SE1–E4 are controlled by and integral with, in respective groups, multiplexing modules Y(A), Y(B), Y(C), Y(D) and Y(E) (all CD4016 AE modules of RCA). The sequencing switch means are shown in their basic positions in the circuit with appropriate in and out terminal pin numbers associated with their respective multiplexing modules (by like suffices).

Te multiplexing modules Y(A) – Y(E) are driven by the sequence control outputs SSA1–A3, SSB1–B3, SSC1, etc., from the front panel logic board FPLB, as follows:

Multiplexer	Terminal No.	Sequence Control Output
Y(A)	13	SSA1
	5	SSA2
	6	SSA3
	12	+6V
Y(B)	13	SSB1
	5	SSB1
	6	SSB3
	12	SSB3
Y(C)	13	SSC1
	5	SSC2
	6	SSC3
	12	SSC4
Y(D)	13	SSD1
	5	SSD2
	6	*f*(SSC4,SSD2)
	12	*f*(UPDATE-RESET LOGIC)
(where *f*() is "a function of")		
Y(E)	13	SSE1
	5	SSE2
	6	SSE3
	12	*f*(UPDATE-RESET LOGIC)

The sequencing switch means integral (by suffix) with the foregoing multiplexing modules have the following IN and OUT terminal numbers in those modules:

Sequence Switch Means	IN Terminal No.	OUT Terminal No.
SA1	1	2
SA2	4	3
SA3	8	9
SA4	10	11
(to be more fully described)		
SB1	3	4
SB2	2	1
SB3	9	8
SB4	10	11
SC1	2	1
SC2	3	4
SC3	9	8
SC4	10	11
SD1	1	2
SD2	4	3
SD3	9	8
SD4	10	11
SE1	1	2
SE2	4	3
SE3	8	9
SE4	10	11

The sequence switch **SA4** is driven by the source of positive bias (+6V) and is an in-line switch means in the common ground connection of **SB2** and **SB4** for the purpose of balancing impedance in the circuits involved. It has no other function.

In the multiplexing module Y(B) the No. **5** terminal is driven by the $\overline{\text{SSB1}}$ control terminal through both inputs (No. **8** and No. **9** terminals) of a NOR gate **Y(B2)** (**CD4001** AE module of RCA) connected as an inverter, the output (NO. **10** terminal) of the latter driving the said No. **5** terminal; and the No. **12** terminal is driven by the **SSB3** control terminal through both inputs (No. **5** and No. **6** terminals) of a like NOR gate Y(B4) connected as an inverter, the output (No. **4** terminal) of the latter driving the said No. **12** terminal.

A number of the inputs of the multiplexing modules Y(A) – Y(E) are connected to the source of negative bias (−6V) through individual resistors, as follows:

Module	Terminal No.	Resistor
Y(A)	13	R60
	5	R61
	6	R62
Y(B)	13	R63
	6	R64
Y(C)	13	R65
	5	R66
	6	R67
	12	R68
Y(D)	13	R69
	5	R70
Y(E)	13	R71
	5	R72
	6	R73

The sequence control terminals **SSC4** and **SSD2** drive the No. **6** terminal of the multiplexing module Y(D) through the following logic network:

SSC4 drives both inputs (NO. **1** and No. **2** terminals) of a NOR gate **Y(D1)** (**CD4001** AE module of RCA), connected as an inverter, with its output (No. **3** terminal) driving one input (No. **12** terminal) of a like NOR gate **Y(D2)**; and

SSD2 drives the other input (No. **13** terminal) of the NOR gate **Y(D2)**, the output (No. **11** terminal) of the latter driving the No. **6** terminal of the multiplexing module Y(D).

The operational amplifiers **Q4, Q5** and **Q6** in the color input circuits and the operational amplifier **Q10** in the integrator circuit **40A**, (all commercially available **SN72558L** amplifier modules of Texas Instruments) have the following (+) and (−) inputs, and output terminal numbers:

Amplifier	(+) Input No.	(−) Input No.	Output No.
Q4	5	6	7
Q5	3	2	1
Q6	5	6	7
Q10	3	2	1

The calibration sequence switches **SE1, SE2** and **SE3** have their No. **2**, No. **3** and No. **9** terminals connected to the source of negative bias (−6V) through, respectively, resistors **RE1, RE2** and **RE3**. The associated sequence switch **SE4** has its No. **10** terminal driven from a junction **JE4** between two series resistors **RE4A** and **RE4B**, the latter having one side thereof connected to the source of negative bias (−6V) and the former having one side driven from one terminal of a field effect transistor **QE4**, the said transistor QE4 having its gate terminal driven from the common line **CL1A** extending from the resistor **R12** and the No. **11** terminal of the fast reset control switch **SD4** and the other terminal thereof connected to the source of positive bias (+6V).

The common line **CL1A** drives one terminal of each of the field effect transistors **QE1, QE2, QE3**, having their gate terminals driven, respectively, by the No. **2**,

No. 3 and No. 9 terminals of the calibration sequence switches SE1, SE2 and SE3 and their remaining terminals driving respectively, the calibration capacitors C6, C7 and C8 and the gate terminals of the field effect transistors Q7, Q3 and Q9 previously described with reference to FIG. 4.

The inputs, No. 6 and No. 2 and No. 6 terminals, respectively, of the operational amplifiers Q4, Q5 and Q6 receive incoming color signals through coupling resistors RA1, RA2 and RA3, respectively; and th outputs No. 7, No. 1 and No. 7 terminals are respectively coupled to those said inputs by capacitors CA1, CA2 and CA3.

The first and second shift registers ST1 and ST2 (CD4015 AE modules of RCA) at the outputs 40BS1 and 40BS2, respectively, of the comparator 40B, are connected to the analog board circuit as follows:

In the shift register ST1:

the No. 7 terminal (data input) is driven by the comparator output 40 BS1;

the No. 9 terminal (clock input) is driven by the sequence control terminal SSD2 of the sample switch SD2;

the No. 6 terminal is connected to the source of negative bias (−6V); and

the No. 4, No. 3 and No. 10 terminals (3-bit output ST1A) drive, respectively, the No. 13, No. 5 and No. 7 terminals (3-bit input ST3A) of the third shift register ST3 (CD4021 AE module of RCA).

In the shift register ST2:

the No. 15 terminal (data input) is driven by the comparator output 40BS2;

the No. 1 terminal (clock input) is driven by the sequence control terminal SSD2 of the sample switch SD2; and

the No. 12, No. 11 and No. 2 terminals (3-bit output ST2A) drive, respectively, the No. 14, No. 4 and No. 6 terminals (3-bit input ST3B) of the third shift register ST3.

In the shift register ST3:

the No. 11 terminal (serial data input ST3E) is driven by the output CPU2 of the CPU(ST5) and is connected to the source of negative bias (−6V) through a resistor R74;

the No. 9 terminal (input ST3F) is driven by the LOAD clock signal (PC2) from the program clock PC;

the No. 10 terminal (input ST3G) is driven by the SHIFT clock signal (PC3) from the program clock PC:

the No. 15 terminal is connected to the source of negative bias (−6V):

the No. 1 and No. 3 terminals (serial data output ST3D) drive the DATA IN terminal (via ST4) of the reject select logic RSL (FIG. 6): and

the No. 2, No. 12 and No. 1 (No. 3) terminals comprise the 3-bit update-reject logic driver output ST3C of the shift register ST3 as will be more fully described hereinafter.

The UPDATE-REJECT logic UL-RL is driven by the 3-bit output ST3C of the shift register ST3 and the 120Hz clock signal (PC8) as follows:

the 120Hz clock (PC8) drives one input (No. 11 terminal) of a flip-flop Y260 (CD4013 AE module of RCA), one input (No. 3 terminal) of a like flip-flop Y261 and one input (No. 1 terminal) of a NAND gate Y262 (CD4011 AE module of RCA) to comprise the clock input UL1-RL1 of the UPDATE-REJECT logic UL-RL;

the No. 2 terminal (ST3C) drives the data input (No. 9 terminal) of the flip-flop Y260;

the No. 12 terminal (ST3C) drives the data input (No. 5 terminal) of the flip-flop Y261; and

the No. 1 terminal (ST3C) drives the other input (No. 2 terminal) of the NAND gate Y262.

The flip-flop Y260 has its No. 8 and No. 10 terminals connected to the source of negative bias (−6V).

The flip-flop Y261 has its No. 4 and No. 6 terminals connected to the source of negative bias (−6V).

The outputs of the flip-flops Y260 and Y261 drive a NAND gate Y263 (CD4011 AE module of RCA) and two NOR gates Y264 and Y265 (DC4001 AE modules of RCA) as follows:

one output (No. 13 terminal) of the flip-flop Y260 drives one input (No. 12 terminal) of the NAND gate Y263 and one input (No. 13 terminal) of the NOR gate Y265, while the other output (No. 12 terminal) of the flip-flop Y260 drives one input (NO. 1 terminal) of the NOR gate Y264; and

one output (No. 1 terminal) of the flip-flop Y261 drives one input (No. 13 terminal) of the NAND gate Y263 and one input (No. 2 terminal) of the NOR gate Y264, while the other output (No. 2 terminal) of the flip-flop Y261 drives the input (No. 12 terminal) of the NOR gate Y265.

The 120 Hz line PC8, LOAD line PC2 and SHIFT line PC3 are connected through resistors R76, R77 and R78, respectively, to the source of negative bias (−6V).

The output (No. 11 terminal) of the NAND gate Y263 drives the No. 12 terminal (input) of the multiplexing module Y(D) to control the FAST RESET sequence switch SD4, via both inputs (No. 8 and No. 9 terminals) of a NAND gate Y(D4) (CD4011 AE module of RCA) the output (No. 10 terminal) of the latter being directly connected to the said No. 12 terminal of the multiplexer Y(D); and further, the said No. 11 terminal of the NAND gate Y263 drives one input (No. 5 terminal) of a like NAND gate Y266, the latter having its other input (No. 6 terminal) driven by the output (No. 3 terminal) of the NAND gate Y262.

The output (No. 4 terminal) of the NAND gate Y266 drives a light emitting diode LED (XC-308) which is connected through a resistor R75 to the source of negative bias (−6V); and also drives the No. 12 terminal on the multiplexer Y(E) to control the actuation of the update control switch SE4.

The diode LED comprises a STATUS lamp which operates in the following modes to indicate the following conditions:

CONDITION	MODE
FAST RESET	BRIGHT
SATISFACTORY	DIM
OFF BACKGROUND	OFF

The No. 3 and No. 11 terminals (outputs) of the NOR gates Y264 and Y265, respectively, comprise the reject logic output 16 (FIG. 4) and drive, respectively, the input terminal pair No. 5 and No. 6 of a like NOR gate Y267 and the input terminal pair No. 8 and No. 9 of a like NOR gate Y268, both connected as inverters. The outputs (No. 4 and No. 10 terminals, respec-

tively) of the NOR gates Y267 and Y268 drive the No. 3 and No. 2 terminals (inputs), respectively, of a dual optical coupler Y269 (MCT2D module of Monsanto).

The UPDATE-REJECT functions are coded by the output ST3C of the shift register ST3 by the following bit patterns on the No. 2, N0. 12 and No. 1 (No. 3) terminals:

FUNCTION	TERMINAL No. 2	TERMINAL No. 12	TERMINAL No. 1 (No. 3)
UPDATE	0	0	1
FAST RESET	1	1	0
TURN ON SOLENOID 18	0	1	0
TURN OFF SOLENOID 18	1	0	0
SIT	0	0	0

The optical coupler Y269 couples the reject select output 16 through a driver circuit to the input 16A of the driver circuit for the solenoid 18 as follows:

the No. 4 terminal of the optical coupler Y269 is connected to the source of positive bias (+6V) through a resistor R79;

The No. 6 terminal is connected to a first alternating current power lead AC1;

the No. 5 terminal of the coupler Y269 drives the No. 5, No. 6, No. 8 and No. 9 terminals of a NOR gate module Y270 (CD4001 AE module of RCA), the latter having its No. 14 terminal connected to the power lead AC1 and its No. 4 and No. 10 terminals both driving the gate electrode of a triac 271 through a resistor R80, and the said No. 5 terminal of the coupler Y269 is connected through a resistor R81 and DC rectifying circuit to the other alternating current power lead AC2 which, with power lead AC1, comprises an alternating current power supply; and

the No. 7 terminal of the coupler Y269 is connected to the power lead AC1 and the No. 8 terminal thereof is connected to the power lead AC2 through a resistor R82 and a DC rectifying circuit and also drives the No. 1, No. 2, No. 12 and No. 13 terminals of the NOR gate module Y270, the latter having its No. 7 terminal driven by the power lead AC2 and having its No. 3 and No. 11 terminals both driving the gate electrode of a second triac Y272 (40535) through a resistor R83.

The first triac Y271 has an input terminal driven by the first power lead AC1 and an output terminal comprising the SOLENOID 18 OFF control terminal.

The second triac Y272 has an input terminal driven by the first power lead AC1 and an output terminal comprising the SOLENOID 18 ON control terminal.

The alternating current is half-wave rectified and suitably smoothed by diode RD1 (IN4004) in-line with the second power lead AC2; an in-line resistor R84 having one end connected to the anode of the diode RD1; a Zener diode RD2 (IN5245) having its anode connected to the other end of the resistor R84 and the second power lead AC2 and its cathode connected to the first power lead AC1; and a capacitor C80 connected across the second diode DR2.

THE POWER SUPPLY

The power supply for the color grader of the present invention is shown in FIG. 17 as comprising a 60Hz alternating current source AC driving a transformer TP with two secondary windings ST1, and ST2, driving, respectively, first and second full wave rectifier modules FWR1 and FWR2 (10DPB1 modules) with first and second capacitors CP1 and CP2, respectively, connected across the output terminals of the said rectifiers FWR1 and FWR2.

A resistor RP1 is connected across the outputs of the second rectifier FWR2 and a blocking diode DP1 is connected from the negative node of the capacitor CP2 to the negative node of the resistor RP1 with its forward direction into the negative output (−) terminal of the second rectifier FRW2. With this configuration, the negative (−) terminal of the second rectifier FRW2 comprises the source of the synchronizing signal W applied to the input of the program clock PC as shown in FIG. 11 to drive the Schmitt trigger circuit Y80–Y81.

The positive (+) output terminals of the first and second rectifiers FWR1 and FWR2 drive the inputs (I1 and I2 terminals) of first and second voltage regulator modules VR1 and VR2 (7806 modules) respectively, the control outputs (G1 and G2) of the said regulators being driven by the negative (−) terminals of the said rectifiers FWR1 and FWR2, respectively.

The output 01 of the first voltage regulator VR1 comprises the source of positive bias (+6V).

The output 02 of the second regulator VR2 comprises the ground for the analog board (color computer 40, integrator 40A, comparator 40B).

The anode side of the blocking diode DP1 (negative node of capacitor CP2) comprises the source of negative bias (−6V).

All components previously described such as Q10 or Y260 are connected to this +6 and −6 volt source per their manufacturers instructions.

A first smoothing capacitor CP3 is connected across the output and control terminals 01 and G1 of the first regulator VR1 and a second smoothing capacitor CP4 is connected across the output and control terminals 02 and G2 of the second regulator VR2.

The 60Hz source AC also drives the first and second alternating current power leads AC1 and AC2 previously shown and described in reference to FIG. 16.

THE ACCESSORY CONTROL LOGIC

The accessory control logic ACL selectively controls the activation of a BLOW-OFF device for clearing the background plate S of stuck leaves and other debris, a TIME CLOCK which indicates the amount of time that a given color grader is actually performing grading operations regardless of actual on time, and an ALARM device which is actuated by the occurrence of a FAST RESET condition.

Referring to FIG. 18, the accessory control logic ACL is driven as a function of the accessory data in the accessory storage register Y242–Y243 in the central processor CPU via the output CPU2 of the latter through the DATA IN terminal of ACL, the SHIFT clock (PC3), the 12OHz clock (PC8), the SLOW clock (PC9) and a MANUAL ALARM RESET button (mounted on the front control panel).

The logic ACL is applicable, as shown, to four (4) channels, i.e., four optics systems OH and associated color computers (four analog cards) of the color comparator and is responsive to CPU data outputs for all four of these channels.

The DATA IN terminal receives the accessory information bits from the accessory storage Y242–Y243 and the shift register ST5 (output CPU2) the CPU under control of the SHIFT clock (PC3) which generates 9th and 10th clock pulses in addition to its regular 8-bit pulse group on every fifth SHIFT clock cycle as shown in FIG. 14. These 9th and 10th bits constitute the SHIFT clock pulses for the accessory logic ACL.

A data transfer buffer and accessory data holding register is provided by a configuration of four flip-flops Y281, Y282, Y283 and Y284 (CD4013 AE modules of RCA), with the DATA IN and SHIFT clock (PC3) driving the data and clock inputs (No. 9 and No. 11 terminals), respectively, of the first shift register Y281. The first and second flip-flops Y281, Y282 transfer data to the shift register ST3 from the CPU and the third and fourth flip-flops Y283, Y284 comprise the accessory data holding register.

An output (No. 13 terminal) of the first flip-flop Y281 drives the data inputs (No. 5 and No. 9 terminals, respectively) of the second and third flip-flops Y282 and Y283, the said flip-flop Y282 having its clock input (No. 3 terminal) driven by the SHIFT clock (PC3), the latter being connected to the source of negative bias (−6V) through a resistor R90.

The 120Hz clock (PC8) is connected to the source of negative bias (−6V) through a resistor R91 and drives the clock inputs (No. 11 and No. 3 terminals, respectively) of the third and fourth flip-flops Y283 and Y284. This clock (120Hz) loads the accessory bits into the accessory holding register Y283–Y284.

The DATA IN terminal is connected to the source of negative bias (−6V) through a resistor R92.

An output (No. 1 terminal) of the second flip-flop Y282 drives the data input (No. 5 terminal) of the fourth flip-flop Y284 and the input terminal ST3E of the shift register ST3, the latter driving the UPDATE-REJECT logic UL-RL in FIGS. 4 and 15.

The No. 10 and No. 4 terminals (reset) of the first and second flip-flops Y281 and Y282, and the No. 8 and No. 6 terminals (set) and No. 10 and No. 4 terminals (reset) of the third and fourth flip-flops Y283 and Y284, respectively, are all connected to the source of negative bias (−6V), as are the No. 8 and No. 6 terminals (set) of the first and second flip-flops Y281 and Y282, respectively.

THE BLOW-OFF ACCESSORY DRIVE

The BLOW-OFF accessory function is generated from the No. 12 and No. 1 terminals (outputs) respectively, of the third and fourth flip-flops Y283 and Y284 which drive, respectively, the No. 2 and No. 1 terminals (inputs) of a NOR gate Y285 (CD4001 AE module of RCA) the output (No. 3 terminal) of the latter driving the input (No. 1 terminal) of a single optical coupler Y286 (MCT2D module of Monsanto).

The No. 2 terminal of the coupler Y286 is connected to the source of negative bias (−6V) through a resistor R93; the No. 7 terminal (output) of the coupler Y286 drives the No. 14 terminal of a NOR gate module Y287 (CD4025) AE Module of RCA); and the No. 8 terminal (output) of the coupler Y286 drives the No. 1, No. 2 and No. 8 terminals of the module Y287 and is connected through a resistor R94 and a DC rectifying circuit to the power lead AC2.

The No. 9 terminal (output) of the NOR module Y287, through a resistor R95, drives the gate electrode of a triac Y288 (40535) having one power terminal connected to the power lead AC1 and the other power terminal connected through the BLOW-OFF accessory to the power lead AC2. The No. 14 terminal of the NOR Module Y287 is connected to the power lead AC1.

THE TIME CLOCK AND ALARM ACCESSORY DRIVES

A count-to-32 counter Y289 (CD4024 AE module of RCA) is provided with the following connections:

The No. 2 terminal (reset) is driven from the No. 1 terminal (output) of the fourth flip-flop Y284;

the No. 4 terminal (output) drives both inputs (No. 5 and No. 6 terminals) of a NOR gate Y290 (CD4001 AE module of RCA), drives one input of a like NOR gate Y291, the other input of the latter being driven by the SLOW CLOCK input PC9 and the output thereof driving the No. 1 terminal of the counter Y289;

the No. 4 terminal of the counter Y289 further driving one input (No. 4 terminal) of a NOR gate Y292 (CD4025 AE module of RCA), the latter having another input (No. 5 terminal) driven by the MANUAL ALARM RESET input, the latter being connected to the source of negative bias (−6V) through a resistor R97.

The NOR gate Y292 has its output (No. 6 terminal) driving one input (No. 1 terminal) of a NOR gate Y293 (CD4001 AE module of RCA) the latter having its output (No. 3 terminal) driving the remaining input (No. 3 terminal) of the NOR gate Y292 as well as an input (No. 9 terminal) of a like NOR gate Y294.

The other input (No. 2 terminal) of the NOR gate Y293 and an input (No. 5 terminal) of a like NOR gate Y295 (the other input (No. 6 terminal) of the latter being driven by the SLOW CLOCK PC9) which is also connected to a source of bias −6V through a resistor R96, are driven by the output (No. 11 terminal) of a like NOR gate Y296, the latter having its No. 12 and No. 13 terminals (inputs) driven, respectively, by the No. 1 and No. 2 terminals (outputs) of the fourth flip-flop Y284.

The output (No. 4 terminal) of the NOR gate Y295 drives, through a timing resistor RMA and circuit node MA, the other input (No. 8 terminal) of the NOR gate Y294.

The ALARM accessory timing circuit (MA), to effect a blinking or flashing condition of the ALARM, includes a diode DMA with its anode at the junction MA and its cathode at the output (No. 4 terminal) of the NOR gate Y295 (parallel to the resistor RMA) and a timing capacitor CMA connected from the junction MA to the source of negative bias (−6V). Thus, the presence or absence of a charge on the timing capacitor CMA controls the state of the NOR gate Y294 to provide a delay in the turn off of the ALARM accessory to allow it to be seen.

The output (No. 10 terminal) of the NOR gate Y294 drives one input (No. 9 terminal) of like NOR gate Y297, the other input (No. 8 terminal) of the latter being driven by one output (No. 13 terminal) of the third flip-flop Y283, and the output (No. 10 terminal) of the said NOR gate Y297 driving both inputs (No. 12 and No. 13 terminals) of a like NOR gate Y298, the output (No. 11 terminal) of the latter driving the ALARM input (No. 1 terminal) of a dual optical coupler Y299 (MCT2D module of Monsanto).

The TIME CLOCK Input (No. 4 terminal) of the dual optical coupler Y299 is driven by the output (No. 4 terminal) of the NOR gate Y290.

The No. 3 and No. 4 terminals of the dual coupler Y299 are connected to the source of negative bias (−6V) through resistors R98 and R99, respectively.

The No. 6 terminal of the optical coupler Y299 is connected to the power lead AC1 and the No. 7 terminal thereof is connected to the power lead AC1 through a resistor R100.

The No. 5 terminal of the coupler Y299 is connected to the power lead AC2 through a resistor R101 and a DC rectifying circuit and also drives the No. 3, No. 4 and No. 5 terminals (inputs) of the NOR gate module Y287, thereby effecting a TIME CLOCK control signal at the No. 6 terminal (output) of the latter which, through a coupling resistor R102 drives the gate electrode of a triac Y300, the latter having one power terminal connected to the power lead AC1 and the other power terminal connected to the power lead AC2 through the TIME CLOCK accessory.

The No. 8 terminal of the dual coupler Y299 and the power lead AC2 are both connected to the No. 7 terminal of the NOR gate module Y287 through a DC rectifying circuit.

The No. 7 terminal of the dual coupler Y299 drives the No. 11, No. 12 and No. 13 terminals of the NOR gate module Y287, the No. 10 terminal (output) of the latter, through a coupling resistor R103, driving the gate electrode of a third triac Y301, the latter having one power terminal connected to the power lead AC1 and the other power terminal connected to the power lead AC2 through the ALARM accessory.

The NOR gate module Y287 thus contains internal modules Y287A, Y287B and Y287C which serve as driver amplifiers for the BLOW-OFF, TIME CLOCK and ALARM accessories, respectively.

The output terminals (No. 13 terminals of first and third flip-flops Y281 and Y283 and No. 1 terminals of second and fourth flip-flops Y282 and Y284) effect the following accessory functions with the following bit patterns:

GRADER CONDITION	Terminal No. 13	Terminal No. 1	FUNCTION
GRADING	0	1	TIME CLOCK: ON (RESET Y289) ALARM: ON/BLINK BLOW-OFF: OFF
BLOW	1	0	BLOW-OFF: ON ALARM: OFF TIME CLOCK: OFF
RESET	1	1	TIME CLOCK: ON (RESET Y289) ALARM: OFF BLOW-OFF: OFF
SITTING	0	0	ALARM: ON/BLINK TIME CLOCK: OFF

The power lead AC2 includes a half-wave rectifier HWR and series resistor R104 between the source AC and a circuit node ACN In the said power lead AC2, a Zener diode ZD and smoothing capacitor CP5 are connected from the node ACN to the other power lead AC1 to complete the power circuit for the accessory logic ACL.

ACCESSORY FUNCTIONS DEFINED

The ALARM accessory may comprise a lamp such as schematically shown in FIG. 18.

In order for the color grader to operate properly the optics head OH must see the background plate S between the leaves for very brief moments in order to update its memory of the background color. Should a leaf become lodged on the background for a period of 30 seconds, the SIDE-BLOW accessory will automatically activate to remove this obstruction from the background plate S.

In the event that the SIDE-BLOW accessory fails to clear the background plate S in 3 seconds, the ALARM accessory lamp will extinguish.

The grader will then recalibrate to the color which is present on the background plate S (obstructed) and the ALARM accessory lamp will come on flashing. This flashing mode of the ALARM indicates to an operator that the color grader has gone through its calibration cycle while grading and that a check of the apparatus should be made.

Now, when the operator checks the grader and finds the obstructed background plate S, he will clear the obstruction and observe the operation of the unit for a moment.

The clearing of the obstruction will change the background color seen by the optics head OH and the grader will accordingly be constrained to undergo another calibration cycle (either automaticaly or manually by pushing the recalibrate button), the initiation of the latter being denoted by the activation of the SIDE-BLOW accessory and the extinguishing of the ALARM accessory lamp.

When recalibration is complete, the ALARM will be energized intermittently to casue the ALARM lamp to come on flashing. Now, if the MANUAL ALARM RESET input (button on the front control panel FCP) is energized the ALARM lamp will cease flashing but remain ON, indicating to the operator that the grader is properly recalibrated and in the GRADING or SITTING (on but not grading) mode.

Alternatively, if the operator finds no obstruction and the grader is otherwise working properly, proper recalibration has taken place and the MANUAL ALARM RESET input in this situation is energized to stop the ALARM lamp from flashing.

A FOUR CHANNEL SYSTEM

With the foregoing details of the several circuit blocks and components of the color grader of the present invention having been described with reference to FIGS. 1–18, a four channel system controlled by a common front control panel 30 and central processor CPU (control circuit 50) will now be described with reference to FIG. 19.

The analog board comprising each of the channels (CHANNEL No. 1–No. 4) has previously been described in detail with reference to FIG. 16.

The common interconnection correlating to flow of data to and from CHANNEL No. 1–No. 4 is the data loop ST3, ST4, ST5 and the DATA BUFFER Y28-1–Y282, the latter being associated with the accessory logic ACL as previously described with reference to FIG. 18.

Each CHANNEL No. 1–No. 4 has its individual 8-bit shift register ST3 No. 1, ST3 No. 2, ST3 No. 3 and ST3

No. 4, all of which are connected in series between the DATA BUFFER (Y281–Y282) and the 8-bit shift register ST4 which provides the input to the REJECT SELECTION LOGIC RSL. As previously described, the DATA BUFFER receives the UPDATE, REJECT and ACCESSORY data from the output CPU2 (10-bit shift register ST5) of the central processor CPU and transfers the UPDATE and REJECT data through the ST3 modules to the several CHANNELS No. 1–No. 4 and transfers the ACCESSORY data bits in to the HOLD ACCESSORY DATA register Y283–Y284 in the accessory logic ACL.

Thus, the ACCESSORY functions are commonly performed for all CHANNELS No. 1–No. 4 as are all of the computations, with the requisite data all circulated in the same serial data loop ST3 No. 1–No. 4, ST4, RSL, CPU, SM, CPU, ST5 and DATA BUFFER Y281–Y282, in that order.

As previously described, the CHANNELS No. 1–No. 4, are coordinated by the clock pulses from the program clock PC as illustrated by the pulse timing diagram of FIG. 14.

The relationship of the Brightness, Greenness, Redness and Update calculation periods to the 120Hz half-cycles (W) from the power supply are shown in FIG. 20. Further, the Zero, Red, Green, Infra-Red and Sample subdivisions for each of the calculation periods is shown together with the relationship of the sequencing switches SA1-A3, SB1-B4, SD1, SD2 and SE1-E4 to these subdivisions is shown. The timing of the various sequencing switches is shown in FIG. 22.

COLOR CALCULATION

As previously described, the purpose of the color computers 40, on the analog boards for each of the CHANNELS No. 1–No. 4, is to calculate the function $rR+fF+iI$, where R, F and I are the three colors Red, Green and Infrared, respectively, and r, f and i are their respective Scalar factors selected by the front control panel 30 and its related logic board FPLB.

To perform the calculation, for each of CHANNELS No. 1–No. 4, with reference to FIGS. 4, 16 and 19, the color sequence switches SA1, SA2 and SA3 are closed in succession to alternately present the color signals RS, FS and IS to the scalar multiplier switches SB1–B2 and SB3–B4.

The scalar multiplier switches SB1–B2 and SB3–B4 then modulate each of the color signals by the scalar factors r, f and i and present then to the integrator portion 40A(Q10, C5, R6) of the color computer 40 for summation. Zero sequence switch SD1 is used to set the integrator 40A at zero before the summation and sample sequence switch SD2 is closed during the summation.

The modulation of the color signals by the said scalar multiplier switches SB1–B2 and SB3–B4 is effected by varying the time periods of the connection of the respective color signals to the integrator 40A.

For example, if the scalar factor is zero, SB1 and SB3 would be open and SB2 and SB4 would be closed for the duration of a given color signal. If a scalar factor is one (1), then SB1 and SB4 would be closed and SB2 and SB3 would be open for the duration of a given color signal. If a scalar factor is one-half (½) then SB1 would be closed for the first half of the color signal duration and SB4 would be closed for the second half (or vice versa). The scalar multiplier switches SB2 and SB4 are compliments, respectively, of SB1 and SB3 such that when SB1 is closed SB2 is open, when SB3 is closed SB4 is open and vice-versa.

To obtain a scalar factor of minus one (−1), SB1 would be open and SB3 would be closed for the duration of the given color signal. Therefore, scalar modulation factors for a given color signal ranging from (−1) to (+1) can be obtained from the sequencing of the said scalar multiplier switches SB1–B2 and SB3–B4.

Since the source of illumination L for the optics heads (OH) are subject to the 120Hz ripple from the alternating current power supply, the effects of this ripple are eliminated by performing a given integration (summation) function once in each of the alternate half cycles of the 120Hz waveform. It is also necessary to provide a means of eliminating the effect of offset in the integrator amplifier Q10 (FIGS. 4 and 16) in the color computer 40A and to provide a means of sampling the integrated voltage that appears at the output 40A3 of the said amplifier Q10 after each calculation.

The first set of calculations of the function $rR'+fF'+iI'$ is stored on one of the capacitors C1 through C4 under the control of the storage sequence switches SC1–SC4, respectively, directly from the said output 40A3 through the now closed sample switch SD2.

For the second set of calculations, the logic controlling the scalar multiplier switches SB1–B2 and SB3–B4 is reversed so that the respective functions calculated in the next half cycle of the 120Hz waveform is $-rR'-fF'-iI'$ and is stored on the integration capacitor C5.

Now, to effect a sampling of a given resultant calculation, the sample switch SD2 is opened and the appropriate storage switch SC1–SC4 is closed causing the first summation stored on a given storage capacitor C1–C4 to be subtracted from the second summation stored on the integration capacitor C5 and the resultant voltage will be amplified by the said amplifier Q10, the latter no longer acting as an integrator while the sample switch SD2 is open.

The amplifier gain when the storage capacitors C1, C2 and C3 are being used in the summation is determined by the resistors R8 and R10. If the storage capacitor C4 is involved, the gain is determined by the resistors R9 and R10 (FIGS. 4 and 16).

The output 40A3 of the color computer is tested by the comparator 40B (Q11–Q14 of FIGS. 4 and 16) to see if the computed function is positive, negative or zero. For example, if the voltage at the output 40A3 is presented to the comparator 40B and is between +0.6V and −0.6V, then the output is considered to be zero and it is assumed by the color grader that no leaves are in the field of view of the optics head OH, i.e., the grader is on background (BKD).

The color of the background plate S (FIG. 1) is stored in the background reference capacitors C6, C7 and C8 which in conjunction with the update sequence switches SE1, SE2 and SE3, respectively, all combined with the master update switch SE4, form three sample and hold circuits for background reference color storage R_B, F_B and I_B, respectively.

Therefore, when no leaf is in the field of view of the optics head OH, i.e., ON BKD., the outputs of the operational amplifiers Q4, Q5 and Q6 are constrained to zero enabling the initial subtractions $R'=R_L-R_B$, F'

$= F_L - F_B$ and $I' = I_L - I_B$ to be performed, respectively in these operational amplifiers.

The quantities R_L, F_L and I_L, respectively, are the color signal inputs from the Red, Green and Infrared pickups of FIGS. **1, 4, 16** and **19.**

To update the background storage R_B, F_B and I_B for each of the Red, Green and Infrared modes, the fourth summation function calculation stored in the storage capacitor C4 is performed with just one of the color sequence switches SA1, SA2 and SA3 closed (FIG. **6**) so that the output **40A3** when the fourth sample is performed consists of the necessary correction factor for the color corresponding to that color sequence switch. This update is repeated for the other colors during successive sets of 120Hz cycles until all three of the colors have been updated to the background reference S.

The UPDATE BACKGROUND information signal is sampled and held by sequence switch SD3 and holding capacitor C9 until the REJECT SELECTION logic RSL can determine whether or not the grader is ON BACKGROUND. If the BKD output of RSL is energized, indicating that only the background S is in view, the master update switch SE4 and the corresponding update sequence switch SE1, SE2 or SE3 are closed to transfer the correction signal from the holding capacitor C9 (FIGS. 4 and **16**) to the corresponding background storage capacitor C6, C7 or C8 under control of the UPDATE LOGIC UL (FIG. **19**).

The timing resistor R12 in series with the holding capacitor C9 and update sequence switches SE1–SE4 limits the speed of the update effect so that only slow changes can take place in the background reference values during operation of the grader.

During the initial set-up of the grader, i.e., when a completely fresh input of background reference information is required, the CPU will close the FAST RESET sequence switch SD4 to by-pass the timing resistor R12 to thereby speed up the background reference correction process.

Because of the disparity between the velocity of tobacco leaves being graded and the speed of modern digital logic, the latter being complex and unnecessarily costly if unduly duplicated, it is preferred to use on logic section and related controls for a multiplicity of individual color computers **40.**

Accordingly, a multiplicity of four-channel graders can be slaved to the controls and logic in a manner similar to CHANNELS No. 1–No. 4 of FIG. **19.** With the preferred embodiment disclosed herein, up to sixty-four (64) such channels (sixteen (16) four-channel graders) can be processed.

The calculations for each grading channel are carried out serially, in fixed sequence until all of the channels have been processed. The controlling logic then shuts down until the commencement of the next 120Hz cycle at which time the sequence of calculations is resumed.

The program clock PC controls the serial processing as previously described herein and counts the channels as they are processed to determine when the calculating is complete for a given sequence of channels.

The three clock signals that control the data handling shift registers for each channel are as follows:

the LOAD signal transfers the data from the temporary storage registers ST1 and ST2 in each channel into the main data registers ST3 of each channel;

the SHIFT signal consists of a series of pulses that circulate the data serially through all of the main data registers ST3, transfer register ST4, CPU output registers ST5, DATA BUFFER Y281–Y282, etc., for both input data and ultimate instructional data from the central processor CPU; and

the 120Hz clock signal (operate pulse) which informs the individual channels that all calculations are completed and that the UPDATE-REJECT data is then available for use by the UPDATE-REJECT logic UL-RL and the ACCESSORY logic ACL.

The various logic sections basically take the logic signals generated in each channel by its associated comparator **40B** and operate on those signals to effect a decision as to whether that channel should KEEP or REJECT a given leaf or other object being graded (if the optics head OH for that channel has such object in its field of view) or whether that channel should update its memory of the background plate S or reset that memory completely (if there is no leaf or object in the field of view of the optics head OH).

The ACCESSORY logic ACL monitors a selected plurality of channels grading as a group and the ALARM, TIME CLOCK and BLOW-OFF accessory functions are common to that group of channels. The functions of these accessories have previously been defined in reference to FIG. **18.**

For example, if one channel of a group of four channels requires a BLOW-OFF to clear an obstruction, all four channels are subjected to the BLOW-OFF; and likewise, if an ALARM condition occurs in any of the channels, the ALARM indication is for the whole group.

The four channels have their respective optics head OH in an array across a single conveyor **12** (FIG. **1**) such that a given tobacco leaf T conceivably could be in the field of view of more than one of the optics heads OH and thereby effect one or more REJECT functions in the group.

THE PROGRAM OF OPERATION

As shown in FIG. **21,** the current data fed into the grader system is from the color computer **40** and the front control panel **30** while the past history data comes from the serial memory SM (which is associated with the central processor CPU).

The decisions of ON or OFF BACKGROUND and KEEP or REJECT LEAF are made from the current data and correlated with the past history data in the CPU.

Depending upon the prior conditions represented by the past history data, as shown in the decision blocks in FIG. **21** with exemplary time periods correlated to the previously described program clock pulses and frequencies, the ultimate decisions of UPDATE, REJECT, FAST RESET, ALARM, BLOW-OFF and TIME CLOCK functions are made.

SCALAR VALUES GENERATION METHOD

To determine color, the quantity $rR' + fF' + iI'$ is computed as a voltage, and compared to a small voltage "d" to see if it is larger than $+d$, less than $-d$, or between $-d$ and $+d$. R', F' and I' are the red, green, and infrared color difference signals which are proportional to the difference in reflectivity of the objects being sorted and the background for each of the colors. The

scalars, r, f and i are constants that are computed from instructions dialed in on the front panel.

For positive scalars (r, f and i) SB3 is grounded and SB1 is connected to the color signal for a duration corresponding to the value of the scalar. For negative scalars, SB3 is connected to the color signal and SB1 is connected to ground for a duration corresponding to the absolute value of the scalar. In practice, the control pulse width to SB1 for negative numbers is the complement of the absolute value of the scalar and the control signal to SB3 is a sign bit. This makes it possible to use the complement plus sign method of representing the negative scalars.

The pulse widths that control SB1 are generated by the carry output of the six bit adder Y32–Y25 combined (FIG. 5C) which adds the signed number representing the scalar to the output of the six bit binary counter Y3 (FIG. 5). The sign in the number is used to control SB3. The process is illustrated for a 3 bit system in FIG. 23.

The use of the signed complement for representation of the scalar greatly simiplifies the generation of the scalar from the front panel control settings. All that is necessary is to implement the algebraic conversion via adders and preset biases. Preset biases will be inserted in the signed complement format also.

Typical values for the bias constants are for brightness:

$R_B = 12$
$I_B = -14$

and for greeness:

$I_B = -8$
$F_B = 22$
$R_B = -22$

The wiring pattern for the scalar bias computer board SSB would be as follows for the most significent bit MSB to the least significant bit LSB numbered from No. 6 to No. 1 in FIG. 5A:

Bit No.	(MSB) No. 6	No. 5	No. 4	No. 3	No. 2	(LSB) No. 1		
	1	1	1	1	0	0	: R/GN-I	SCALAR BIAS PARAMETERS (SBP)
	0	0	1	0	1	1	: R/GN-G	
	1	1	0	1	0	1	: R/GN-R	
	0	0	0	1	1	0	: BN-R	
	0	1	1	0	0	1	: BN-I	
	0	0	0	0	1	0	: +6V	

BRIGHTNESS COMPUTATION

The equation $rR' + fF' + iI' = 0$ represents a dividing place for the color determination in R', F', and I' spaces. Setting the voltage $d = 0$ is justified because d is such a small voltage. Objects being sorted will either be "above" or "below" this plane.

Since for vegetable matter I' is relatively constant, the equation can be written in three dimensions as $r(R'/I') + f(F'/I') + i = 0$. A plot of the objects to be sorted can be made with axis R'/I' and F'/I' such as previously described with reference to FIG. 8 for tobacco leaves.

For brightness measurements, f is made zero. This makes green suckers appear as dark as possible, making it easier to reject these smallish leaves.

The divider equation for brightness is therefore $R'/I' = -i/r$.

Since there is but one control for brightness ZBD, this equation to be implemented reduces to $R'/I' = -I_B + (15 - BS)/R_B$ where I_B and R_B are "wired in" bias numbers and R_B was arbitrarily picked to be a positive number. The brightness switch ZBD should be wired so that the output of the switch is (15 − BS) where BS is the number on the readout of the said switch ZBD.

Thus if $R'/I' = (R'/I')_{Min}$ when (BS) = 0, $R'/I' = (R'/I')_{Max}$
when (BS) = 15 then it can be shown that

$$I_B = -15\,(R'/I')_{Max}/(R'/I')_{Max} - (R'/I')_{Min} \qquad R_B = 15/(R'/I')_{Max} - (R'/I')_{Min}$$

GREENNESS AND REDNESS SCHEME

For operator convenience, it is desirable to provide two greenness selectors, one for bright greens (ZBG), and one for dark greens (ZDG). A fairly simple scheme for accomplishing this with a minimum of interaction between the switches is as follows:

Redness is accomplished with the same circuitry used for greenness. The only change is to reverse the dials so that a two (2) on a greenness selector (ZBG, ZDG) corresponds to 15–2 or 13 on the corresponding redness selector (ZBR, ZDR). This allows the operator to "pick green harder" by increasing the number on the greenness dial or to "pick red harder" by increasing the number on the redness dial. Since the dial settings are complimentary, it is possible to determine the degree of overlap by mentally adding corresponding green and red dial settings.

It is convenient to rotate the axis of reference −45° when discussing greenness, since this makes the X-Axis redness-greenness and the Y-Axis brightness. Starting with

$$r(R'/I') + f(F'/I') + i = 0$$

and rotating with the algorithm

$$R'/I' = \cos(-45°) - Y \sin(-45°)$$
$$F'/I' = \sin(-45°) + Y \cos(-45°)$$

one obtains

$$X = 1/f - r\,[(f+r)\,Y + \sqrt{2}\,i]$$

The sense of X is such that as X increases, the dividing line moves toward red, or if X decreases, the dividing line moves toward green.

A dark background is normally used with the device, so if $Y = 0$, we get the desired locus line for the dark control.

$$X = 1/f - r\,[\sqrt{2}i]$$

To make this control linear, $f - r$ must be a constant and i should be a linear function of the dark green setting, DGS of the selector switch ZDG. Hence let

$f - r = C$, a constant

$i = DGS + I_B$

where I_B is a fixed basis.

The former equation then reduces to

$$X = 1/C\,[(C + 2r)\,Y + \sqrt{2}\,(DGS + I_B)]$$

It is desired to make this equation strictly a function of BGS, the bright green setting of the selector switch ZBG, for some value of Y. One method of accomplishing this is to let $Y = \sqrt{2}/2$ and $r = BGS + (15\ DGS) + R_B$ where R_B is a fixed bias. Since $f - r$ is to be a constant, then $f - BGS + (15 - DGS) + F_B$ where F_B is a fixed bias. Therefore, if $Y = \sqrt{2}/2$,

$$X = \sqrt{2}/F_b - R_B\,[BGS + I_B + \tfrac{1}{2}\,(F_B + R_B) + 15]$$

To clarify these equations, they can be translated back to the R′/I′ and F′/I′ axis.

Then the dark control locus line

$$Y = 0$$

$$X = \sqrt{2}\,(DGS + I_B)/F_B - R_B$$

BECOMES

$$F'/I' = -\,DGS + I_B/F_B - R_B$$

$$R'/I' - DGS + I_B/F_B - R_B$$

AND THE BRIGHT CONTROL LOCUS LINE

$$Y = \sqrt{2}/2$$

$$X = \sqrt{2}/F_B - R_B\,[BGS + I_B + \tfrac{1}{2}\,(F_B + R_B) + 15]$$

BECOMES

$$F'/I' = -1/F_B - R_B[BGS + I_B + R_B + 15]$$

$$R'/I' = 1/F_B - R_B[BGS + I_B + F_B + 15]$$

These can be most easily utilized in a graphical analysis as shown in FIG. **24.**

The invention described herein may be modified as would occur to one of ordinary skill in the art without departing from the spirit and scope of this invention.

What is claimed:

1. Transducer means determining the relative brightness and color tones of articles to predetermined standards and classifying same into categories comprising:

a background surface having a predetermined color;

source means impinging polychromatic light on the obverse face of said background surface to reflect light therefrom in both the presence and absence of articles on said obverse face;

detector means receiving reflected light from said obverse face in first, second and third bands of the spectrum and producing, for each band, first output parameters representative of the respective intensities of reflected light in each said band in the presence of an article on said obverse face of said background reference;

reference means storing a second parameter for each band representative of the intensity of reflected light in each band in the absence of an article over said obverse face;

differential means operating on said parameters and producing, for each band, a third parameter representing the magnitude of the difference of said first and second parameters;

means modulating said third parameter for each band to vary the magnitude thereof by predetermined interrelated scalar multipliers;

summing means operating on said modulated third parameters and producing the sum thereof;

control means providing, as said predetermined standards, comparison parameters defining divisions of relative brightness and color tones, said divisions defining a plurality of quality zones of known color characteristics for which said articles might qualify;

selection means designating said zones as acceptable and unacceptable;

comparison means comparing said comparison parameters and said sums of said third parameters determining the presence and absence of said articles over said obverse face of said background surface and the zone for which said articles qualify;

and correlating means responsive to said selection means and said comparison means classifying said articles into acceptable and unacceptable categories.

2. The invention defined in claim **1,** wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

3. The invention defined in claim **2,** wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

4. The invention defined in claim **1,** wherein said summing means includes integrating means sequentially integrating said third parameter for each said spectral band over respectively predetermined intervals correlated to said respective scalar multipliers and storing the sum of such integrations in discreet storage means correlated to each of said division lines; and

said control means further including sampling means constraining said discreet storage means to apply said sums of said third parameters to said comparison means in synchronism with the respective correlated comparison parameters for said division lines.

5. The invention defined in claim **4,** wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

6. The invention defined in claim **5**, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

7. The invention defined in claim **1**, wherein said detector means provide a fourth output parameter for each said band representative of the intensity of reflected light in the absence of an article over said obverse face;

said differential means presenting the difference in said second and fourth parameters to said summing means as modulated by said modulating means for each said band to the exclusion of the other said bands;

said summing means including update storage means for storing said modulated difference in said second and fourth parameters; and

update switch means selectively connecting said update storage means with said reference means to update the magnitude of said second parameter with said modulated difference in said second and fourth parameters for each said spectral band.

8. The invention defined in claim **7**, wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

9. The invention defined in claim **8**, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

10. The invention defined in claim **7**, wherein said summing means includes integrating means sequentially integrating said third parameter for each said spectral band over respectively predetermined intervals correlated to said respective scalar multipliers and storing the sum of such integrations in discreet storage means correlated to each of said division lines; and

said control means further including sampling means constraining said discreet storage means to apply said sums of said third parameters to said comparison means in synchronism with the respective correlated comparison parameters for said division lines.

11. The invention defined in claim **10**, wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

12. The invention defined in claim **11**, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

13. The invention defined in claim **1**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

14. The invention defined in claim **1**, wherein said correlating means comprises:

digital processing means;

program clock means coordinating said processing means with said control means, said modulating means, said selection means and said comparison means;

first register means responsive to said clock means and said control means for storing a digital data representation of the determinations of said comparison means;

second register means controlled by said clock means for receiving said data from said first register means and transferring said data to said selection means;

first decoding logic means in said selection means for operating on said data to provide an indication to said processing means of the presence, absence, acceptable or unacceptable status of a given article over said obverse face of said background;

instruction generating means in said processing means supplying instruction data to said second register means; and

second decoding logic means driven by said second register means in response to said instruction data for providing command signals indicative of the acceptable or unacceptable status of a given article.

15. The invention defined in claim **14**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

16. The invention defined in claim **2**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

17. The invention defined in claim **3**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

18. The invention defined in claim **4**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

19. The invention defined in claim **5**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said artices to the size of said background.

20. The invention defined in claim **6**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

21. The invention defined in claim **7**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

22. The invention defined in claim **8**, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

23. The invention defined in claim 9, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

24. The invention defined in claim 10, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

25. The invention defined in claim 11, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

26. The invention defined in claim 12, wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

27. The invention defined in claim 14, wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

28. The invention defined in claim 27, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

29. The invention defined in claim 14, wherein said summing means includes integrating means sequentially integrating said third parameter for each said spectral band over respectively predetermined intervals correlated to said respective scalar multipliers and storing the sum of such integrations in discreet storage means correlated to each of said division lines; and

said control means further including sampling means constraining said discreet storage means to apply said sums of said third parameters to said comparison means in synchronism with the respective correlated comparison parameters for said division lines.

30. The invention defined in claim 29, wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, and division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

31. The invention defined in claim 30, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

32. The invention defined in claim 14, wherein said detector means provide a fourth output parameter for each said band representative of the intensity of reflected light in the absence of an article over said obverse face;

said differential means presenting the difference in said second and fourth parameters to said summing means as modulated by said modulating means for each said band to the exclusion of the other said bands;

said summing means including update storage means for storing said modulated difference in said second and fourth parameters; and

update switch means selectively connecting said update storage means with said reference means to update the magnitude of said second parameter with said modulated difference in said second and fourth parameters for each said spectral band.

33. The invention defined in claim 32, wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

34. The invention defined in claim 33, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

35. The invention defined in claim 32, wherein said summing means includes integrating means sequentially integrating said third parameter for each said spectral band over respectively predetermined intervals correlated to said respective scalar multipliers and storing the sum or such integrations in discreet storage means correlated to each of said division lines; and

said control means further including sampling means constraining said discreet storage means to apply said sums of said third parameters to said comparison means in synchronism with the respective correlated comparison parameters for said division lines.

36. The invention defined in claim 35, wherein said divisions of relative brightness and color tones comprise a bright and dark division line and two color division lines, said division lines intersecting to define said quality zones; and

adjusting means in said control means constraining said division lines in selectively oriented relative positions to vary selectively the color characteristics defined by each said zone.

37. The invention defined in claim 36, wherein said control means further includes logic means responsive to said adjusting means constraining said modulating means to correlate said scalar multipliers with said orientation of said division lines.

38. Means selectively grading articles by brightness and two color tones relative to predetermined standards as said articles traverse a background surface of known color illuminated by polychromatic light, comprising:

detecting and calculating means receiving reflected light from said articles and said background in three distinct spectral bands R, F and I and deriving for each said article a linear summation of the intensities of reflected light in the form $rR' + fF' + iI'$, for determining brightness and each of said color tones, wherein r, f and i are predetermined scalar multipliers respectively associated with said bands and R', F' and I' are functions of the intensity of reflected light in said bands from said articles and said background surface;

control means generating said scalar multipliers and a brightness and two color tone standards compris-

ing division lines in the form $rR' + fF' + iI' = \pm d$ where d is a predetermined constant, said division lines intersecting to form a plurality of color quality zones; and

means comparing said linear summations with the correlative ones of said brightness and color tone standards, determining the relative magnitudes of said summations to that of the quantity $\pm d$ and identifying the color quality zones characterizing each said article as a function of said relative magnitudes.

39. The invention defined in claim **38,** wherein said grading means further includes selection means designating said quality zones as acceptable or unacceptable; and

correlating means responsive to said comparing means and said selection means providing for each said article an acceptable or unacceptable indication.

40. The invention defined in claim **39,** wherein said articles traverse said background surface in a first ballistic path; and

wherein said grading means further includes means constraining a said article into a second ballistic path in response to a unacceptable indication for said article from said correlating means.

41. The invention defined in claim **38,** wherein R', F' and I' comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

42. The invention defined in claim **41,** wherein said grading means further includes selection means designating said quality zones as acceptable or unacceptable; and

correlating means responsive to said comparing means and said selection means providing for each said article an acceptable or unacceptable indication.

43. The invention defined in claim **42,** wherein said articles traverse said background surface in a first ballistic path; and

wherein said grading means further includes means constraining a said article into a second ballistic path in response to an unacceptable indication for said article from said correlatig means.

44. The invention defined in claim **38,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

45. The invention defined in claim **39,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

46. The invention defined in claim **40,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

47. The invention defined in claim **41,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

48. The invention defined in claim **42,** wherein the refelectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

49. The invention defined in claim **43,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

50. Means selectively grading articles by brightness and two color tones relative to predetermined standards as said articles traverse one or more background surfaces of known color illuminated by polychromatic light comprising:

at least one detecting and calculating means associated with each said background surface receiving reflected light from said articles and said background in three distinct spectral bands R, F and I and deriving for each said article a linear summation of the intensities of reflected light in the form $rR' + fF' + iI'$, for determining brightness and each of said color tones, wherein r, f and i are predetermined scalar multipliers respectively associated with said bands and R', F' and I' are functions of the intensity of reflected light in said bands from said articles and said background surface;

control means common to all said detecting and calculating means generating said scalar multipliers and a brightness and two color tone standards comprising division lines in the form $rR' + fF' + iI' = \pm d$ where d is a predetermined constant, said division lines intersecting to form a plurality of color quality zones;

means in each said detecting and calculating means comparing said linear summations with the correlative ones of said brightness and color tone standards, determining the relative magnitudes of said summations to that of the quantity $\pm d$ and identifying the color quality zones characterizing each said article as a function of said relative magnitudes; and

encoding means for each detecting and calculating means encoding and storing data characterizing said quality zone identities.

51. The invention defined in claim **50,** wherein said grading means further includes:

selection means common to all said detecting and calculating means designating said quality zones as acceptable or unacceptable;

sequencing means in said control means coordinating said detecting and calculating means, said comparing means, and said encoding means and sequentially shifting said encoded zone data through said selection means from each said encoding means to identify said zone data therefrom as characterizing acceptable or unacceptable zones.

52. The invention defined in claim **51,** wherein said selection means provides acceptable and unacceptable output indications in response to said encoded zone data for each said encoding means; and

wherein said grading means further includes instruction generating means responsive to said output indications providing instructions to each said detecting and calculating means to accept and reject said acceptable and unacceptable articles, respectively.

53. The invention defined in claim **50,** wherein said articles traverse said background surface in a first ballistic path; and

wherein said grading means further includes, for at least each said background surface, means constraining a said article into a second ballistic path

in response to an unacceptable indication for said article from said correlating means.

54. The invention defined in claim **51,** wherein said articles traverse said background surface in a first ballistic path; and

wherein said grading means further includes, for at least each said background surface, means constraining a said article into a second ballistic path in response to an unacceptable indication for said article from said correlating means.

55. The invention defined in claim **52,** wherein said articles traverse said background surface in a first ballistic path; and

wherein said grading means further includes, for at least each said background surface, means constraining a said article into a second ballistic path in response to an unacceptable indication for said article from said correlating means.

56. The invention defined in claim **50,** wherein R′, F′ and I′ comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

57. The invention defined in claim **51,** wherein R′, F′ and I′ comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

58. The invention defined in claim **52,** wherein R′, F′ and I′ comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

59. The invention defined in claim **53,** wherein R′, F′ and I′ comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

60. The invention defined in claim **54,** wherein R′, F′ and I′ comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

61. The invention defined in claim **55,** wherein R′, F′ and I′ comprise the difference in magnitudes of the intensity of reflected light from said background alone and from said background with an article traversing same in each said spectral band.

62. The invention defined in claim **50,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

63. The invention defined in claim **51,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

64. The invention defined in claim **52,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

65. The invention defined in claim **53,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

66. The invention defined in claim **54,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

67. The invention defined in claim **55,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

68. The invention defined in claim **56,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

69. The invention defined in claim **57,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

70. The invention defined in claim **58,** wherein the reflectivity in one of said spectral bands from said artiles is substantially uniform to normalize the relative size of said articles to the size of said background.

71. The invention defined in claim **59,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

72. The invention defined in claim **60,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

73. The invention defined in claim **61,** wherein the reflectivity in one of said spectral bands from said articles is substantially uniform to normalize the relative size of said articles to the size of said background.

74. Means selectively grading articles by brightness and two color tones relative to predetermined standards as said articles traverse a background surface of known color illuminated by polychromatic light and wherein said light is driven by an alternating current source, comprising:

detecting and calculating means performing calculations for brightness and said two color tones of each said article in each of two consecutive half cycles of said alternating current source;

logic means controlling said detecting and calculating means constraining storage of said calculations in the first said half cycle, a reverse logic for said calculations in the second said half cycle, and a summation of like ones of said first and second half cycle calculations;

said summation, for each such calculation, providing resultant calculations for said brightness and said color tones compensated for alternating current induced variations in said polychromatic light and operating offsets in said detecting and calculating means;

and means comparing said summations to said predetermined standards.

75. The invention defined in claim **74,** wherein said detecting and calculating means includes summing means effecting said summations comprising:

integrating means including an integration capacitor consecutively storing each of said first and second half cycle calculations;

storage capacitors means for each of said first half cycle calculations;

first switch means selectively transferring each of said first half cycle calculations from said integration capacitor to a corresponding storage capacitor as each said calculation is completed; and

second switch means selectively converting said integrating means to an amplifier means subsequent to each of said second half cycle calculation and constraining said summation of said like first and second half-cycle calculations, sequentially, and the application of said summations, in sequence, to said comparing means.

76. Means grading and sorting tobacco leaves in reference to predetermined standards of brightness, greenness and redness, comprising:

a background surface of known color;

conveyor means constraining tobacco leaves to traverse the obverse face of said background surface;

optical means impinging said obverse face and said leaves with polychromatic light and receiving reflected light therefrom in red, green and infrared bands of the spectrum;

control means providing first, second and third reference parameters representative of the said standards of brightness, greenness and redness, respectively;

calculating means responsive to said reflected light received by said optical means providing first, secoud and third operating parameters representative of the brightness, greenness and redness, respectively, of each said leaf traversing said obverse face of said background;

comparator means responsive to said control means and said calculating means providing first, second and third resultant parameters representing, respectively, the relative brightness, greenness and redness of said leaves to said standards; and reject selection means operating on said leaves in response to said resultant parameters when the latter represent predetermined deviations from said standards.

77. The invention defined in claim **76,** wherein said reference parameters mutually define a plurality of color quality zones; and

wherein said reject selection means includes zone selecting means selectively establishing said zones as said predetermined deviations from said standards.

78. The invention defined in claim **76,** wherein said tobacco leaves traverse said obverse face of said background surface in a predetermined first ballistic path; and

wherein said reject selection means includes rejecting means responsive to the occurrence of said predetermined deviations constraining said leaves into a second predetermined ballistic path.

79. The invention defined in claim **77,** wherein said tobacco leaves traverse said obverse face of said background surface in a predetermined first ballistic path; and

wherein said reject selection means includes rejecting means responsive to the occurrence of said predetermined deviations constraining said leaves into a second predetermined ballistic path.

80. Transducer means for classifying an object with reference to allowable deviations from predetermined standards of brightness and first and second color tones, comprising:

a background surface of known color having an obverse face over which said object is positioned;

optical means impinging said obverse face and said object with polychromatic light and receiving reflected light therefrom in three distinct bands of the spectrum;

control means providing first, second and third reference parameters representative of the said standards of brightness and first and second color tones, respectively;

calculating means respective to said reflected light received by said optical means providing first, second and third operating parameters representative of the brightness and first and second color tones, respectively, of said object;

comparator means responsive to said control means and said calculating means providing first, second and third resultant parameters representing, respectively, the relative brightness and first and second color tones of said object to said standards; and

means responsive to said resultant parameters to indicate when at least one of said relative brightness and first and second color tones of said object exceeds the corresponding one of said allowable deviations from said predetermined standards.

81. Means classifying a succession of objects with reference to allowable deviations from predetermined standards of brightness and first and second color tones, comprising:

a background surface of known color having an obverse face over which said objects are successively positioned;

optical means impinging said obverse face and said objects with polychromatic light and receiving reflected light therefrom in first, second and third bands of the spectrum;

control means providing first, second and third reference parameters representative of the said standards of brightness and first and second color tones, respectively;

calculating means responsive to said reflected light received by said optical means providing first, second and third operating parameters representative of the brightness and first and second color tones, respectively, of each said object over said obverse face of said background;

comparator means responsive to said control means and said calculating means providing first, second, and third resultant parmeters representing, respectively, the relative brightness and first and second color tones of said objects to said standards; and

means responsive to said resultant parameters for each said object to indicate when at least one of said relative brightness and first and second color tones of a said object exceeds the corresponding one of said allowable deviations from said predetermined standards.

82. The invention defined in claim **81** wherein one of said spectral bands is characterized by substantially uniform reflection from each of said succession of objects to normalize the size of said objects to that of said background.

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