



(51) International Patent Classification:

H03H 17/06 (2006.01) *H03H 17/02* (2006.01)

(21) International Application Number:

PCT/US2018/058574

(22) International Filing Date:

31 October 2018 (31.10.2018)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

62/579,809 31 October 2017 (31.10.2017) US

(71) Applicant: **SYNAPTICS INCORPORATED** [US/US];
1251 McKay Drive, San Jose, California 95131 (US).(72) Inventors: **POULSEN, Jens Kristian**; 1251 McKay Drive,
San Jose, California 95131 (US). **THORMUNDSSON, Trausti**; 1251 McKay Drive, San Jose, California 95131 (US). **MILANI, Ali Abdollahzadeh**; 1251 McKay Drive, San Jose, California 95131 (US). **MILLER, Mark**; 1251 McKay Drive, San Jose, California 95131 (US).(74) Agent: **GALLAGHER, Dennis R.**; Suite 700, 2323 Victory
Avenue, Dallas, Texas 75219 (US).(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP,
KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,
MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: LOW DELAY DECIMATOR AND INTERPOLATOR FILTERS

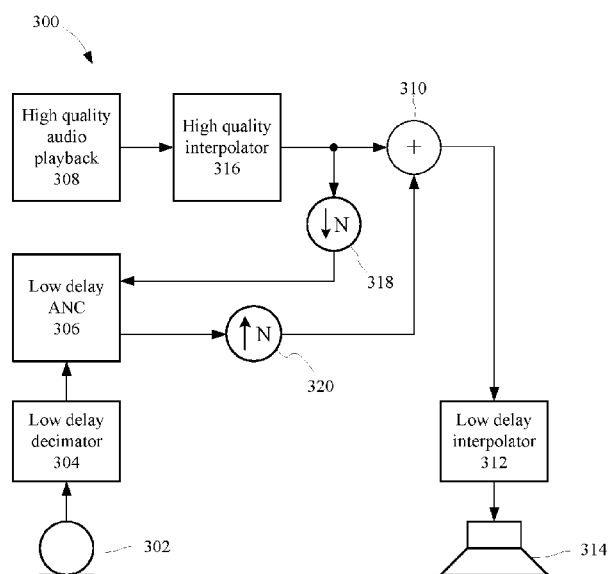


FIG. 3

(57) Abstract: Systems and methods for low latency adaptive noise cancellation include an audio sensor to sense environmental noise and generate a noise signal, an audio processing path to receive an audio signal, process the audio signal through an interpolation filter, and generate a primary audio signal having a first sample frequency, an adaptive noise cancellation processor to receive the noise signal and generate an anti-noise signal, a direct interpolator to receive the anti-noise signal and generate an anti-noise signal having the first sample frequency, and a limiter to provide clipping to reduce a number of bits in the anti-noise signal, an adder operable to combine the primary audio signal and the anti-noise signal and generate a combined output signal, and a low latency filter to process the combined output signal.

LOW DELAY DECIMATOR AND INTERPOLATOR FILTERS

Jens Kristian Poulsen, Trausti Thormundsson, Ali Milani and Mark Miller

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit of and priority to U.S. Provisional Patent Application Number 62/579,809, filed October 31, 2017, which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The present application relates generally to systems and methods for digital signal processing, and more particularly to sample rate conversion, for example, in adaptive noise cancellation systems.

BACKGROUND

[0003] The conversion of digital signals to different sample rates suitable for various digital components and processes is well known. For example, it is common for a digital signal processing system to use different sampling rates depending on a desired signal quality, required bandwidth, latency requirements, processing economy, available silicon area and other considerations. In audio processing systems, different sample rates may be used to achieve low latency and high performance. For example, in a digital adaptive noise cancellation (ANC) system, audio processing and ANC processing may be performed at different sample rates allowing for increased bandwidth of the ANC system (see, e.g., “Understanding Active Noise Cancellation”, Colin H. Hansen, ISBN 0415231922).

[0004] There are, however, issues in combining signals with uniform delay in systems using oversampled converter structures. One solution is to perform the processing in the analog domain, thereby circumventing the delay problems associated with digital oversampled processing. However, this will typically have limited ability to adapt over a wide frequency range, and other solutions suffer from a limited frequency resolution and limited attenuation of the undesired noise. Furthermore, these solutions are often sensitive to changes in components and implementation dependent. In view of the foregoing, there is a continued need for improved systems and methods for adaptive noise cancellation processing using oversampled converter structures.

SUMMARY

[0005] Systems and methods are disclosed herein for providing low latency adaptive noise cancellation (ANC). In various embodiments, a system includes an audio sensor operable to sense environmental noise and generate a noise signal, an audio processing path operable to receive an audio signal, process the audio signal through an interpolation filter, and generate a primary audio signal having a first sample frequency, an adaptive noise cancellation processor operable to receive the noise signal and generate a corresponding anti-noise signal, a direct interpolator operable to receive the anti-noise signal and generate an upsampled anti-noise signal having the first sample frequency, the direct interpolator comprising a sign extension stage operable to extend most significant bits of the anti-noise signal to avoid overflow, and a limiter operable to provide clipping to reduce a number of bits in the upsampled anti-noise signal, an adder operable to receive and combine the primary audio signal and the upsampled anti-noise signal and generate a combined output signal, and a low latency filter operable to process the combined output signal.

[0006] In some embodiments the low latency filter includes a plurality of filters, each performing filtering at a different sample frequency. The low latency filter may include a plurality of lattice wave filters disposed in a cascaded arrangement, wherein each of the plurality of lattice wave filters processes a different frequency band. In some embodiments, the sample frequency is increased in integer steps in each successive filter. The lattice wave filters may include a plurality of delay elements, and direct sampling at a particular output sample frequency may be achieved by interlacing multiple filters. In one implementation, N delay elements are provided in reflector sections (two-port adaptors) and one path is delayed by $N/2$ delay elements, and another path is directly connected to an input signal, for N equals a sequence of positive integer exponents of two. In another implementation, the lattice wave filter comprises two paths, including one path including a plurality of reflector elements with each reflector element delayed by N unit delays, where N is an integer greater than one, and one path delayed by M delay elements, where M is an integer greater than one. In some embodiments, the adaptive noise cancellation processor is further operable to derive the anti-noise signal by the adaptive cancellation processor, where the filter coefficients are calculated by a filtered-X least mean squares process, either operating in the time- or frequency domain.

[0007] In various embodiments, a system includes an audio processing path operable to receive and process a primary audio signal having a first sample frequency, an adaptive noise cancellation path comprising a decimator operable to downsample the primary audio signal to a second sampling frequency, an adaptive noise cancellation processor operable to receive the

primary audio signal and a noise signal at the second sample frequency and generate an anti-noise signal having the second sample frequency, and an interpolator operable to upsample the anti-noise signal to the first sample frequency, and an adder operable to combine the anti-noise signal and the primary audio signal at the first sample frequency. The decimator and interpolator each comprise a plurality of filters operable to perform filtering at corresponding plurality of sample frequencies.

[0008] In some embodiments, each of the adaptive noise cancellation path and the audio processing path includes oversampled lattice filters comprising a plurality of delay elements arranged to enable uniform delay. The system may further comprise a microphone operable to sense environmental noise and generate corresponding electrical signals, and a low delay decimator to generate the noise signal at the second sample frequency. The system may further comprise an oversampled interpolation filter that has input and output sample frequencies that match the first sample frequency, and is operable to remove aliased images generated by the interpolator in the adaptive noise cancellation path. In some embodiments, each of the plurality of filters comprises a multi-stage lattice wave filter structure where each stage changes an operating sample rate by a factor of two. The decimator and interpolator may each comprise a sign extension stage operable to extend the most significant bits of a received signal to avoid overflow, and a limiter operable to provide clipping to reduce a number of output bits.

[0009] In various embodiments, a method comprises sensing environmental noise and generating a noise signal, processing an audio signal through an interpolation filter to generate a primary audio signal having a first sample frequency, generating, from the noise signal, an anti-noise signal having a second sample frequency, directly interpolating the anti-noise signal to generate an upsampled anti-noise signal having the first sample frequency, wherein directly interpolating include extending most significant bits of the anti-noise signal to avoid overflow and multiplying the ANC reference by a gain factor equal to the interpolation factor, and clipping to reduce a number of output bits in the upsampled anti-noise signal, combining the primary audio signal and the upsampled anti-noise signal to produce a combined output signal; and processing the combined output signal through a low latency filter.

[00010] In some embodiments, the method further includes applying a plurality of lattice wave filters disposed in a cascaded arrangement, wherein each of the plurality of lattice wave filters processes a different sample frequency that is successively changed in each successive filter. Applying the plurality of lattice wave filters may include applying a plurality of delay

elements. Direct sampling at a particular output sample frequency may be achieved by interlacing multiple filters. In various embodiments, decimating the primary audio signal to downsample the primary audio signal to the second sample frequency, and generating, from the noise signal, the anti-noise signal having the second sample frequency may further include analyzing the downsampled primary audio signal. In some embodiments, the method includes generating, from the noise signal, the anti-noise signal having the second sample frequency comprises calculating filter coefficient using a filtered-X least mean squares process.

[00011] The scope of the invention is defined by the claims, which are incorporated into this section by reference. A more complete understanding of embodiments of the invention will be afforded to those skilled in the art, as well as a realization of additional advantages thereof, by a consideration of the following detailed description of one or more embodiments. Reference will be made to the appended sheets of drawings that will first be described briefly.

BRIEF DESCRIPTION OF THE DRAWINGS

[00012] Aspects of the disclosure and their advantages can be better understood with reference to the following drawings and the detailed description that follows. It should be appreciated that like reference numerals are used to identify like elements illustrated in one or more of the figures, wherein showings therein are for purposes of illustrating embodiments of the present disclosure and not for purposes of limiting the same. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present disclosure.

[00013] FIG. 1 is a first example of an adaptive noise cancellation system, in accordance with one or more embodiments.

[00014] FIG. 2 is a second example of an adaptive noise cancellation system, in accordance with one or more embodiments.

[00015] FIG. 3 is a third example of an adaptive noise cancellation system, in accordance with one or more embodiments.

[00016] FIG. 4 is an example of an adaptive noise cancellation system similar to FIG. 3 using an oversampled interpolation filter, in accordance with one or more embodiments.

[00017] FIG. 5 illustrates a topology of an eight times oversampled interpolation or decimation filter, in accordance with one or more embodiments.

[00018] FIGs. 6A and 6B illustrate the frequency response and group delay of the oversampled filter of FIG. 5, assuming a sample frequency of 3072 kHz.

[00019] FIG. 7 illustrates a topology of a four times oversampled interpolation or decimation filter, in accordance with one or more embodiments.

[00020] FIGs. 8A and 8B illustrate the frequency response and group delay of the oversampled filter of FIG. 7, in accordance with one or more embodiments, assuming a sample frequency of 3072 kHz.

[00021] FIG. 9 illustrates a topology of a two times oversampled interpolation or decimation filter, in accordance with one or more embodiments.

[00022] FIGs. 10A and 10B illustrate the frequency response and group delay of the oversampled filter of FIG. 9, in accordance with one or more embodiments, assuming a sample frequency of 3072 kHz.

[00023] FIG. 11 illustrates a topology of an oversampled filter, in accordance with one or more embodiments.

[00024] FIGs. 12A and 12B illustrate the frequency response and group delay of the oversampled interpolator of FIG. 11, in accordance with one or more embodiments, assuming a sample frequency of 3072 kHz.

[00025] FIGs. 13A, 13B, and 13C illustrate a combined frequency response of the filter chain of FIG. 4, in accordance with one or more embodiments, assuming a sample frequency of 3072 kHz.

[00026] FIGs. 13D and 13E illustrate an overall group delay of the filter chain of FIG. 4, in accordance with one or more embodiments, assuming a sample frequency of 3072 kHz.

[00027] FIG. 14 illustrates a decimator, in accordance with one or more embodiments.

[00028] FIG. 15 illustrates a measurement of filter group delay, in accordance with one or more embodiments, assuming a sample frequency of 3072 kHz.

[00029] FIGs. 16A, 16B, and 16C illustrate a decimator and logic for performing sign extension and saturation of output, in accordance with one or more embodiments.

[00030] FIGs. 17A, 17B, and 17C illustrate an interpolator and logic for performing sign extension and saturation of output, in accordance with one or more embodiments.

[00031] FIG. 18 illustrates a generalized oversampled filter topology, in accordance with one or more embodiments.

[00032] FIGs. 19A-B illustrate decimation and interpolation using lattice wave filter structures, in accordance with one or more embodiments.

[00033] FIGs. 20A-B illustrate a single section of a lattice wave filter and an example implementation, in accordance with one or more embodiments.

[00034] FIG. 21 illustrates an oversampled decimator/interpolator having multiple delay elements and multiple allpass filters, in accordance with one or more embodiments.

[00035] FIG. 22 illustrates an oversampled decimator/interpolator having multiple delay elements and multiple allpass filters, in accordance with one or more embodiments.

DETAILED DESCRIPTION

[00036] In accordance with various embodiments of the present disclosure, systems and methods for achieving low latency and high-quality audio output in adaptive noise cancellation filters are disclosed.

[00037] Noise cancellation and noise reduction techniques are used in a variety of applications to improve user experiences in noisy environments. In one approach a listening device, such as headphones, headsets or ear buds, includes one or more audio sensors to pick up environmental noise and adaptive noise cancellation processing circuitry to generate an anti-noise signal to cancel or reduce the environmental noise for the user. It is desirable for the generated anti-noise signal to be equal to the inverse of the noise disturbance (thereby cancelling the noise) while desired audio, such as the playback from a high-fidelity audio source, is provided with minimal disturbance. To obtain desired attenuation of the environmental noise, ANC systems are designed for low latency processing of the received noise signals to generate an inverted output signal that has a minimal phase shift with respect to the original noise signal to obtain a wide bandwidth of noise cancellation. In many listening environments, a feedback signal having a latency of around 10 μ s can be used to obtain a noise reduction bandwidth of around 20 kHz, with the actual obtained bandwidth depending on the topology of the noise cancellation system and the actual acoustics system.

[00038] Various embodiments of the present disclosure are directed to noise cancellation systems that use oversampled converters in high-quality audio playback systems. In one embodiment, delta-sigma analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) are used for audio signal processing. As compared to Nyquist sample rate converters, delta-sigma converters utilize a higher sample rate and are generally cheaper to implement because they require less precision in the analog signal components. Therefore, both from a cost and processing perspective, it is often advantageous to perform the noise

cancellation at a higher sample rate than required by the Nyquist criterion and this can be used to obtain a wider noise cancellation bandwidth.

[00039] One complication with multi-rate signal processing is the possibility of increased latency. In ANC systems, it is desirable to provide a time-accurate reference for the active noise processing system, both of the measured noise (undesired signal) and high fidelity audio (desired signal), in order to generate an anti-noise signal that is in phase with the environmental noise to be cancelled. In some embodiments, lattice wave filters, which are known for low sensitivity to coefficient changes, are used to obtain simplified filter solutions that do not require multiplication. To obtain low latency, a low filter order is desired, but this may have the unfortunate property that the attenuation for out-of-band signals is lower which can be a problem for high-quality audio signals where good out-of-band attenuation is desired.

[00040] A system 100 for performing adaptive noise cancellation (ANC) in accordance with embodiments of the present disclosure will now be described with reference to FIG. 1. The system 100 may be implemented in noise cancelling headphones, ear buds or other systems that sense noise from an environment and generate a noise cancelling signal. The system 100 includes at least one microphone 102 or other audio sensor to sense the environmental noise from one or more noise sources and generate corresponding electrical signals representing the sensed noise. In various embodiments, the at least one microphone 102 may be arranged in a feed-forward, feedback, or combined feed forward/feedback ANC system. The output of the microphone 102 may be a digital oversampled bit stream, e.g. the output from a single-bit digital microphone, or an analog signal that is provided to a pre-amplifier and a delta-sigma converter (single-bit or multi-bit) to produce the digital oversampled audio signal. The digital audio signal is decimated to a lower sample rate by a low delay decimator 104, such as a multi stage lattice wave filter, for input to a low delay ANC processor 106.

[00041] The low delay ANC processor 106 generates an anti-noise signal corresponding to the environmental noise sensed by the microphone 102. The ANC processor 106 also receives a time-accurate, audio playback signal from the high-quality audio playback processor 108, which is used as an audio reference signal. In various embodiments, the ANC processor 106 uses a time or frequency update of internal filter nodes to adaptively filter the environmental noise from the microphone signal, which may also include desired audio played through a speaker 114. For example, the ANC processor 106 may implement a filtered-x least mean squares (FXLMS) algorithm to adaptively modify filter coefficients to

filter out the environmental noise. To obtain a low latency, finite impulse response (FIR) topologies are often used while the filter updates are often performed in the frequency domain to obtain fast adaption even when there is a significant spread among the power spectrum of the noise. This enables fast adaptation even at frequencies where the energy content is significantly smaller than any dominant nodes by separating the signals in the frequency domain. An inverse frequency transform may be used to transform the adapted weights back to the time domain.

[00042] The audio playback processor 108 generates the desired audio signal (also referred to herein as the primary audio signal) for playback through an audio output, such as speaker 114. The desired audio signal may be generated from a source file (e.g., recorded music or movie file) or output from another source, such as a near end microphone or an audio signal received from a far end microphone in a voice over IP system. The desired audio signal is combined with the anti-noise signal output by the ANC processor 106 by the adder 110. The summed output of these signals is filtered and upconverted using a low latency interpolator 112 and output to the speaker 114 (sometimes called a receiver).

[00043] It will be appreciated that, for simplicity, some standard components are not shown in FIG. 1, for example, a microphone preamplifier, a possible microphone high voltage pump used in MEMS microphones, low noise power supply unit, speaker amplifier, a power source and other components of the system 100. These components are known to those skilled in the art and will be included in various practical system implementations, but have been omitted here for clarity in the showing the processing path.

[00044] In various embodiments of the system 100, both the high-fidelity audio signal and the ANC output signals are represented at the same low sample rate (e.g. 192 kHz) and are therefore both subjected to the same low-fidelity interpolation filter – provided a low latency in the processing path is a design goal. While it is possible to increase the processing sample rate, this will increase power consumption and physical size of the design considerably. Therefore, it is desired to simultaneously be able to combine a high-quality interpolation filter for audio playback and a low latency filter path for the ANC processing (also referred to herein as the adaptive noise cancellation path). This may be implemented as shown in the embodiment of Fig. 2, which illustrates components of a system 200 for performing adaptive noise cancellation (ANC).

[00045] The system 200 includes a microphone 202, low delay decimator 204 and low delay ANC processor 206 for receiving a noise signal and generating an anti-noise signal. The anti-noise signal is provided to a low latency interpolator 212 to produce the anti-noise

signal 218 to be combined with the high-quality audio signal (also referred to herein as the primary audio signal) by adder 210. High-quality audio is provided by high-quality audio playback 208 to the ANC processor 206 for use as the ANC reference signal. As illustrated, the high-quality audio signal and the noise signal are at the same low sample rate (e.g., 192 kHz), suitable for efficient ANC processing. A high-quality interpolator 216 ("high-quality" meaning including sufficient dynamic range, attenuation etc. for the system requirements) increases the sampling rate of the high-quality audio signal for output to the speaker 214 and adds latency to the high-quality audio signal processing path. Because the ANC processor 206 uses a time-accurate audio reference of the audio output, the different signal processing paths of the two signals (output from block 208 and 206) experience a different signal processing path (i.e. through filters 212 and 216 respectively), which creates differences in the internal group delays, leading to less than optimal adaption in the ANC processing unit. The different latencies between blocks 212 and 216 will cause the signals to be out of phase which decreases performance of the noise cancellation. Therefore, the issues with the system of FIG. 1 cannot be solved by simply adding the output from a high-fidelity quality interpolator 216 and a low latency interpolation filter 212. Thus, neither system 100 nor system 200 solves the problem of time accurate references for the ANC system while providing both a low delay path for the ANC signal and a high-fidelity signal path for the reference audio signal.

[00046] An embodiment of a system 300 providing time accurate references for the ANC system while providing both a low delay path for the ANC signal and a high-fidelity signal path for the reference audio signal is illustrated in FIG. 3. The microphone 302, low delay decimator 304, low delay ANC processor 306, high-quality audio playback processor 308, high-quality interpolator 316 and speaker 314 may be implemented as illustrated in FIGs. 1 and 2, previously discussed. The high-quality audio playback processor 308 generates a high-quality audio signal which is fed to the high-quality interpolator 316 (i.e., a high-fidelity interpolation filter). To avoid problems with high power consumption, excessive complexity or differences in delays, this high-fidelity oversampled output of the high-quality interpolation filter is decimated by a factor of N by decimator 318 which operates without filtering (i.e., selects every Nth sample). Filtering (e.g., anti-aliasing) is not required because out-of-band signals are removed by the high-quality interpolator 316 and the signal bandwidth is therefore unchanged. The ANC processor 306 output signal (anti-noise signal) is directly upsampled to a higher frequency in interpolator 320 by a factor of N to match the frequency of the high-quality audio signal. In one embodiment, the output signal is

upsampled to a higher frequency by inserting $N-1$ samples equal to zero between each original sample. This operation will introduce multiple mirror aliases of the original noise signal. The anti-noise signal is combined with the high-fidelity oversampled output by adder 310, and the combined output signal is sent to the low delay interpolator 312.

[00047] The low delay interpolator 312 in this embodiment is an oversampled interpolator that operates at the higher sample rate of the initial audio output times N , and removes the aliased images that will be output from the directly interpolated signal from the ANC processor 306, while the original oversampled high-fidelity oversampled audio signal will pass through unchanged since the aliased images have already been removed by the high-quality interpolator. The oversampled interpolator 312 may be implemented by adding extra delay elements inside each filter section, i.e. each filter section includes N , $N/2$, $N/4$ etc. times the original delay elements to obtain the same frequency response as the original filter configuration operating at N , $N/2$, $N/4$ times lower sample frequency. Furthermore, this filter configuration solves practical implementation problems, because the filter elements are updated at the much higher sample rate of N times the original sample rate, thereby enabling an optimal group delay of the filters. In this case, the theoretical performance may be obtained without introducing extra delays due to a practical register transfer level implementation that often can give delays when transferring values between systems with different sample rates (i.e., difference sample frequencies). Other filter configurations than Lattice Wave filter may be used in the general solution shown in Fig. 3 and any solution should not be limited to these.

[00048] In various embodiments, the oversampled interpolation filter has same input and output sample frequency, and can also be used as a low latency decimation filter and thereby lower latency further by reducing the input path delay. It is essentially a low pass filter with very low delay and wide bandwidth, and it is possible to add a second decimation path for high-fidelity applications.

[00049] For various implementations, the filter may be optimized by first designing a filter with a response that may be ideal from an out-of-band attenuation point of view, and then further optimize the filter by adjusting the coefficients to improve the actual signal-to-noise-ratio (SNR) at the output of the filter, thereby taking the actual noise shaping of the used delta-sigma converters into account. Further, the coefficients may be discretized to remove multiplications in the actual implementation thus lowering silicon area, cost and power consumption significantly.

[00050] Embodiments of an oversampled filter implementation 400 will now be described with reference to FIG. 4. As previously discussed, to obtain low latency, low power, low silicon area and high performance in a digital ANC feedback loop, it may be an advantage to perform audio and ANC processing at different sample rates. In the illustrated embodiment the audio signal is sampled at a 3.072 MHz rate, and the ANC processing at a lower 192 kHz rate, though it will be appreciated that other sampling rates may be used in accordance with system requirements. The audio processing itself may be performed at the same rate as the ANC (192 kHz) or at a lower rate, e.g. 48 kHz. There are however, problems in combining these signals with uniform delay when using oversampled converter structures. While the decimation path can be performed separately, there may be problems in combining the ANC processing and audio path together with uniform delay. If the interpolation path has been optimized for low latency, there will not be much attenuation of out-of-band mirror images from the audio path and similarly, if there is made a compromise on the latency to improve the audio path, bandwidth and ANC performance suffers.

[00051] To obtain both high audio quality and low uniform path delay of the audio signal and the ANC anti-noise signal, the embodiment of FIG. 4 includes oversampled interpolators in a topology that enables uniform delay of both paths. As illustrated, the high-quality audio input signal is sampled at 48 kHz, and upsampled by halfband filters (sections S1 and S2) to 192 kHz. The interpolation filter 416 is a high-quality interpolator that removes aliased mirror images and upsamples the signal by a factor of 16 to the output audio sample rate of 3.072 MHz. The audio signal is filtered in the audio processing path and the combination of the audio signal and the anti-noise signal is performed at the oversampled output frequency (3.072 MHz). In this embodiment, a short ANC delay and sufficient audio mirror attenuation is achieved simultaneously. In various embodiments, the audio path is filtered after the original path (i.e., after the combination with the anti-noise signal), and this may result in a slight attenuation of the highest frequencies and further reduction of out-of-band noise. Undesired in-band attenuation of the audio signal by the ANC oversampled interpolator can be corrected by a small equalization done before the upsampling of the signal occurs. In various embodiments low delay lattice wave filters are used for the oversampled interpolation filter to minimize latency in the loop. The oversampled interpolation filter may be used with slight modification for decimation in the noise signal path for the ANC to ensure low latency in this path too, i.e., the digital signal from the microphone to decimated output is processed using an oversampled decimator with similar structure as the oversampled interpolator.

[00052] In the illustrated embodiment, ANC processing is performed at a 192 kHz sample rate. The audio signal is decimated by a factor of $N=16$ by decimator 418 (i.e., pull out every 16th sample) to generate the 192 kHz reference signal for ANC processing. The ANC processor 406 outputs a 192 kHz anti-noise signal, which is upsampled by a factor of $N=16$ by interpolator 420 to produce a 3.072 MHz anti-noise signal which is combined with the audio signal by adder 410. In a practical implementation, there may be included a multiplier after interpolator 420 to ensure the low frequency energy levels from section S3 and block 420 are matching. This multiplier is not shown in FIG. 4. The multiplier would typically consist of a simple shifting of the bits (e.g. shift 4 times for a multiply by 16). Thus, the interpolator 420 would not merely consist of inserting zeros between samples, but furthermore multiply every output sample by the same factor as the interpolation rate. In one embodiment, the interpolated anti-noise signal includes multiple aliased images because the signal was interpolated without filtering. Next, oversampled interpolation filters 412 (sections S5, S6, S7, S8) remove the out-of-band images from the combined signal, while allowing the audio signal to pass through unfiltered in the passband. Each of the oversampled interpolation filters 412 has a different number of internal delays (e.g., 8, 4, 2, 1) which causes the filters to run at different speeds to remove the out-of-band images, step by step. This way, the ANC signal and the audio signal will have the same group delay at all frequencies and thereby enable high-quality noise suppression.

[00053] It will be appreciated by those skilled in the art that the embodiments disclosed herein provide numerous advantages over conventional systems. The embodiments enable low and well controlled latency, independent filtering of the ANC and audio path and enable the same delay of both paths after the summation point.

[00054] In one embodiment, a word length of 24 fraction bits is used to connect directly to conventional audio components, and an internal representation of 25 bits is used that include one overflow bit. In theory, up to two overflow bits may be necessary to avoid overflow under all conditions, but in a practical implementation, one overflow bit may be enough. The audio components may be connected directly to the filter. The ANC processor may be directly connected to the filter. In one embodiment, the least significant bit (LSB) of node X3 (the node X3 is shown in subsequent figures) is set to zero in all the oversampled filters to avoid limit cycles. Tests have shown no significant deterioration in the SNR if only 22 bits are used (instead of 25 bits) given the already limited dynamic range of the chosen delta-sigma converters. It will be appreciated that, although the filter S5 to S8 has been illustrated

in the sequence {S5, S6, S7, S8} in FIG. 4, other sequences of these filters may also be used due to the oversampled natures of these filters.

[00055] Referring to Fig. 5, an embodiment of a topology of an oversampled interpolation filter will now be described. In this embodiment, a lattice wave interpolation filter 500, such as interpolation filter at section S5 of FIG. 4, receives the 16 times oversampled audio signal and anti-noise signal. The oversampled interpolation filter has same input and output sample frequency. By operating the interpolator at a higher sample rate, it is possible to remove the aliased images that will be generated by the directly interpolated signal from the ANC processor, while the original oversampled high-fidelity oversampled audio signal will pass through virtually unchanged since the aliased images have already been removed. The oversampled interpolator operates at the higher sample rate of the initial audio output times N, and is implemented by adding extra delay elements inside each filter section, i.e. each filter section includes N (illustrated in Fig. 5), N/2, N/4 etc. times the original delay elements to obtain the same frequency response as the original filter configuration operating at N, N/2, N/4 times lower sample frequency, respectively. Furthermore, this filter configuration solves practical implementation problems, because the filter elements are updated at the much higher sample rate of N times the original sample rate, thereby enabling an optimal group delay of the filters (i.e. the theoretical performance may be obtained). One can also view this solution as a generalization of traditional lattice wave filters that have an internal delay of one or two time units in each reflector section, with the general solution being any integer used for the delays.

[00056] The transfer function for this filter can be derived with reference to the node equations as follows:

$$\begin{aligned}
 Y_0 &= X_0 z^{-N} \\
 X_1 &= X_0 + X_2 z^{-2N} = X_0 + (X_1 - X_3) z^{-2N} = X_0 + X_1 z^{-2N} - X_3 z^{-2N} \\
 X_1 &= (X_0 - X_3 z^{-2N}) / (1 - z^{-2N}) \\
 X_3 &= X_2 z^{-2N} + \gamma X_1 = (X_1 - X_3) z^{-2N} + \gamma X_1 \\
 X_3(1 + z^{-2N}) &= (z^{-2N} + \gamma) X_1 = (z^{-2N} + \gamma)(X_0 - X_3 z^{-2N}) / (1 - z^{-2N}) \\
 X_3(1 + z^{-2N})(1 - z^{-2N}) + X_3(z^{-2N} + \gamma) z^{-2N} &= (z^{-2N} + \gamma) X_0 \\
 X_3 &= (z^{-2N} + \gamma) X_0 / (1 + \gamma z^{-2N})
 \end{aligned}$$

$$\text{Out} = Y_0 + X_3 = X_0 z^{-N} + X_3 = X_0(\gamma + z^{-N} + z^{-2N} + \gamma z^{-3N}) / (1 + \gamma z^{-2N})$$

For the filter illustrated in FIG. 5 with N=8,

$$\text{Out} = Y_0 + X_3 = X_0 z^{-8} + X_3 = X_0(\gamma + z^{-8} + z^{-16} + \gamma z^{-24}) / (1 + \gamma z^{-16}).$$

[00057] The value of γ will determine the filter cutoff frequency. The value of γ was first found from maximizing the attenuation in the stopband and minimizing the attenuation in the passband. However, a slightly better value can be found by optimizing the SNR of the output from a given delta-sigma converter structure, because this will also take into account the actual noise-shaping of this converter. After performing this optimization, a value of γ equal to 0.346656 was obtained. Due to the low sensitivity of lattice wave filters, this value may be approximated with a few add/shift operations using the following value: $\gamma = 1/4 + 1/16 + 1/64 + 1/128$. This approximation resulted in a decrease in the SNR of less than 0.1dB using fixed point arithmetic as compared to using floating point multiplication and the optimal value of γ . In this manner, a full multiplication operation can be replaced with 3 additions while the shifts may be hardwired, thereby saving significant silicon real estate and power. In this implementation a nonlinearity is deliberately introduced by setting the least significant bit (LSB) output from node X_3 to zero to avoid limit cycle problems resulting in spurious small amplitude oscillations in the filter. The frequency response and group delay of the eight times oversampled interpolator of FIG. 5 are illustrated in FIGs. 6A and 6B, respectively.

[00058] Referring to Fig. 7 an embodiment of an oversampled interpolator topology 700 suitable for use in section S6 of FIG. 4 is illustrated. As illustrated, the lattice wave interpolation filter is oversampled four times and the transfer function is calculated as ($N=4$):

$$\text{Out} = Y_0 + X_3 = X_0 z^{-4} + X_3 = X_0(\gamma + z^{-4} + z^{-8} + \gamma z^{-12}) / (1 + \gamma z^{-8})$$

This filter behaves like a filter with unit delays running at four times the original sample frequency and allows processing of signals that are oversampled four times. The frequency response and group delay of the interpolator of FIG. 7 are illustrated in FIGs. 8A and 8B, respectively.

[00059] Referring to Fig. 9, an embodiment of an oversampled interpolator topology 900 suitable for use as filter S7 of FIG. 4 is illustrated. As illustrated, the lattice wave interpolation filter is oversampled two times and the transfer function is calculated as follows ($N=2$):

$$\text{Out} = Y_0 + X_3 = X_0 z^{-2} + X_3 = X_0(\gamma + z^{-2} + z^{-4} + \gamma z^{-6}) / (1 + \gamma z^{-4})$$

The frequency response and group delay of the two times oversampled interpolator of FIG. 9 are illustrated in FIGs. 10A and 10B, respectively.

[00060] Referring to Fig. 11, an embodiment of an oversampled interpolator topology 1100 suitable for use in section S8 of FIG. 4 is illustrated. As illustrated, the final lattice

wave interpolation filter is a direct filter (i.e., no oversampling) and the transfer function is calculated as ($N=1$):

$$\text{Out} = Y_0 + X_3 = X_0 z^{-1} + X_3 = X_0(\gamma + z^{-1} + z^{-2} + \gamma z^{-3}) / (1 + \gamma z^{-2})$$

The frequency response and group delay of the direct interpolator of FIG. 11 are illustrated in FIGs. 12A and 12B, respectively.

[00061] The combined response of the entire filter chain (i.e. sections S5-S8 of FIG. 4) is illustrated in FIGs. 13A-E. FIGs. 13A-C illustrate the overall frequency response at various audio bands. FIGs. 13D-E illustrate the overall group delay through the entire filter chain, assuming a sample frequency of 3072 kHz. Referring to FIG. 13E, it can be seen, that the group delay variation within the audio band 0-20 kHz may vary between 4.87 to 4.99 μs (14.95 to 15.34 input samples), or less than 3%, in an embodiment.

[00062] Referring to FIG. 14, an example filter arrangement 1400 for use as a decimator will now be described. In this embodiment, the low latency oversampled interpolation filter of the present disclosure is used as an oversampled decimator filter. One difference from the interpolation filter is that the output is decimated by a factor of 16. The figure shows an example configuration, where the signals take different paths to ensure the combination of low latency and high-quality audio is maintained. In various embodiments, it is possible to implement a decimation filter with almost the same latency but lower gate count by implementing all sections with $N=1$ and using multi-stage multi-rate signal processing, where each stage reduces the sample rate by a factor of two (i.e. running the sections at 3072, 1536, 768 and 384 kHz) or running an oversampled decimator at a lower frequency, e.g. 1536 or 768 kHz, because most of the delay occur in the sections with a high number of internal delays. Similarly, if allowing to compromise the high-quality audio very slightly, it is possible to perform the summation of audio and ANC signal at a lower frequency than the final output, e.g. at 1536 kHz with a final output of 3072 kHz and thereby obtain significantly lower gate count and lower power consumption. Furthermore, it is possible to design a multi-stage, multi-rate interpolator where each stage upsamples a signal by a factor of two using the same ($N=1$) low delay lattice wave filter. This has the advantage of lower gate count, but a slightly higher delay, due to slight delays between the sections in a practical implementation.

[00063] Referring to Fig. 15, a measurement of group delay will now be described in accordance with an embodiment of the present disclosure. The group delay can be measured using a single sine wave (e.g. a 1 kHz tone) or using multiple sine waves (e.g., in the range 1-95 kHz). To analyze the group delay of a single sine wave, a simple plot may be made of the

input and output of an oversampled sine wave (1 kHz, sampling frequency 3072 kHz). A computer program can be prepared to compare the input sine wave with the output, such as by manual comparison using a zoom function to zoom in on the graph. Alternatively, the group delay can be calculated accurately using a program that uses a band of frequencies (e.g. 1-95 kHz, each tone spaced 1 kHz apart) and calculates the group delay using spectral methods (e.g., estimation of the phase of the input and output data). The original input is compared against the output and the group delay may be provided as a function of frequency. The phase as a function of frequency can be obtained by performing a fast Fourier transform (FFT) on the input and output data and subtracting these values. To avoid problems with phase aliasing, the phase ϕ may be unwrapped before used for calculation of the group delay. The group delay ΔT can be calculated from $\Delta T = -\phi/(2\pi f)$, where f is the frequency.

[00064] Referring to FIGs. 16A-C, an embodiment of a decimator will now be described. FIG. 16A illustrates a decimator 1600 arranged to receive a digital audio input from an analog to digital converter and output an audio signal at a reduced sampling rate by a factor of two. The illustrated embodiment shows additional components included when performing decimation to avoid problems with internal overflow during processing. A first stage 1602 is illustrated in FIG. 16B and includes a sign extension to 22 bits, i.e. extending the most significant bit (MSB) to avoid overflow and setting the lowest bits to zero to act as an interface between the limited number of bits from the converter and the internal precision used in the filter. The decimator 1600 is arranged similar to the interpolator of FIG. 11 except the two processing paths (Y_0 and X_0) may be calculated at half the input sample rate to reduce power consumption. The double delay Z^{-2} following node X_2 may even be implemented using a single delay element updated at half the input sample rate to save register space and power. In the illustrated embodiment, all nodes of the decimator 1600 are 22 bits, including 2 overflow bits and 20 fractional bits. In one embodiment, the value of $\gamma_1 = 1/4 + 1/16 + 1/64 + 1/128$, and is used for a multiplication free topology. The last stage includes a limiter 1604 (illustrated in FIG. 16C) which provides hard clipping and generates a 20 bits output. The limiter works by checking if the three highest bits are equal. If this is the case, the original lower bits are copied directly to the output. However, if the three upper bits are not all the same, an overflow condition has been detected and all lower bits will be the inverted value of the MSB, to signify the most extreme value that is possible with a two's complement notation. Other values of the number of overflow bits can be chosen.

[00065] Referring to FIGs. 17A-C, an embodiment of an interpolator will now be described. FIG. 17A illustrates an interpolator 1700 arranged to receive a digital audio input from an adaptive noise cancellation processor to output an audio signal having a higher sampling rate by a factor of two. The illustrated embodiment shows additional components included when performing interpolation to avoid problems with overflow during processing. A first stage 1702 (also referred to herein as a sign extension stage) is illustrated in FIG. 17B and includes a sign extension to 22 bits (i.e. extending the MSB and setting the lowest bits to zero). In the illustrated embodiment, all nodes of the interpolator 1700 are 22 bits, including 2 overflow bits and 20 fractional bits. In one embodiment, the value of $\gamma_1 = 1/4 + 1/16 + 1/64 + 1/128$, and is used in a multiplication free implementation. The last stage includes a limiter 1704 (illustrated in FIG. 17C and similar to FIG. 16C) which provides hard clipping and generates a 20 bits output.

[00066] Referring to FIG. 18, a generalized oversampled lattice wave filter topology 1800 is illustrated, in accordance with one or more embodiments. As illustrated, the generalized filter topology 1800 shows a structure (two-port adaptor) with multiple delay elements inside (delay N, 2N). In operation, the oversampled filter includes xN delay elements (e.g. 2x, 4x, 8x, 16x, etc.), and the filter is run at a higher frequency than required by the Nyquist sampling criterion. The input stream is perceived as many streams coming through at a lower frequency and the signal “bubbles” through these delays. For example, to process the signals at twice the original anticipated sample rate the filter may include twice the delays and run at twice the rate. As a recursive system, the signal rotates around the system allowing the filter to process an oversampled signal because of the extra delays. In various embodiments, the concepts disclosed herein may be extended to include delays (M, N) and (N, 2N) might be used, where M and N are arbitrary positive integers. In other words, this works like a polyphase IIR filter.

[00067] Various implementation embodiments will now be described with referenced to FIGs. 19-22. FIG. 19A illustrates a decimator 1900 using a lattice wave filter structure. FIG. 19B illustrates an interpolator 1950 using a lattice wave filter structure. As illustrated in FIGs. 19A & B, each path represents one or more cascaded allpass filters (based on two-port adaptors) that pass through all frequencies. In various embodiments, the allpass filter is a filter with a unity response that changes the signal only in phase. FIG. 20A illustrates a single section (a single two-port adaptor) 2000 of a lattice wave filter, and FIG. 20B illustrates an example implementation of a two-port adapter 2050. FIGs. 21 and 22 illustrate

embodiments in which the number of delay elements may be an arbitrary number (e.g., $N > 2$). FIG. 21 illustrates a general lattice wave filter structure 2100 for an oversampled

decimator/interpolator having multiple delay elements and multiple allpass filters. As illustrated the order of the filter is $N(2K+3)+M$. By choosing more delay elements than two, multiple mirror images of the original transfer function may be obtained, even though these are recursive filters. This may be used for efficient and fast filter structures. FIG. 22

illustrates a general lattice wave filter structure 2200 for an oversampled decimator/interpolator having multiple filters that process outputs from other filters. By using more than one or two delay elements, multiple mirror images may be obtained that may be beneficial for direct decimation or interpolation of factors higher than a value of two. In some embodiments, high pass filters may be obtained using similar approaches by subtracting instead of adding the two filter paths at the final output node.

[00068] In the previous embodiments, a particular structure of an oversampled lattice wave filter has been presented. It is well known within the open literature that many topologies of the original lattice waveform filter exist (see, e.g., L. Gasci, "Explicit Formulas for Lattice Wave Digital Filters", IEEE Trans. Circuits and Systems, Jan 1985, Fig.9, for multiple examples of two-port adaptors). The embodiments should not be limited to the topology described here but also include all that have previously been described, e.g., including the multiple delay elements in these existing structures with an oversampling factor higher than two or the use multiple delay element, where the number is higher than two in general applications.

[00069] Where applicable, various embodiments provided by the present disclosure may be implemented using hardware, software, or combinations of hardware and software. Also, where applicable, the various hardware components and/or logic components set forth herein may be combined into composite components comprising software, hardware, and/or both without departing from the scope of the present disclosure. Where applicable, the various hardware components and/or logic components set forth herein may be separated into sub-components comprising software, hardware, or both without departing from the scope of the present disclosure. In addition, where applicable, it is contemplated that software components may be implemented as hardware components and vice versa.

[00070] The foregoing disclosure is not intended to limit the present disclosure to the precise forms or particular fields of use disclosed. As such, it is contemplated that various alternate embodiments and/or modifications to the present disclosure, whether explicitly described or implied herein, are possible in light of the disclosure. For example, although the

low delay decimators and low delay interpolators disclosed herein are described with reference to adaptive noise cancellation systems, it will be appreciated that the low delay filters disclosed herein may be used in other signal processing systems. Having thus described embodiments of the present disclosure, persons of ordinary skill in the art will recognize that changes may be made in form and detail without departing from the scope of the present disclosure. Thus, the present disclosure is limited only by the claims.

CLAIMS

What is claimed is:

1. A system comprising:
 - an audio sensor operable to sense environmental noise and generate a noise signal;
 - an audio processing path operable to receive an audio signal, process the audio signal through an interpolation filter, and generate a primary audio signal having a first sample frequency;
 - an adaptive noise cancellation processor operable to receive the noise signal and generate a corresponding anti-noise signal;
 - a direct interpolator operable to receive the anti-noise signal and generate an upsampled anti-noise signal having the first sample frequency;
 - an adder operable to receive and combine the primary audio signal and the upsampled anti-noise signal and generate a combined output signal; and
 - a low latency filter operable to process the combined output signal.
2. The system of claim 1, wherein the low latency filter comprises a plurality of filters, each performing filtering at a different sample frequency.
3. The system of claim 2, wherein the low latency filter comprises a plurality of lattice wave filters disposed in a cascaded arrangement, wherein each of the plurality of lattice wave filters processes a different frequency band.
4. The system of claim 3, wherein the sample frequency is increased in integer steps in each successive filter.
5. The system of claim 3, wherein the lattice wave filters include a plurality of delay elements; and wherein direct sampling at a particular output sample frequency is achieved by interlacing multiple filters.
6. The system of claim 5, wherein N delay elements are provided in reflector sections (two-port adaptors) and one path is delayed by N/2 delay elements, and another path

is directly connected to an input signal; and wherein N is a sequence of positive integer exponents of 2.

7. The system of claim 3, wherein each lattice wave filter comprises two paths, including one path including a plurality of reflector elements (two-port adaptors) with each reflector element delayed by N unit delays, where N is an integer greater than one, and one path delayed by M delay elements, where M is an integer greater than one.

8. The system of claim 1, wherein the adaptive noise cancellation processor is further operable to derive the anti-noise signal by calculating filter coefficients using by a filtered-X least mean squares process.

9. The system of claim 1 wherein the direct interpolator comprises a sign extension stage operable to extend most significant bits of the anti-noise signal to avoid overflow, and a limiter operable to provide clipping to reduce a number of bits in the upsampled anti-noise signal.

10. A system comprising:
a first lattice wave filter comprising
a first path including a plurality of reflector elements (two-port adaptors) with each reflector element delayed by N delay elements, where N is an integer greater than two;
and
a second path delayed by M delay elements, where M is an integer greater than one.

11. The system of claim 10, further comprising an adaptive noise cancellation system comprising:

an audio processing path operable to receive and process a primary audio signal having a first sample frequency;

an adaptive noise cancellation path comprising a decimator operable to downsample the primary audio signal to a second sampling frequency, an adaptive noise cancellation processor operable to receive the primary audio signal and a noise signal at the second sample frequency and generate an anti-noise signal having the second sample frequency, and an interpolator operable to upsample the anti-noise signal to the first sample frequency; and

an adder operable to combine the anti-noise signal and the primary audio signal at the first sample frequency; and

wherein the decimator comprises the first lattice wave filter, and the interpolator comprises a second lattice wave filter having two paths with N delay elements and M delay elements, respectively.

12. The system of claim 11, further comprising a microphone operable to sense environmental noise and generate corresponding electrical signals; and a low delay decimator to generate the noise signal at the second sample frequency.

13. The system of claim 11, further comprising an oversampled interpolation filter that has input and output sample frequencies that match the first sample frequency; and
wherein the oversampled interpolation filter is operable to remove aliased images generated by the interpolator in the adaptive noise cancellation path.

14. The system of claim 11, wherein the first lattice wave filter and the second lattice wave filter each comprise a multi-stage lattice wave filter structure where each stage changes an operating sample rate by a factor of two.

15. The system of claim 14, wherein the decimator and interpolator each comprise a sign extension stage operable to extend most significant bits of a received signal to avoid overflow, and a limiter operable to provide clipping to reduce a number of output bits.

16. A method comprising
sensing environmental noise and generating a noise signal;
processing an audio signal through an interpolation filter to generate a primary audio signal having a first sample frequency;
generating, from the noise signal, an anti-noise signal having a second sample frequency;
directly interpolating the anti-noise signal to generate an upsampled anti-noise signal having the first sample frequency;
combining the primary audio signal and the upsampled anti-noise signal to produce a combined output signal; and
processing the combined output signal through a low latency filter.

17. The method of claim 16, wherein filtering comprises applying a plurality of lattice wave filters disposed in a cascaded arrangement, wherein each of the plurality of lattice wave filters processes a different sample frequency that is successively changed in each successive filter.

18. The method of claim 16, wherein directly interpolating includes extending most significant bits of the anti-noise signal to avoid overflow, and clipping to reduce a number of output bits in the upsampled anti-noise signal

19. The method of claim 16, further comprising decimating the primary audio signal to downsample the primary audio signal to the second sample frequency; and wherein the generating, from the noise signal, the anti-noise signal having the second sample frequency further includes analyzing the downsampled primary audio signal.

20. The method of claim 16, wherein generating, from the noise signal, the anti-noise signal having the second sample frequency comprises calculating filter coefficient using a filtered-X least mean squares process.

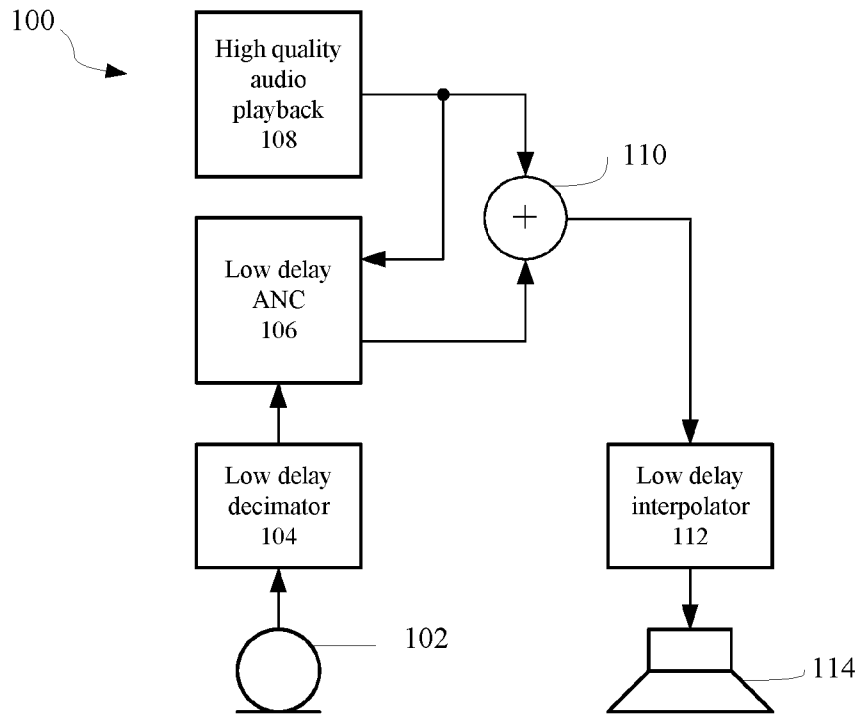


FIG. 1

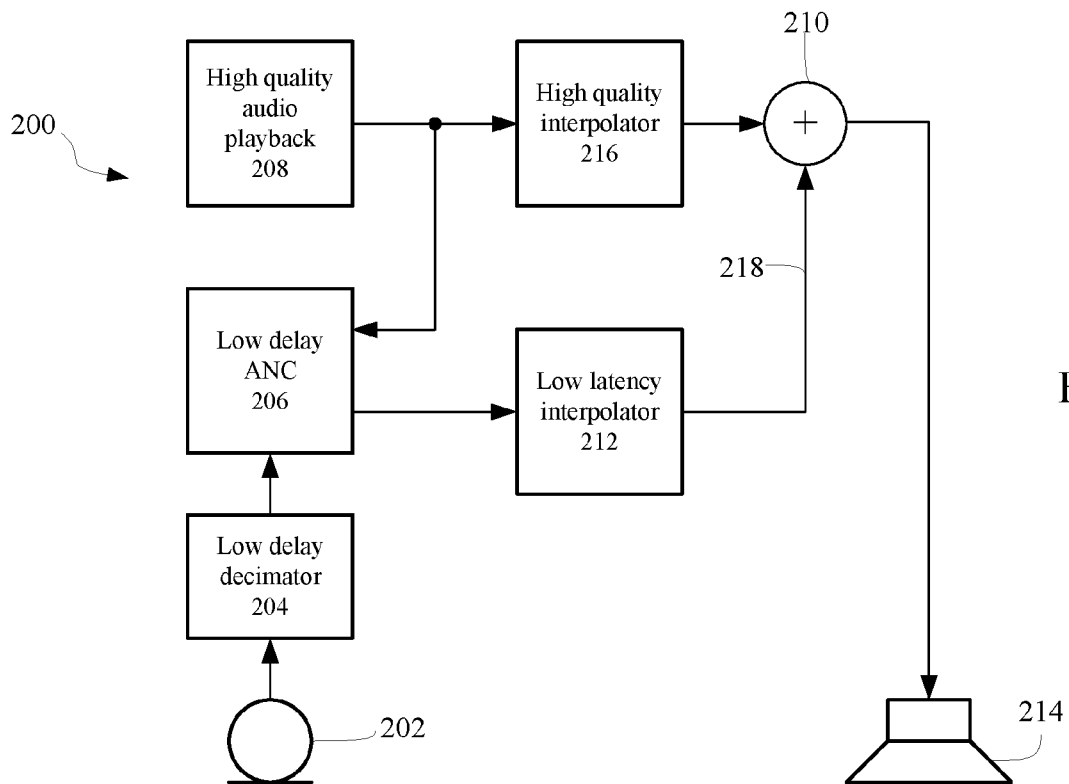


FIG. 2

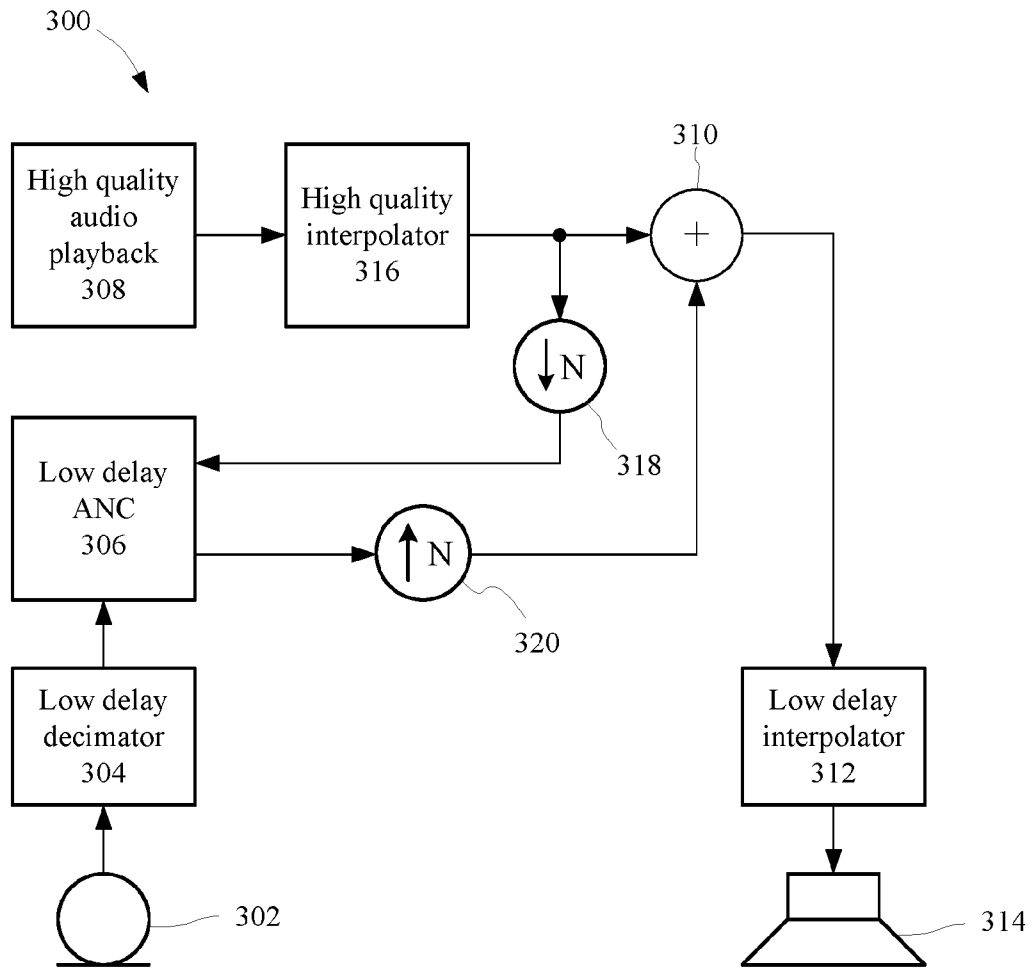


FIG. 3

3/22

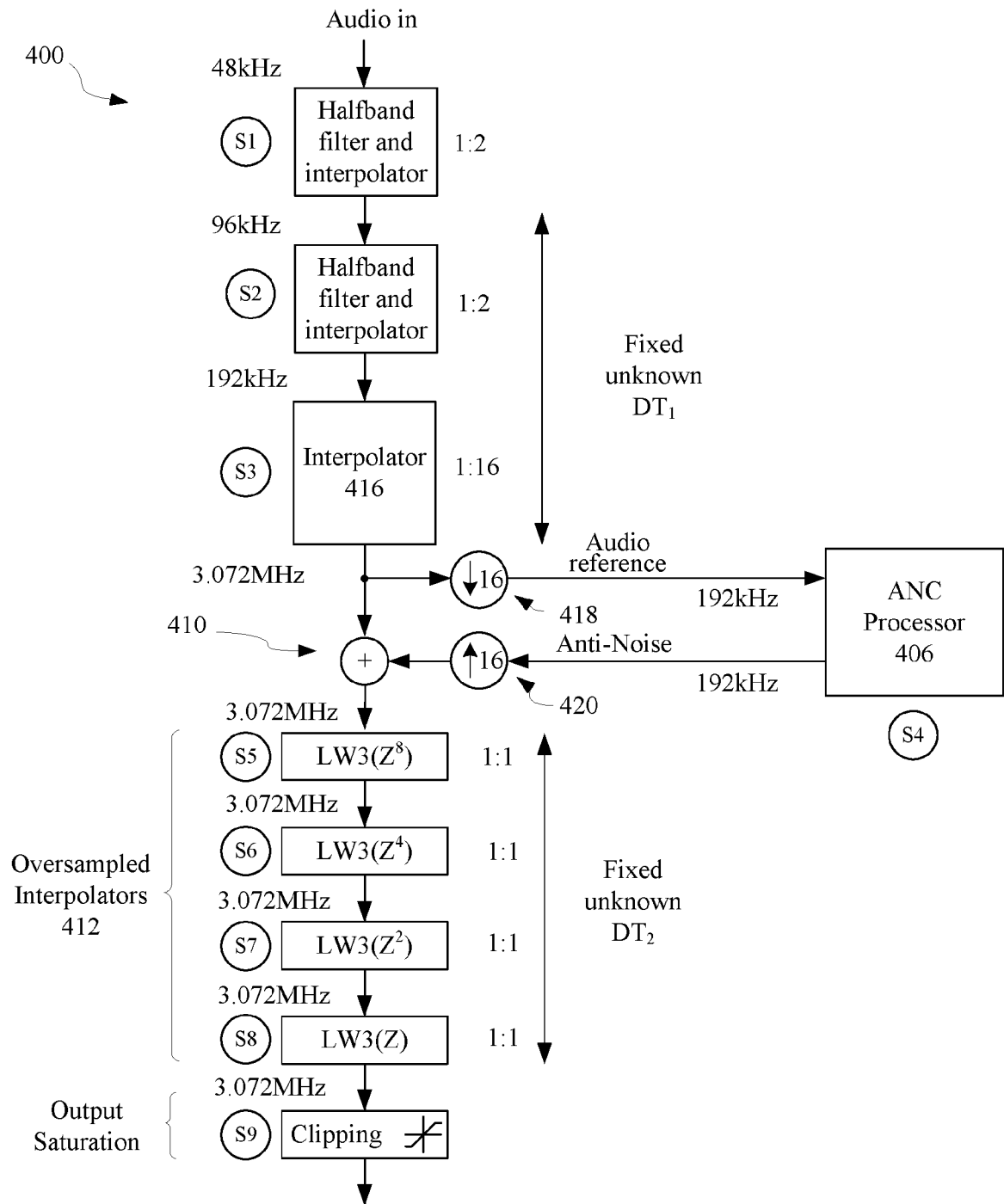


FIG. 4

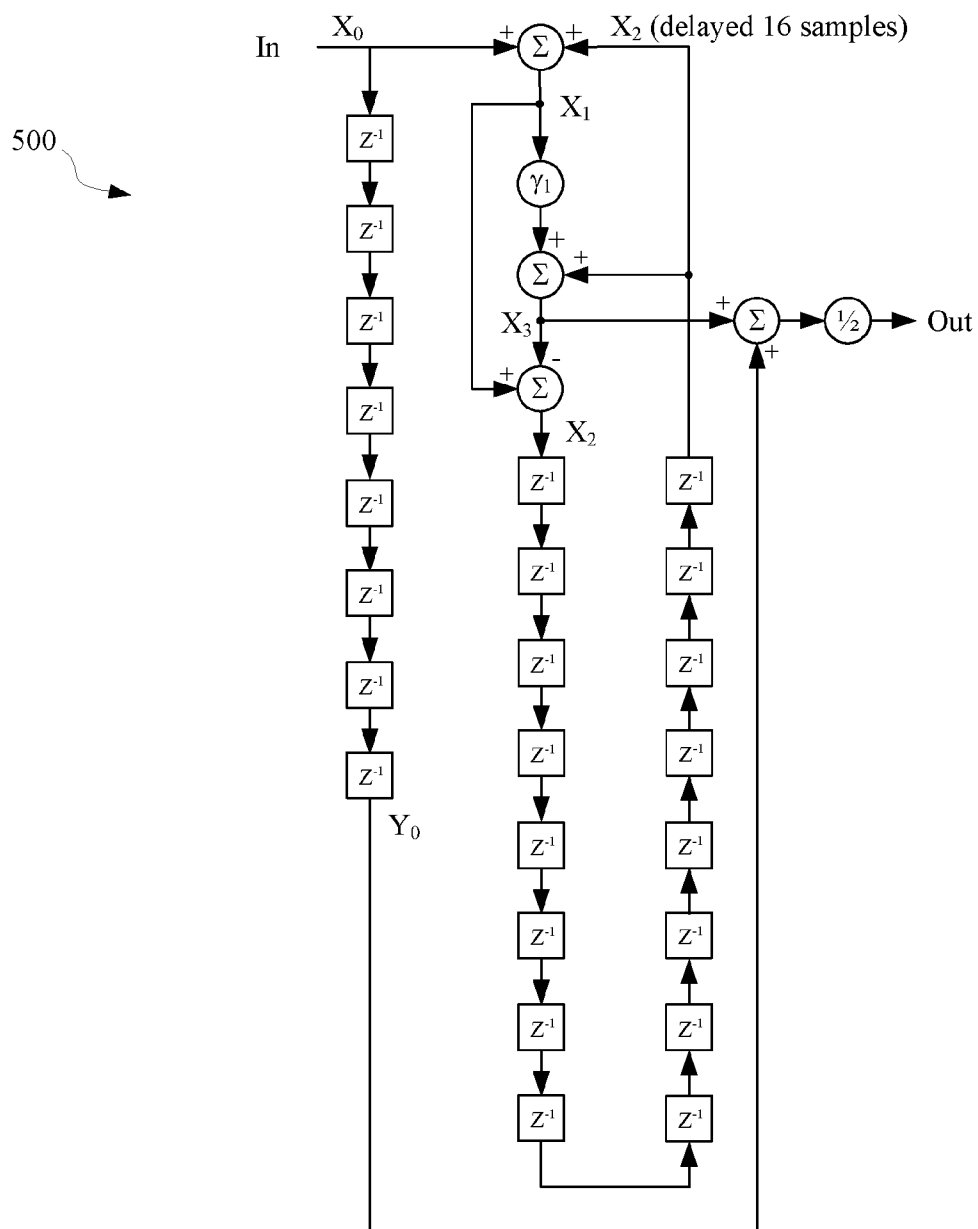


FIG. 5

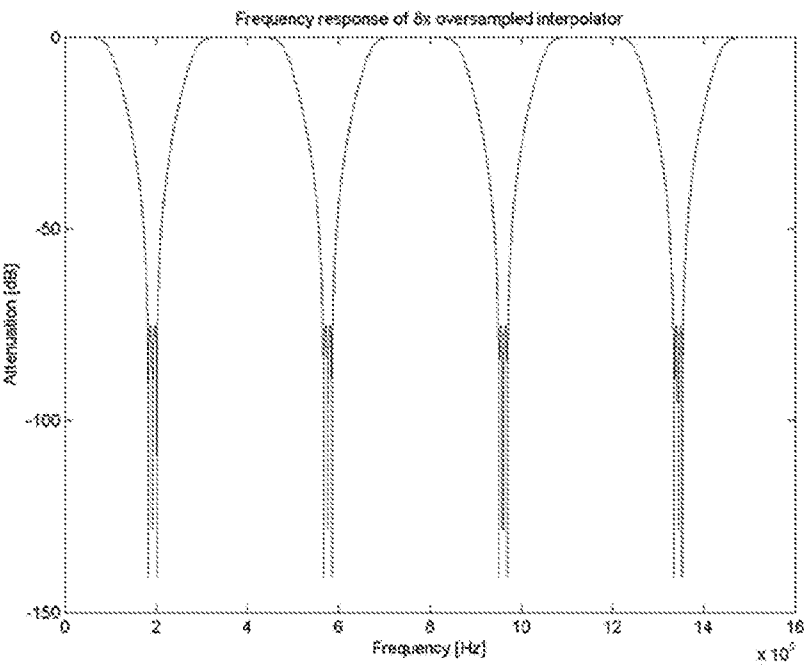


FIG. 6A

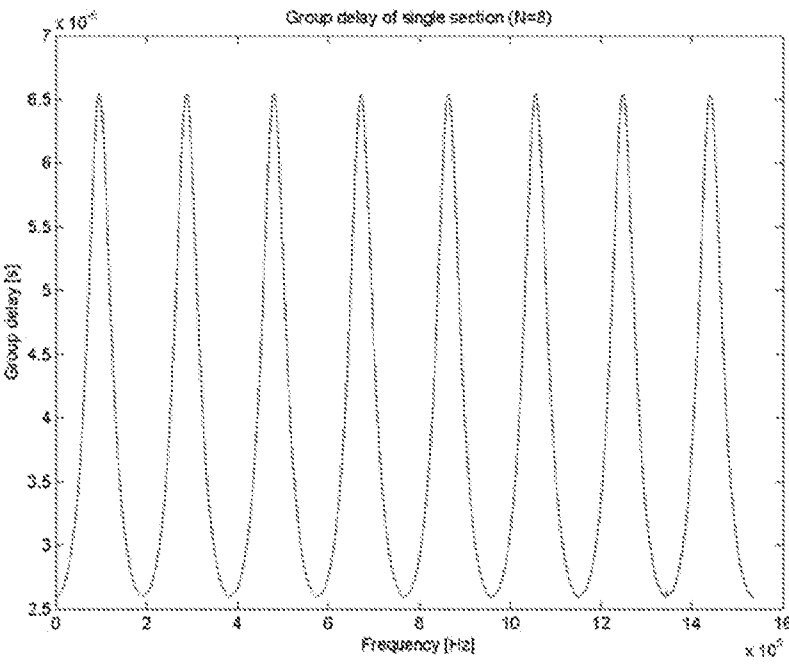


FIG. 6B

6/22

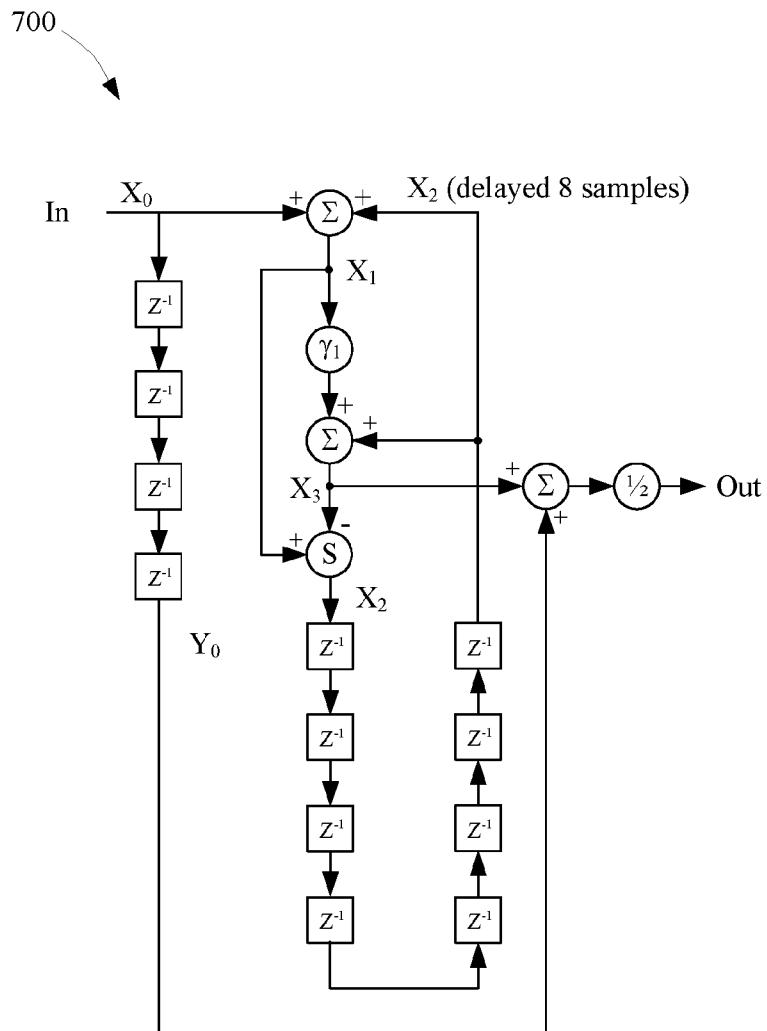


FIG. 7

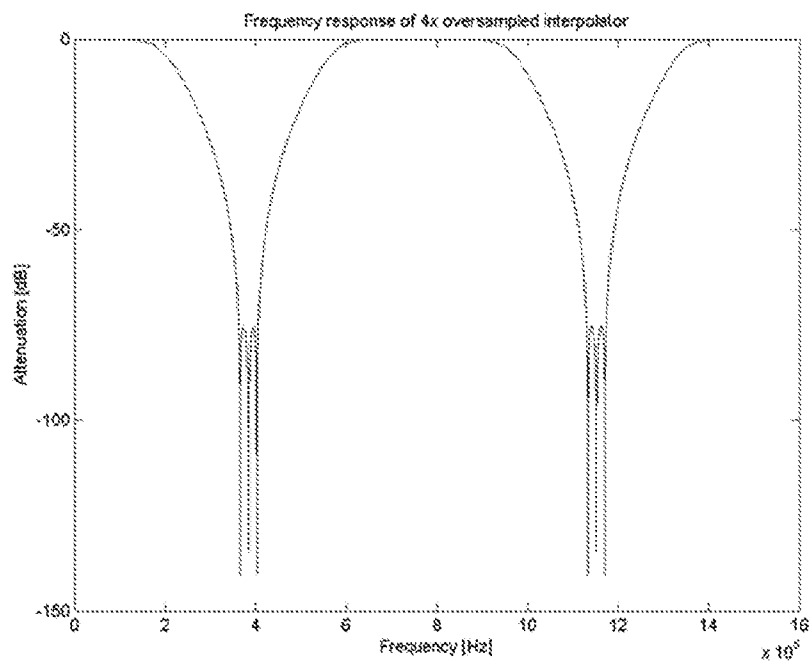


FIG. 8A

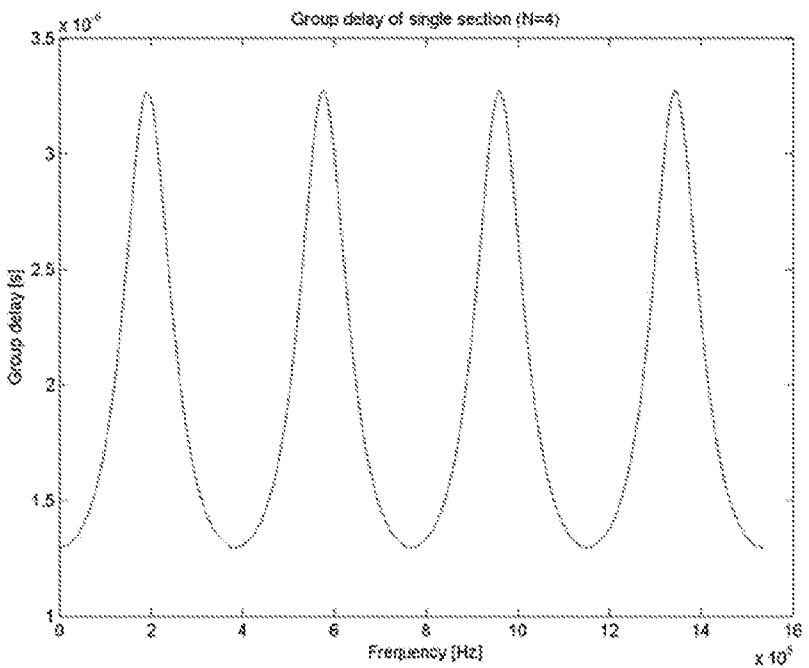


FIG. 8B

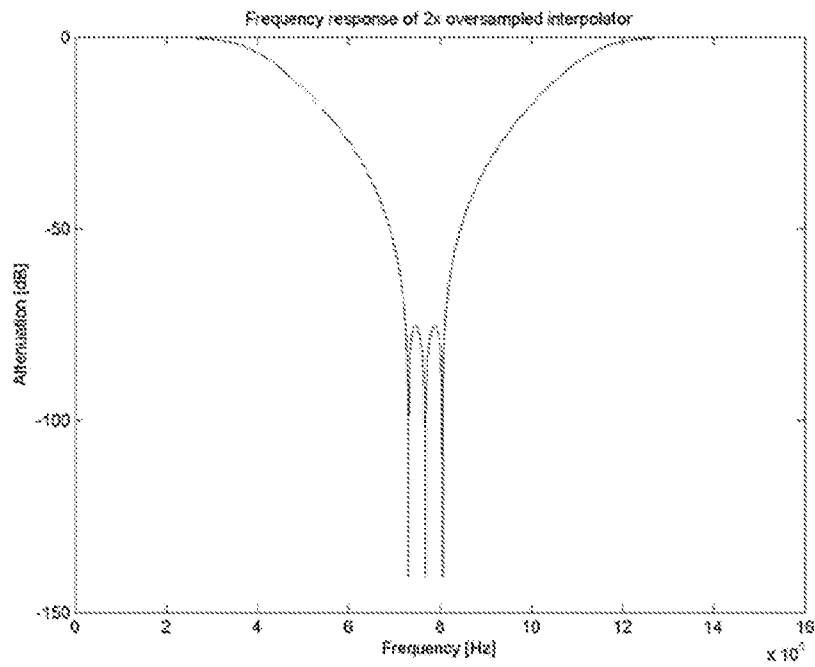


FIG. 10A

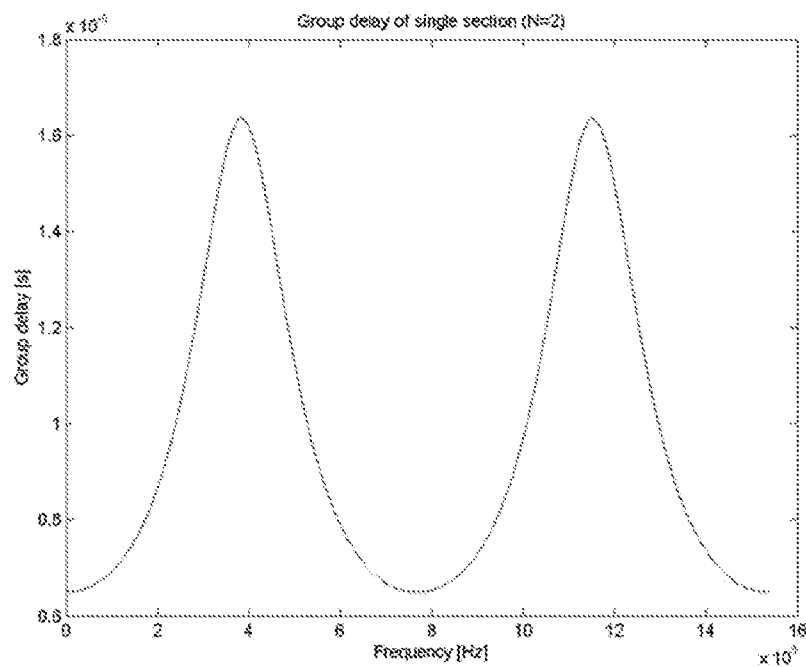


FIG. 10B

10/22

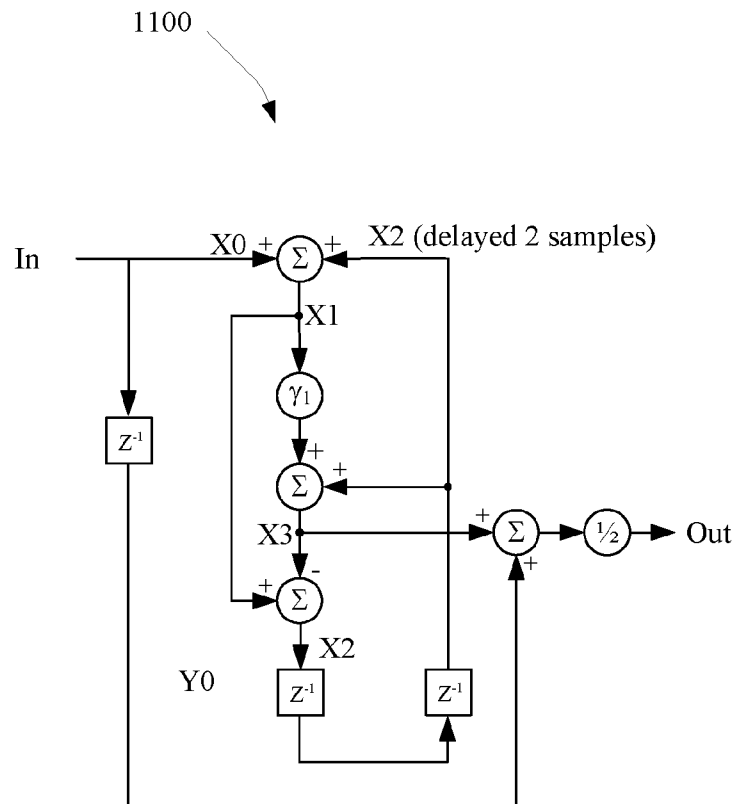


FIG. 11

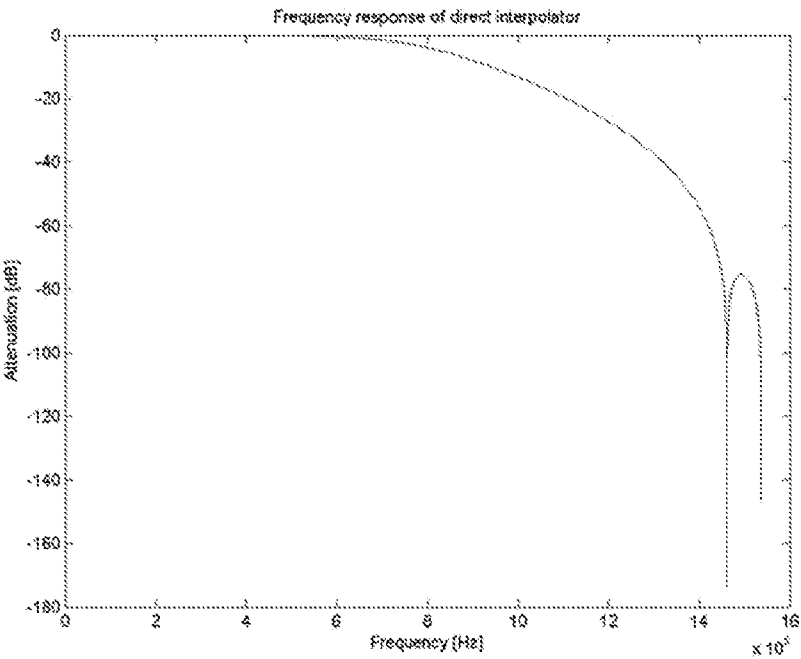


FIG. 12A

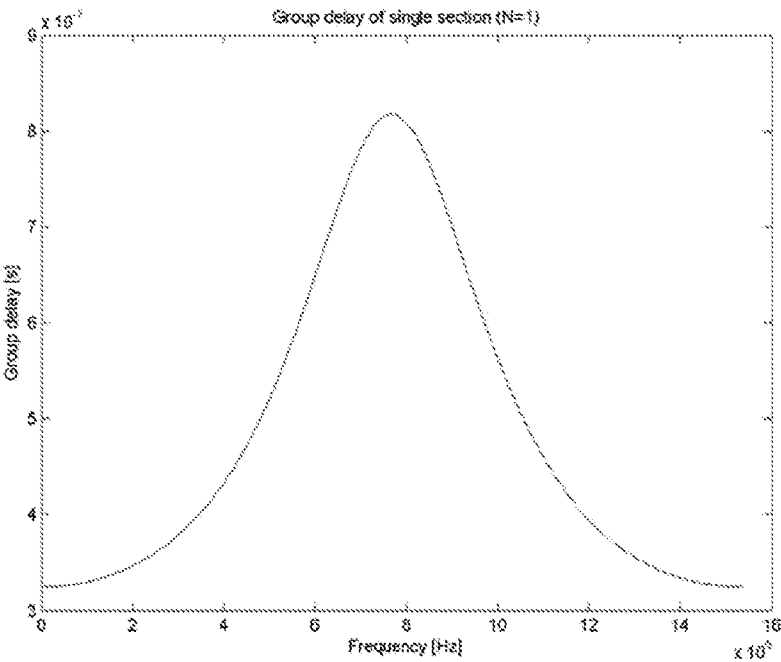


FIG. 12B

Overall frequency response 0-1536 kHz

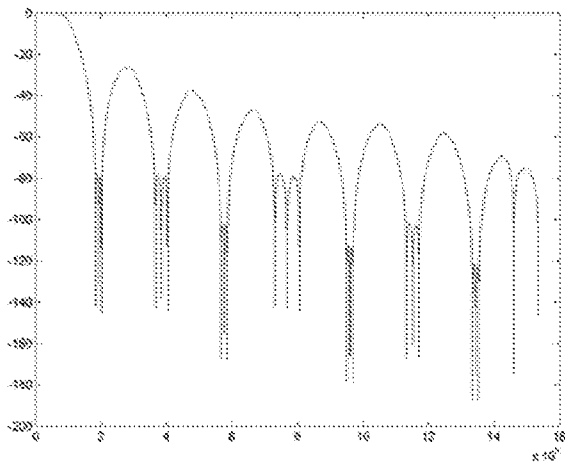


FIG. 13A

Overall frequency response 0-384kHz

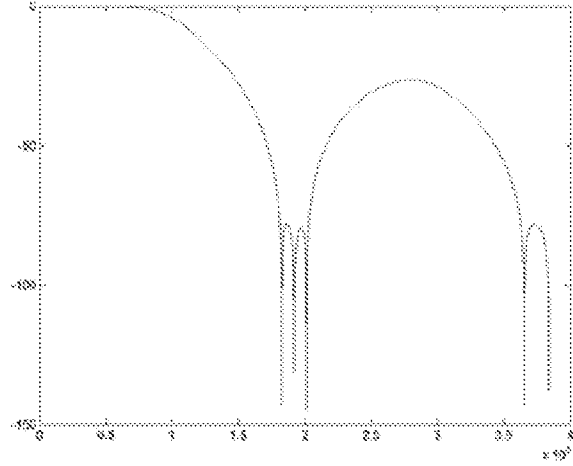


FIG. 13B

Overall frequency response 0-20kHz

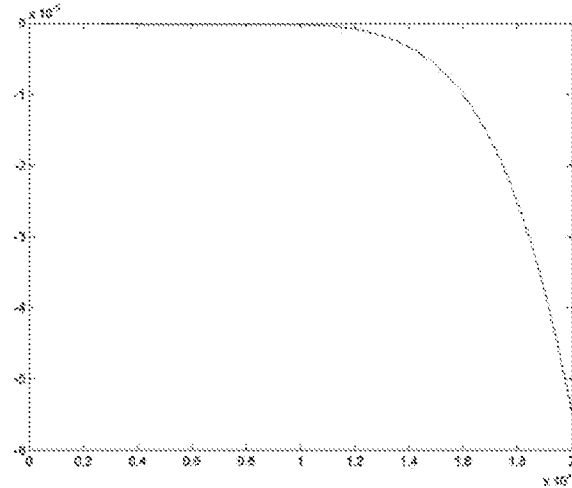


FIG. 13C

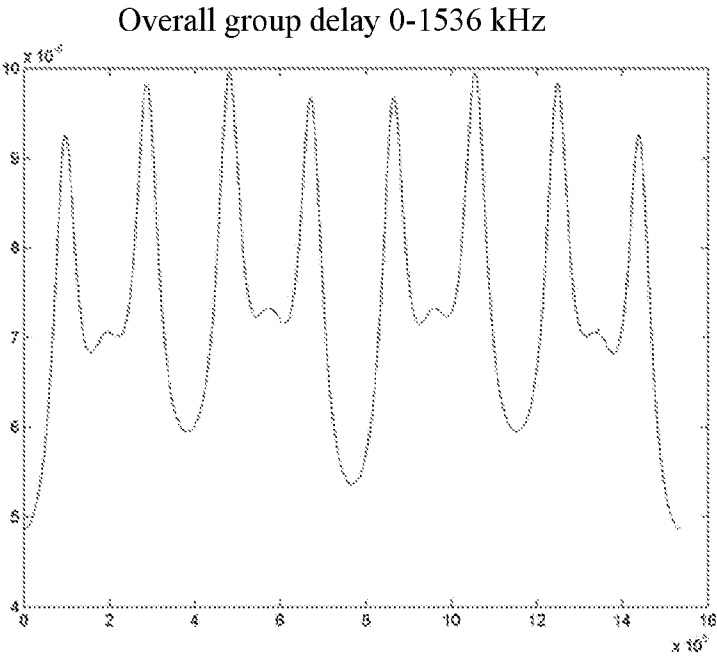


FIG. 13D

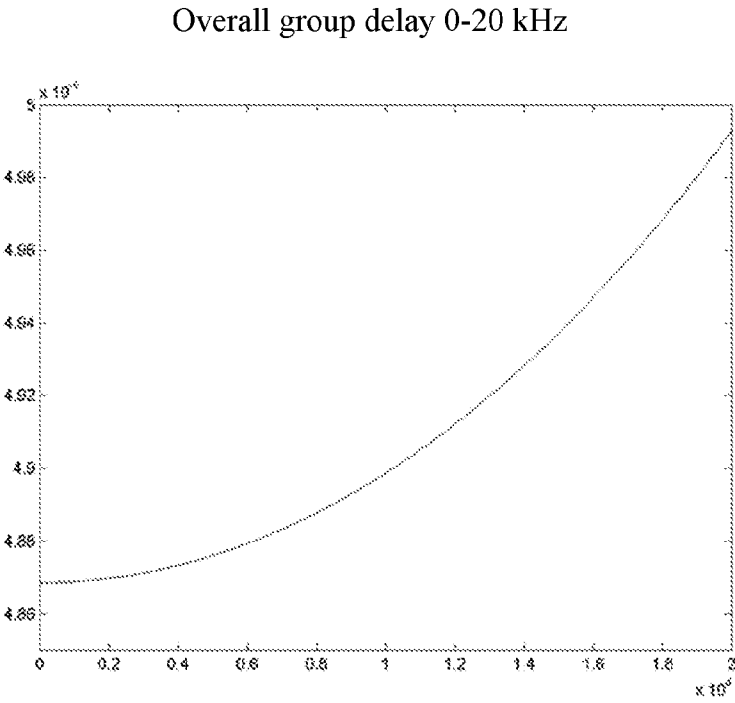


FIG. 13E

14/22

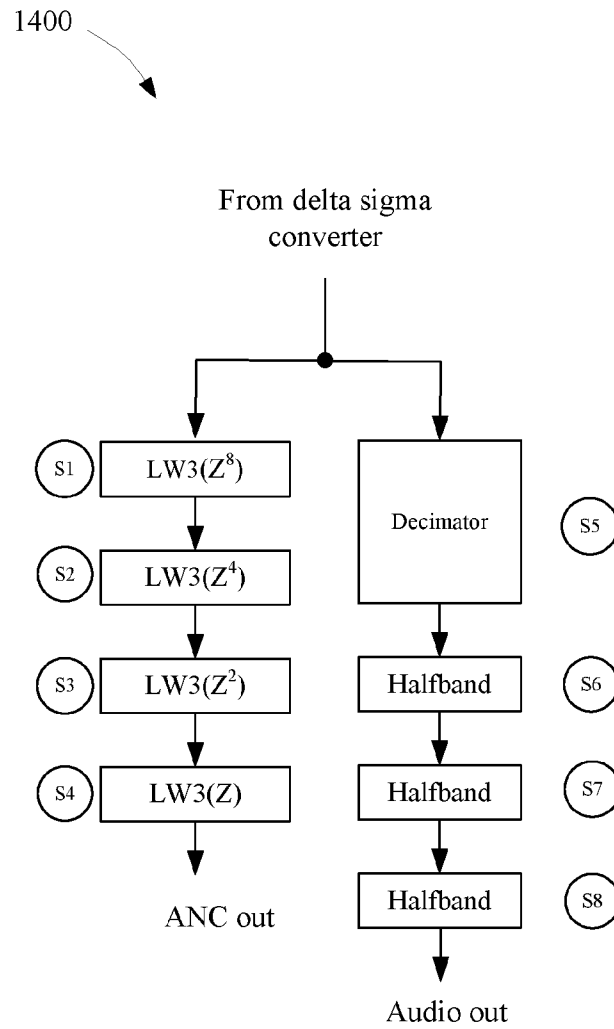


FIG. 14

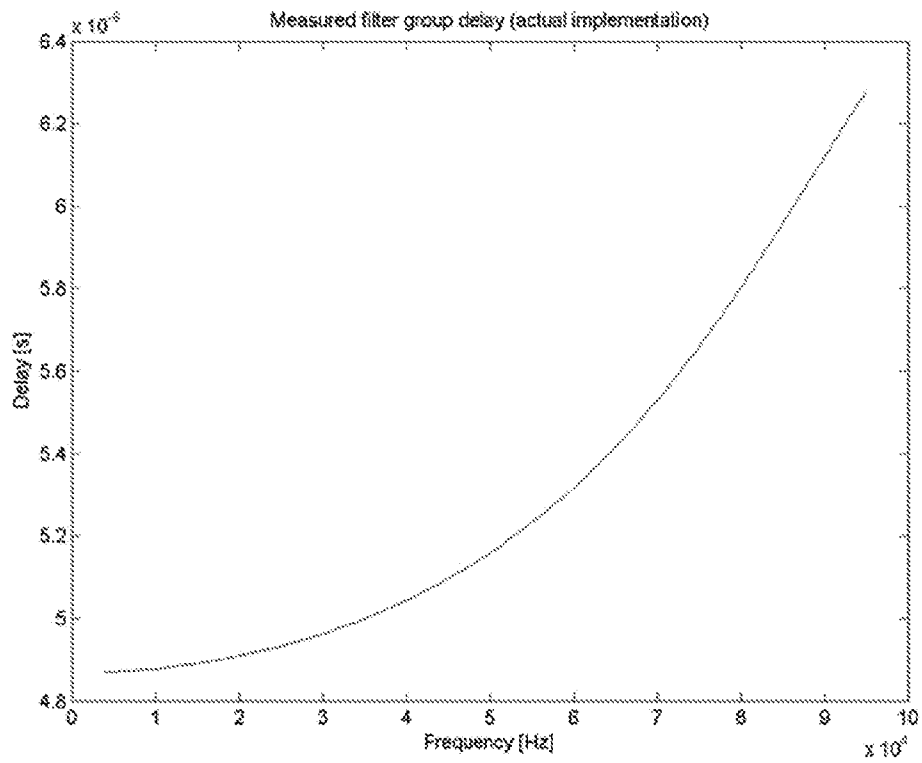


FIG. 15

16/22

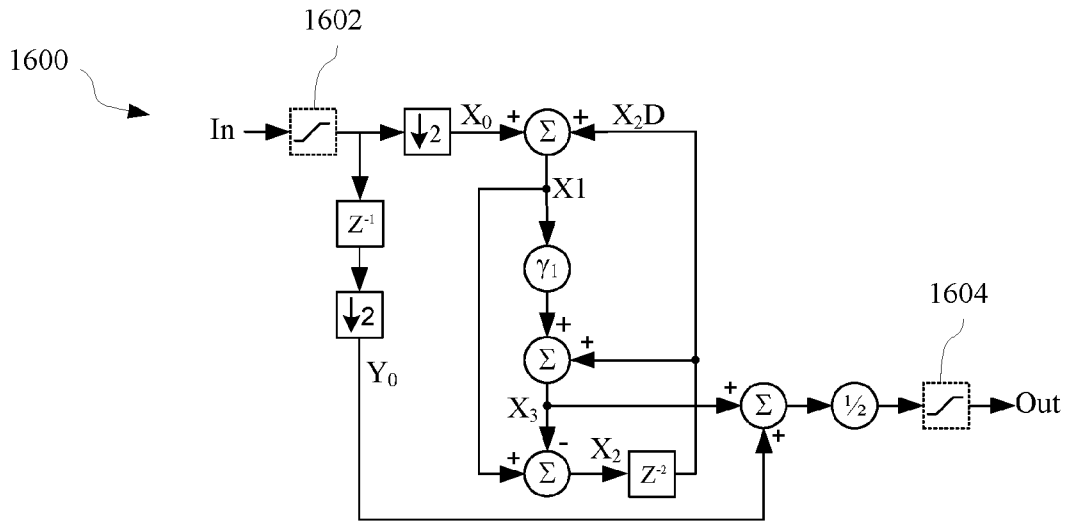


FIG. 16A

1602

First stage, sign extension

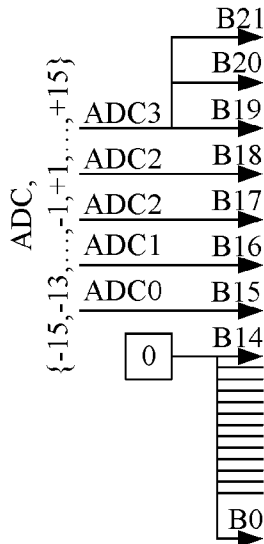


FIG. 16B

Last stage, limiter

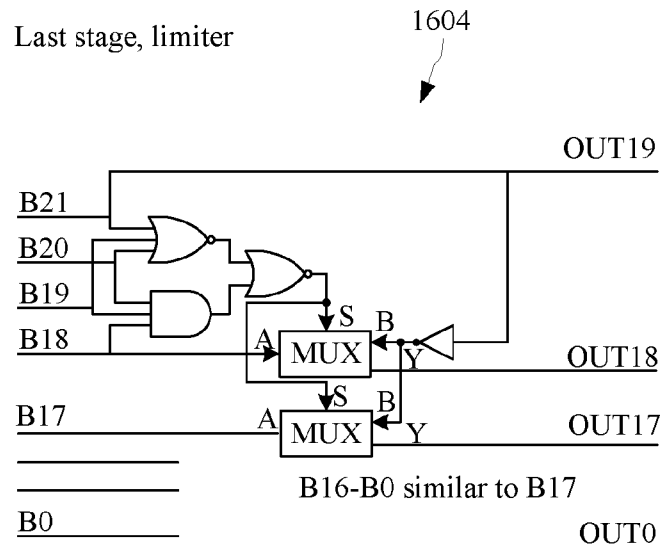


FIG. 16C

17/22

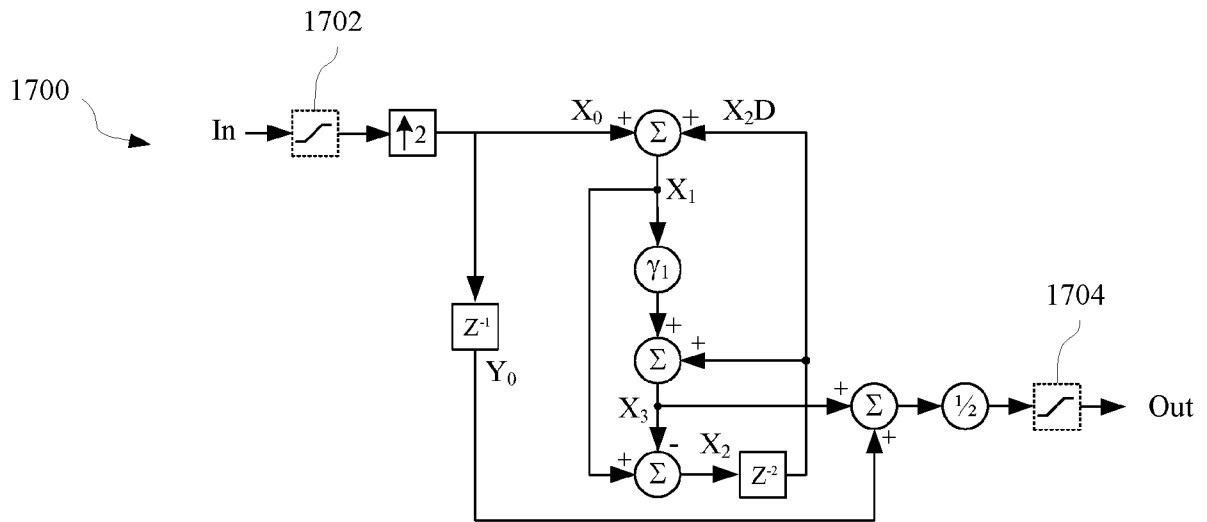


FIG. 17A

1702

First stage, sign extension

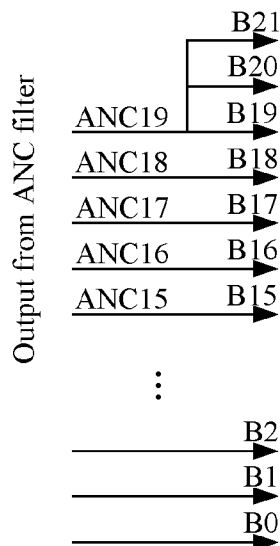


FIG. 17B

Limiter (last stage only)

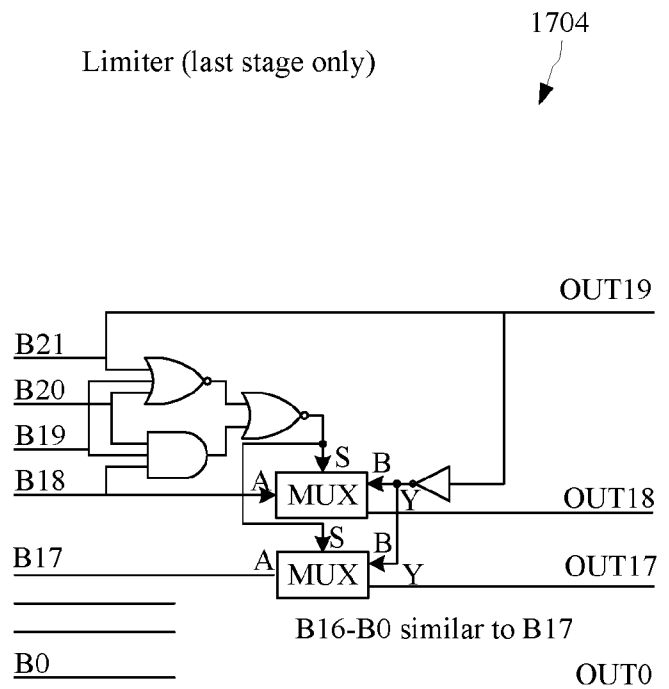


FIG. 17C

1704

1800

Oversampled lattice wave filter for interpolation
and decimation, N is an integer

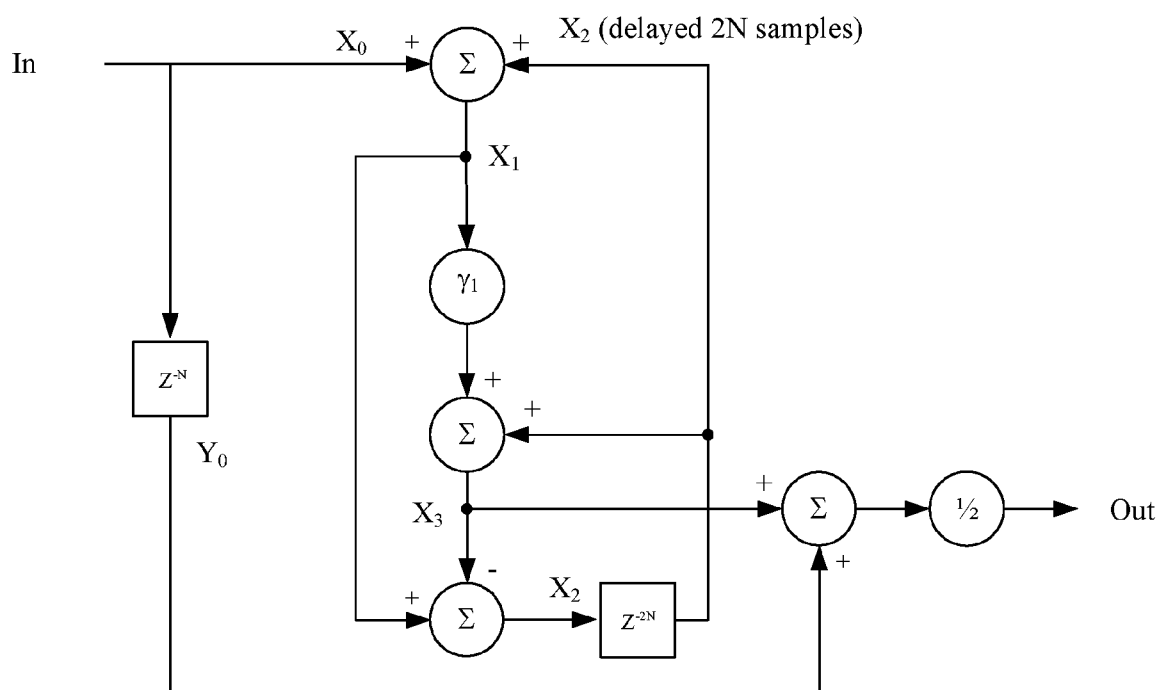


FIG. 18

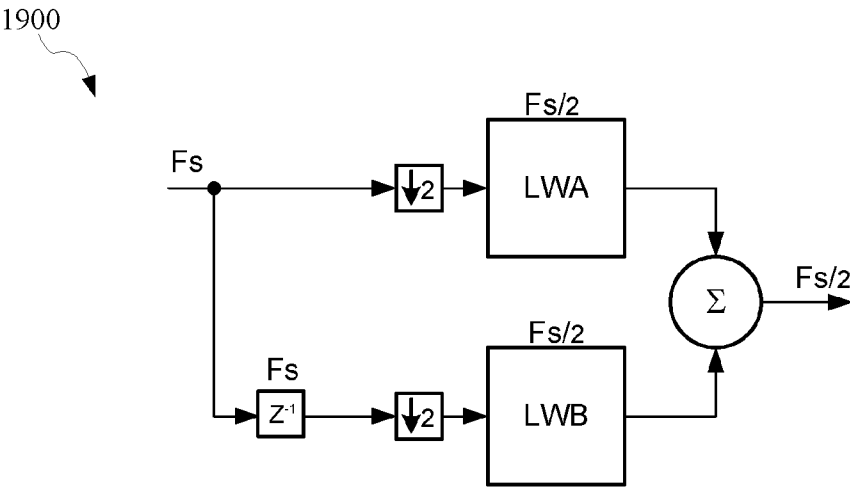


FIG. 19A

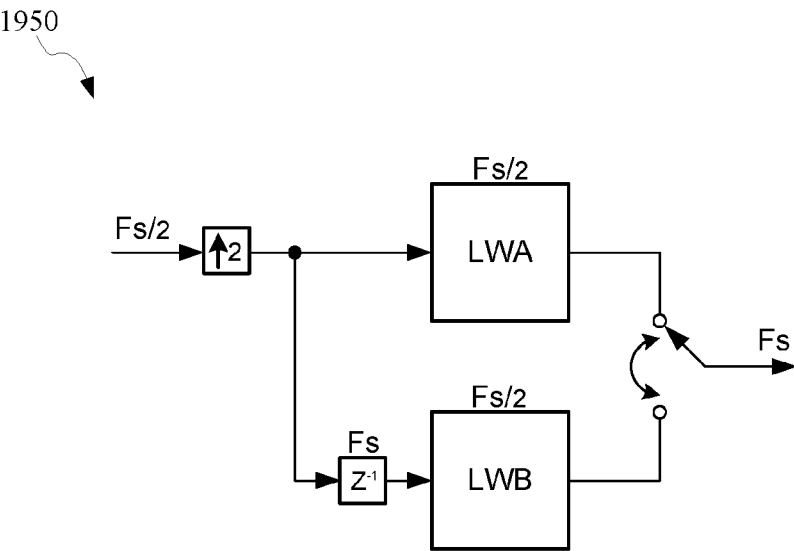


FIG. 19B

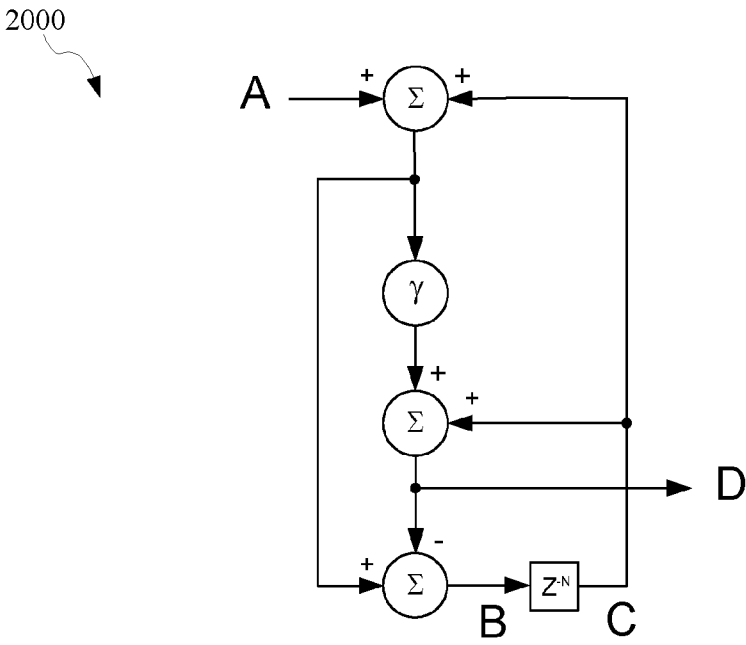


FIG. 20A

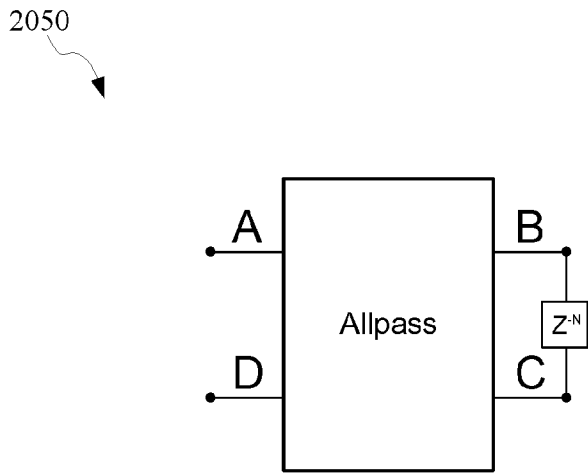


FIG. 20B

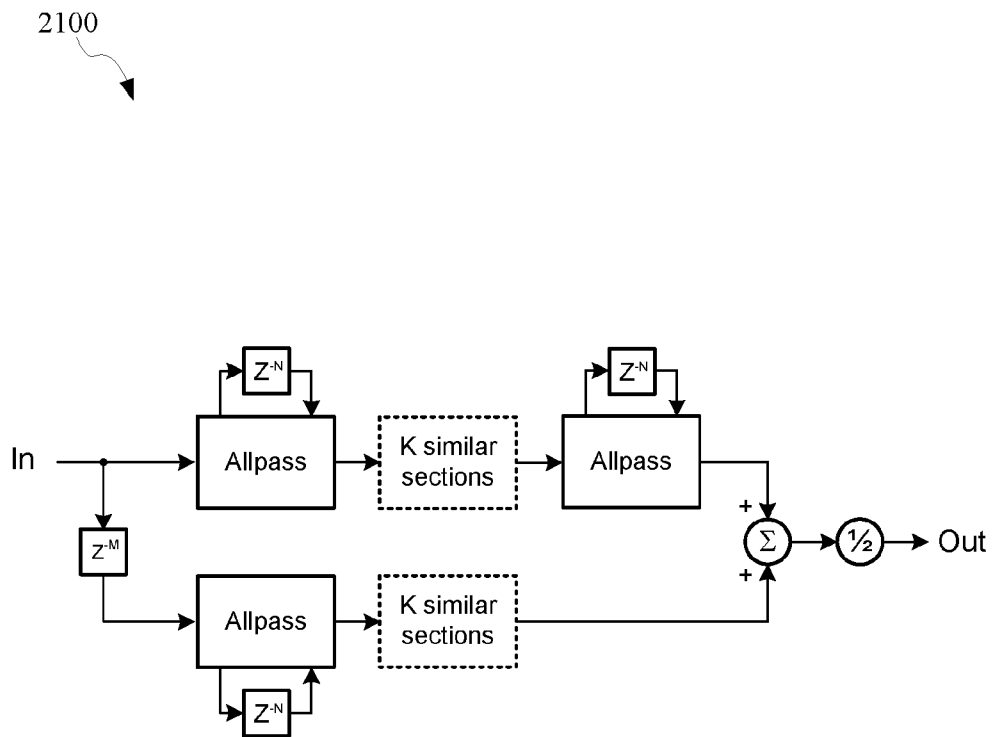


FIG. 21

22/22

2200

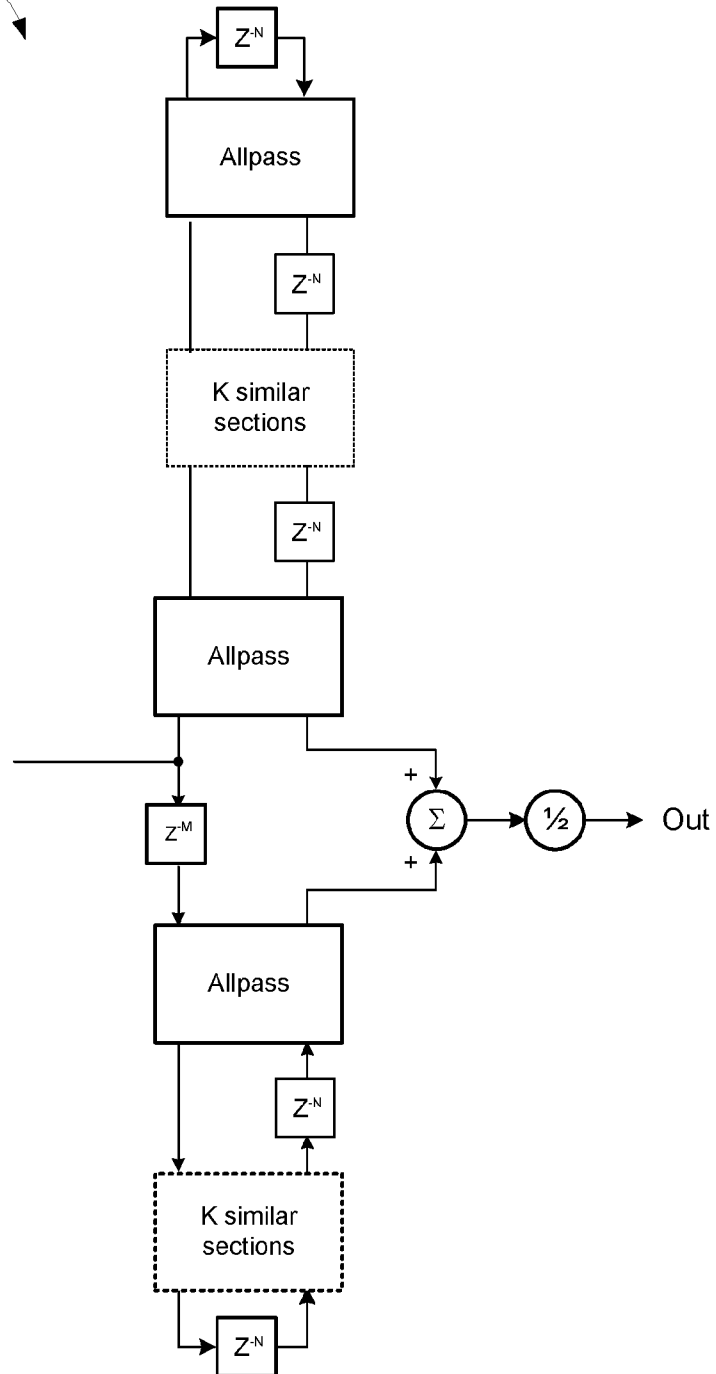


FIG. 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/058574**A. CLASSIFICATION OF SUBJECT MATTER****H03H 17/06(2006.01)i, H03H 17/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03H 17/06; A61F 11/06; G10K 11/16; H03H 17/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: audio, noise, sampling-rate, match, decimator, interpolator, lattice

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0308025 A1 (JON D. HENDRIX et al.) 06 December 2012 See paragraphs [0021], [0026]; claims 1, 3; and figures 2, 4.	1-9,11-20
X	HAKAN JOHANSSON et al., `DESIGN OF BIRECIPROCAL LINEAR PHASE LATTICE WAVE DIGITAL FILTERS`, Department of Electrical Engineering, Linkping University S-581 83 Linkping, Sweden, 31 January 1996, pp 1-17 See pages 1, 5-6; equation 2.10; and figures 2.4-2.6.	10
Y		1-9,11-20
Y	JOHN KNIGHT, `Laboratory 2.0 A 3-BIT BINARY SIGN-EXTENDED ADDER/SUBTRACTER`, CARLETON UNIVERSITY, Department of Electronics, ELEC 2607, Switching Circuits, 30 January 2008, pp Lab2-1-Lab2-12 See page lab2-5; and figures 6-9.	9,15,18
Y	US 2010-0310086 A1 (ANTHONY JAMES MAGRATH et al.) 09 December 2010 See claims 1-2; and figure 2.	11-15,19
A	US 8611551 B1 (DANA MASSIE et al.) 17 December 2013 See column 7, line 5 - column 8, line 53; claims 1-8; and figures 1-6.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 February 2019 (20.02.2019)

Date of mailing of the international search report

20 February 2019 (20.02.2019)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

AHN, Jeong Hwan

Telephone No. +82-42-481-8633



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/058574

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0308025 A1	06/12/2012	CN 103270552 A	28/08/2013
		CN 103270552 B	22/06/2016
		CN 103597540 A	19/02/2014
		CN 103597540 B	06/06/2017
		CN 103597541 A	19/02/2014
		CN 103597541 B	31/05/2017
		CN 103597542 A	19/02/2014
		CN 103718238 A	09/04/2014
		CN 103718238 B	23/03/2016
		CN 103718239 A	09/04/2014
		CN 103718239 B	20/01/2016
		CN 103733254 A	16/04/2014
		CN 103733254 B	02/01/2018
		CN 103765505 A	30/04/2014
		CN 103765505 B	31/08/2016
		CN 106205594 A	07/12/2016
		CN 106205595 A	07/12/2016
		CN 107295443 A	24/10/2017
		EP 2647002 A2	09/10/2013
		EP 2715715 A2	09/04/2014
		EP 2715716 A2	09/04/2014
		EP 2715716 B1	11/05/2016
		EP 2715717 A2	09/04/2014
		EP 2715718 A2	09/04/2014
		EP 2715719 A2	09/04/2014
		EP 2715719 B1	08/07/2015
		EP 2715720 A2	09/04/2014
		EP 2715721 A2	09/04/2014
		EP 2715721 B1	11/05/2016
		EP 2793225 A2	22/10/2014
		EP 2793225 A3	15/07/2015
		EP 2804173 A2	19/11/2014
		EP 2804173 A3	11/11/2015
		EP 2804174 A2	19/11/2014
		EP 2804174 A3	30/09/2015
		EP 2824660 A2	14/01/2015
		EP 2824660 A3	30/09/2015
		JP 2014-503844 A	13/02/2014
		JP 2014-517351 A	17/07/2014
		JP 2014-519624 A	14/08/2014
		JP 2014-519625 A	14/08/2014
		JP 2014-519758 A	14/08/2014
		JP 2014-521988 A	28/08/2014
		JP 2014-521989 A	28/08/2014
		JP 2014-522508 A	04/09/2014
		JP 2016-029510 A	03/03/2016
		JP 2016-106276 A	16/06/2016
		JP 2017-107240 A	15/06/2017
		JP 5937611 B2	22/06/2016

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/058574

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		JP 5955949 B2	20/07/2016
		JP 6042420 B2	14/12/2016
		JP 6050336 B2	21/12/2016
		JP 6075798 B2	08/02/2017
		JP 6092197 B2	08/03/2017
		JP 6106163 B2	29/03/2017
		JP 6106164 B2	29/03/2017
		JP 6208792 B2	04/10/2017
		JP 6289699 B2	07/03/2018
		KR 10-1894708 B1	05/09/2018
		KR 10-1909432 B1	18/10/2018
		KR 10-1915450 B1	06/11/2018
		KR 10-1918463 B1	15/11/2018
		KR 10-1918465 B1	15/11/2018
		KR 10-1918466 B1	15/11/2018
		KR 10-1918911 B1	15/11/2018
		KR 10-1918912 B1	15/11/2018
		KR 10-2013-0123414 A	12/11/2013
		KR 10-2014-0033440 A	18/03/2014
		KR 10-2014-0035414 A	21/03/2014
		KR 10-2014-0035443 A	21/03/2014
		KR 10-2014-0035445 A	21/03/2014
		KR 10-2014-0035446 A	21/03/2014
		KR 10-2014-0039002 A	31/03/2014
		KR 10-2014-0039003 A	31/03/2014
		KR 10-2018-0122030 A	09/11/2018
		TW 201237846 A	16/09/2012
		TW I570706 B	11/02/2017
		US 2012-0140943 A1	07/06/2012
		US 2012-0207317 A1	16/08/2012
		US 2012-0308021 A1	06/12/2012
		US 2012-0308024 A1	06/12/2012
		US 2012-0308026 A1	06/12/2012
		US 2012-0308027 A1	06/12/2012
		US 2012-0308028 A1	06/12/2012
		US 2012-0310640 A1	06/12/2012
		US 2014-0211953 A1	31/07/2014
		US 2015-0092953 A1	02/04/2015
		US 2015-0104032 A1	16/04/2015
		US 2016-0063988 A1	03/03/2016
		US 2016-0232887 A1	11/08/2016
		US 2018-0040315 A1	08/02/2018
		US 8848936 B2	30/09/2014
		US 8908877 B2	09/12/2014
		US 8948407 B2	03/02/2015
		US 8958571 B2	17/02/2015
		US 9076431 B2	07/07/2015
		US 9142207 B2	22/09/2015
		US 9214150 B2	15/12/2015
		US 9318094 B2	19/04/2016

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/058574

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0310086 A1	09/12/2010	US 9325821 B1	26/04/2016
		US 9368099 B2	14/06/2016
		US 9633646 B2	25/04/2017
		US 9646595 B2	09/05/2017
		US 9711130 B2	18/07/2017
		US 9824677 B2	21/11/2017
		WO 2012-075343 A2	07/06/2012
		WO 2012-075343 A3	28/02/2013
		WO 2012-166272 A2	06/12/2012
		WO 2012-166272 A3	01/08/2013
		WO 2012-166273 A2	06/12/2012
		WO 2012-166273 A3	19/09/2013
		WO 2012-166320 A2	06/12/2012
		WO 2012-166320 A3	06/06/2013
		WO 2012-166321 A2	06/12/2012
		WO 2012-166321 A3	23/05/2013
		WO 2012-166386 A2	06/12/2012
		WO 2012-166386 A3	16/05/2013
		WO 2012-166388 A2	06/12/2012
		WO 2012-166388 A3	01/08/2013
		WO 2012-166507 A2	06/12/2012
		WO 2012-166507 A3	16/05/2013
		WO 2012-166511 A2	06/12/2012
		WO 2012-166511 A3	06/06/2013
US 2010-0310086 A1	09/12/2010	CN 101903941 A	01/12/2010
		CN 101903941 B	19/09/2012
		CN 102881281 A	16/01/2013
		CN 102881281 B	08/04/2015
		CN 104751839 A	01/07/2015
		GB 2455822 A	24/06/2009
		GB 2455822 B	09/06/2010
		US 10147413 B2	04/12/2018
		US 2015-0078569 A1	19/03/2015
		US 2017-0213537 A1	27/07/2017
		US 2017-0213538 A1	27/07/2017
		US 2017-0213539 A1	27/07/2017
		US 2018-0247634 A1	30/08/2018
		US 8908876 B2	09/12/2014
		US 9654871 B2	16/05/2017
US 8611551 B1	17/12/2013	WO 2009-081187 A1	02/07/2009
		US 8526628 B1	03/09/2013
		US 8848935 B1	30/09/2014