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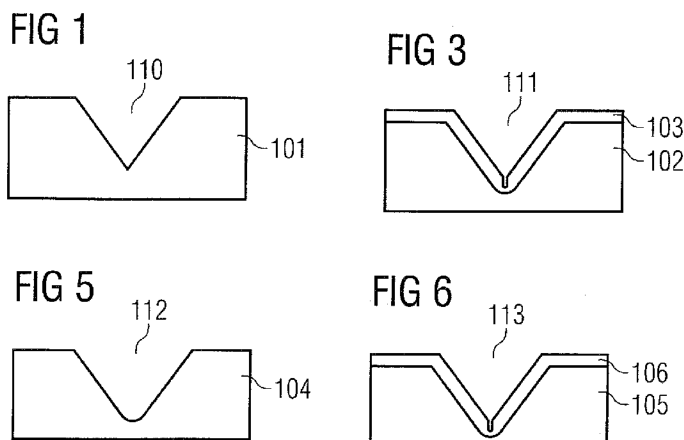
(54) **Title**: METHOD TO PRODUCE A FIELD-EMITTER ARRAY WITH CONTROLLED APEX SHARPNESS



(57) **Abstract**: A methodof manufacturing field-emitter arrays by a molding technique is described, wherein the shape of the mold holes (113) is uniformly controlled to obtain field emitter tips having diameters below 100 nm and blunted side edges. The method utilizes the repeated oxidation and etching of the mold substrate (101) consisting of single-crystal semiconductor mold wafers, where the mold holes (110) for individual emitters are fabricated by utilizing the crystal orientation dependence of the etching rate.

Method to produce a field-emitter array with controlled apex sharpness

The present invention relates to a method for producing a
5 field-emitter structure having controlled apex sharpness.

In the following specification of the present invention, the pertinent prior art comprises the following documentation:

10 **Reference cited**

Henry F. Gray, Richard F. Greene, *Method of manufacturing a field-emission cathode structure*, U.S. Pat. No. 4,307,507 issued Dec. 29, 1981.

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H. Umimoto, S. Odanaka, and I. Nakao, *Numerical Simulation of Stress-Dependent Oxide Growth at Convex and Concave Corners of Trench Structures*, IEEE Electron Device Letters, Vol. 10, No. 7, July 1989, pp.330

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M. Sokolich, E.A. Adler, R.T. Longo, D.M. Goebel, R.T. Benton, *Field emission from submicron emitter arrays*, International Electron Device Meeting, 1990. IEDM '90. Technical Digest, IEDM90-159.

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Henry F. Gray, George J. Campisi, Process for fabricating self-aligned field-emitter arrays, U.S. Pat. No. 4964946 issued Oct. 23, 1990.

30 Steven M. Zimmerman, *Structures and processes for fabricating field emission cathodes*, U.S. Pat. No. 5,141,459 issued Aug. 25, 1992.

Robert B. Marcus and Tirunelvell S. Ravi, *Method for making*
35 *tapered microminiature silicon structures*, U.S. Pat. No. 5,201,992 issued Apr. 13, 1993.

Shinya Akamine, *Casting sharpened microminiature tips*, U.S. Pat. No. 5,580,827 issued Dec. 3, 1996

Byeong Kwon Ju, Myung Hwan Oh, *Micro-tip for emitting electric field and method for fabricating the same*, U.S. Pat. No. 5,827,752 issued Oct. 27, 1998.

Takayuki Yagi, Tsutomu Ikeda, Zasuhiro Shimada, *Female mold substrate having a heat flowable layer, method to make the same, and method to make a microprobe tip using the female substrate*, U.S. Pat. No. 6,227,519 B1 issued May 8, 2001.

Egbert Österschulze, Rainer Kassing, Georgi Georgiev, *Verfahren zur Herstellung einer schmale Schneide oder Spitze aufweisenden Struktur und mit einer solchen Struktur versehener Biegebalken*, DE 102 36 149 A1 issued February 26, 2004.

W. P. Dyke and J. K. Trolan, *Field emission: large current densities, space charge, and the vacuum arc*, Phys. Rev. 89, 799-808 (1953).

M. Dehler, A. E. Candel, E. Gjonaj, *Full scale simulation of a field-emitter arrays based electron source for free electron lasers*, J. Vac. Sci. Technol. B24 (2), pp.892-897 (2006).

In this specification, a method to precisely control the shape of the mold holes is described for the purpose of producing field-emitter arrays with uniform apex sharpness and blunted side ridges. The field-emitter arrays are produced by the deposition of the electron emitter material onto the mold substrates and subsequent removal of the mold substrates. The sharpness of the emitter apex and the side ridges of the emitters are controlled by precisely shaping the mold holes by the crystal orientation dependent etching of single-crystal substrates in combination with the topography-dependence of the oxidation rate.

Background of the Invention

1. Field of Invention

5 This invention relates to new methods of controlling the shape of the mold used for manufacturing high-current emitting field-emitter array structures.

One prior art method is described in U.S. Pat. No. 4,307,507
10 issued Dec. 29, 1981 to Gray et al. This patent describes a method of manufacturing field-emitter array structures by using pyramidal-shaped mold holes, formed by lithography and crystal-orientation dependent etching on a single-crystal semiconductor wafer, with an optional passivation layer, such
15 as a thermal SiO_2 layer, a Si_3N_4 layer, or a metal layer, typically 30 Angstrom thick. The field-emitter array structures are formed by the deposition of the electron emitter material onto the mold wafer and the subsequent removal of the mold wafer. In this way, pyramidal-shaped
20 electron emitter arrays with sharp emitter apex are obtained. However, in this method, the sharpness of the emitter apex fabricated by a mold without a passivation layer, or by a mold with an insufficiently thick passivation layer, is often degraded during the wafer removing process. When a
25 sufficiently thick thermal SiO_2 layer is used on a Si wafer as described by a prior art in U.S. Pat. No. 5,580,827 issued Dec. 3, 1996 to Akamine, the fast oxidation rate of the side facets of the pyramidal-shaped mold compared to the slow oxidation rate of recessed areas due to the stress dependent
30 reduction of the oxygen diffusion rate (H. Umimoto, S. Odanaka, and I. Nakao, Numerical Simulation of Stress-Dependent Oxide Growth at Convex and Concave Corners of Trench Structures, IEEE Electron Device Letters, Vol. 10, No. 7, July 1989, pp.330) results in several undesirable consequences such
35 as;

1) The field-emitter apex becomes extremely sharp and the resultant narrow electron emitting area at the emitter

apex cannot sustain the high currents required from the individual emitters for certain applications.

2) The side ridges of the pyramidal shaped field-emitters become extremely sharp, which leads to parasitic electron emission. The electron emission from the side ridges is undesirable in particular for the field-emission performance of arrays with additional gate electrodes fabricated e.g. following the prior art method described by Sokolich et al. (M. Sokolich, E.A. Adler, R.T. Longo, D.M. Goebel, R.T. Benton, *Field emission from submicron emitter arrays*, International Electron Device Meeting, 1990. IEDM '90. Technical Digest, IEDM90-159). For example, field-emitted electrons from the side ridges are likely to bombard the gate electrodes, which results in the premature failure of the device at low current level.
3) The electron beam emitted from thus formed sharp side ridges degrades the emittance of the beam directly due to its low symmetry and indirectly due to the space-charge effect.
4) Thus formed sharp side ridges of the pyramidal shaped field-emitter affect the topography of the insulating layers and the metallic layers to be deposited on top of the field-emitter array to manufacture gate electrodes, resulting in deformation of the shape of the gate aperture holes and undesirable degradation of the emittance of the electron beams from the individual emitters.

The importance of the optimal apex diameter for the high current can be illustrated by a following numerical example: as reported by Dyke and Trolan (W. P. Dyke and J. K. Trolan, *Field emission: large current densities, space charge, and the vacuum arc*, Phys. Rev. 89, 799-808 (1953)), the stable field-emission current is obtained when the current density is kept at most around ~10^7 A/cm^2 with the corresponding emitter apex field in the order of 50-100 MV/cm. Accordingly, when the apex diameter is 1 nm, the total emission current per emitter is at

most ~300 nA. However, when the apex diameter is 100 nm, the total emission current per emitter is ~3 mA. When the apex diameter is somewhere in between the two values and ~0.2 mA/tip is realized, a field-emitter array device with 40,000 tips in 0.5 mm diameter (or array with 5 micrometer pitch) can emit total current below 10 A with the total thermal emittance below 0.1 mm mrad. Recent numerical calculation by M. Dehler et al. (M. Dehler, A. E. Candel, E. Gjonaj, *Full scale simulation of a field-emitter arrays based electron source for free electron lasers*, J. Vac. Sci. Technol. B24 (2), pp.892-897 (2006)) has demonstrated that an electron gun using a field-emitter cathode equipped with an extraction gate and a focusing gate can indeed produce such a high quality electron beam that is applicable to construct a compact free-electron laser for sub-nanometer emission wavelength.

2. Description of the Related Art

Zimmerman (U.S. Pat. 5,141,459) disclosed a method to fabricate a field-emitter structure with non-sharp tip apex diameter by incompletely filling the mold holes with the sacrificial material. However, with this method, achieving uniform apex diameter is not an easy task.

Marcus et al. (U.S. Pat. 5,201,992) disclosed a method to manufacture a field-emitter structure made of silicon having a flat top as an intermediate step to manufacture ultra-sharp tips with apex diameter of a few nanometers. As such, the uniformity of the flat-topped emitter apex is an issue here. They disclosed a method to control the apex diameter larger than a few nanometers by first repeatedly applying oxidation to the flat-topped structure to form emitter structures having uniform but sharp apex diameters less than a few nanometers, and then applying further oxidation processing to thus formed emitter structures with sharp apex to increase the apex diameter above 2.5 nm.

B. K. Ju et al. (U.S. Pat. 5,827,752) disclosed a method to form mold holes with large apex diameters in a silicon substrate by first manufacturing pyramidal shaped holes by the crystal-orientation-dependent etching of a silicon (100) substrate, then oxidizing the substrate, and finally removing the silicon dioxide.

Yagi et al. (U.S. Pat. 6,227,519 B1) disclosed a method to control the tip-shape based on the molding method by applying a heat flowable material in the mold holes.

Österschulze et al. (DE 102 36 149 A1) disclosed a method to form mold recesses to manufacture tips with 100 nm and below by utilizing a selective etching of a thin film deposited on a pre-recessed semiconductor substrate.

3. Brief Description of the Invention

Accordingly, it is therefore an object of the present invention to fabricate uniform field-emitter array structures with controlled apex sharpness and controlled sharpness of the side ridges of the pyramidal-shaped field-emitters.

The object of the present invention is achieved by modifying the shape of the mold produced using a single-crystal semiconductor wafer by lithography and crystal-orientation dependent etching, whilst maintaining the thickness of a passivation layer on the mold to protect the electron emitting material during the substrate removal process. The field emission cathode structure is formed in the thus modified mold by coating the inside with electron emitting material, followed by removal of the mold substrate.

In particular, a method according to the present invention is presented in more detail.

The method provides a way of manufacturing a field-emitter structure with apex of desired sharpness with diameter between 1 and 100 nm and blunted side riges; comprising the steps of:
a) providing a substrate wafer (101) of a single-crystal
5 material having a number of pyramidal shaped holes (110);
b) oxidizing the substrate wafer with the holes by thermal oxidation of the substrate wafer at least in the region of said holes in order to form an oxidized layer (103) on the surface of the regions of the substrate wafer;
10 c) removing the oxidized layer (103) from the substrate wafer (102) to form a pre-treated substrate wafer (104);
d) oxidizing the substrate wafer (104) with the holes by thermal oxidation of the substrate wafer at least in the region of said holes (112) in order to form an oxidized layer
15 (106) on the surface of the regions of the substrate wafer;
e) coating the pre-treated substrate wafer with an electron emitting material to form the field-emitter structure;
f) removing the substrate wafer by chemical etching in order to excavate the field-emitter structure (Fig.10).
20
Further additional features can be taken from the remaining dependent claims.

Preferred examples of the present invention are described
25 hereinafter with reference to the following drawings, which depict the following.

Figures 1 to 3 depict several of the basic preliminary steps in manufacturing substrate wafers to be used to manufacture a
30 field emitter array structure with controlled shape in accordance with the invention, up to the stage described by Gray et al (Henry F. Gray, Richard F. Greene, *Method of manufacturing a field-emission cathode structure*, U.S. Pat. No. 4,307,507 issued Dec. 29, 1981) comprising a sharpened tip
35 and side ridges.

Figure 4 depicts the top plan view of the mold resulting from the processing steps described with relation to Figures 1 to 3.

5 Figures 5 and 6 depict the final steps to manufacture a field-emitter array structure with controlled shape.

Figure 7 depicts the top plan view of the mold resulting from the processing steps depicted in Figure 6.

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Figure 8 shows a scanning electron microscopy image of a molybdenum field emitter structure manufactured by using a single-oxidation mold as depicted in Figures 3 and 4 where the present invention was not applied.

15

Figure 9 shows a scanning electron microscopy image of a molybdenum field emitter structure manufactured by using a mold as depicted in Figures 6 and 7 where the shape of the holes is modified in accordance with the present invention.

20

Figure 10 shows an enlarged view of the scanning electron microscopy image of the emitter apex of a molybdenum field emitter structure manufactured by using a mold where the shape of the holes are modified in accordance with the present

25 invention.

Description of the preferred embodiment

The invention can be best described with reference to Figures

30 1 to 7, which depict the initial, intermediate, and final shapes of the mold.

The starting point of the invented process is a wafer substrate 101 (see Fig. 1 for cross-sectional and Fig. 2 for

35 plan view) where pyramidal shaped holes 110 having four facets with the [111] crystal orientation are etched in the single-crystal semiconductor wafer with [001] crystal orientation. In

a preferred embodiment, the holes 110 are within the range 0.5×0.5 to 3×3 μm^2 in size and the precise shape of the holes 110 is determined by the anisotropy of the crystal-orientation dependent etching rate to secure the uniformity of the holes
5 110.

In the next step, a thermal oxidation process is applied to the wafer substrate 101, which forms a superficial oxide layer 103 (see Figure 3 for cross-sectional and Figure 4 for plan
10 view). In a preferred embodiment, the thickness of the oxide layer 103 is chosen to be equal to 400-500 nm. Oxide growth is slower at the tips and ridges in the holes 110 of the wafer structure 101 (mold) where less oxygen is available. Consequently, the surface of the oxide becomes cusp-shaped at
15 these junctions. On the other hand, the sharpness of the junctions is blunted at the interface between the oxide film 103 and a so-modified wafer substrate 102.

Following the thermal oxidation to form the oxide layer 103,
20 the oxide film 103 is selectively removed and the mold wafer 104 having smooth, concave junctions at the bottom of the modified holes 112 and at the side ridges is formed (see Fig. 5 for cross-sectional view). For example, the oxide removal can be effectively achieved by wet etching using hydrofluoric
25 acid for silicon wafers or GaAs wafers. The diameter of the bottom of the modified holes 112 typically has a radius greater than several hundred nm.

In the next step, thermal oxidation is again applied to the
30 so-modified wafer 104, which forms another oxide layer 106 on top of the resulting wafer 105 (see Figure 6 for cross-sectional and Figure 7 for plan view). The oxide layer 106 also protects the electron emitter material to be deposited on top of it during the process to remove the resulting wafer
35 substrate 105. Therefore, the thickness of the oxide layer 106 is set to be sufficiently thick in the range of 300-600 nm. In a preferred embodiment, the thickness of the oxide layer 106

is chosen to be 400 nm. As the result of topography dependent oxidation rate on the surface of the holes 112, the surface of the oxide film 106 is rounded at the junctions between the side facets and at the bottom of the holes 113.

5

The field-emitter array cathode is subsequently obtained by coating the mold with electron emitting layer, which is extended to sufficient thickness to sustain the resultant field-emitter array, and then by removing the resulting wafer

10 substrate 105 and the oxide film 106 by chemical etching. The apex diameter of individual emitters is now typically in the range of tens of nanometers (see Figures 9 and 10) with the apex size uniformity in the range of 15%.

Patent Claims

1. A method of manufacturing a field-emitter structure (120) having the apex diameter between 1 and 100 nm with blunted side ridges; comprising the steps of:
a) providing a substrate wafer (101) of a single-crystal material having a number of pyramidal shaped holes (110), prepared by use of the crystal-orientation dependent etching,
b) oxidizing the substrate wafer (101) by thermal oxidation of the substrate wafer (101) at least in the region of said holes (110) in order to form an oxidized layer (103) at least within said regions of the substrate wafer (101);
c) removing the oxidized layer (103) from the substrate wafer (102) to form a pre-treated substrate wafer (104);
d) oxidizing the substrate wafer (104) by thermal oxidation of the substrate wafer (104) at least in the region of said holes (112) in order to form an oxidized layer (106) at least within said regions of the substrate wafer (104) to form modified pyramidal shaped holes (113);
e) coating the pre-treated substrate wafer (102) with an electron emitting material to form the field-emitter structure (120);
f) removing the substrate wafer (105) by chemical etching in order to excavate the field-emitter structure (120).

2. The method according to claim 1, wherein between the step (d) and the step (e), the wafer is treated by the following steps by more than once at least within said regions of the substrate wafer; i) removing the oxidized layer on the mold substrate surface, ii) oxidizing the substrate wafer by thermal oxidation.

3. The method according to any of the preceding claims 1 and 2, wherein the thicknesses of the oxidized layers (103) and (106) are in the range of 200 nm to 1000 nm, preferably in the range of 400 nm to 600 nm.

4. The method according to any of the preceding claims 1 to 3, wherein silicon is used as the substrate material.

5. The method according to any of the preceding claims 1 to 4, wherein silicon dioxide is the oxide layer material.

6. The method according to any of the preceding claims 1 to 4, wherein silicon oxynitride is used as the oxide layer material.

FIG 1

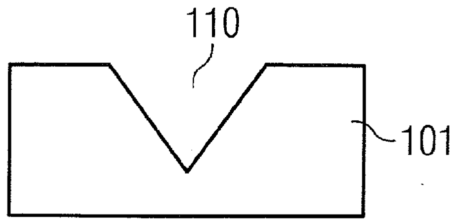


FIG 2

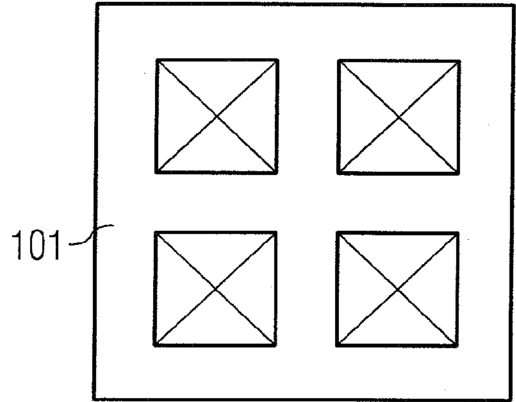


FIG 3

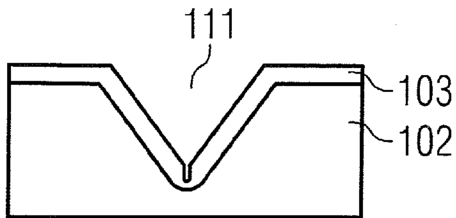


FIG 4

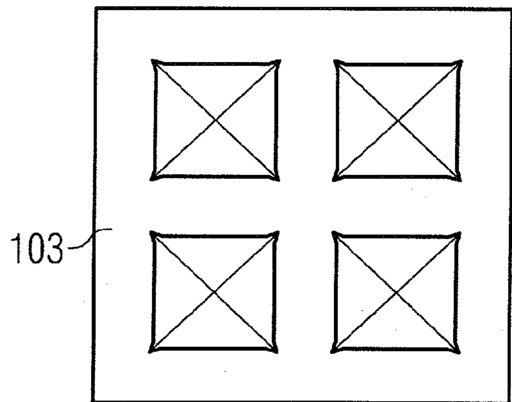


FIG 5

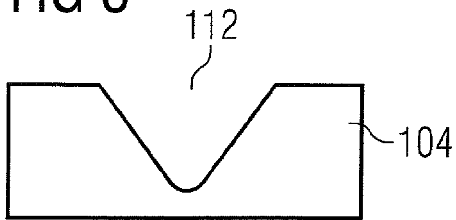


FIG 6

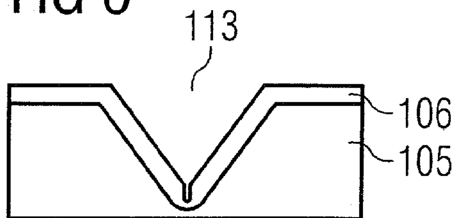


FIG 7

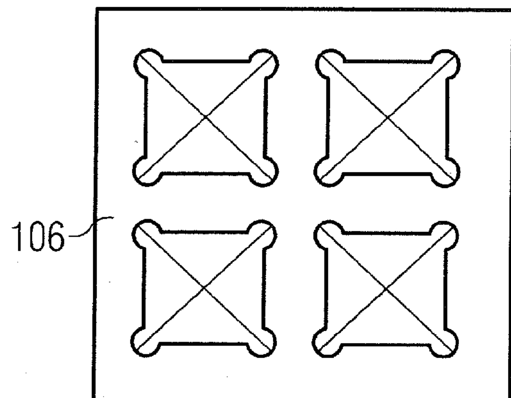


FIG 8

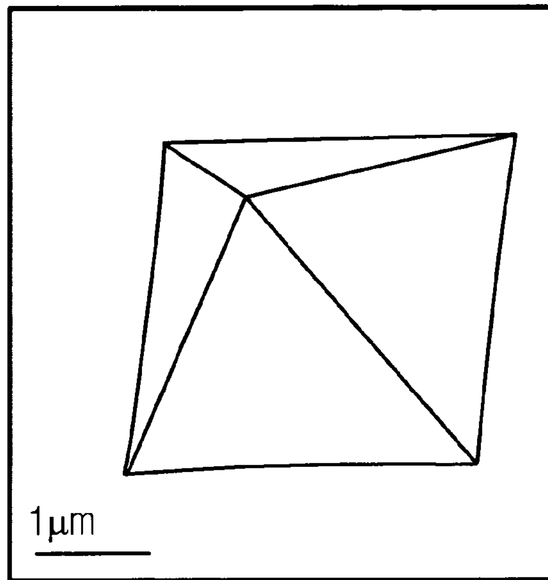


FIG 9

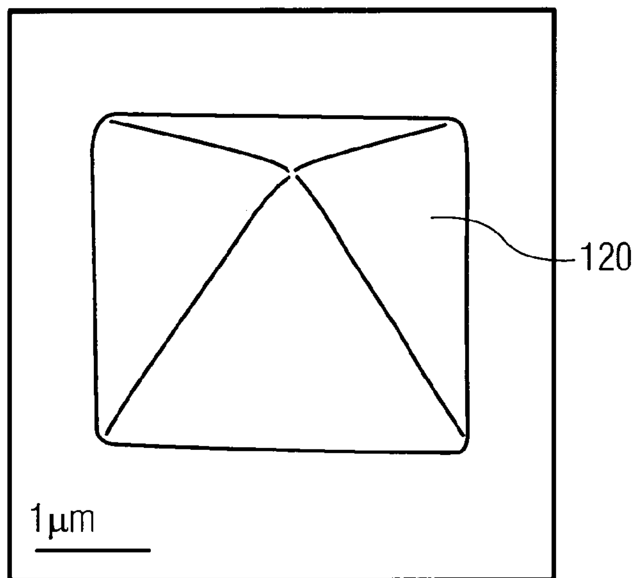
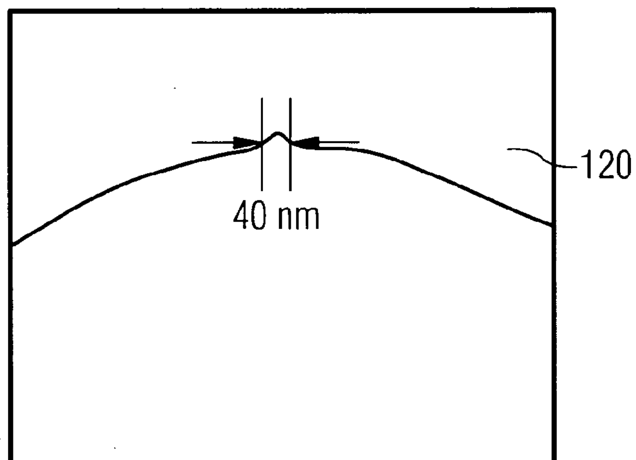


FIG 10



INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/056595

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01J9/02 H01J1/304 H01J37/073

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 580 827 A (AKAMINE SHINYA [US]) 3 December 1996 (1996-12-03) abstract figure 4 column 1, lines 26-30 column 2, line 60 - column 3, line 4 column 4, lines 8-41 column 5, lines 8-45 -----	1-6
A	DE 102 36 149 A1 (UNIV KASSEL [DE]) 26 February 2004 (2004-02-26) abstract figures 1,3,4,6,7 paragraph [0002] paragraphs [0021], [0022], [0026] paragraph [0030] paragraph [0041] -----	1-6

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
7 September 2009	15/09/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Manini, Adriano

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/056595

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2006/084192 A1 (ZHANG TIANHONG [US]) 20 April 2006 (2006-04-20) abstract figure 4 paragraph [0004] paragraphs [0023], [0025] paragraphs [0044], [0050], [0051] -----	1-6
A	US 4 604 304 A (FARAONE LORENZO [US] ET AL) 5 August 1986 (1986-08-05) abstract column 1, lines 9-19,45-51 -----	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2009/056595

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 5580827	A	03-12-1996	NONE	
DE 10236149	A1	26-02-2004	WO 2004015362 A2	19-02-2004
US 2006084192	A1	20-04-2006	NONE	
US 4604304	A	05-08-1986	JP 63015425 A	22-01-1988