



- (51) **International Patent Classification:**
H02M 3/28 (2006.01) *H02M 3/335* (2006.01)
- (21) **International Application Number:**
PCT/CN2010/079419
- (22) **International Filing Date:**
3 December 2010 (03.12.2010)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (71) **Applicant** (for all designated States except US): **HUAWEI TECHNOLOGIES CO., LTD.** [CN/CN]; Huawei Administration Building, Bantian, Longgang, Shenzhen, Guangdong 518129 (CN).
- (72) **Inventors; and**
- (75) **Inventors/Applicants** (for US only): **PALMGREN, Michael** [SE/SE]; Nybohovsgrand 8,2tr, S-117 63 Stockholm (SE). **TORRICO BASCOPE, Grover Victor** [BO/SE]; Sibeliussgatan 44, 4tr, S-164 72 Kista (SE). **RODULFO, Philip** [GB/AU]; Klagenfurter strasse, 32, ST.Veit a.d.Glan 9300 (AU).
- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

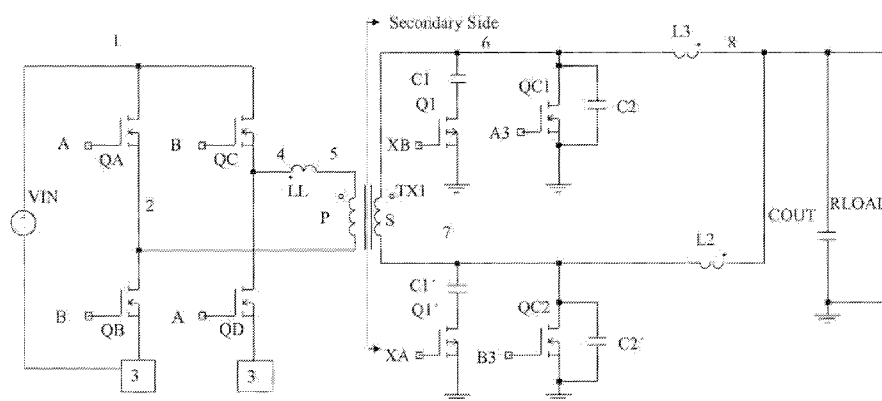
(54) **Title:** POWER CONVERTER

FIG 7

(57) **Abstract:** A power converter for DC/DC or AC/DC conversion includes a primary side and a secondary side separated by a transformer (TX1). The primary side is connected to a primary winding of the transformer (TX1) and is the input circuit of the power converter. The secondary side is connected to a secondary winding of the transformer (TX1) and is an output circuit of the power converter. The power converter further includes at least one active clamp circuit (ACC) connected to the secondary side. The at least one ACC includes a first capacitor (C1) connected in series with a parallel combination of a switch (S1) and a diode (D1), and a second capacitor (C2) connected in parallel with the series combination of the first capacitor (C1) and the parallel combination of the switch (S1) and the diode (D1).

POWER CONVERTER

Technical Field

The present invention relates to a power converter, or more particularly to a power converter according to the preamble of claim 1. Furthermore, the invention also relates to a method, a system, a computer program and a computer program product.

Background of the Invention

Figure 1 shows an example of a power converter according to prior art. The power converter in figure 1 comprises a primary side and a secondary side separated by a transformer TX1 having a primary winding on the primary side and a secondary winding on the secondary side. The primary and secondary sides are input and output circuits of the power converter, respectively. Further, the transformer TX1 has a leakage inductance LL.

Moreover, an Active Clamp Circuit (ACC) is connected to the primary side of the power converter as shown in figure 1. A primary switch QA is also connected to the primary side and is Pulsed Width Modulated (PWM) with a control signal A. The primary switch QA chops up the input voltage VIN so that the voltage at the input of the output filter (node LOUT, QA2) will be equal to $VIN \cdot NS/NP$ (NS/NP is the turns ratio of the transformer TX1 and is defined as number of secondary turns NS over number of primary turns NP) when the primary switch QA is turned on, and 0 V when the primary switch QA is turned off. Hence, the power converter converts the input voltage VIN to an output voltage VOUT.

The circuit in figure 1 further comprises synchronous rectifiers QA1 and QA2 connected to the secondary side, and a resistance R2 in series with a capacitance C3 which together form a lossy RC snubber that reduces voltage ringing on the secondary side of the power converter.

An inductance LOUT and a capacitance COUT form an averaging output filter of the power converter. By changing a duty cycle D of the control signal A, the output voltage VOUT can be regulated as $VOUT = VIN \cdot (NS/NP) \cdot D$. Finally, a resistance RLOAD is connected to the secondary side and is the output load resistor over which the output voltage VOUT can be found.

Figure 1 shows a control logic for an ACC in a power converter according to prior art, wherein $f_S = 1/TS$ is the switching frequency of the power converter and TS is the period time. The duty cycle D is defined as $D = TON/TS$, where TON is the time interval when the primary switch QA is turned on. In figure 2, QAC is turned on when the primary switch QA is turned off, and vice versa. It should however be noted that the ACC in this case is realised with a PMOS transistor which means that the ACC is turned on when the control signal for the ACC is set to low.

Furthermore, the above described types of power converters according to prior art are often employed as Switched Mode Power Supplies (SMPS). Unlike a linear power supply, the pass transistor of a SMPS switches very quickly between full-on and full-off states, typically between 50 kHz and 1 MHz, which minimizes wasted energy. Voltage regulation is provided by varying the ratio D. In contrast, a linear power supply must dissipate the excess voltage to regulate the output. This higher efficiency is the chief advantage of a SMPS.

A major goal when converting an input voltage to an output voltage in SMPS is to perform this power conversion with so small losses as possible. When a semiconductor switch in a high frequency SMPS is turned on and off, respectively, it is associated with a switching loss which adds to the total losses of the SMPS. Normally, the switch-off losses are dominant due to the trapezoidal current waveform thru the switch, i.e. the current is higher at turn-off. During turn-on, the leakage inductance of the transformer TX1 limits the derivate of the current, i.e. di/dt , making the turn-on losses smaller in this case.

Another issue is voltage transients generated from parasitic inductances in the transformer TX1 that occurs over the secondary side rectifiers which mainly are due to leakage inductance. These transients or voltage spikes forces the designer to use higher voltage rating on the semiconductors and lossy snubbers (a circuit that limits voltage spikes, often with significant additional loss), which contributes to higher losses in the power converter.

Document US 7,606,051 shows fully clamped coupled inductors in power conversion circuits.

Summary of the Invention

An object of the present invention is to provide a power converter which fully or in part solves the drawbacks and disadvantages of prior art power converters. Another object of the invention is to provide a power converter with reduced switching losses compared to prior art power converters. A yet another object of the invention is to provide an alternative solution to the problem of power conversion using a power converter.

According to one aspect of the invention, the objects are achieved with a power converter for DC/DC or AC/DC conversion, said power converter having a primary side and a secondary side separated by a transformer, said primary side being connected to a primary winding of said transformer and being an input circuit of said power converter, and said secondary side being connected to a secondary winding of said transformer and being an output circuit of said power converter, said power converter further comprising at least one active clamp circuit connected to said secondary side; said at least one active clamp circuit comprising:

- a first capacitor connected in series with a parallel combination of a switch and a diode, and
- a second capacitor connected in parallel with said series combination of said first capacitor and said parallel combination of said switch and said diode.

Embodiments of the power converter above are disclosed in the dependent claims 2-15.

According to another aspect of the invention the objects are achieved with a system comprising at least one power converter above and at least one control circuit arranged for controlling one or more switches in said power converter.

According to yet another aspect of the invention, the objects are also achieved with a method for controlling at least one active clamp circuit in a power converter, said power converter having a primary side and a secondary side separated by a transformer;

- said primary side being connected to a primary winding of said transformer and being an input circuit of said power converter, and said secondary side being connected to a secondary winding of said transformer and being an output circuit of said power converter;
- said power converter further comprising at least one active clamp circuit connected to said secondary side and at least one corresponding primary switch connected to said primary side, wherein said at least one active clamp circuit is arranged to alter a shape of a current waveform in said at least one corresponding primary switch so that said current waveform is

higher when said corresponding primary switch is turned on than when said corresponding primary switch is turned off; wherein:

- said at least one active clamp circuit is turned on and off substantially at the same time as when said at least one corresponding primary switch is turned on and off.

5

The method according to the invention may also be modified, *mutatis mutandis*, according to the different embodiment of the power converter above.

10

The invention also relates to a computer program and a computer program product when run in a computer causes the computer to execute the method. Also, the invention relates to a system.

15

One advantage with the present invention is the fact that it alters the shape of the current waveform, e.g. in primary switches and in secondary rectifiers, to be higher at turn-on and lower at turn-off, thereby reducing the dominant turn-off losses in a power converter according to the invention. Hence, the present invention provides more efficient power conversion compared to prior art power converters and may achieve efficiency > 96%.

20

Furthermore, the voltage stress on rectifiers on the secondary side is also reduced which means that lower voltage rating on the rectifiers on the secondary side may be used. Lower voltage rating over the rectifiers normally means lower resistance over the transistor when it is turned on in case of a synchronous rectifier or lower forward voltage drop in case of a diode rectifier. Hence higher efficiency can be achieved.

25

Other advantages and applications of the present invention will be apparent from the following disclosure.

Brief Description of the Drawings

30

The appended drawings are intended to clarify and explain different embodiments of the present invention in which:

- Figure 1 shows an example of a power converter according to prior art;
- Figure 2 shows control logic for controlling an ACC according to prior art;
- Figure 3 schematically shows an ACC according to the present invention;

- Figure 4 shows the peak current thru the ACC in figure 3 versus a value $C2$ for the second capacitance $C2$;
- Figure 5 shows the voltage over the ACC in figure 3 and currents in the ACC during the time interval when the ACC is active;
- 5 - Figure 6 shows the current waveform thru $L1$ for two different values $C2$ on the second capacitance $C2$;
- Figure 7 shows an embodiment of a PC according to the present invention - a full bridge primary and a current doubler secondary with two ACCs;
- Figure 8 shows control logic waveforms for controlling all switches of the PC in
10 figure 7;
- Figure 9 shows the current waveform and the instantaneous power in a primary switch in a circuit according to figure 7;
- Figure 10 shows in detail the graph in figure 9 at the time the switch is turned off;
- Figure 11 shows another embodiment of the present invention - a full bridge primary
15 and a full bridge secondary with two ACCs;
- Figure 12 shows another embodiment of the present invention - an active clamp forward converter with two ACCs; and
- Figure 13 shows yet another embodiment of the present invention - a full bridge
20 primary and a current doubler alt. 2 on the secondary with two ACCs;

Detailed Description of Embodiments of the Invention

An ACC according to prior art consists of a controllable switch $S1$ in series with a capacitor $C1$, and in parallel with the controllable switch $S1$ there is a diode $D1$. The diode $D1$ is oriented in such a way that it will automatically clamp the unipolar voltage spike to the
25 voltage over the capacitor $C1$, and the capacitor $C1$ will resonate with the inductor LL which is in series with the primary winding of the transformer $TX1$.

Usually, the switch $S1$ is turned on shortly after that the diode $D1$ has started to conduct and it will be held on allowing the current in the capacitor $C1$ to resonate. Thus, the current in the
30 capacitor $C1$ will initially charge and thereafter discharge the capacitor $C1$ to its initial value during one switching cycle. This configuration has proven efficient and it clamps the voltage on the primary side efficiently, however it does not solve the problem with voltage spikes on the secondary side.

Therefore, the present invention provides a Power Converter (PC) having a primary side and a secondary side separated by a transformer TX1. The primary side is connected to a primary winding of the transformer TX1 and is an input circuit of the PC. The secondary side is connected to a secondary winding of the TX1 and is an output circuit of the PC.

The PC according to the invention further comprises at least one ACC connected to the secondary side of the PC. The at least one ACC comprises: a first capacitor C1 connected in series with a parallel combination of a switch S1 and a diode D1, and a second capacitor C2 connected in parallel with the series combination of the first capacitor C1 and the parallel combination of the switch S1 and the diode D1.

This configuration of a PC results in lower switching losses and thereby higher efficiency, and eliminated voltage spikes over the secondary side rectifiers.

According to an embodiment of the invention, the ACC further comprises: a first node 1; 1' connected to the first capacitor C1 and to the second capacitor C2; a second node 2; 2' connected to the first capacitor C1, the switch S1 and to an anode of the diode D1; and a third node 3; 3' connected to the switch S1, a cathode of the diode D1 and to the second capacitor C2.

Figure 3 schematically shows the nodes 1, 2, 3 of an ACC according to the invention and with reference to said figure: the first node 1; 1' is connected to a first node of said secondary winding of the transformer TX1 or to a high ohmic node, and the third node 3; 3' is connected to a low ohmic node of the secondary side according to yet another embodiment of the invention.

A low ohmic node, also called AC-ground, is a node which is virtually fixed in voltage when current is sourced or sinked into the node in a time interval of interest. Ground is the ideal low ohmic node. A voltage source with one side connected to ground is an ideal low ohmic node at its other end. Also a big capacitor connected to ground will have the other node as AC-ground. A high ohmic node is the opposite of a low ohmic node. Injecting a current into such a node will make the voltage increase substantially during the time interval of interest.

Figure 2 shows a simplified schematic of a secondary side of a PC with an ACC according to the invention, and should be understood to be used to analyse the ACC during one switching cycle. It is assumed that the circuit in figure 3 has reached its stationary state.

5

The initial conditions in the circuit are set to correspond to the stationary state at the time voltage over the secondary side, here simplified to a voltage source V1 has reached 100 V, where V1 is the secondary side voltage. V2 has a turn-on delay relative V1 and is the voltage that controls the switch S1 of the ACC. Inductance L1 in this description is: a leakage inductance transformed to the secondary side, or the leakage inductance transformed to the secondary side plus at least one external inductance. The initial current thru L1=0 A. C1 is the first capacitor of the ACC having an initial voltage 100 V. Further, D1 is a secondary rectifier diode; D2 is the freewheel rectifier of the output stage; L2 is the output inductor, initial current=4 A; and C3 is the output capacitor, initial voltage=28 V.

15

The second capacitance C2 includes the output capacitance of the (synchronous) rectifier, and is an essential component for the correct functionality of the ACC and PC according to the invention; initial voltage over the second capacitance C2=0 V.

At t=0 the following holds: V1=100 V, $I_{L1}=0$ A, $V_{C2}=0$ V, $V_{C1}=100$ V, $I_{L2}=4$ A, $U_{C3}=28$ V, and current I_{L2} is freewheeling thru D2. Figure 5 shows how I_{L1} starts to ramp-up and support the output inductor L2 with current. When I_{L1} has reached 4 A it will start to charge the second capacitor C2 of the ACC. As soon as V_{C2} is above the forward voltage drop of D2, D2 will be reversed and I_{L1} will supply current to I_{L2} which initially is at 4 A. The Peak Current (PK) of I_{C2} (i.e. IPK_{C2}) is set by the resonance circuit formed by the inductance L1 and the second capacitor C2. Since law of energy conservation applies: $C2 \cdot V1^2 = L1 \cdot IPK_{C2}^2$, and V_{C2} will charge to 100 V. The inventors used the following values in the exemplary configuration above: $V1=100$ V, $L1=400 \cdot 10^{-9}$ H, $C2=10 \cdot 10^{-9}$ F, $IPK_{C2}=15.811$ A, $IPK_{L1}=IPK_{C2} + I_{L2}$ where $IPK_{L1}=19.811$ A and $I_{L2}=4$ A.

30

Further, as shown in figure 5, when the voltage V(C2) over the second capacitance C2 reach 100V D3 will start to conduct ($t \approx 115$ ns in figure 3). The previous peak current in second capacitor C2 will now charge the first capacitor C1 thru the inductance L1 ($IPK_{C1}=IPK_{C2}$).

After a small delay the switch S1 of the ACC will be turned on and current is now allowed to flow in the opposite direction, i.e. the first capacitor C1 can be discharged to the output inductor L2. The first capacitance C1 and the inductance L1 now form a resonance circuit. When the “primary side” modelled by V1 is turned-off after 1.32 μ s most of the current to the output inductor L2 is supported from the first capacitor C1, thereby reducing turn-off loss for the primary side switches and for secondary side rectifier here modelled by D1.

Finally, the turn-off of the ACC switch S1 can be done at almost Zero Voltage Switching (ZVS) as the second C2 capacitor will deliver current to the output inductor L2 and hold the voltage over the switch S1 at a low voltage during the turn-off. As can be seen in figure 5 $I(L1)=I(L2)+I(C1)+I(C2)$, i.e. the ACC reduces the turn-off current of the primary side switches and the secondary side rectifier, thereby reducing turn-off loss significantly in the PC. ZVS means that the voltage over a switch is zero volt or close to zero during transition from one state to another, e.g. from open to closed state or vice versa.

Dimensioning the ACC and PC

During the time when the primary switch(es) QA; QB; QC; QD conduct, the ACC corresponding to the primary switch(es) QA; QB; QC; QD does also conduct. At this time the current ramps-up in the output inductor L2 with a constant slope equal to: $(V1-VOUT)/L2$.

The peak current, IPK_{L2} , in the output inductor L2 is calculated using Eq. 1 below.

$$IPK_{L2} = IOUT + \frac{(V1 - VOUT)}{2 \cdot L2} \cdot TON, \quad (1)$$

The inventors used the following values in an exemplary configuration: $V1=100$ V, $VOUT=28$ V, $L2=10 \cdot 10^{-6}$, $IOUT=8$ A, $VOUT=28$ V, $TON=1.32 \cdot 10^{-6}$, which gives $IPK_{L2}=12.752$.

The first capacitor C1 and the inductance L1 form a resonant circuit with resonance frequency f_R given by the relation in Eq. 2:

$$f_R = \frac{1}{2\pi\sqrt{L1 \cdot C1}}, \quad (2)$$

The resonance frequency f_R is chosen to ring a half cycle during TON for optimal performance. The current in the first capacitor C1 will then go from its maximum value at turn on to its minimum at turn-off. The resonance frequency f_R is 0.5 - 4.0 times the switching frequency f_s of the PC, and preferably 1.0 – 2.0 times the switching frequency f_s .

5

The value of the first capacitance is given by:

$$C1 = \frac{1}{(2 \cdot \pi \cdot f_R)^2 L1}, \quad (3)$$

10 The inventors used the following values in an exemplary configuration: $L1=400 \cdot 10^{-9}$, $f_R=1/TON=3.788 \cdot 10^5$, $VOUT=28$ V, $TON=1.32 \cdot 10^{-6}$, which gives $C1=4.414 \cdot 10^{-7}$.

To achieve Zero Current Switching (ZCS) at turn-off for the primary switches and the secondary rectifier, the first capacitor C1 has to deliver all output current to the output
15 inductor L2 at turn-off, i.e. the peak current thru the first capacitor C1 equals the peak current thru output inductor L2, $IPK_{C1}=IPK_{L2}$. ZCS means that when the current thru a switch is zero ampere or close to zero ampere during transition from one state to another, e.g. from open to closed state or vice versa.

20 The following relation has been proved to hold:

$$IPK_{C1} = V1 \cdot \sqrt{\frac{C2}{L1}}, \quad (4)$$

25 The inventors used the following values in an exemplary configuration: $L1=400 \cdot 10^{-9}$, $V1=100$ V, $C2 = ((IPK_{C1})^2 \cdot L1) / V1^2 = 6.503 \cdot 10^{-9}$, which gives $IPK_{C1} = 12.75$ A.

From above, the dimensioning of an ACC according to an embodiment of the invention can be summarised as:

- Find a peak current in the output inductor L2 from Eq. 1;

- Choose a value $C2$ for the second capacitance $C2$ from Eq. 4 so that the relation $IPK_{C1} = IPK_{L2}$ holds; and
- Choose a value $C1$ for the first capacitor $C1$ from Eq. 2 so that the current in first capacitor $C1$ resonates one half period during the time the current flows in the first capacitor $C1$. This time $TON = D \cdot TS$ is the same as the ramp-up time in the output inductor $L2$.

Figure 6 shows the effects of different values $C2$ for the second capacitor $C2$ on the shape of the current thru inductance $L1$. The undotted curve shows when $C2 = 100$ pF and the dotted curve shows when $C2 = 10$ nF. By increasing the value of $C2$ of the second capacitor $C2$, the shape of the current $I(L1)$ thru the inductance is changed in such away that it is lower at turn-off. In its extreme, as shown in the figure 6 for $C2 = 10$ nF, ZCS at turn-off is achieved.

Further embodiments and effects

Figure 7 shows the schematic of ACC in a current doubler configuration having two ACCs connected to the secondary side of the PC. The first ACC is formed by a first capacitor $C1$ together with a second capacitor $C2$ of the first ACC; while the second ACC is formed by a first capacitor $C1'$ together with $Q1'$ and a second capacitor $C2'$ of the second ACC. The capacitors $C2$ and $C2'$ can be considered as lumped capacitors including the parasitic capacitance of the transformer $TX1$ and the output capacitance of the Mosfets.

Figure 8 shows the timing diagram of control logic for the current doubler, and since control signals A, B, A3 and B3 control NMOS transistors, these transistors are turned on when their control signal are high. It should be noted that the ACC switches $Q1$ and $Q1'$ are PMOS transistors in this implementation. Thus they are turned on when their control signals XA and XB are set to low. As can be seen from figure 8, control signal A drives QA and QD , while control signal B drives QB and QC . The secondary rectifiers are controlled by control signals A3 and B3. Further, the ACCs are controlled by control signals XA and XB .

Figure 9 shows the waveforms in a PC having ACCs according to the invention connected to the secondary side. The upper curve in figure 9 shows instantaneous power in one of the primary switches QD , while the lower curve shows current thru QD . It should be noted that

the dominant turn-off loss is reduced due to the lower turn-off current with the ACC. Further, the average power loss has dropped from 2.4 W down to 1.33 W.

Figure 10 shows zoomed in turn-off losses of figure 9 on a primary MOSFET in a PC having ACCs according to the invention connected to the secondary side (see figure 7).

Topologies

The present invention is applicable to all transformer based topologies due to the inherent leakage inductance of transformers TX1s, such as current doubler, fullbridge, forward, and flyback topologies. However, the present invention is also applicable to none transformer based topologies like the Buck converter that has a structure similar to the structure in figure 3.

According to an embodiment of the invention, the following topologies comprise a first and a second ACC, wherein each of the first nodes 1, 1' of the ACCs are connected to different nodes of the secondary winding of the transformer TX1. Preferably, the third node 3, 3' of the ACC are at the same time connected to a low ohmic node. This common configuration for the different topologies has shown good results in tests by the inventors.

Figure 11 schematically shows ACCs in a fullbridge configuration. The first ACC is formed by a first capacitor C1 together with Q1 and a second capacitor C2 of the first ACC. The second ACC is formed by a first capacitance C1' together with a Q1' and a second capacitor C2' of the second ACC. Capacitors C2 and C2' can be considered as lumped capacitors including the parasitic capacitance of the transformer TX1 and the output capacitance of the Mosfets.

Figure 12 schematically shows ACCs in an Active Clamp Forward Converter (ACF) configuration. The first ACC is formed by a first capacitor C1 together with Q1 and a second capacitor C2 of the first ACC. The second ACC is formed by a first capacitor C1' together with a Q1' and a second capacitor C2' of the second ACC. Capacitors C1 and C2 can be considered as lumped capacitors including the parasitic capacitance of the transformer TX1 and the output capacitance of the Mosfets.

Figure 13 schematically shows an alternative current doubler configuration. It should be noted

that the ACCs in this configuration are NMOS transistors and are therefore controlled by positive logic, see below.

The timing diagrams for the control signals for the different topologies follow the same principle as explained above in connection with the timing diagram in figure 8.

Furthermore, the present invention also relates to a system comprising at least one power converter PC according to any of the embodiments above and at least one control circuit arranged for controlling one or more switches in the power converter PC.

The invention further relates to a method for controlling at least one ACC in a PC, the PC comprises at least one ACC connected to the secondary side and at least one corresponding primary switch QA; QB; QC; QD connected to the primary side. The at least one ACC is arranged to alter a shape of a current waveform in the at least one corresponding primary switch QA; QB; QC; QD so that the current waveform is higher when said corresponding primary switch QA; QB; QC; QD is turned on than when the corresponding primary switch QA; QB; QC; QD is turned off. According to the present method: the at least one ACC is turned on and off substantially at the same time as when the at least one corresponding primary switch QA; QB; QC; QD is turned on and off.

According to an embodiment of the method above, the at least one ACC is turned on and off with a delay d when the at least one corresponding primary switch QA; QB; QC; QD is turned on and off, which has been described above.

According to yet another embodiment of the method, the delay d is less than the time interval TON when the at least one corresponding primary switch QA; QB; QC; QD is turned on, and preferably less than one tenth of TON , i.e. $d < TON/10$.

Furthermore, as understood by the person skilled in the art, a method according to the present invention may be implemented in a computer program, having code means, which when run in a computer causes the computer to execute the steps of the method. The computer program is included in a computer readable medium of a computer program product. The computer readable medium may consist of essentially any memory, such as a ROM (Read-Only

Memory), a PROM (Programmable Read-Only Memory), an EPROM (Erasable PROM), a Flash memory, an EEPROM (Electrically Erasable PROM), or a hard disk drive.

5 Finally, it should be understood that the present invention is not limited to the above described embodiments but incorporates all embodiments within the scope of the appended independent claims.

CLAIMS

1. Power converter for DC/DC or AC/DC conversion, said power converter (PC) having a primary side and a secondary side separated by a transformer (TX1), said primary side being connected to a primary winding of said transformer (TX1) and being an input circuit of said power converter, and said secondary side being connected to a secondary winding of said transformer (TX1) and being an output circuit of said power converter (PC), said power converter (PC) further comprising at least one active clamp circuit (ACC) connected to said secondary side; **characterised in** that said at least one active clamp circuit (ACC) comprises:

- a first capacitor (C1) connected in series with a parallel combination of a switch (S1) and a diode (D1), and
- a second capacitor (C2) connected in parallel with said series combination of said first capacitor (C1) and said parallel combination of said switch (S1) and said diode (D1).

2. Power converter according to claim 1, wherein said active clamp circuit (ACC) further comprises:

- a first node (1; 1') being connected to said first capacitor (C1) and to said second capacitor (C2),
- a second node (2; 2') being connected to said first capacitor (C1), said switch (S1) and to an anode of said diode (D1), and
- a third node (3; 3') being connected to said switch (S1), a cathode of said diode (D1) and to said second capacitor (C2).

3. Power converter according to claim 2, wherein said first node (1; 1') is connected to a first node of said secondary winding (10) and said third node (3; 3') is connected to a low ohmic node of said secondary side.

4. Power converter according to claim 2 or 3, comprising a first (ACC1) and a second active clamp circuit (ACC2), wherein:

- a first node (1) of said first active clamp circuit (ACC1) is connected to a first node (10) of said secondary winding, and

- a first node (1') of said second active clamp circuit (ACC2) is connected to a second node (11) of said secondary winding.

5. Power converter according to claim 4, wherein:

5 - a third node (3) of said first active clamp circuit (ACC1) is connected to a low ohmic node of said secondary side, and

- a third node (3') of said second clamp circuit (ACC2) is connected to a low ohmic node of said secondary side.

10 6. Power converter according to claim 5, wherein said power converter (PC) is arranged as a current doubler, fullbridge, flyback or a forward topology.

7. Power converter according to claim 1, wherein said secondary winding is connected in series with an inductance $L1$, said inductance $L1$ being: a leakage inductance transformed to said secondary side, or said leakage inductance transformed to said secondary side plus at least one external inductance.

8. Power converter according to claim 7, wherein said first capacitor (C1) and said inductance $L1$ form a resonant circuit with a resonance frequency $f_R = \frac{1}{2\pi\sqrt{L1 \cdot C1}}$, where
20 C1 is a value of said first capacitance (C1).

9. Power converter according to claim 8, wherein said resonance frequency f_R is 0.5 - 4.0 times a switching frequency f_s of said power converter (PC), and preferably 1.0 - 2.0 times said switching frequency f_s .

25 10. Power converter according to claim 7, wherein a value $C2$ of said second capacitance (C2) is dependent on said inductance $L1$, a peak current IPK_{C1} in said first capacitance (C1), and a voltage $V1$ defined as a input voltage of said power converter (PC) times a turn ratio of said transformer (TX1).

11. Power converter according to claim 10, wherein said value $C2$ of said second capacitance ($C2$) is given by the relation: $C2 = \frac{IPK_{C1}^2 \cdot L1}{V1^2}$.

12. Power converter according to claim 1, further comprising at least one primary switch (QA; QB; QC; QD) wherein:

- said at least one primary switch (QA; QB; QC; QD) is a corresponding switch to said at least one active clamp circuit (ACC), and
- said at least one active clamp circuit (ACC) is arranged to be turned on and off substantially at the same time as when said corresponding primary switch (QA; QB; QC; QD) is turned on and off.

13. Power converter according to claim 12, wherein:

- said at least one active clamp circuit (ACC) is turned on and off with a delay d when said at least one corresponding primary switch (QA; QB; QC; QD) is turned on and off, and
- said delay d being less than a time interval TON , when said at least one corresponding primary switch (QA; QB; QC; QD) is turned on, and preferably less than $TON/10$.

14. Power converter according to claim 1, wherein said parallel combination of said switch (S1) and said diode (D1) is a PMOS or a NMOS transistor.

15. Power converter according to claim 1, wherein said switch (S1) is a bipolar transistor or an IGBT transistor.

16. System comprising at least one power converter (PC) according to any of the preceding claims and at least one control circuit arranged for controlling one or more switches in said power converter (PC).

17. Method for controlling at least one active clamp circuit (ACC) in a power converter (PC), said power converter (PC) having a primary side and a secondary side separated by a transformer (TX1);

- said primary side being connected to a primary winding of said transformer (TX1) and being an input circuit of said power converter (PC), and said secondary side being connected to a

secondary winding of said transformer (TX1) and being an output circuit of said power converter (PC);

- said power converter (PC) further comprising at least one active clamp circuit (ACC) connected to said secondary side and at least one corresponding primary switch (QA; QB; QC; QD) connected to said primary side, wherein said at least one active clamp circuit (ACC) is arranged to alter a shape of a current waveform in said at least one corresponding primary switch (QA; QB; QC; QD) so that said current waveform is higher when said corresponding primary switch (QA; QB; QC; QD) is turned on than when said corresponding primary switch (QA; QB; QC; QD) is turned off; **characterised in that:**

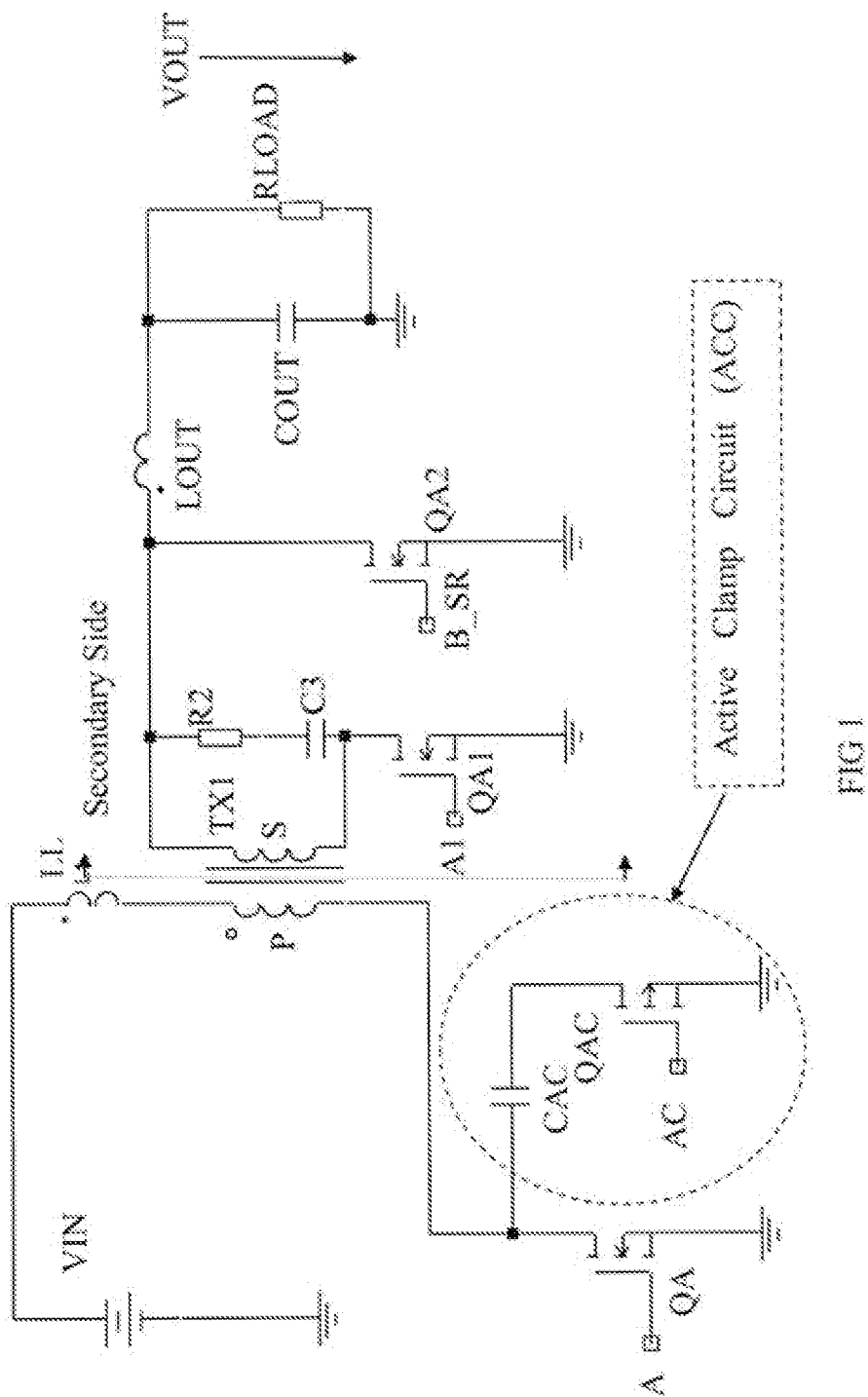
- said at least one active clamp circuit (ACC) is turned on and off substantially at the same time as when said at least one corresponding primary switch (QA; QB; QC; QD) is turned on and off.

18. Method according to claim 17, wherein said at least one active clamp circuit (ACC) is turned on and off with a delay d when said at least one corresponding primary switch (QA; QB; QC; QD) is turned on and off.

19. Method according to claim 18, wherein said delay d is less than a time interval T_{ON} , when said at least one corresponding primary switch (QA; QB; QC; QD) is turned on, and preferably less than $T_{ON}/10$.

20. Computer program, characterised in code means, which when run in a computer causes said computer to execute said method according to any of claims 17-19.

21. Computer program product comprising a computer readable medium and a computer program according to 20, wherein said computer program is included in the computer readable medium, and consist of one or more from the group: ROM (Read-Only Memory), PROM (Programmable ROM), EPROM (Erasable PROM), Flash memory, EEPROM (Electrically EPROM) and hard disk drive.



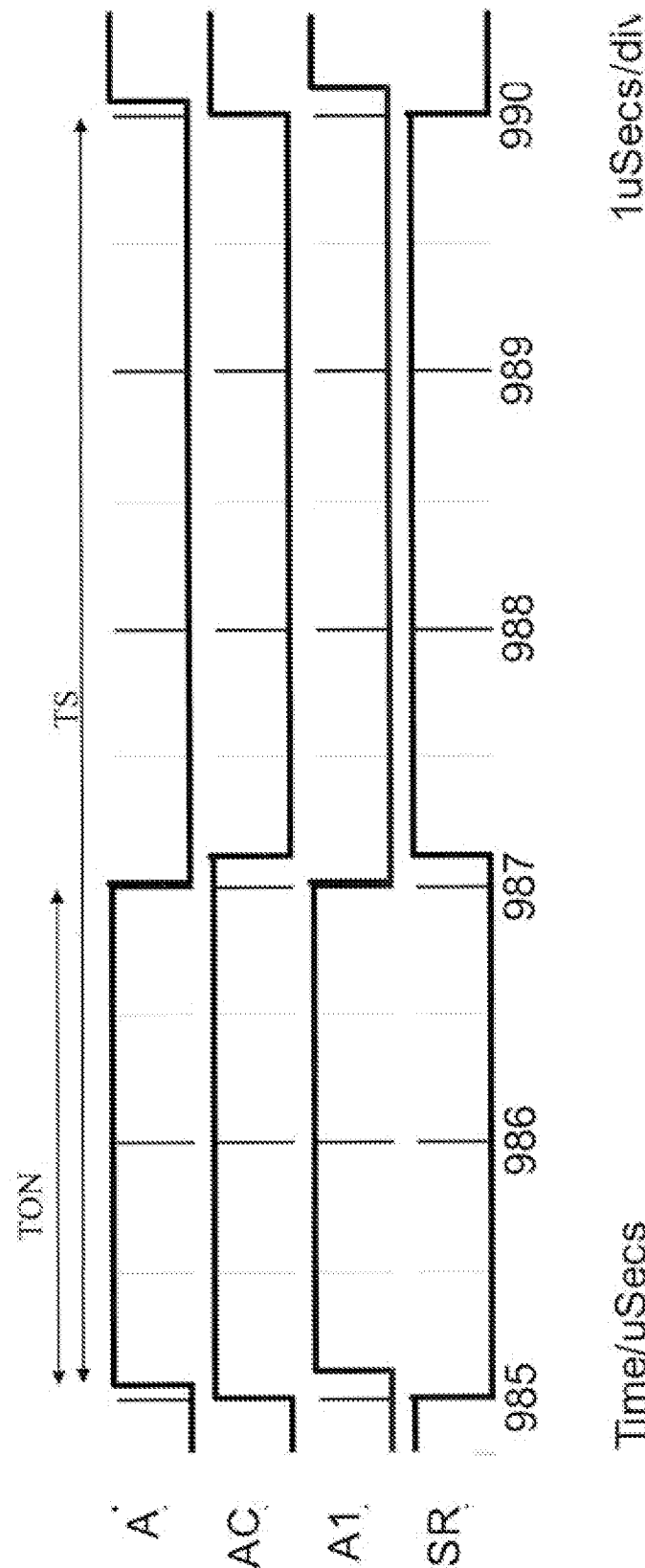


FIG 2

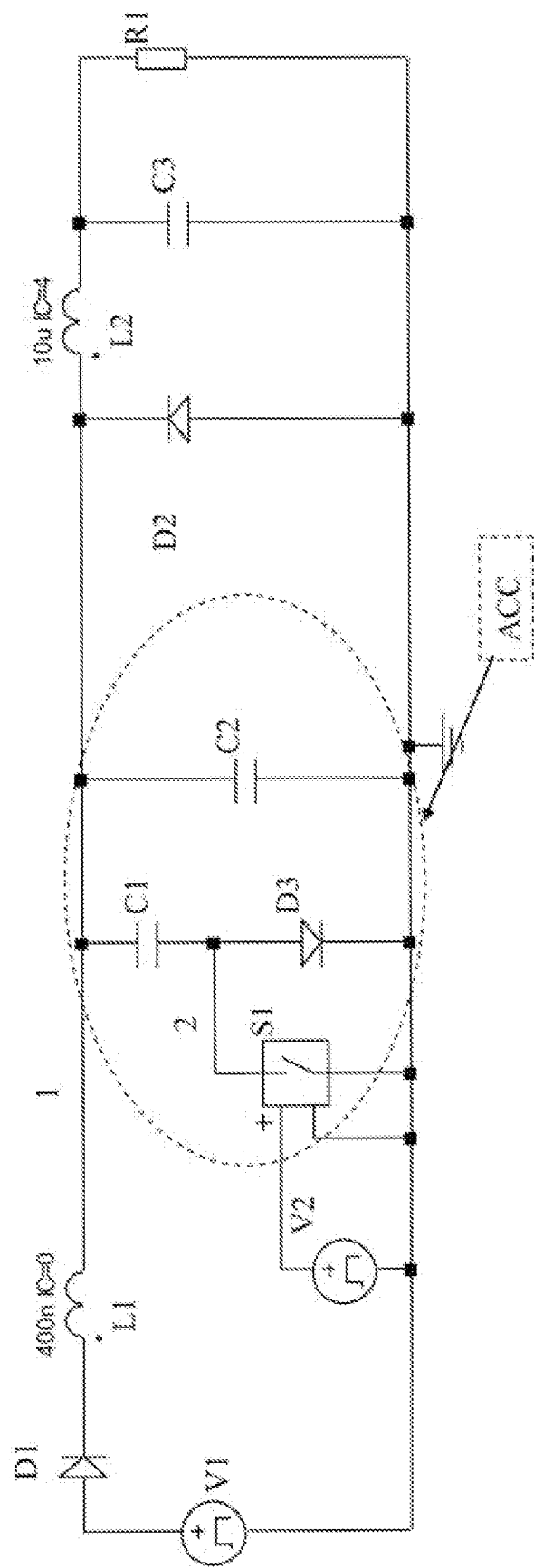


FIG 3

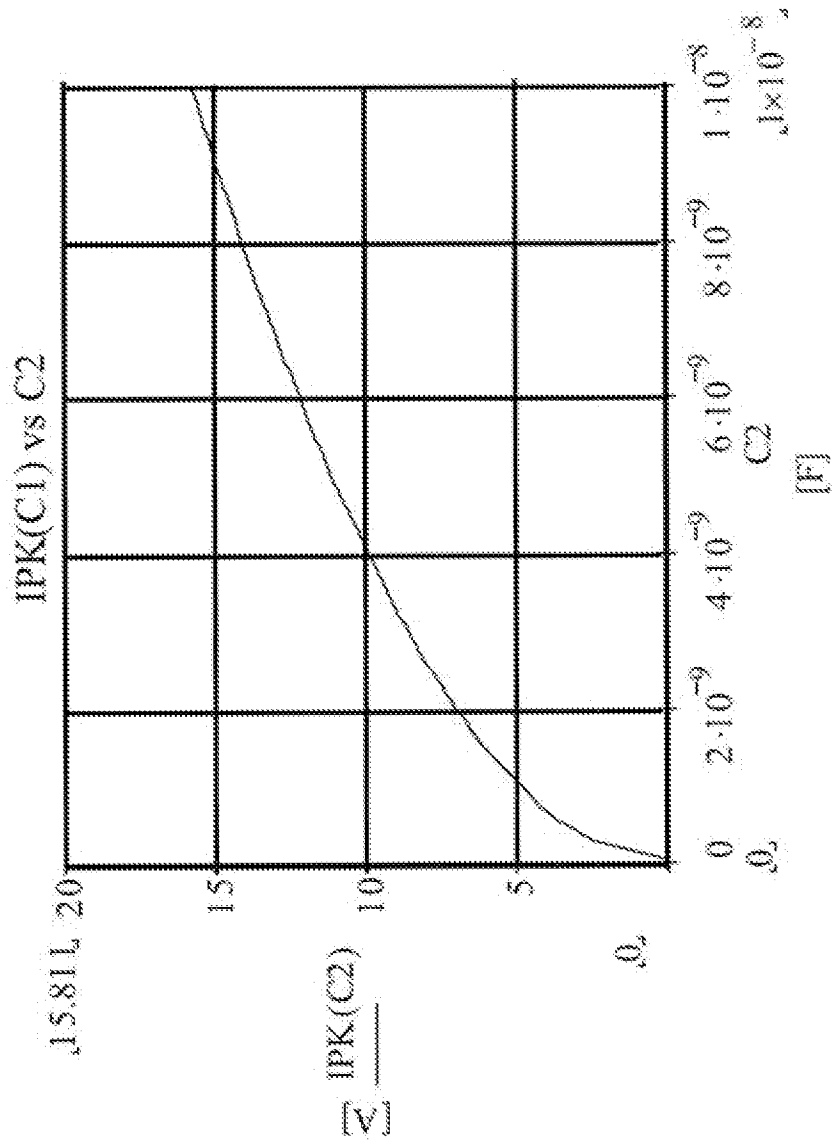


FIG 4

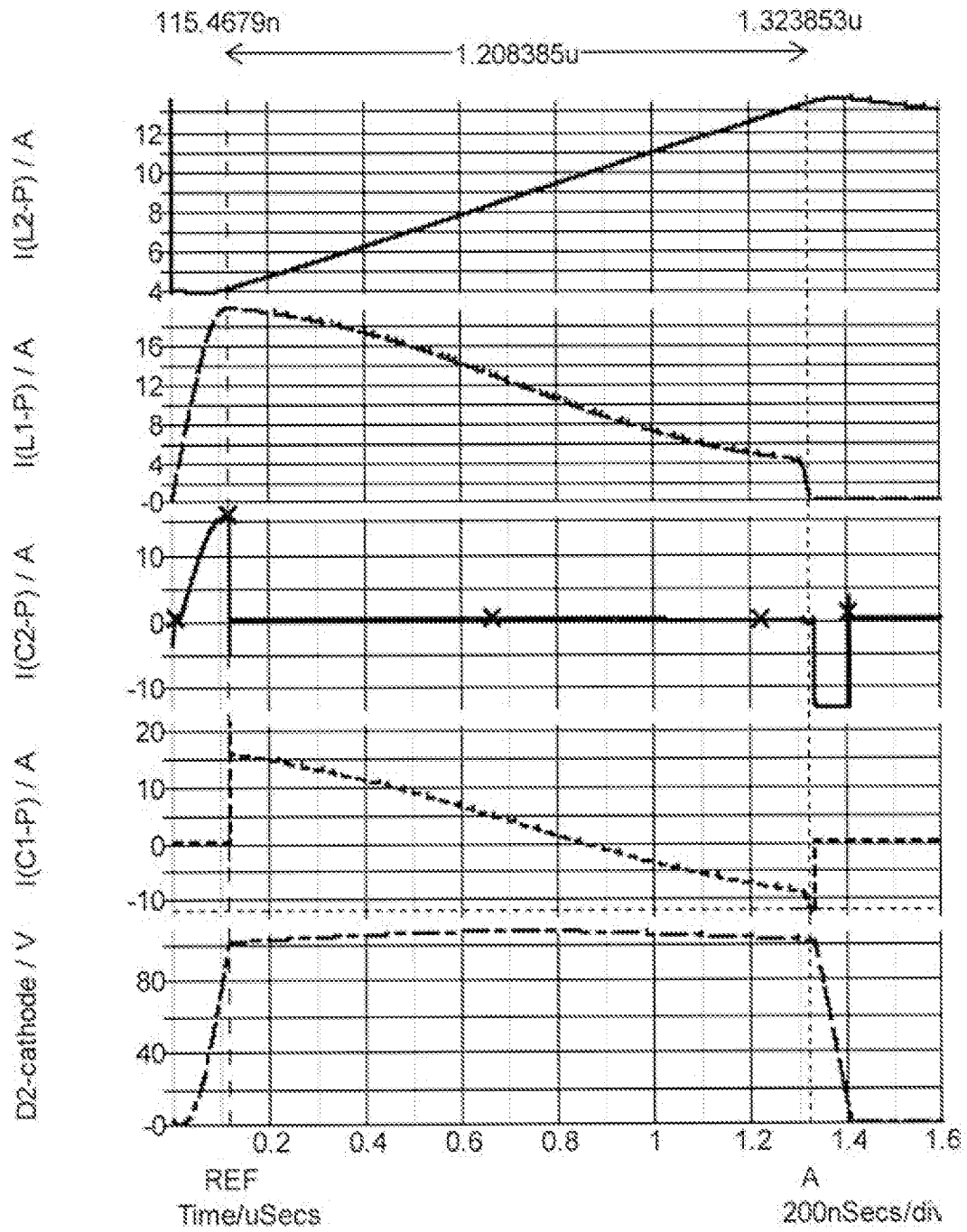


FIG 5

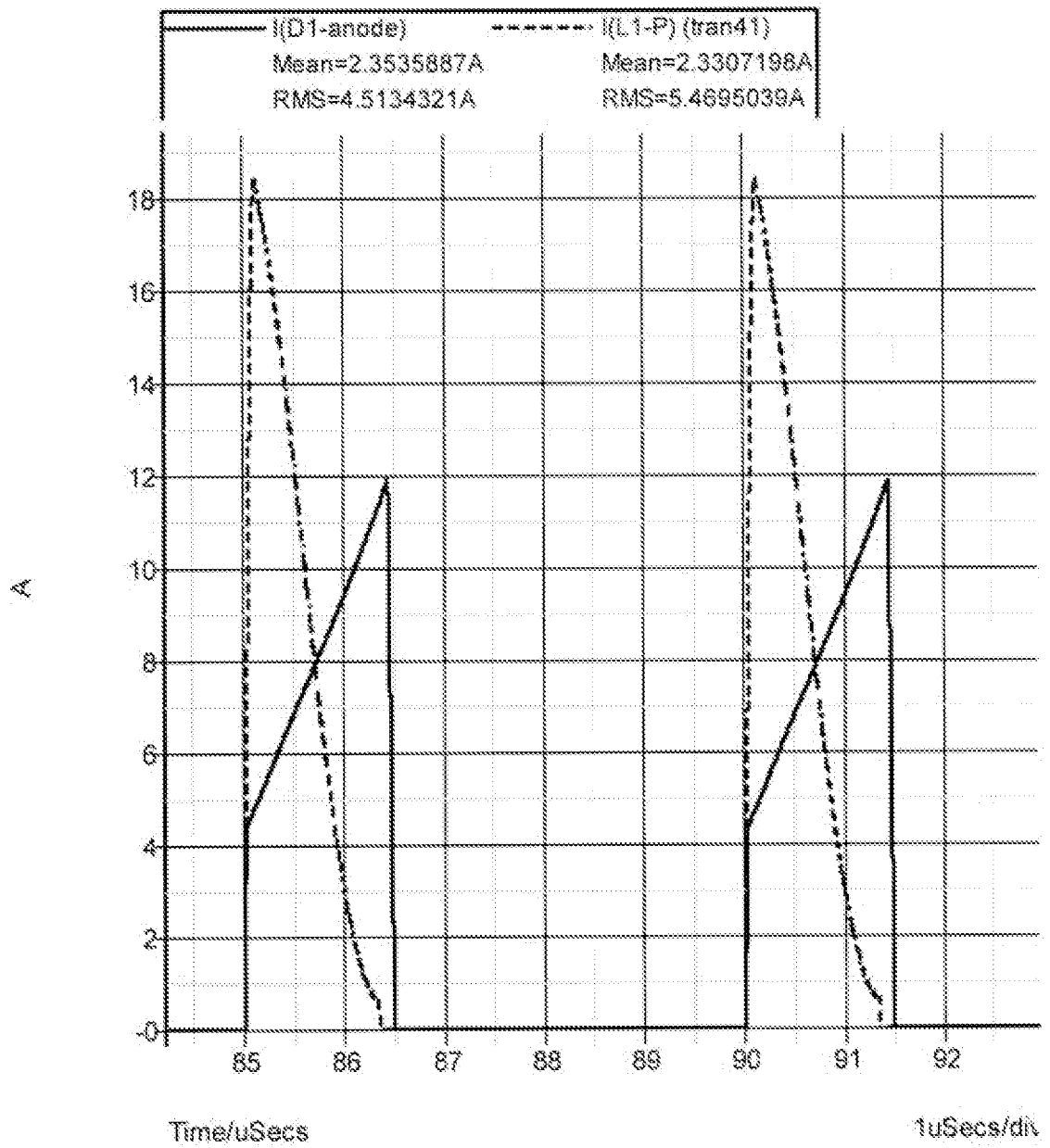


FIG 6

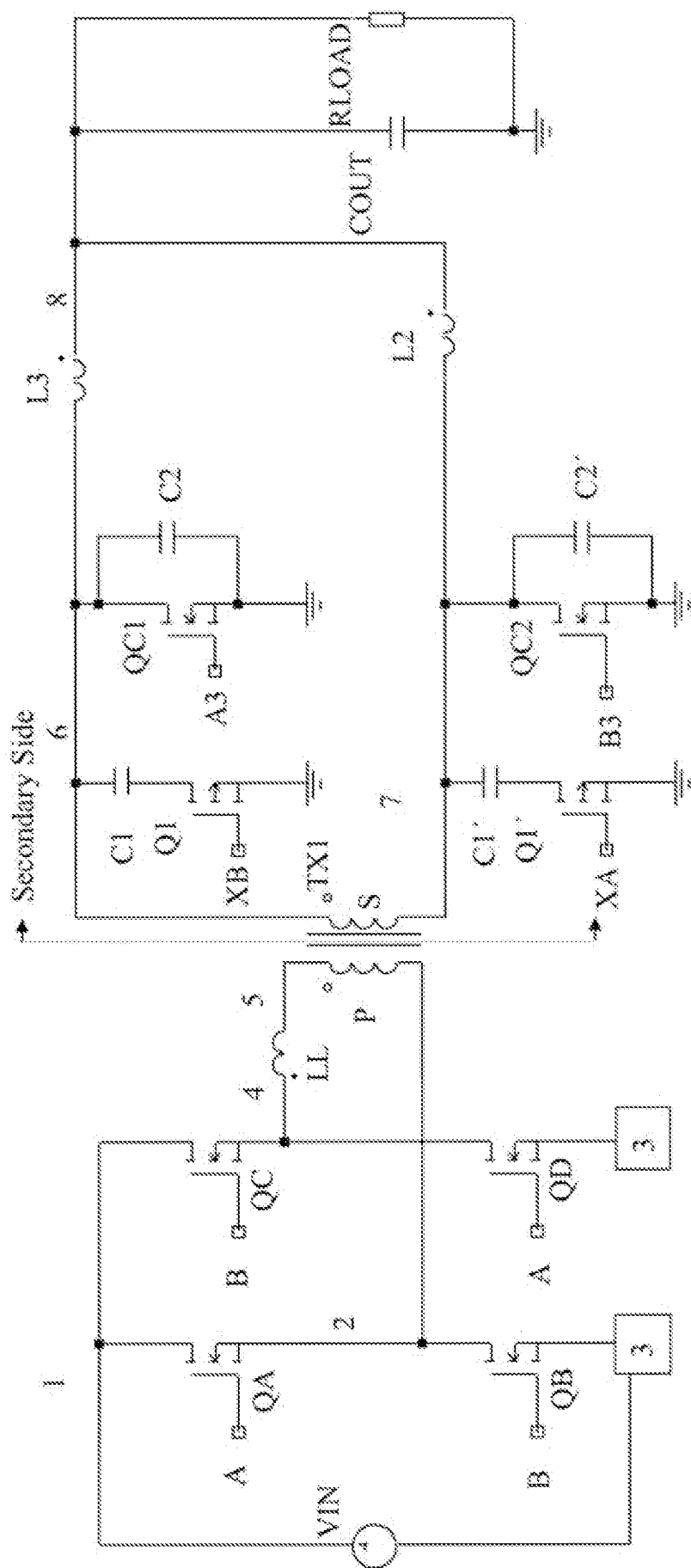


FIG 7

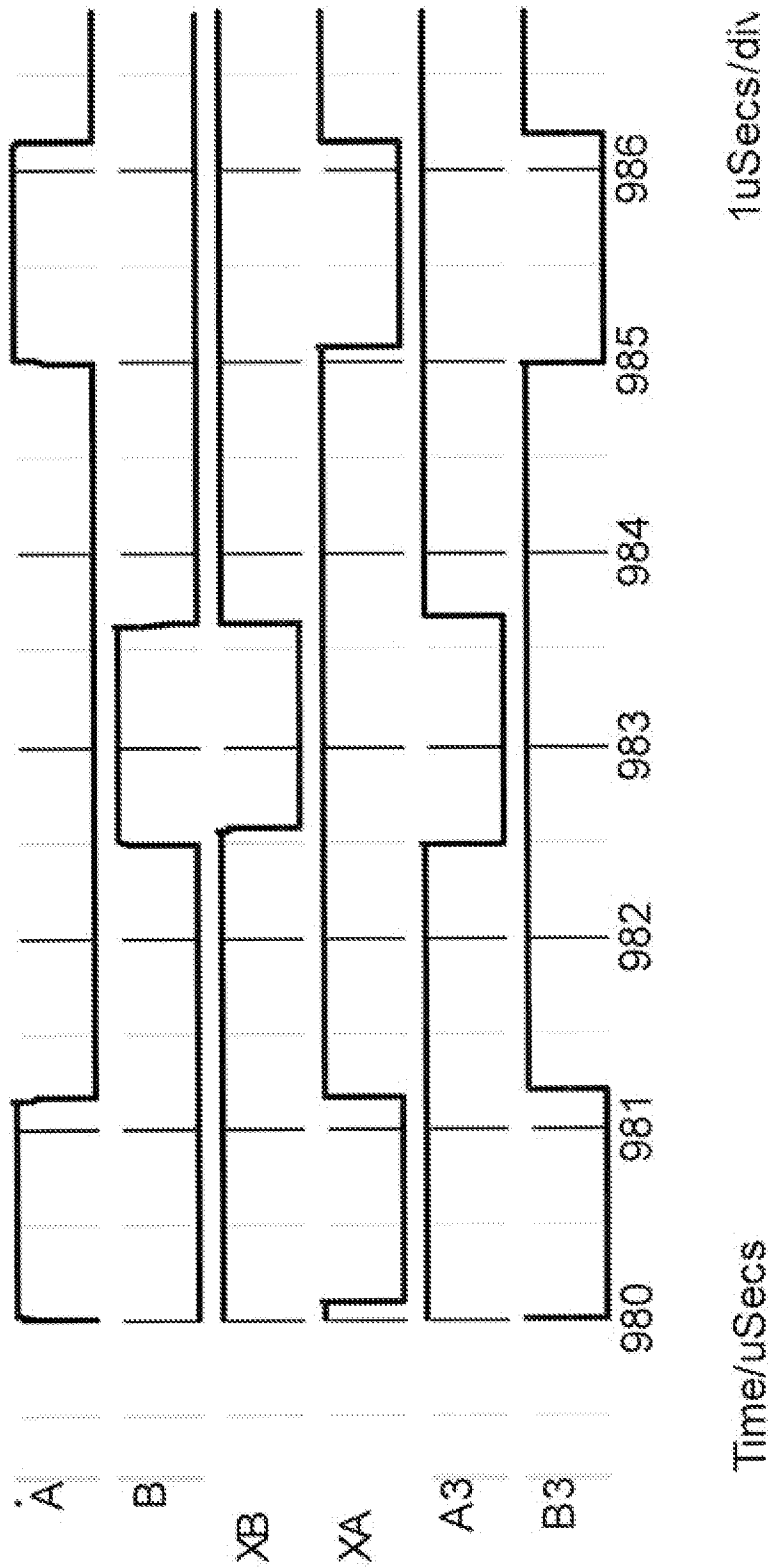


FIG 8

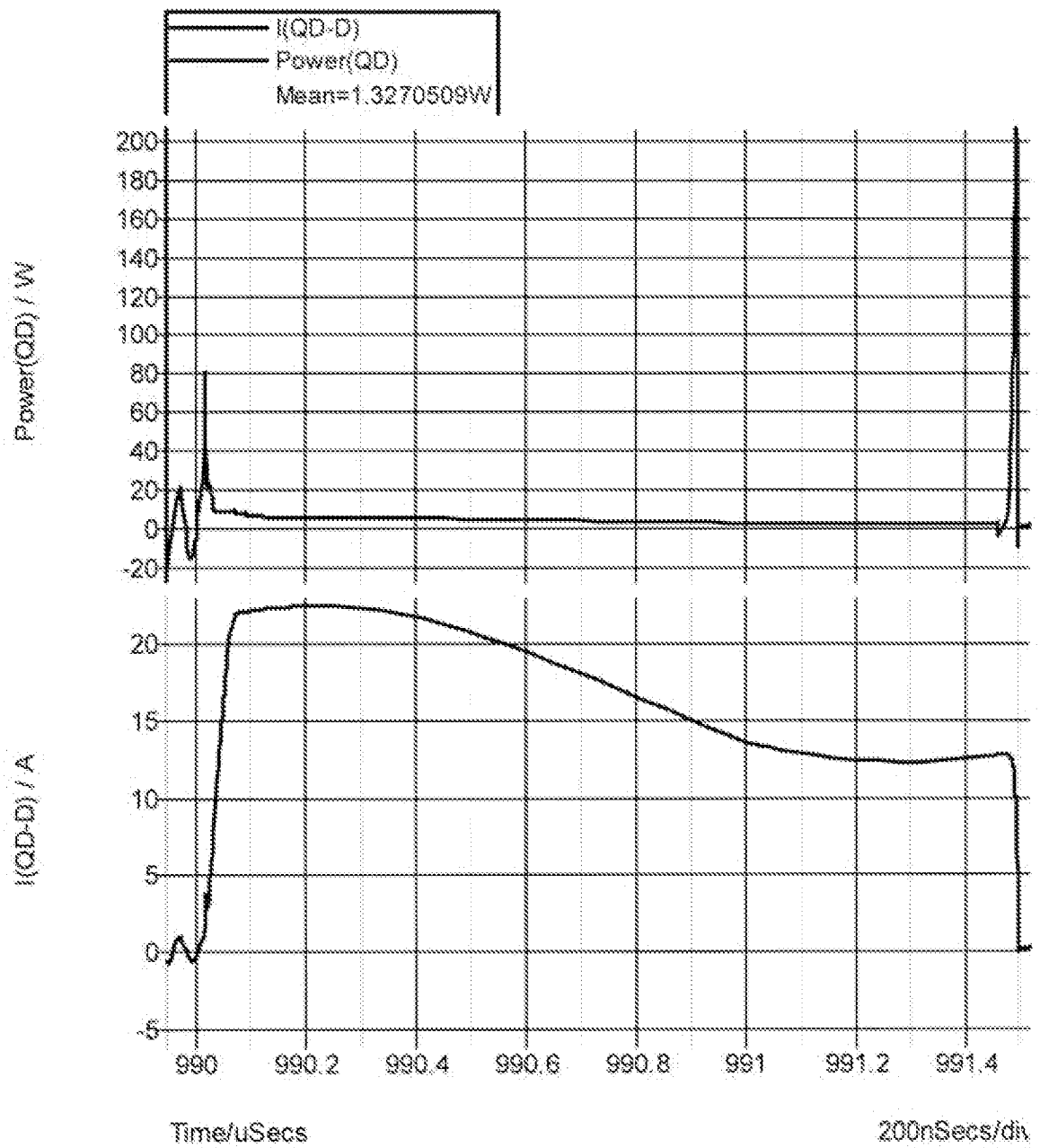


FIG 9

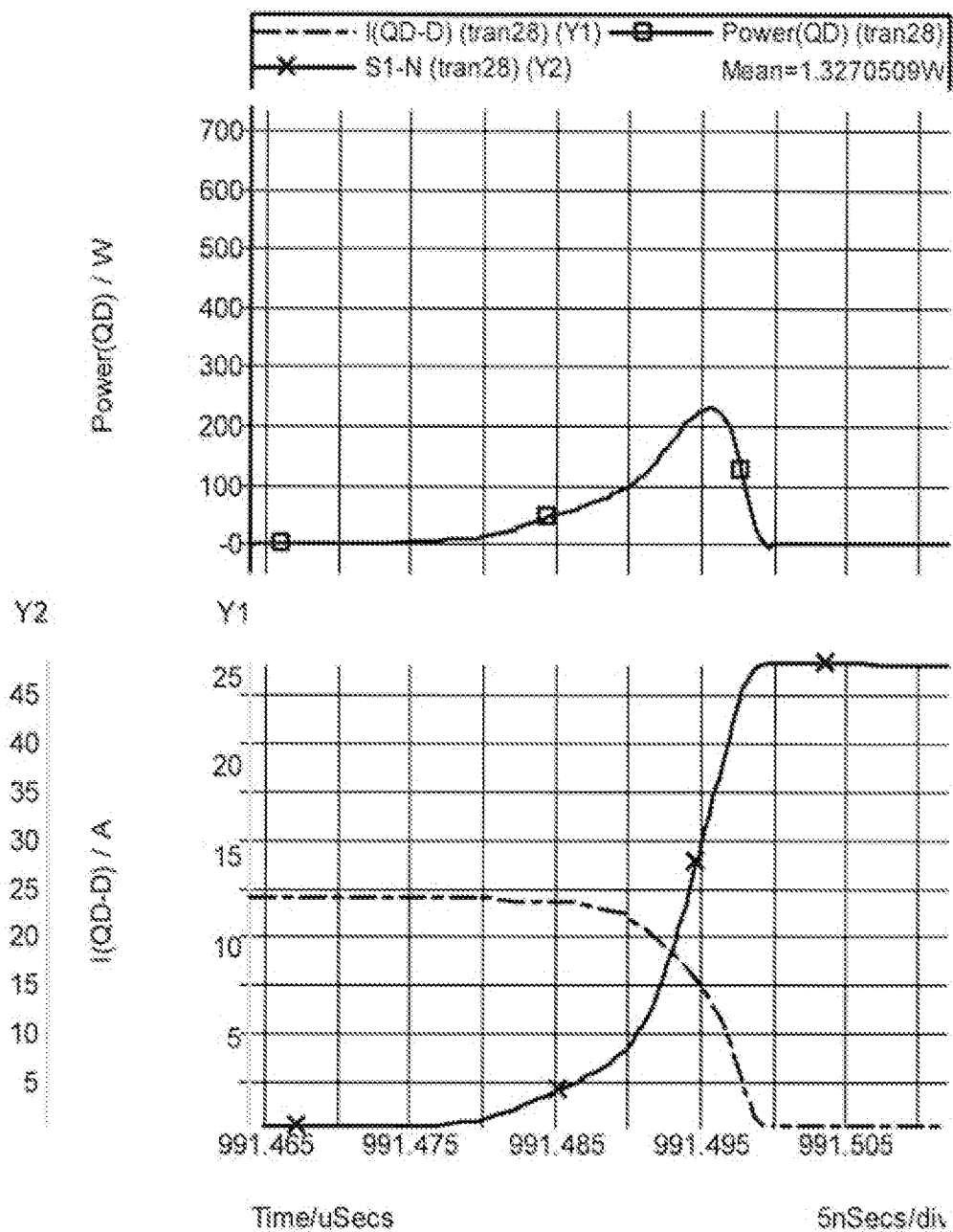


FIG 10

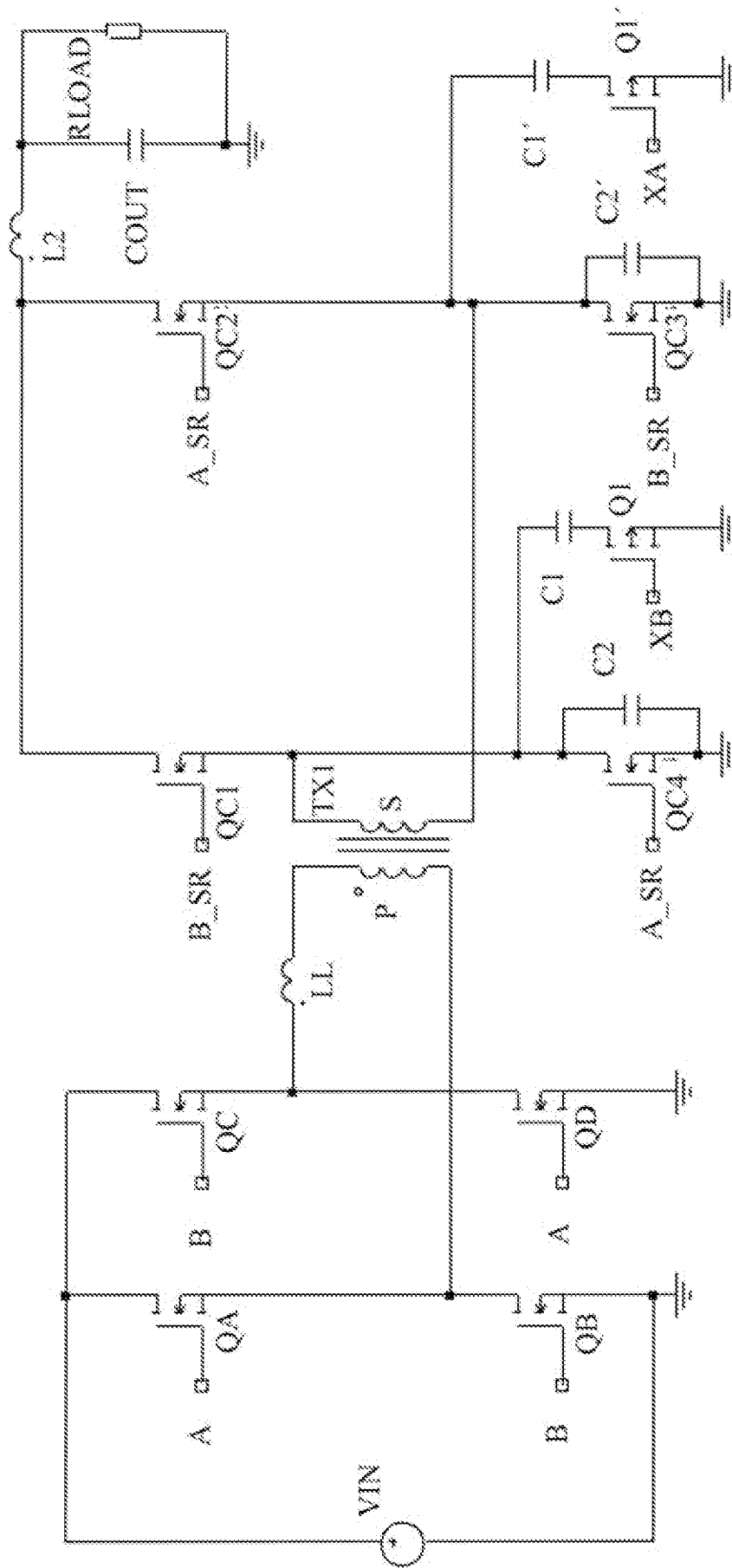


FIG 11

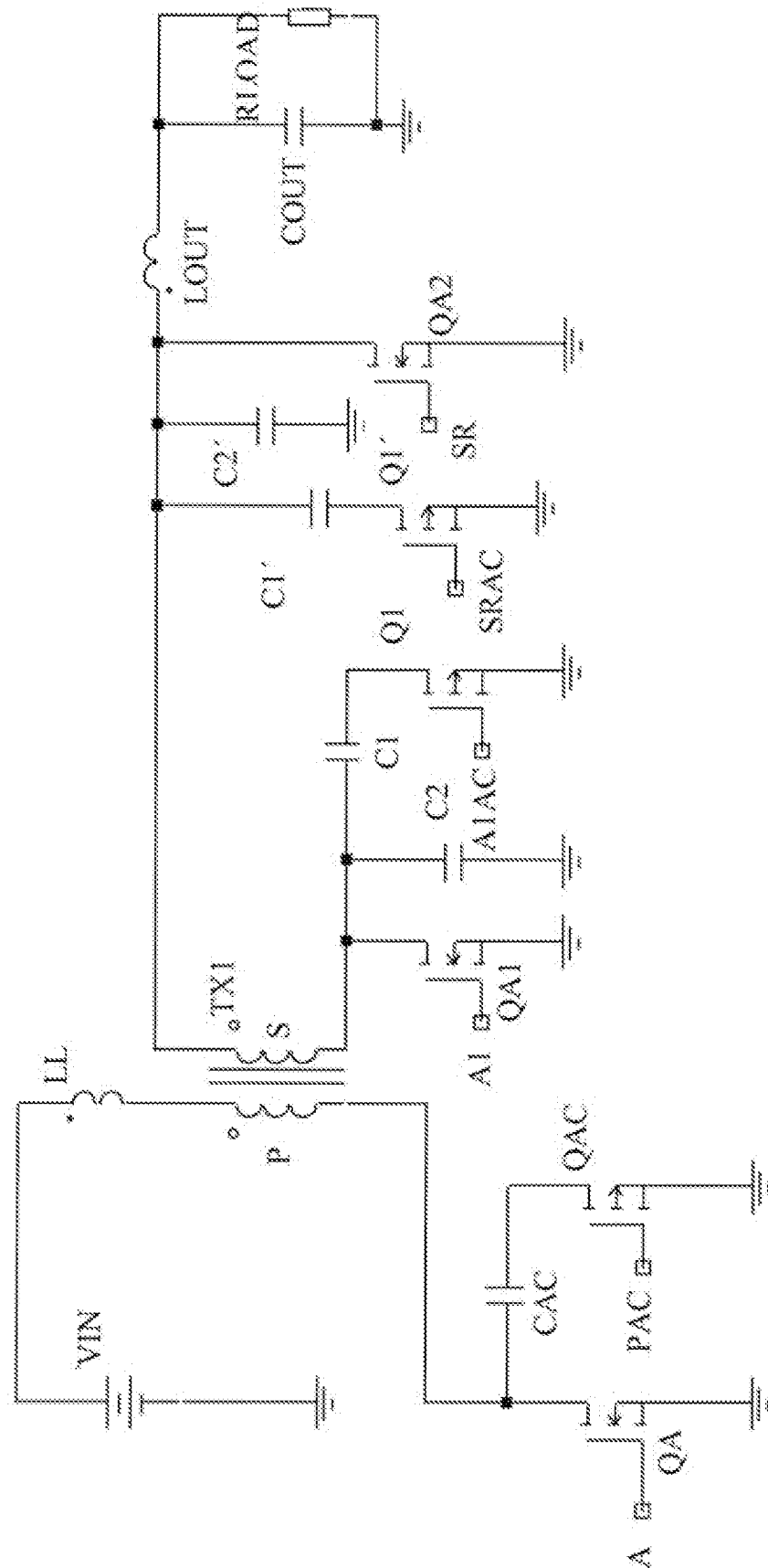


FIG 12

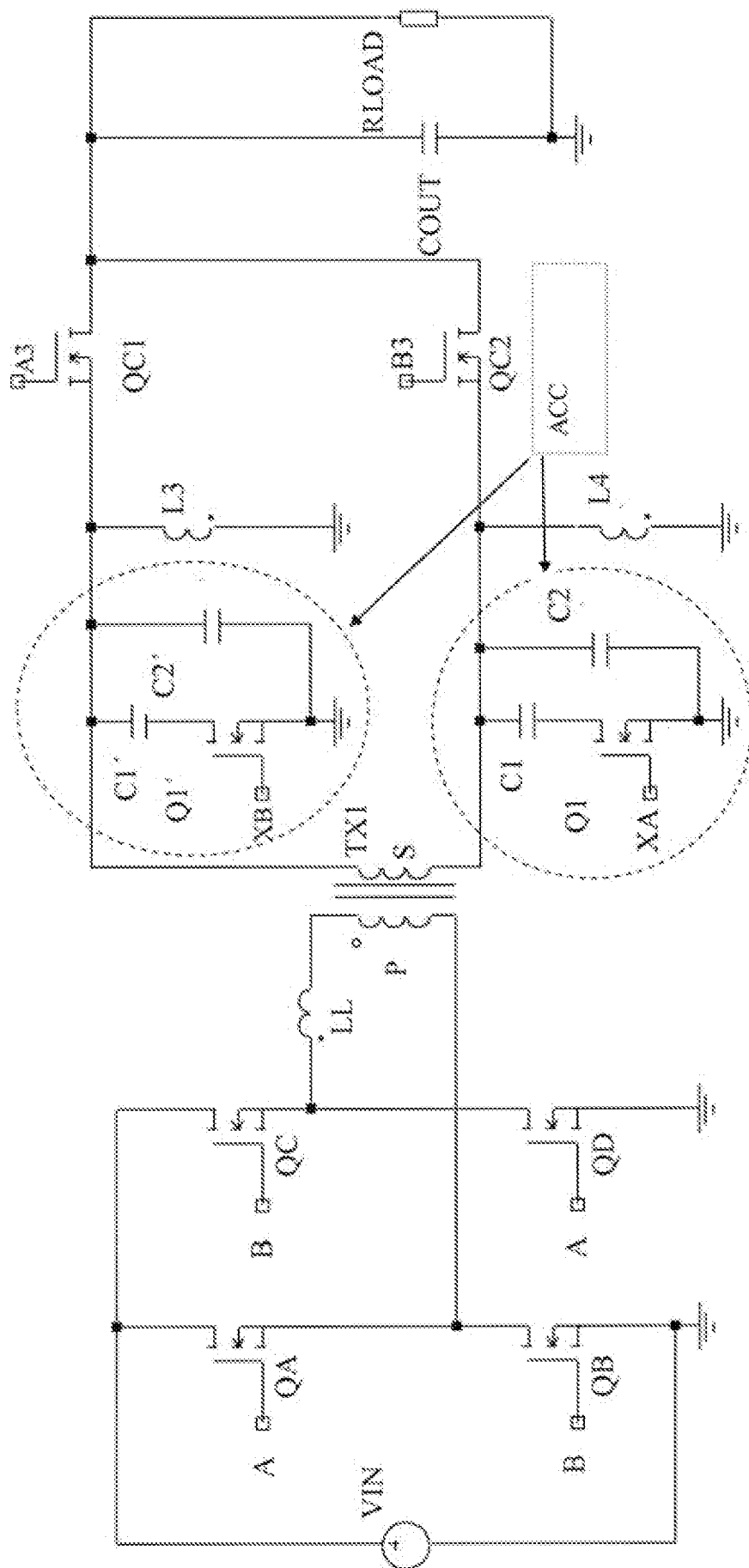


FIG 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/079419

A. CLASSIFICATION OF SUBJECT MATTER

see extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H02M3/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI, CNTXT, TWABS: ACC, active, clamp+, capacity+, diode?, switch+, power converter, power supply, electric source

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 201015031 Y (SPI ELECTRONIC CO LTD) 30 Jan. 2008 (30.01.2008) the whole document	1-21
A	US 6882548 B1 (TYCO ELECTRONICS POWER SYSTEMS INC) 19 Apr. 2005 (19.04.2005) column 5, line 29 to column 7, line 25 of the description, and Fig. 1	1-21
A	JP 2007295709 A (YOKOGAWA DENKI KK) 08 Nov. 2007 (08.11.2007) the whole document	1-21
A	CN 201118530 Y (HIGH EFFICIENCY ELECTRONIC CO LTD) 17 Sep. 2008 (17.09.2008) the whole document	1-21
A	CN 101022244 A (UNIV ZHEJIANG) 22 Aug. 2007 (22.08.2007) the whole document	1-21

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 20 Jul. 2011 (20.07.2011)	Date of mailing of the international search report 25 Aug. 2011 (25.08.2011)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer XU, Zhenxia Telephone No. (86-10)62411785

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/079419

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see extra sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☒ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2010/079419

Continuation of : Observations where unity of invention is lacking

The Authority considers that there are two inventions covered by the claims indicated as follows:

1. Claims 1-16 directed to: a power converter;

2. Claims 17-19, 20, 21 respectively directed to: a method for controlling at least one active clamp circuit in a power converter, a computer program thereof and a computer program product thereof.

The same or corresponding technical features between independent claim 1 in the first invention and independent claims 17, 20 and 21 in the second invention is that a power converter includes a primary side and a secondary side separated by a transformer, the primary side being connected to a primary winding of the transformer and being an input circuit of the power converter, and the secondary side being connected to a secondary winding of the transformer and being an output circuit of the power converter, besides the power converter further including at least one active clamp circuit connected to the secondary side. However, D1 (US 6882548 B1) discloses the said same or corresponding technical features. Therefore the above two inventions do not exist a technical relationship involving the same or corresponding special technical features which make a contribution to the prior art so as to form a single general inventive concept. The application hence does not meet the requirements of unity of invention as defined in Rules 13.1 PCT.

Continuation of : CLASSIFICATION OF SUBJECT MATTER

H02M 3/28 (2006.01) i

H02M 3/335 (2006.01) i

International application No.
PCT/CN2010/079419

Form PCT/ISA /210 (patent family annex) (July 2009)