(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 December 2005 (08.12.2005)

PCT

(10) International Publication Number
WO 2005/117085 A2

(51) International Patent Classification[7]: H01L 21/311

(21) International Application Number: PCT/US2005/018050

(22) International Filing Date: 23 May 2005 (23.05.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/709722 25 May 2004 (25.05.2004) US

(71) Applicant (*for all designated States except US*): **INTERNATIONAL BUSINESS MACHINES CORPORATION?** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(72) **Inventor; and**
(75) **Inventor/Applicant** (*for US only*): **STAMPER, Anthony, K.** [US/US]; 46 Evergreen Drive, Williston, VT 05495 (US).

(74) **Agent: CANALE, Anthony, J.**; International Business Machines Corporation, Intellectual Property Law--Zip 972E, 1000 River Street, Essex Junction, VT 05452 (US).

(81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

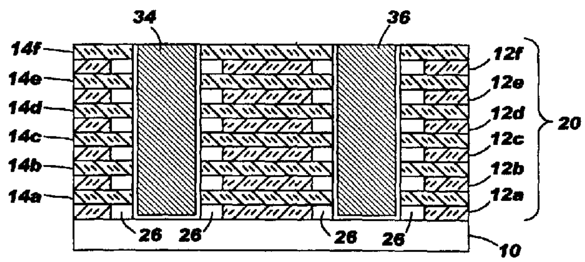
(84) **Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHOD AND FORMING A SEMICONDUCTOR DEVICE HAVING AIR GAPS AND THE STRUCTURE SO FORMED



(57) **Abstract:** A method of forming a semiconductor device, and the device so formed. Depositing alternating layers of a first dielectric material (12a-f) and a second dielectric material (14a-f), wherein the first and second dielectric materials are selectively etchable at different rates. Forming a first feature (22, 24) within the alternating layers of dielectric material. Selectively etching the alternating layers of dielectric material to remove at least a portion (26) of the first dielectric material in each layer having the first dielectric material and leaving the second dielectric material as essentially unetched.

WO 2005/117085 A2

METHOD OF FORMING A SEMICONDUCTOR DEVICE HAVING AIR GAPS AND THE STRUCTURE SO FORMED

TECHNICAL FIELD

The present invention relates generally to semiconductor devices, and more particularly, to a method of forming a semiconductor device having air gaps within the wiring levels, and the structure so formed.

BACKGROUND ART

As semiconductor devices continue to shrink, the distance between device features is reduced. Within metal wiring layers reducing the distance between features causes an increased capacitance. Therefore, there is a need in the industry for a method of forming a semiconductor device capable of maintaining a lower capacitance while reducing the distance between device features that overcomes the above and other problems.

DISCLOSURE OF INVENTION

The present invention provides a method of forming a semiconductor device having air gaps within the metal wiring level, and the structure so formed, that solves the above-stated problems.

A first aspect of the invention provides a method of forming a semiconductor device, comprising: depositing alternating layers of a first and a second dielectric material, wherein the first and second dielectric materials are selectively etchable at different rates; forming a first feature within the alternating layers of dielectric material; and selectively etching the alternating layers of dielectric material to remove at least a portion, but not all, of the first dielectric material in each layer having the first dielectric material and leaving the second dielectric material as essentially unetched.

A second aspect of the invention provides a method of forming a semiconductor device, comprising: depositing alternating layers of a first and a second insulative material; forming a damascene feature; and forming openings within the layers of first insulative material.

A third aspect of the invention provides a semiconductor device, comprising: semiconductor device, comprising: a metal wiring level having alternating layers of a first dielectric material and a second dielectric material having a first feature formed within the alternating layers of first and second dielectric material; and a plurality of openings within the first dielectric material.

A fourth aspect of the invention provides a semiconductor device, comprising: a plurality of alternating first and second insulative layers, wherein the first and second insulative layers have different etch rates; a first feature formed within the first and second insulative layers; a plurality of openings within the plurality of first insulative layers formed during a selective etch.

The foregoing and other features and advantages of the invention will be apparent from the following more particular description of the embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of this invention will be described in detail, with reference to the following figures, wherein like designations denote like elements, and wherein:

Fig. 1 depicts a cross-sectional view of a device comprising a pre-metal dielectric layer and a first insulative layer thereon, in accordance with embodiments of the present invention;

Fig. 2 depicts the device of Fig. 1 having a second insulative layer thereon;

Fig. 3 depicts the device of Fig. 2 having a third insulative layer thereon;

Fig. 4 depicts the device of Fig. 3 having a fourth insulative layer thereon;

Fig. 5 depicts the device of Fig. 4 having a plurality of insulative layers thereon forming a first metal wiring level;

Fig. 6 depicts the device of Fig. 5 having a pair of damascene features formed therein;

Fig. 7 depicts the device of Fig. 6 having a plurality of air gaps formed within select insulative layers;

Fig. 8 depicts the device of Fig. 7 having a conformal liner formed thereover;

Fig. 9 depicts the device of Fig. 8 having a conductive layer deposited thereon;

Fig. 10 depicts the device of Fig. 9 following polishing;

Fig. 11 depicts the device of Fig. 10 having an insulative layer formed over the first metal wiring level;

Fig. 12 depicts the device of Fig. 11 having a plurality of insulative layers forming a second metal wiring level;

Fig. 13 depicts the device of Fig. 12 having a first damascene feature formed therein;

Fig. 14 depicts the device of Fig. 13 having second damascene features formed therein;

Fig. 15 depicts the device of Fig. 14 having a plurality of air gaps formed within select insulative layers;

Fig. 16 depicts the device of Fig. 15 having a conductive layer deposited thereon; and

Fig. 17 depicts the device of Fig. 16 following polishing.

BEST MODE FOR CARRYING OUT THE INVENTION

Although certain embodiments of the present invention will be shown and described in detail, it should be understood that various changes and modifications might be made without departing from the scope of the appended claims. The scope of the present invention will in no way be limited to the number of constituting components, the materials thereof, the shapes thereof, the relative arrangement thereof, etc. Although the drawings are intended to illustrate the present invention, the drawings are not necessarily drawn to scale.

Fig. 1 depicts a cross-sectional view of a pre-metal dielectric (PMD) 10 upon which a first insulative layer 12a is formed. The PMD 10 comprises one or more dielectric materials, such as a SiO_2-based material, i.e., SiO_2, PSG, BPSG, SiCOH (OSG), SiLK™ (Dow Chemical Corp.), SiN, SiC, SiCN, C-H, etc. The first insulative layer 12a comprises a dielectric material, in this example, an organic dielectric material, such as, polyarylene ether (SILK™), parylene (N or F), Teflon, or other porous versions of these films. The type of organic dielectric material used may depend upon the deposition technique used. For example, if the first insulative layer 12a is formed using chemical vapor deposition (CVD) or plasma enhanced chemical vapor deposition (PECVD), the parylene (N or F), Teflon, or other porous versions of these films may be used. If, however, first insulative layer 12a is formed using spin-on deposition, the SILK™ may be used. The first insulative layer 12a may be formed having a thickness within the range of 5-10 nm.

A second insulative layer 14a is then formed on the first insulative layer 12a, as illustrated in Fig. 2. The second insulative layer 14a comprises a dielectric material, in this example, an inorganic dielectric material, such as, SiCOH (OSG), SiO_2, florinated SiO_2 (FSG), such as methylsilesquoxane (MSQ), or porous versions of these materials. As with the first insulative layer 12a, the second insulative layer 14a may be formed using CVD, PECVD, spin-on deposition, or other similar deposition techniques. The second insulative layer 14a may be formed having a thickness within the range of 5-10 nm.

As illustrated in Fig. 3, a third insulative layer 12b is formed on the second insulative layer 14a. The third insulative layer 12b comprises an organic dielectric material similar to that of the first insulative layer 12a. The third insulative layer 12b is formed using similar techniques, and having a similar thickness, to that of the first insulative layer 12a.

As illustrated in Fig. 4, a fourth insulative layer 14b is formed on the third insulative layer 12b. The fourth insulative layer 14b comprises an inorganic dielectric material similar to that of the second insulative layer 14a. The fourth insulative layer 14b is formed using similar techniques, and having a similar thickness, to that of the second insulative layer 14a.

Alternating layers of organic and inorganic dielectric material may be formed in this manner on the substrate 10, as illustrated in Fig. 5, to a desired thickness for a first metal wiring level 20. In the present example layers 12c-12f comprise an organic dielectric material similar to that of the first and third insulative layers 12a, 12b. Likewise, layers 14c-14f comprise an inorganic dielectric material similar to that of the second and fourth insulative layers 14a, 14b. The number of layers depicted in the present invention is for illustrative purposes only, and is not intended to be limiting in any way, so long as at least one organic layer and one inorganic layer are present. Also, it should be noted that the organic dielectric material is deposited first in the present example for illustrative purposes only. Either the inorganic or organic dielectric material may be deposited first.

It should also be noted that it may be desirable to deposit the alternating layers of organic and inorganic insulative material in-situ. For example, a single PECVD chamber may be used to deposit both the inorganic and organic layers without leaving the chamber. Also, a spin-apply track may be used wherein the alternating layers are both deposited and cured within the same chamber. Using either technique, the first insulative layer 12a may alternatively be deposited having twice the desired thickness. Thereafter, the first insualtive layer 12a is exposed to a plasma or thermal treatment wherein an upper portion of the first insulative layer 12a is converted into the material needed in the second insulative layer 14a. These methods may help to decrease unevenness in thickness between the organic and inorganic insulative layers, and may increase adhesion between the organic and inorganic insulative layers.

As illustrated in Fig. 6, after the desired thickness for the first wiring level 20 has been achieved, a first feature 22 and, in this example, a second feature 24, are formed within the first wiring level 20. The first and second features 22, 24 are wire trenches for wiring lines that may be formed using conventional patterning and etching techniques.

Following formation of the first and second features 22, 24, a selective etch is performed to remove at least portions of the organic dielectric material within the first wiring level 20, in this example, within layers 12a-12f (Fig. 7). In the present example, where the organic dielectric material comprises p-SILK™ and the inorganic dielectric material comprises p-OSG, an N_2 plasma, H_2 plasma, or other similar plasma etch may be used to selectively remove the organic dielectric material. The N_2 or H_2 etch may be operated in a pressure range of about 3-200 mT at typical parallel plate or high density plasma power and flow conditions. Alternatively, portions of the inorganic dielectric material (p-OSG) may be etched using a wet etchant, such as a 100:1 DHF, leaving the SiLK™ material within layers 14a-14f.

As illustrated in Fig. 7, openings or air gaps 26 are formed following the selective etch of the organic dielectric material within layers 12a-12f. The air gaps 26 are formed within the organic dielectric material of layers 12a-12f, and not within the inorganic dielectric material within layers 14a-14f, because the etch rate of the organic dielectric material of layers 12a-12f is faster than the etch rate of the inorganic dielectric material of layers 14a-14f. The air gaps 26 within the first wiring level 20 reduce the capacitance within the overall device. The size of the air gaps 26 is determined by calibrating the selective etch to remove a portion, but not all, of the organic dielectric material. At least some of the organic dielectric material should remain after the selective etch to prevent mechanical failure of the device, e.g., collapse of the inorganic dielectric layers 14a-14f.

Table 1 below shows estimated comparisons of the capacitance value of the device, using different organic and inorganic materials, with and without the air gaps 26. In particular, the data is modeled from a sample having a first wiring level 20 wire width of about 100nm and a wire spacing of about 100nm, wherein about 33nm of the 100nm organic dielectric within the wire spacing has been removed. This results in about a 20% reduction in Keff (the effective dielectric constant of the device), which translates into about a 20% reduction in the capacitance of the device, since Keff is proportional to the capacitance of the device.

Table 1: Comparison of Keff with air gaps and Keff without air gaps.

Inorganic Dielectric	Organic Dielectric	Keff no air gaps	Keff with air gaps	% reduction in Keff
SiO_2 (K=4)	SiLK(K=2.6)	3.30	2.70	18%
SiCOH (K=3)	SiLK(K=2.6)	2.80	2.24	20%
p-SiCOH*(K=2.5)	SiLK(K=2.6)	2.55	1.99	22%
p-SiO_2*(K=2)	p-SiLK*(K=2.2)	2.10	1.68	20%

(* The "p-" indicates that the dielectric is a porous dielectric.)

After the air gaps 26 are formed, the surface 28 of the first metal wiring layer 20 is sealed to prevent metal, deposited in the next step, from leaking into the air gaps 26. This may be accomplished in several different ways. For example, a conformal liner 30, such as a dielectric having a low dielectric constant, i.e., SiCOH, SiO_2, SiN, SiC, and SiCN, etc., is deposited over the surface 28 of the first metal wiring layer 20 (Fig. 8). The liner 30 may be deposited, having a thickness in the range of about 1-10nm, using PECVCD, HDPCVD, SACVD, APCVD, THCVD, or other similar deposition techniques.

Alternatively, if the air gaps 26 are small, e.g., in the range of about 1-10nm, the metal deposited in the following step may be sufficient to seal the air gaps 26. A plasma vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or other similar deposition technique may also be used to deposit the metal such that very few metal ions actually penetrate the air gaps 26.

After the air gaps 26 are sealed, if a separate sealing process is used as described supra, a conductive material 32 is deposited over the surface 28 of the first wiring level 20 filling the first and second features 22, 24 (Fig. 9). The conductive material 32 may comprise copper lined with a thin refractory metal liner, such as tantalum, as known in the art, or other similarly used material. The surface 28 of the first wiring level 20 is polished, using conventional techniques, to remove the excess conductive material 32, leaving the conductive material 32 within the first and second features 22, 24 to form a first wire 34 and a second wire 36 (Fig. 10).

The first metal wiring level 20 illustrated in this example is a single damascene wiring level. As illustrated in Figs. 11-17, the present invention is designed for use in conjunction with a dual damascene wiring level as well. As shown in Fig. 11, a third insulative layer 38 may be deposited over the surface 28 of the first wiring level 20. The third insulative layer 38 may comprises one or more dielectric materials, having a low dielectric constant, that is not susceptible to removal during the subsequent etch process used to form the air gaps (formed infra). For example, the third insulative layer 38 may comprise porous SiCOH (p-OSG), SiO_2, florinated SiO_2 (FSG), SiCOH (OSG), such as methylsilesquoxane (MSQ), or porous versions of all these materials. The third insulative layer 38 may be formed using CVD, PECVD, spin-on deposition, or other similar deposition techniques, and may consist of multiple layers, such as SiN, SiC, FSG, etc. The third insulative layer 38 may be formed having a thickness approximately equal to the final via height, e.g., 0.1 to 1.0 micron.

Alternating layers of organic dielectric material 40a-40f and inorganic dielectric material 42a-42f are deposited on the surface 40 of the third insulative layer 38, as shown in Fig. 12, to form a second wiring level 50. The alternating layers are similar to those formed in the first metal wiring level 20 (that is, organic dielectric material, inorganic dielectric material, organic dielectric material, inorganic dielectric material, etc.), and are formed in a similar manner.

After the second wiring level 50 is formed, a first dual damascene feature 44 is formed within the alternating layers of inorganic dielectric material 40a-40f, organic dielectric material 42a-42f, and the third insulative layer 38. As illustrated in Fig. 13, the first dual damascene feature 44 is a via trench. The via trench 44 is formed down to the first metal wiring level 20 using conventional patterning and etching techniques.

As illustrated in Fig. 14, a second dual damascene feature 46 and a second trench 48 are formed within the alternating layers of organic dielectric material 40a-40f and inorganic dielectric material 42a-42f. The second dual damascene feature 46 is also a wire trench formed, using conventional patterning and etching techniques, down to the surface of the third insulative layer 38. Alternatively, a trench first-via second process, as known in the art, may be employed. Likewise, a multi-layer hardmask may be used, in which the first damascene feature is patterned and etched into the upper hardmask, as known in the art.

After the first and second dual damascene features 44, 46, 48 are formed, a selective etch is performed to remove at least portions of the organic dielectric material 40a-40f within the second wiring level 50. As described above, where the organic dielectric material comprises p-SILK™ and the inorganic dielectric material comprises p-OSG, an N_2 plasma, H_2 plasma, or other similar plasma etch may be used to selectively remove the organic dielectric material. The N_2 or H_2 etch may be operated in a pressure range of about 3-200 mT at typical parallel plate or high density plasma power and flow conditions.

As illustrated in Fig. 15, openings or air gaps 52 are formed within the second wiring level 50 following the selective etch. It should be noted that no air gaps 52 are formed in the third insulative layer 38 of the present example to add mechanical strength and stability to the overall device. A conformal liner 53 is then formed on the surface of the second metal wiring level 50 sealing the second metal wiring level 50 to prevent metal, deposited in the next step, from leaking into the air gaps 52.

A conductive material 54 is deposited over the surface of the second wiring level 50 filling the via trench 44 and trenches 46, 48 (Fig. 16). The conductive material 54 may comprise copper lined with a thin refractory metal liner, e.g., tantalum, or other similarly used material. The surface of the second wiring level 50 is polished, using conventional techniques, to remove the excess conductive material 54, leaving the conductive material 54 within the via trench 44 and wire trenches 46, 48 to form a conductive dual damascene feature 60 and a conductive single damascene feature 62 (Fig. 17).

Formation of air gaps within the metal wiring levels of the present invention provides a decreased overall capacitance of the device. This is particularly helpful as devices become smaller and smaller, and the distance between device features continues to decrease.

Claims

1. A method of forming a semiconductor device, comprising the steps of:

depositing alternating layers of a first and a second dielectric material, wherein the first and second dielectric materials are selectively etchable at different rates;

forming a first feature within the alternating layers of dielectric material; and

selectively etching the alternating layers of dielectric material to remove at least a portion, but not all, of the first dielectric material in each layer having the first dielectric material and leaving the second dielectric material as essentially unetched.

2. The method of claim 1, wherein the first dielectric material comprises a material that etches selectively to the second dielectric material.

3. The method of claim 1, wherein the first dielectric material comprises an organic dielectric material and the second dielectric material comprises an inorganic dielectric material.

4. The method of claim 1, wherein the first dielectric material comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK^{TM}), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK^{TM}), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second dielectric material comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

5. The method of claim 1, wherein the first feature comprises a single damascene feature or a dual damascene feature.

6. The method of claim 5, wherein the portion of the first dielectric material is removed from a wire trench portion of the dual damascene feature and not removed from a via trench portion of the dual damascene feature.

7. The method of claim 1, following the step of selectively etching the alternating layers of dielectric material further comprising:

depositing a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers.

8. The method of claim 7, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

9. The method of claim 7, following the step of depositing a conformal liner further comprising:

depositing a layer of conductive material over a surface of the device filling the first feature; and

polishing the surface of the device to remove excess conductive material on the surface of the device, leaving the conductive material within the first feature.

10. A method of forming a semiconductor device, comprising the steps of:

depositing alternating layers of a first and a second insulative material;

forming a first feature within the alternating layers of the first and the second insulative materials; and

forming openings within the layers of the first insulative material.

11. The method of claim 10, wherein the first insulative material comprises a material that etches selectively to the second insulative material.

12. The method of claim 10, wherein the first insulative material comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK™), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK™), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second insulative material comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

13. The method of claim 10, wherein the first feature comprises a single damascene feature or a dual damascene feature.

14. The method of claim 13, wherein the first insulative material is removed from a wire trench portion of the dual damascene feature and not a via trench portion.

15. The method of claim 10, following the step of forming openings within the layers of first insulative material further comprising:

depositing a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

16. A semiconductor device, comprising:

a metal wiring level having alternating layers of a first dielectric material and a second dielectric material and having a first feature formed within the alternating layers of first and second dielectric material; and

a plurality of openings within the first dielectric material.

17. The semiconductor device of claim 16, wherein the first dielectric material comprises a material that etches selectively to the second dielectric material.

18. The semiconductor device of claim 16, wherein the first dielectric material comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK™), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK™), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second dielectric material comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

19. The semiconductor device of claim 18, wherein the first dielectric material is removed from a wire trench portion of the dual damascene feature and not a via trench portion.

20. The semiconductor device of claim 16, further comprising:

a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

21. The semiconductor device of claim 16, further comprising:

a conductive material within the first feature.

22. The semiconductor device of claim 16, further comprising:

a second metal wiring level, having alternating layers of a first dielectric material and a second dielectric material, formed on the metal wiring level having openings within the first dielectric material of the second metal wiring level;

a second feature formed within the alternating layers of first and second dielectric material of the second metal wiring level; and

a plurality of openings within the first dielectric material of the second wiring level.

23. A semiconductor device, comprising:

a plurality of alternating first and second insulative layers, wherein the first and second insulative layers have different etch rates;

a first feature formed within the first and second insulative layers;

a plurality of openings within the plurality of first insulative layers formed during a selective etch.

24. The semiconductor device of claim 23, wherein the first insulative layer comprises a material that etches selectively to the second insulative layer.

25. The semiconductor device of claim 23, wherein the first insulative layer comprises an organic dielectric material and the second insulative layer comprises an inorganic dielectric material.

26. The semiconductor device of claim 23, wherein the first insulative layer comprises an organic dielectric material selected from the group consisting of: polyarylene ether (SILK^{TM}), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILK^{TM}), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second insulative layer comprises an inorganic dielectric material selected from the group consisting of: OSG, SiO_2, FSG, MSQ, porous OSG, porous SiO_2, porous FSG, and porous MSQ.

27. The semiconductor device of claim 23, wherein the first feature comprises a single damascene feature or a dual damascene feature.

28. The semiconductor device of claim 27, wherein the openings are within a wire trench portion of the dual damascene feature and not a via trench portion.

29. The semiconductor device of claim 23, further comprising:

a conformal liner over a surface of the alternating layers of dielectric material to seal the alternating layers, wherein the conformal liner comprises a material selected from the group consisting of: SiCOH, SiO_2, SiN, SiC, and SiCN.

30. The semiconductor device of claim 23, further comprising:

a conductive material within the first feature.

FIG. 1

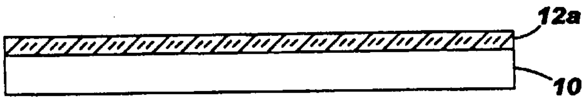


FIG. 2

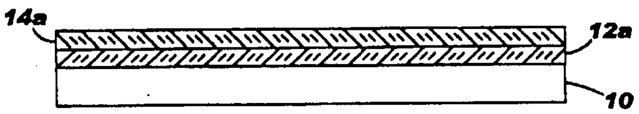


FIG. 3

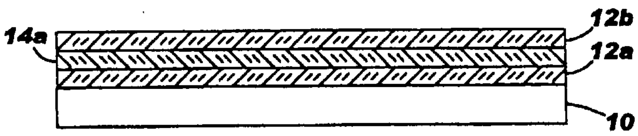


FIG. 4

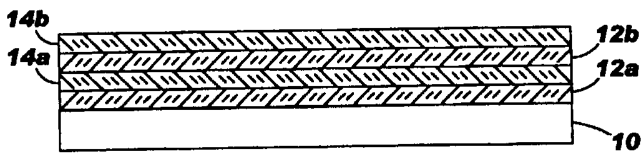

14b
14a
12b
12a
10

FIG. 5

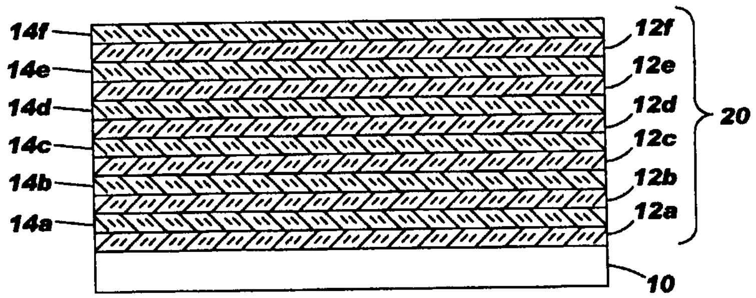

14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
10

FIG. 6

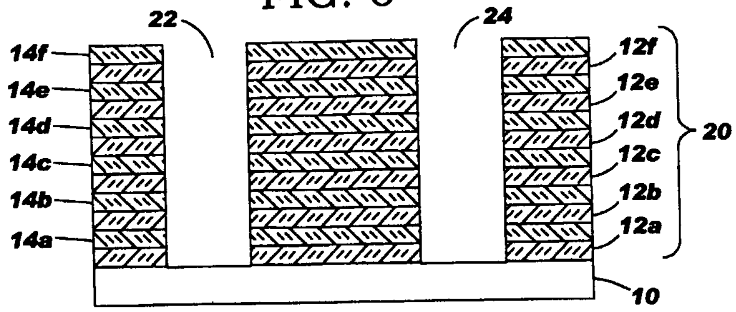


FIG. 7

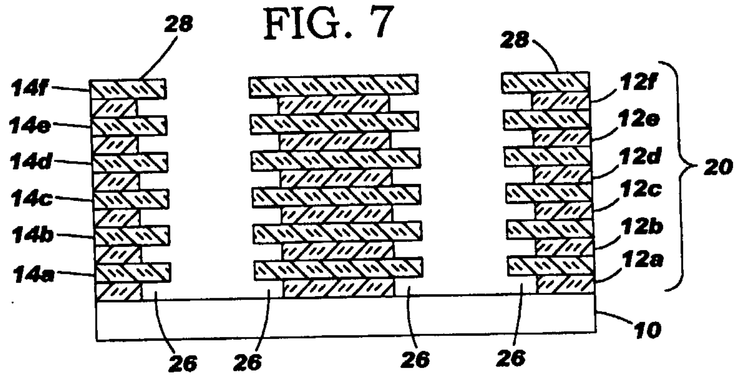


FIG. 8

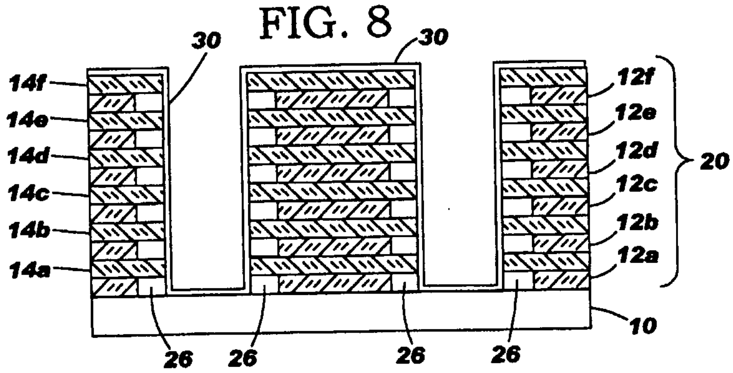


FIG. 9

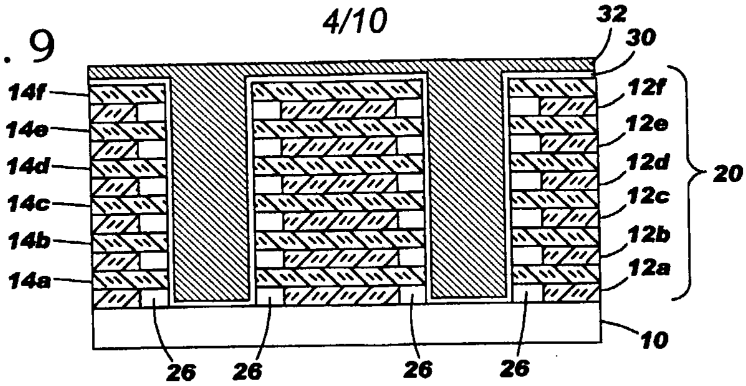


FIG. 10

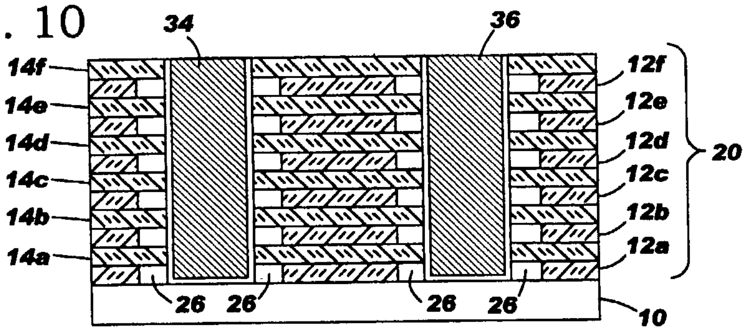


FIG. 11

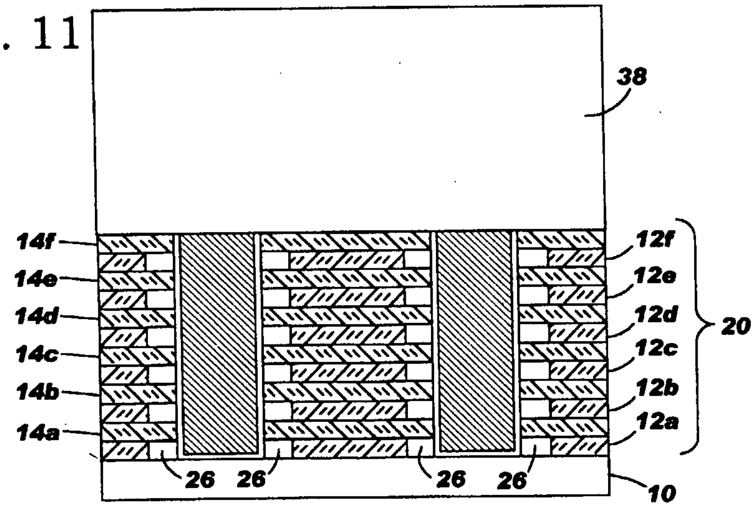


FIG. 12

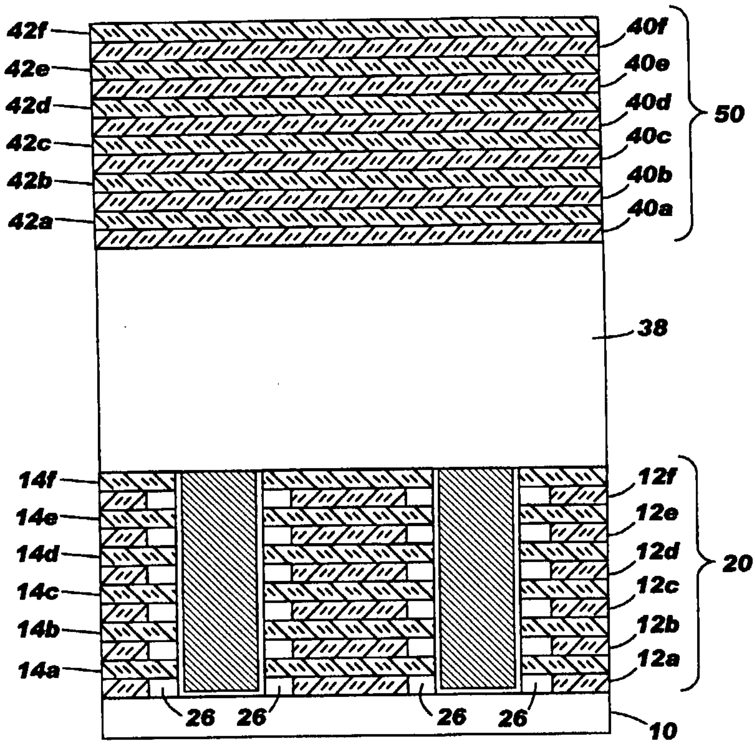

42f
42e
42d
42c
42b
42a
40f
40e
40d
40c
40b
40a
50
38
14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
26
26
26
26
10

FIG. 13

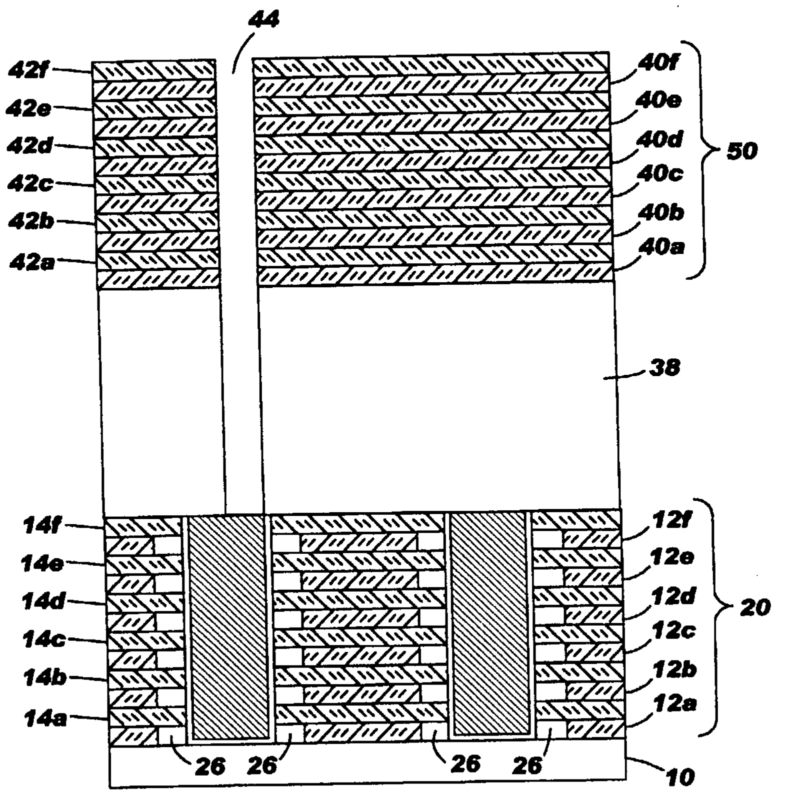

44
42f
42e
42d
42c
42b
42a
40f
40e
40d
40c
40b
40a
50
38
14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
26
26
26
26
10

FIG. 14

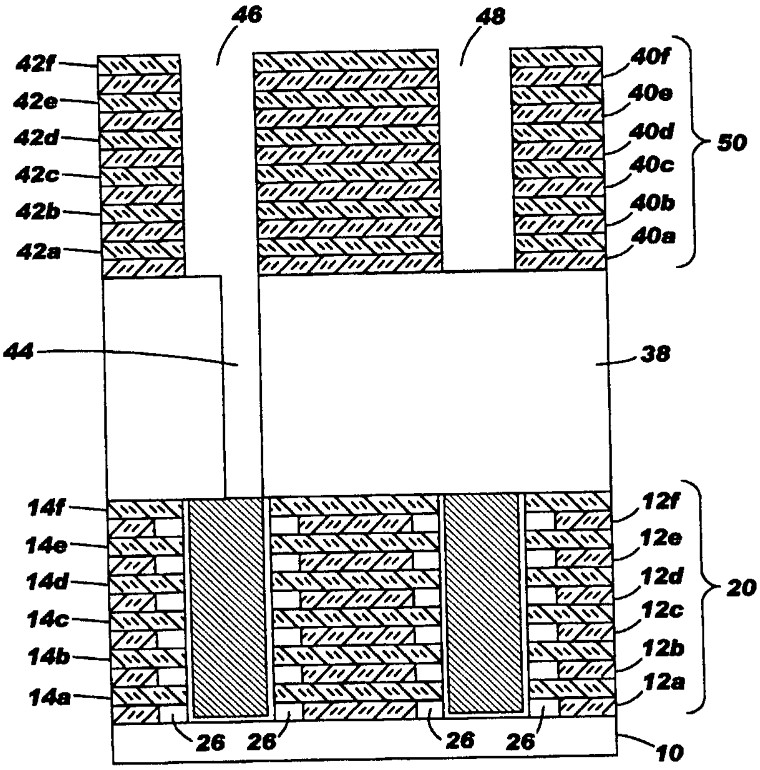

46
48
42f
42e
42d
42c
42b
42a
40f
40e
40d
40c
40b
40a
50
44
38
14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
26
26
26
26
10

FIG. 15

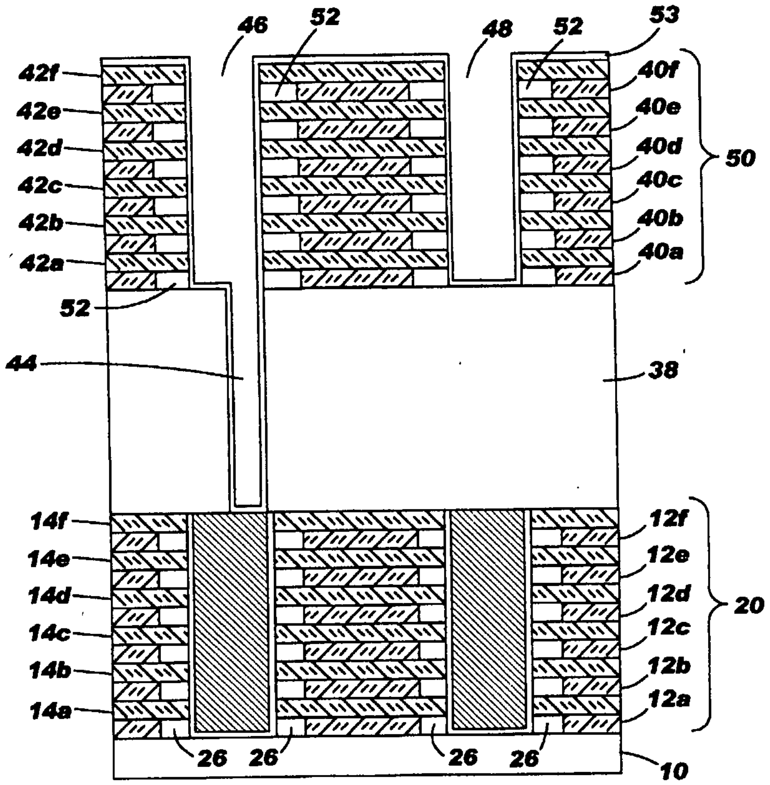

46
52
48
52
53
42f
42e
42d
42c
42b
42a
52
40f
40e
40d
40c
40b
40a
50
44
38
14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
26
26
26
26
10

FIG. 16

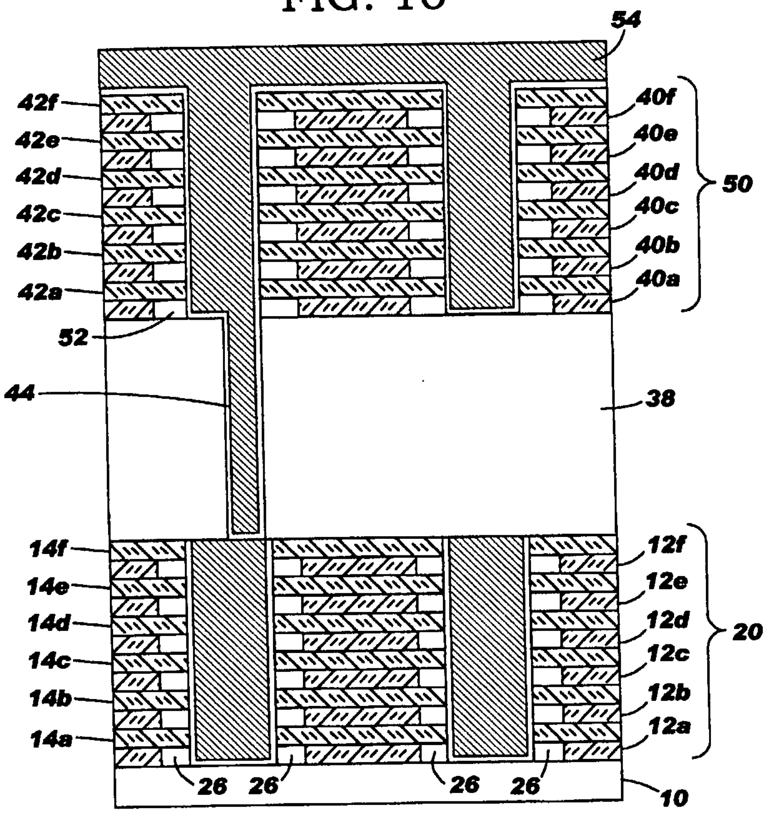
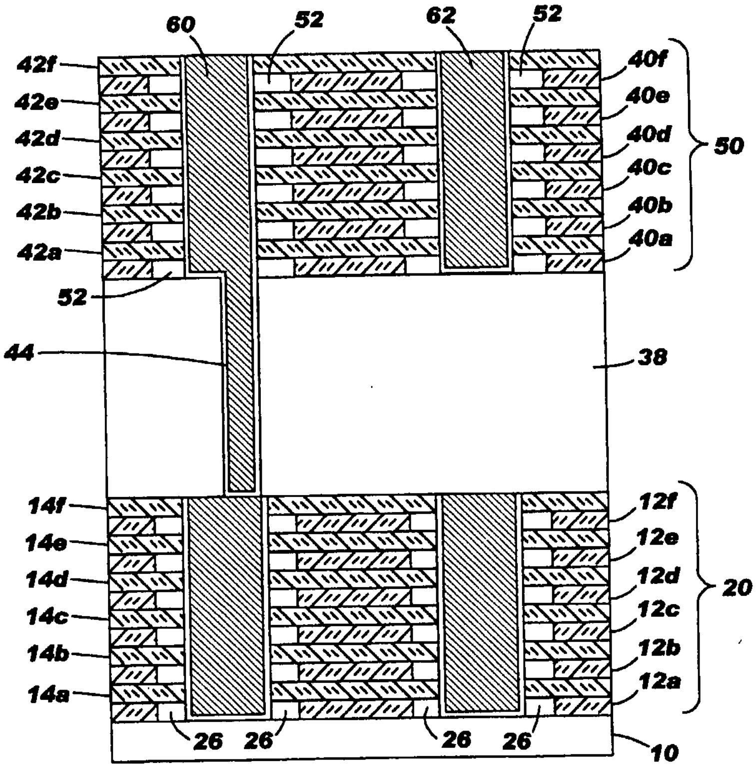

54
42f
42e
42d
42c
42b
42a
52
44
40f
40e
40d
40c
40b
40a
50
38
14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
26
26
26
26
10

FIG. 17


60
52
62
52
42f
42e
42d
42c
42b
42a
52
44
40f
40e
40d
40c
40b
40a
50
38
14f
14e
14d
14c
14b
14a
12f
12e
12d
12c
12b
12a
20
26
26
26
26
10