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(54) Title: SPATIAL LIGHT MODULATOR WITH CHARGE-PUMP PIXEL CELL

(57) Abstract: A voltage storage cell circuit includes an access transistor and a storage capacitor, wherein the source of said access transistor is connected to a bitline, the gate of said access transistor is connected to a wordline, and wherein the drain of said access transistor is connected to a first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal. This arrangement allows for a novel pixel circuit design with area requirements comparable to that of a 1T1C DRAM-like pixel cell, but with the advantage of an output voltage swing of the full range allowed by the breakdown voltage of the pass transistor. A spatial light modulator such as a micromirror array can comprise such a voltage storage cell.



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SPATIAL LIGHT MODULATOR WITH CHARGE-PUMP PIXEL CELL

TECHNICAL FIELD OF THE INVENTION

[0001] This invention relates generally to spatial light modulators used for display systems, and more particularly, to methods and apparatus for applying drive voltages to the pixels of such display systems.

BACKGROUND OF THE INVENTION

[0002] The well-known cathode ray tube (CRT) is widely used for television (TV) and computer displays. Other display technologies such as the transmissive liquid crystal display (LCD) panel are widely used in certain specialized applications such as displays for portable computers and video projectors.

[0003] Market demand is continuously increasing for video displays with higher resolution, greater brightness, lower power, lighter weight, and more compact size. But, as these requirements become more and more stringent, the limitations of conventional CRTs and LCDs become apparent. Microdisplays the size of a silicon chip offer advantages over conventional technologies in resolution, brightness, power, and size. Such microdisplays are often referred to as spatial light modulators (SLMs) since, in many applications, (for example, video projection) they do not generate light directly but instead produce an image by modulating an incident light source. In projection applications, an SLM modulates a bright light source such as an arc lamp, forming a projected image on a screen. In other applications such as ultraportable or head-mounted displays, an image on the surface of the SLM may in fact be viewed by the user directly or through magnification optics.

[0004] CRTs currently dominate the market for desktop monitors and consumer TVs. But large CRTs are very bulky and expensive. LCD panels are much lighter and thinner than CRTs, but are prohibitively expensive to manufacture in sizes competitive with large CRTs. SLM microdisplays enable cost-effective and compact projection displays, reducing the bulk and cost of large computer monitors and TVs.

[0005] Transmissive LCD microdisplays are currently the technology of choice for video projection systems. But, one disadvantage of LCDs is that they require a source of polarized light. LCDs are therefore optically inefficient. Without expensive

polarization conversion optics, LCDs are limited to less than 50%-efficient use of an unpolarized light source. Unlike LCDs, micromirror-based SLM displays can use unpolarized light. Using unpolarized light allows projection displays using micromirror SLMs to achieve greater brightness than LCD-based projectors with the same light source, or equivalent brightness with a smaller, lower-power, cheaper light source.

[0006] The general operation and architecture of SLMs and SLM-based displays is well known in the industry as shown, for example, in U.S. Pat. No. 6,046,840, U.S. Pat. No. 5,835,256, U.S. Pat. No. 5,311,360, U.S. Pat. No. 4,566,935, and U.S. Pat. No. 4,367,924, the disclosures of which are each incorporated herein by reference.

[0007] Figure 1 shows the optical design of a typical micromirror SLM-based projection display system. A light source 20 and associated optical system, comprising optical elements 2a, 2b, and 2c, focus a light beam 6 onto the SLM 4. The pixels of the SLM are individually controllable and an image is formed by modulating the incident light beam 6 as desired at each pixel. Micromirror-based projection displays typically modulate the direction of the incident light. For example, to produce a bright pixel in the projected image, the state of the SLM pixel may be set such that the light from that pixel is directed into the projection lens 8. To produce a dark pixel in the projected image, the state of the SLM pixel is set such that the light is directed away from the projection lens 8. Other technologies, such as reflective and transmissive LCDs, use other modulation techniques such as techniques in which the polarization or intensity of the light is modulated.

[0008] Modulated light from each SLM pixel passes through a projection lens 8 and is projected on a viewing screen 10, which shows an image composed of bright and dark pixels corresponding to the image data loaded into the SLM 4.

[0009] A "field-sequential color" (FSC) color display may be generated by temporally interleaving separate images in different colors, typically the additive primaries red, green, and blue, though often a white image is added to boost the brightness of the image. This may be accomplished as described in the prior art using a color filter wheel 12 as shown in Figure 1. As color wheel 12 rotates rapidly, the color of the projected image cycles rapidly between the desired colors. The image on the SLM is synchronized to the wheel such that the different color fields of the full-color

image are displayed in sequence. When the color of the light source is varied rapidly enough, the human eye perceives the sequential color fields as a single full-color image. Grayscale in the image can be achieved by pulse width modulation, such as set forth in WO 01/84531 to Richards, incorporated herein by reference.

[0010] Other illumination methods may be used to produce a field-sequential color display. For example, in an ultraportable display, colored LEDs could be used for the light source. Instead of using a color wheel, the LEDs may simply be switched on and off as desired.

[0011] An additional color technique is to use more than one SLM, typically one per color, and combine their images optically. This solution is bulkier and more expensive than a single-SLM solution, but allows the highest brightness levels for digital cinema and high-end video projection.

[0012] In a CRT or conventional LCD panel the brightness of any pixel is an analog value, continuously variable between light and dark. In fast SLMs, for example those based on micromirrors, other MEMS structures, or some types of LCDs, one can operate the pixels in a digital manner. That is, pixels of these devices are driven to one of two states: fully on (bright) or fully off (dark).

[0013] To produce the perception of a grayscale or full-color image using such a digital SLM, it is necessary to rapidly modulate the pixels of the display between on and off states such that the average of each pixel's modulated brightness waveform corresponds to the desired 'analog' brightness for that pixel. This technique is generally referred to as pulse-width modulation (PWM). Above a certain modulation frequency, the human eye and brain integrate a pixel's rapidly varying brightness (and color, in a field-sequential color display) and perceive an effective 'analog' brightness (and color) determined by the pixel's average illumination over a video frame.

[0014] It is generally advantageous to drive the pixels of a digital SLM with as large a voltage as possible. For example, in a MEMS based microdisplay such as those disclosed in US patents 5,835,256 and 6,046,840 (both to Huibers and incorporated herein by reference) a large actuation voltage increases the available electrostatic force available to move the micromechanical pixel elements. Greater electrostatic forces provide more operating margin for the micromechanical elements—increasing yield—and actuate them more reliably and robustly over variations in processing and environment. Greater electrostatic forces also allow the hinges of the MEMS structures

to be made correspondingly stiffer; stiffer hinges may be advantageous since the material films used to fabricate them may be made thicker and therefore less sensitive to process variability, improving yield. A further benefit of larger electrostatic forces and stiffer micromechanical hinges is that more force is available to overcome the stiction force that is present between contacting MEMS structures. The pixel switching speed may also be improved by raising the drive voltage to the pixel, allowing higher frame rates, or greater color bit depth to be achieved.

[0015] Higher actuation voltages may be of benefit for other SLM types, as well. For example, many LCD materials can be made to switch states faster with a larger drive voltage, allowing greater frame rates and/or color bit depth.

[0016] Designing high-voltage circuitry to individually control the pixels of an SLM is challenging. Due to fundamental principles of semiconductor physics, transistors that tolerate higher voltages must be physically larger than those that tolerate lower voltage. Larger, HV-tolerant transistors may unacceptably reduce the cell area available for other critical cell components (such as the capacitor in a DRAM-type cell) or not fit in the cell at all. On the other hand, it is desirable for cost reasons to minimize the physical size of the microdisplay pixel. Thus it is highly desirable to improve the maximum drive voltage of an SLM pixel circuit while maintaining small pixel size.

[0017] The 1-transistor, 1-capacitor (1T1C) DRAM charge-storage cell illustrated in Fig. 2 is a well-known circuit for storing a data voltage in many applications. The 1T1C circuit is widely applied to ordinary data storage in commercial DRAMs and other integrated-circuit applications. This 1T1C circuit structure is also used in display applications—TFT active-matrix LCD panels work on the same principle, and the idea has also been applied to microdisplays as described in US Pat. 5,671,083.

[0018] A well-known drawback of the 1T1C DRAM circuit is the nonideal performance of the pass transistor. Ideally the transistor would act as a perfect switch; the voltage on the bitline 101 would be passed through without change to the storage node 102 when the wordline 100 is activated. A real NMOS pass transistor can pull the stored cell voltage 102 down all the way to the minimum bitline 101 voltage V_{bmin} . However the highest voltage that can be driven on the cell storage node 102 is limited by the threshold voltage of the pass transistor 104. The transistor can only pull the

voltage V_c on cell storage node 102 up to no higher than $V_g - V_t$, where V_g is the wordline 'on' voltage applied to the gate of the pass transistor, and V_t is the transistor's threshold voltage. To maximize V_c , V_g would typically be driven to V_{dd} , the maximum supply voltage allowed by the breakdown limits of the IC process in which the circuit is fabricated. In this case the resulting cell voltage will be $V_{dd} - V_t$, whereas the bitline voltage is driven to V_{dd} . So the transistors of the cell are themselves capable of tolerating $V_c = V_{dd}$, but the maximum actual V_c is limited to only $V_{dd} - V_t$ due to the inherent properties of the 1T1C cell circuit.

[0019] Compounding the problem is the well-known MOSFET 'body effect.' This causes the effective V_t of the pass transistor to become even larger as the transistor's source node (the storage node 102) rises in voltage, as is the case when the cell is charged to $V_{dd} - V_t$. This reduces the maximum available output V_c still further.

[0020] One of ordinary skill in the art of circuit design will appreciate that the above discussion applies equally well to a PMOS transistor, which will suffer similar voltage degradation when pulling the stored voltage down.

[0021] Clearly, a circuit that could store the full supply voltage of V_{dd} on V_c would be more desirable. Many candidate circuit designs are impractical in a microdisplay due to the small pixel cell size. For example, a 2-transistor (PMOS+NMOS) pass gate could be used to get the full supply voltage swing on the storage node. However, the large design rules required for adequate spacing between PMOS and NMOS devices and their associated wells are impractical for small pixel sizes. Alternatively, an SRAM pixel cell could be used, but this cell requires 6 transistors that also would likely not fit in the available pixel area. Alternatively a PMOS transistor or diode could be added to the cell to 'precharge' the pixel cell high before writing it to a low value, but high-voltage PMOS devices or diodes also occupy an unacceptably large amount of area for small microdisplay pixels due to their associated well implants. A further alternative would be to increase the gate voltage to the wordline by V_t over the maximum cell voltage. However, this would require even higher-voltage transistors than the high-voltage transistor in the cell. Fabricating two types of high voltage (HV) transistors would increase cost and the cell would still not be able to use the highest-voltage transistors available.

SUMMARY OF THE INVENTION

[0022] The present invention describes a novel pixel circuit design with area requirements comparable to that of a 1T1C DRAM-like pixel cell, but with the advantage of an output voltage swing of the full range allowed by the breakdown voltage of the pass transistor.

[0023] According to one aspect of the present invention, the second plate of the cell's storage capacitor is connected to a 'pump' signal which allows the stored cell voltage to be boosted during the cell write cycle.

[0024] According to a further aspect of the present invention, the cell's bitlines and wordlines are controlled during the write cycle to avoid forward-biasing the access transistor's drain junction while the cell voltage is boosted during the write cycle.

[0025] According to a further aspect of the present invention, the pass transistor type (NMOS vs. PMOS) and the voltage levels of the wordline, bitline, and 'pump' signal are selected to minimize leakage, light sensitivity, and other undesirable parasitic effects of using high voltages.

[0026] According to a further aspect of the present invention, a high voltage may be obtained on the pixel electrode while using only low voltages on the pixel array's bitlines and wordlines; high voltage drivers are only required on the 'pump' signal for each row of the array.

[0027] According to a further aspect of the present invention, an asymmetrical (low-voltage source and gate) high-voltage MOS transistor may be used in the cell, reducing the cell area required by the cell's transistor.

[0028] According to a further aspect of the present invention, standard logic voltage levels of 5 volts or less (e.g. 3.3 or 5 volts) may be used on the bitline and wordline of a pixel cell, but by providing a pump signal, a total pixel voltage swing of at least 5 volts may be obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] FIG. 1 illustrates a typical SLM-based projection display system;

[0030] FIG. 2 illustrates a 1T1C DRAM circuit as is well-known in the prior art;

[0031] FIG. 3 illustrates a pixel circuit diagram according to an embodiment of the invention;

[0032] FIG. 4 is a simplified cross-sectional view of a pass transistor and capacitor of the pixel circuit of FIG. 3; and

[0033] FIG. 5 is a diagram showing exemplary voltage waveforms applied to the pixel circuit of FIG. 3.

DESCRIPTION OF THE EMBODIMENTS

[0034] Fig. 2 is an illustration of a prior art DRAM cell circuit, whereas Fig. 3 is an illustration of a cell circuit of the present invention. As can be seen in both figures, each pixel contains a pass transistor 104 and a storage capacitor 103, as well as a wordline signal 100 for enabling access to a row of cells and a bitline signal 101 for reading and writing data to a column of cells. The cell's state is stored as a high or low voltage on the storage node 102. In a conventional DRAM illustrated in Fig. 2, first plate 103a of the storage capacitor is connected to the drain of the pass transistor. And the second plate node of the storage capacitor 103 is connected to a fixed supply voltage such as Vdd, Ground, or some intermediate supply voltage such as Vdd/2 as is shown in Fig. 2. In the present invention illustrated in Fig. 3, the second capacitor plates of pixels in each row are connected to a 'pump' signal 105.

[0035] A simplified cross section of the circuit as implemented in a typical 2-poly CMOS process is shown in Fig. 4. Of course, the following is exemplary only and many other designs are possible. Metal interconnect and contacts to the source/drain diffusions and polysilicon gates are not shown for clarity. The methods for fabricating this structure are readily commercially available and well-known. The circuit is fabricated on a p-type silicon substrate 200. Gate oxide 204 and field oxide 202 are then formed, and N⁺ (heavy doping) diffusions 201a, 201b are created to form the source and drain of the pass transistor 104. The diffusions 201a, 201b may be simple diffusions or any other source-drain structure well-known to those skilled in the art. For example, double-diffused-drain ("DDD") or lightly-doped drain ("LDD") type diffusions may be advantageous for high-voltage operation. Polysilicon is then deposited and patterned to form the transistor gate 203 on top of the thin gate oxide 204, and the bottom plate 208 of the storage capacitor 103. Subsequently the capacitor dielectric 206 is deposited and then the top polysilicon plate 207 is deposited and

patterned. Alternatively the bottom plate 208 may be formed first, and the gate 203 and top plate 207 may subsequently be deposited and patterned.

[0036] Using metal interconnect and vias (not shown), the polysilicon gate 203 is connected to the wordline signal 100. The source diffusion 201a is connected to the bitline signal 101. The drain diffusion 201b is preferably connected to the top plate of the capacitor 207 and the 'pump' signal 105 is connected to the other plate of the capacitor 208. Alternatively the drain diffusion 201b may be connected to the bottom capacitor plate 208 and the pump signal 105 to the top plate 207. The connection of the transistor drain 201b and capacitor plate 207 forms the cell's charge-storage node 102.

[0037] In typical 2-poly processes, design rules often do not allow the top poly 207 to overlap the edge of the bottom poly 208, often for step-coverage reasons. Since the 'pump' signal 105 is common to a row of pixels, it is preferable to connect the pump signal to the bottom poly and connect the pump signal 105 of neighboring cells by abutting the bottom poly 208. The pump signal 105 could be connected to the top poly 207, but in this case since top poly cannot cross over the bottom-poly 208 boundaries between neighboring cells, the available capacitor area would be reduced by gap required between the poly layers of neighboring cells. For this reason it is preferable to connect the pump signal to the bottom plate 208.

[0038] By driving the 'pump' signal 105 in conjunction with the bitline 101 and wordline 100 as described in this invention, it is possible to store a voltage range larger than $V_{dd} - V_t$ on the storage node 102.

[0039] According to one embodiment of the invention, the pass transistor 104 is an NMOS transistor. Bitline 101 and wordline 100 take on logic levels of logic '0' = 0V and logic '1' = V_1 , where $V_1 > 0$. Pump signal 105 takes on logic levels of logic '0' = V_{PL} and logic '1' = V_{PH} , where $V_{PH} > V_{PL}$.

[0040] The voltage waveforms applied to the pixel are illustrated in Fig. 5. In the cell's 'hold' state 301, the cell stores a value as a high or low voltage on the storage node 102. The cell's control signals (collectively the wordline, bitline, and pump signal) are set as follows in the 'hold' state. The wordline 100 is held low, turning off the pass transistor 104. The pump signal 105 is held in a high state. The bitline 101 may be in either a high or low state; the bitline state does not matter since the pass transistor 104 is off. In this state the bitlines and other rows' wordlines and pump

signals may be driven as necessary to access other rows of cells while the illustrated row remains stable in its 'hold' state.

[0041] In order to prepare the cell to be written, the 'pump' signal voltage must be brought low. However, if the voltage on the storage node 102 is already low, care must be taken so that the storage node voltage 102 is not driven below the potential of the substrate 200 (usually GND) when the pump signal 105 falls. For example, suppose the stored voltage V_q on the storage node 102 is 0 and the wordline is maintained in the low state while the pump signal 105 is driven low. Since the pass transistor is off, coupling through the capacitor will drive the storage node 102 voltage down as the pump signal 105 falls—until the storage node 102 goes a diode-drop below ground, forward-biasing the PN junction between the device's drain 201b and the substrate 200. This is highly undesirable as it would inject minority carrier current into the substrate, likely causing problems with latchup, noise, and/or leakage in nearby circuits.

[0042] One approach to mitigating the substrate-current problem is to set the bitline 101 low and the wordline 101 high while the pump signal 105 is brought low, effectively connecting the storage node to ground through the turned-on 'switch' formed by the pass transistor. If the pass transistor 104 acted as an ideal switch this would then prevent the storage node 102 from being driven below ground. However, the finite on-resistance of the pass transistor, bitline, and bitline driver will still allow some excursion below GND as the pump signal falls. While the pass transistor drain junction may not be fully forward-biased in this case, the situation is still marginal and a more robust solution is desirable.

[0043] A preferred solution to the substrate-current problem is to drive the bitline and wordline high before the pump signal is brought low. This limits the minimum voltage excursion on the storage node 102 to be $V_{dd}-V_t$, well above ground and positively safe from any undesired substrate-injection effects. Thus, in preparation for a write cycle to the pixel cell, it is preferable that the bitline, wordline and pump signal are first set to a 'pre-discharge' state 302 in which the bitline, wordline, and pump signal are all high. If the pixel originally was storing a low voltage, its voltage is pulled up to $V_{dd}-V_t$. If the pixel was originally storing a high voltage, the stored voltage is unaffected.

[0044] Subsequently, in the 'discharge' state 303, the pump signal is set low. If the pixel originally stored a high voltage, the stored voltage is brought down to $V_{dd}-V_t$. If the pixel originally stored a low voltage, the stored voltage is clamped to $V_{dd}-V_t$ as the pump signal falls.

[0045] Due to second-order effects such as leakage and capacitive charge-sharing, the final voltage after the 'discharge' state may depend slightly on the original pixel state. To guarantee that the previous pixel state is fully cleared, the control signals may optionally be set to the 'clear' state 304 in which the bitline is set low, the wordline is high, and the pump signal is low, thereby forcing the stored voltage to zero volts.

[0046] After the 'discharge' state 303 and the optional 'clear' state 304, the cell is ready to be written with a new stored value. The control signals are set to the 'write' state 305 in which the bitline of the pixel is set high or low depending on the desired final pixel value, the wordline is high, and the pump signal is low. The stored pixel voltage will go to 0 or $V_{dd}-V_t$ depending on whether the bitline is low or high. Subsequently, the control signals are set to the 'charge' state 306 in which the pump signal is set high, and the bitline and wordlines retain their previous states from the 'write' state. If the bitline is low, the pass transistor will be on and the pixel's stored voltage will be clamped at zero volts as the pump signal rises. However, if the bitline is high, the transistor will be off and the stored voltage will be driven above the bitline and wordline voltage by the rising edge of the pump signal coupling through the storage capacitor.

[0047] Finally, the wordline is brought low, returning the control signals to the 'hold' state 301 and completing the write cycle. The desired high or low voltage has been stored in the cell.

[0048] Ideally, in the 'charge' state, the pumpline's upward step of $V_{ph}-V_{pl}$ volts would result in an upward step on the cell voltage of $V_{ph}-V_{pl}$ volts from the initial value of $V_{dd}-V_t$, for a final voltage of $V_{dd}-V_t+V_{ph}-V_{pl}$. For example, if V_{pl} is 0 and V_{ph} is the maximum rated voltage of the process, then the maximum final pixel voltage is approximately $V_{dd}-V_t+V_{max}$, which would be greater than the maximum allowed voltage. The chosen value for V_{dd} and/or $V_{ph}-V_{pl}$ can be reduced as necessary to keep the maximum cell voltage within acceptable limits while providing substantial margin below the maximum rated supply voltages.

[0049] Nonideal effects such as charge-sharing reduce the size of upward 'step' on the stored pixel voltage during the 'charge' state from $V_{ph}-V_{pl}$ to $K(V_{ph}-V_{pl})$, where K is slightly less than 1. By increasing V_{dd} or $V_{ph}-V_{pl}$ slightly this effect may typically be overcome; in typical cases the required increase is still within the maximum rated supply voltages for V_{ph} and V_{pl} .

[0050] An additional advantage of this invention is that the source node 201a and gate 203 of the pass transistor do not need to support the full output voltage swing. This enables an asymmetrical high-voltage transistor to be used where only the drain is HV-tolerant, resulting in a more compact layout. Also a thinner gate oxide can be used since the wordline voltage is low, improving the drive characteristics of the pass transistor. Additionally, the circuitry that drives the bitlines and wordlines is simplified due to the reduced voltage swing, high-voltage level shifters and drivers are only required on the pump signals. The reduced voltage swing on the bitlines also greatly reduces the power consumption of the device.

[0051] An equivalent circuit could equally well be implemented using a PMOS pass transistor in an n-type substrate or well, with the appropriate change in polarity of voltage levels the control signals as shown in Table 1.

Table 1

| Transistor type | Wordline 'active' | Wordline 'inactive' | Bitline 'active' | Bitline 'inactive' | Pumpline 'active' | Pumpline 'inactive' |
|-----------------|-------------------|---------------------|------------------|--------------------|-------------------|---------------------|
| NMOS | high | Low | High | Low | high | low |
| PMOS | low | High | Low | High | low | high |

[0052] A potential problem with this circuit exists due to the 'field threshold' of the bottom capacitor plate over the field oxide and substrate. When large voltages are applied to this bottom plate, the surface of the substrate may be inverted, producing an undesired parasitic FET. The minority carriers and depletion region associated with this parasitic FET may interact unfavorably with the cell's pass transistor, and it is desired to avoid this effect.

[0053] A solution to this problem might be (in the case of an NMOS pass transistor in a p-substrate) to offset the levels of the pump signal. For example, $V_{pl}=-10V$ and $V_{ph}=+10V$ could be used equally well instead of $V_{pl}=0V$ and $V_{ph}=+20V$.

However, in the case of a conventional p-substrate, n-well process, the negative voltage of V_{pl} presents practical difficulties, as NMOS device cannot be fabricated to drive the pump signal below ground.

[0054] A preferred alternative is to use a PMOS pass transistor, fabricated in an n-well biased to V_{dd} , where V_{dd} is the maximum positive voltage on the bitline and wordline. In this case we can choose $V_{pl}=0V$ and $V_{ph}=+20V$, driving the pump signal low with an NMOS device fabricated in the substrate and high with a PMOS device fabricated in an electrically separate n-well biased to V_{ph} .

[0055] This design will result in the stored pixel voltage being driven below ground—however this is acceptable as the voltage is only present on the p+ diffusion of the pass transistor within an n-well.

[0056] An advantage of fabricating the pass transistor in a well with a bias voltage between V_{ph} and V_{pl} is that the pump voltage creates less-harmful accumulation in the substrate surface instead of inversion. In the case of a p-substrate process, this would require choosing a PMOS device and an n-well bias below the maximum pump signal voltage V_{ph} . One skilled in the art will appreciate that a similar but complementary circuit provides this advantage if substrate is n-type; then an NMOS device should be used in a p-well with bias voltage above the minimum pump signal voltage.

[0057] A further advantage of fabricating the pass transistors in a well (as opposed to the substrate) is that light-induced leakage current is reduced. While some incident photons from the projection system's light source will create hole-electron pairs in the well, contributing to cell leakage, a significant fraction of the incident photons from the projection system's light source will pass through the well and generate hole-electron pairs in the substrate, creating harmless leakage between the well and substrate.

[0058] An advantage of using a PMOS pass transistor is that, at high bias voltages, it exhibits reduced impact ionization compared to an NMOS transistor, which in an NMOS transistor can result in multiplication of the leakage current and increased leakage compared to a PMOS device.

[0059] A further advantage of this well-biasing scheme is that the maximum absolute value of the voltage across the storage capacitor is reduced, enabling a thinner oxide to be used for greater capacitance and more reliable operation.

[0060] A still further advantage of the circuit of the present invention is that the pass transistor of the circuit can function as an asymmetric high-voltage transistor. Specifically, the absolute value of the drain voltage can be greater than that of the source. Moreover, the absolute value of the difference between the maximum voltage and the minimum voltage of the drain can also be greater than that of the source.

[0061] A still further advantage of the circuit provided by the present invention is that the asymmetric high-voltage pass transistor allows more area for the capacitor. Moreover, the asymmetric high-voltage transistor enables the storage capacitor to maintain a high voltage. For example, the capacitor can maintain a voltage at least 10 volts, 15 volts or 20 volts.

[0062] A further advantage of the circuit provided by the present invention is that a standard logic voltage level of 5 volts or less (e.g. 3.3 or 5 volts) may be used on the bitline and wordline of a pixel cell. However, by providing a pump signal, a total pixel voltage swing of at least 5 volts may be obtained. Voltage swings of 10 volts or more (or even 20 volts or more) can be achieved in the present invention.

[0063] The circuit as discussed above has varieties of applications. For example, the circuit can be used in a spatial light modulator. In this application, the storage node (e.g. 102 in FIG. 3) can be used to control optical states of a pixel in the spatial light modulator, wherein the pixel can be a liquid crystal pixel cell.

[0064] While the invention has been described by way of example and in terms of the specific embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. In particular, the storage capacitor (103 in FIG. 3) can be any type of capacitors, such as a typical MOS-type capacitor (a MOS-type capacitor is a MOS-type transistor with the gate functions as a first plate, and the source and drain connected together for forming a second plate). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

CLAIMS

We claim:

1. A voltage storage cell, comprising:
a transistor having a source, a gate, and a drain;
a storage capacitor having a first plate and a second plate; and
wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.
2. The circuit of claim 1, further comprising a control circuit, the control circuit operable to drive a plurality of control signals comprising the bitline signal, the wordline signal, and the pump signal, wherein each control signal has an active voltage level and an inactive voltage level, according to a predetermined sequence of states.
3. The circuit of claim 2, wherein the sequence of states comprises:
a discharge-state, during which the pump signal is driven to an inactive voltage level; and
a charge-state, during which the pump signal is driven to an active voltage level
4. The circuit of claim 3, wherein during the discharge-state the wordline is driven to an active voltage level.
5. The circuit of claim 4, wherein during the discharge-state the bitline is driven to an active voltage level.
6. The circuit of claim 5, wherein the sequence of states further comprises:
a hold-state, in which the wordline is driven to an inactive voltage level and the pump signal is driven to an active voltage level;
a pre-discharge-state, in which the bitline and wordline are driven to an active voltage level while the pump signal remains at an active voltage level,

a write-state, in which the wordline is held at an active voltage level, and the pump signal is held at an inactive voltage level, and in which the bitline is set to an active or inactive voltage level depending upon a desired final voltage state of the storage node.

7. The circuit of claim 1, wherein the transistor is a PMOS device fabricated in an n-well.
8. The circuit of claim 7, wherein the n-well is fabricated in a p-type substrate.
9. The circuit of claim 8, wherein the n-well is connected to an electric voltage lower than the maximum pump signal voltage.
10. The circuit of claim 8, wherein the storage node may store a voltage lower than the voltage of the p-type substrate
11. The circuit of claim 1, wherein the transistor is an NMOS device fabricated in a p-well.
12. The circuit of claim 11, wherein the p-well is fabricated in an n-type substrate.
13. The circuit of claim 12, wherein the p-well is connected to a voltage higher than the minimum pump signal voltage.
14. The circuit of claim 12, wherein the storage node stores a voltage higher than the voltage of the n-type substrate.
15. The circuit of claim 2, wherein the bitline and wordline have voltage swings lower than the pump signal's voltage swing.
16. The circuit of claim 2, wherein the cell voltage swing is greater than the bitline voltage swing.

17. The circuit of claim 2, wherein the cell voltage swing is greater than the wordline voltage swing.

18. The circuit of claim 1, wherein the transistor is an asymmetrical transistor with a high-voltage tolerant drain and a low-voltage tolerant source and gate.

19. The circuit of claim 1, wherein the second plate of the storage capacitor is formed in a first layer of polysilicon.

20. The circuit of claim 19, wherein the first plate of the storage capacitor is formed in a second layer of polysilicon.

21. The circuit of claim 20, wherein the circuit abuts a second voltage storage cell circuit, the circuits having a shared pump signal, and said shared pump signal formed by abutting the first layer of polysilicon between the cells.

22. The circuit of claim 1, wherein said storage node controls an optical state of a pixel in a spatial light modulator.

23. The circuit of claim 22, wherein the pixel is an electrostatically deflectable micro-mirror.

24. The circuit of claim 22, wherein said pixel is a liquid-crystal pixel cell.

25. A method for making a voltage storage cell circuit, comprising in any order:
providing a silicon substrate;
forming gate oxide and field oxide areas on said substrate;
forming a gate corresponding to a gate of a transistor;
forming first and second plates and a dielectric there between to define a capacitor;
forming diffusion areas of doping type opposite to that of the substrate, said diffusion areas corresponding to a source and a drain of the transistor;
connecting the gate to a word line signal;

connecting the source to a bit line signal;
connecting the drain to the first plate of the capacitor, and
connecting the second plate of the capacitor to a pump signal.

26. A circuit comprising a transistor and a capacitor, wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of said transistor is connected to a first plate of said capacitor, and wherein the second plate of said capacitor is connected to a pump signal.

27. A method for operating a voltage storage cell, wherein the cell comprises a substrate, a MOS- type transistor having a source, a drain and a gate, a capacitor having first and second plates, and wherein the source is connected to a bitline, the gate is connected to a wordline, the drain is connected to the first plate, and the second plate is connected to a pump signal, the method comprising:

setting the wordline to an inactive voltage level and the pump signal to an active voltage level for holding a voltage level stored in the cell;

setting the wordline to an active voltage level and the pump signal to an inactive voltage level for discharging the voltage level stored in the cell; and

setting the voltage level stored in the cell in accordance with the voltage level of the bitline.

28. The method of claim 27, further comprising:

after setting the wordline to an inactive voltage level and the pump signal to an active voltage level for holding a voltage level stored in the cell and before setting the wordline to an active voltage level and the pump signal to an inactive voltage level for discharging the voltage level stored in the cell, setting the wordline to an active voltage level for pre-discharge.

29. The method of claim 27, further comprising:

after setting the wordline to an active voltage level and the pump signal to an inactive voltage level for discharging the voltage level stored in the cell and before setting the voltage level stored in the cell in accordance with the voltage level of the bitline,

setting the bitline to an inactive voltage level such that the voltage level stored in the cell is dropped to an inactive voltage level for clearing the stored voltage level in the cell.

30. The method of claim 27, further comprising:
in setting the voltage level stored in the cell in accordance with the voltage level of the bitline, if the bitline is in an active voltage level,
setting the pump signal to an active voltage level such that the voltage level stored in the cell is boosted up to a high voltage level.
31. The method of claim 27, wherein the voltage storage cell is a part of a spatial light modulator.
32. The method of claim 31, wherein the spatial light modulator is a micro-mirror array having one or more micro-mirrors.
33. A spatial light modulator having at least one pixel cell, comprising
an electrostatically deflectable micro-mirror;
an electrode for electrically controlling a rotation of the micro-mirror; and
a memory cell storing an activation or an inactivation voltage level for applying an voltage to the electrode, the cell further comprising:
a MOS transistor having a source connected to a bitline, a drain and a gate connected to a wordline, and
a capacitor having a first and second plates wherein the first plate is connected to the drain of the transistor and the second plate is connected to a pump signal.
34. The spatial light modulator of claim 33, wherein the memory cell is capable of maintaining:
a holding state for holding the voltage level stored in the cell;
a discharging state for setting the stored voltage in the cell to an inactive voltage level; and
a writing state for setting the voltage level stored in the cell in accordance with a voltage level of the bitline.

35. The spatial light modulator of claim 34, wherein the memory cell is capable of maintaining:

a pre-discharging state for preparing for setting the stored voltage in the cell to an inactive voltage level

36. The spatial light modulator of claim 34, wherein the memory cell is capable of maintaining:

a clearing state for setting the stored voltage level to a low voltage level.

37. The spatial light modulator of claim 34, wherein the holding state is defined as that;

the wordline has an inactive voltage level; and
the pump signal has an active voltage level.

38. The spatial light modulator of claim 34, wherein the discharging state is defined as that:

the bitline has an active voltage level;
the wordline has an active voltage level; and
the pump signal has an inactive voltage level.

39. The spatial light modulator of claim 34, wherein the writing state is defined as that;

the wordline has an active voltage level; and
the pump signal has an inactive voltage level.

40. The spatial light modulator of claim 35, wherein the pre-discharging state is defined as that:

the bitline has an active voltage level;
the wordline has an active voltage level; and
the pump signal has an active voltage level.

41. The spatial light modulator of claim 36, wherein the clearing state is defined as that:

the bitline has an inactive voltage level;
the wordline has an inactive voltage level; and
the pump signal has an inactive voltage level.

42. The spatial light modulator of claim 33, wherein the transistor is a PMOS transistor fabricated within a n-type well that is formed in a p-type substrate.

43. The spatial light modulator of claim 33, wherein the transistor is a NMOS transistor fabricated within a p-type well that is formed in an n-type substrate.

44. The spatial light modulator of claim 42, wherein the substrate is a silicon substrate.

45. The spatial light modulator of claim 43, wherein the substrate is a silicon substrate.

46. A spatial light modulator having at least one pixel cell, said pixel cell comprising:

an electrostatically deflectable micro-mirror; and
a memory cell operable to store an actuation voltage, wherein the voltage stored in said memory cell determines an rotational angle of deflection of said micro-mirror, and wherein said memory cell comprises a PMOS transistor, said PMOS transistor being fabricated within an n-type well formed in a p-type substrate.

47. A spatial light modulator having at least one pixel cell, said pixel cell comprising

an electrostatically deflectable micromirror;
a memory cell operable to store an actuation voltage; and
wherein the voltage stored in said memory cell determines the angle of deflection of said micromirror, and wherein said memory cell includes an NMOS

transistor, said NMOS transistor being fabricated within a p-type well formed in an n-type substrate.

48. A projector comprising:
a light source; and
a spatial light modulator having at least one pixel cell, comprising:
an electrostatically deflectable micro-mirror;
an electrode for electrically controlling a rotation of the micro-mirror;
and
a memory cell storing an activation or an inactivation voltage level for applying an voltage to the electrode, the cell further comprising:
a MOS transistor having a source connected to a bitline, a drain and a gate connected to a wordline, and
a capacitor having a first and second plates wherein the first plate is connected to the drain of the transistor and the second plate is connected to a pump signal.
49. A memory cell comprising:
a MOS-type transistor having a source, a gate and a drain;
a capacitor having a first plate connected to the drain of the transistor, and a second plate;
a wordline connected to the gate of the transistor for addressing the cell;
a bitline having a maximum voltage, connected to the source of the transistor for writing the cell; and
a pump line connected to the second plate of the capacitor such that the absolute value of the voltage of the first plate of the capacitor is greater than the absolute value of the voltage of the bitline.
50. The memory cell of claim 49, wherein the MOS-type transistor is a PMOS-transistor; and the first plate of the capacitor has an voltage that is less than the maximum voltage of the bitline.

51. The memory cell of claim 49, wherein the MOS-type transistor is an NMOS-transistor; and the first plate of the capacitor has an voltage that is greater than the minimum voltage of the bitline.

52. The memory cell of claim 49, wherein the memory cell is part of a spatial light modulator.

53. The memory cell of claim 49, wherein the spatial light modulator is a micro-mirror array having one or more micro-mirrors.

54. A memory cell comprising:
a MOS-type transistor having a source, a gate and a drain;
a capacitor having a first plate connected to the drain of the transistor, and a second plate;
a wordline connected to the gate of the transistor for addressing the cell;
a bitline having a maximum voltage, connected to the source of the transistor for writing the cell;
a pump line connected to the second plate of the capacitor such that the absolute of the voltage of the first plate of capacitor is greater than the absolute value of the maximum voltage of the bitline; and
wherein the absolute value of a difference between the maximum and minimum voltages of the first plate of the capacitor is greater than the absolute value of a difference between the maximum and minimum voltages of the bitline.

55. The memory cell of claim 54, wherein the memory cell is part of a spatial light modulator.

56. The memory cell of claim 54, wherein the spatial light modulator is a micro-mirror array having one or more micro-mirrors.

57. A memory cell comprising:
a substrate;
a first region of n-type doping in the substrate;

- a second region of p-type doping in the substrate;
- a first electric supply potential connected to the first region;
- a second electric supply potential connected to the second region;
- a circuit that further comprises:
 - a transistor having a source and a drain, wherein the drain voltage can be either higher than both supply potentials or lower than both supply potentials.

58. The memory cell of claim 57, wherein the circuitry further comprises:
a capacitor having a first plate connected to the drain of the transistor; and a second plate connected to a pump signal.

59. The memory cell of claim 57, wherein the memory cell is part of a spatial light modulator.

60. The memory cell of claim 59, wherein the spatial light modulator is a micro-mirror array having one or more reflective micro-mirrors.

61. A memory cell comprising:
a substrate;
a first region of n-type doping in the substrate;
a second region of p-type doping in the substrate;
a first electric supply potential connected to the first region;
a second electric supply potential connected to the second region;
a circuit that further comprises:

- a transistor having a source and a drain, wherein the absolute value of a difference between a maximum voltage and a minimum voltage of the drain is greater than a difference between the supply potentials.

62. The memory cell of claim 61, wherein the memory cell is part of a spatial light modulator.

63. The memory cell of claim 61, wherein the spatial light modulator is a micro-mirror array having one or more micro-mirrors.

64. A spatial light modulator, comprising:
a reflective micro-mirror for reflecting an incident light;
a circuit for controlling a rotation of the micro-mirror plate, the circuitry further comprises:

a transistor having a source and a drain, wherein the absolute value of a difference between a maximum voltage and a minimum voltage of the drain is greater than a difference of the supply potentials.

65. The spatial light modulator of claim 64, further comprising:
an electrode connected to the circuitry for electrically controlling the rotation of the micro-mirror.

66. The spatial light modulator of claim 64, wherein the circuitry further comprises:
a capacitor having a first and second plates wherein the first plate is connected to the drain of the transistor, and the second plate is connected to a pump signal.

67. The spatial light modulator of claim 66, further comprising:
a wordline connected to the gate of the transistor for addressing the memory cell; and
a bitline connected to the source of the transistor.

68. A memory cell, comprising:
a transistor having a source, a gate and a drain; and
a capacitor having a first and second plates for storing a voltage, wherein the stored voltage is at least 10 volts.

69. The memory cell of claim 68, wherein the stored voltage is at least 15 volts.

70. The memory cell of claim 68, wherein the stored voltage is at least 20 volts.

71. The memory cell of claim 68 is part of a spatial light modulator.
72. The memory cell of claim 71, wherein the spatial light modulator further comprises: a micro-mirror for reflecting an incident light.
73. The memory cell of claim 68, wherein the transistor is made in a crystalline silicon substrate.
74. The memory cell of claim 68, wherein the memory cell is part of a spatial light modulator.
75. The memory cell of claim 74, wherein the spatial light modulator is a micro-mirror array having one or more micro-mirrors.
76. A circuit, comprising:
an asymmetric high-voltage transistor having a high-voltage tolerant drain and a low-voltage tolerant source and gate.
77. The circuit of the claim 76, further comprising:
a capacitor having a first and second plates, wherein the first plate is connected to the drain of the transistor, and the second plate is connected to a pump signal.
78. The circuit of claim 76, further comprising:
an organic light emission diode.
79. The circuit of claim 76, wherein the transistor is a PMOS transistor formed on a silicon substrate.
80. The circuit of claim 76, wherein the transistor is a NMOS transistor formed on a silicon substrate.
81. The circuit of claim 76, wherein the circuit is part of a spatial light modulator.

82. The circuit of claim 76, wherein the spatial light modulator is a micro-mirror array having one or more micro-mirrors..

83. A circuit, comprising:
a transistor having a source a gate and a drain;
a wordline connected to the gate;
a bitline connected to the source;
a capacitor having a first and second plates, wherein the first plate is connected to the drain of the transistor and the second plate is connected to a pump signal; and
wherein the wordline maintains an active voltage level while the pump signal changes between an active voltage level and inactive voltage level.

84. The circuit of claim 83, wherein the circuit is part of a spatial light modulator.

85. The circuit of claim 83, wherein the spatial light modulator is a micro-mirror array.

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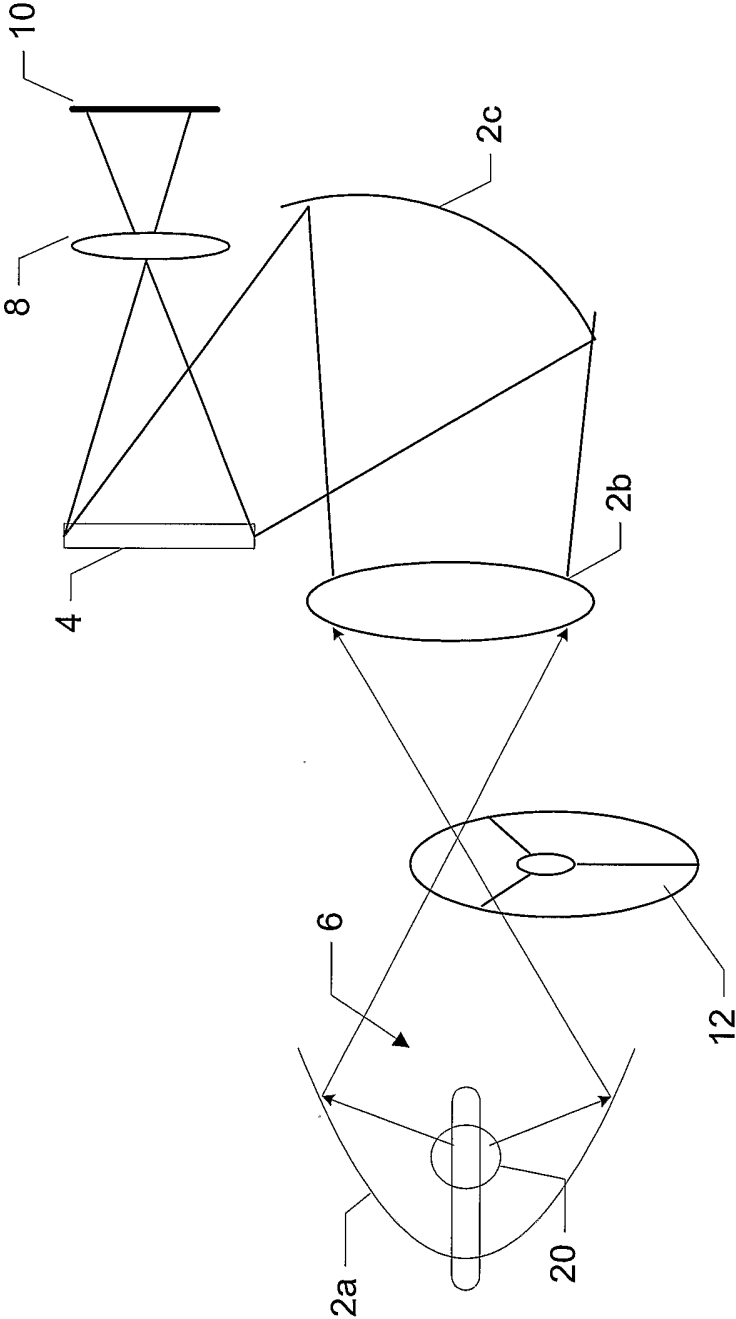
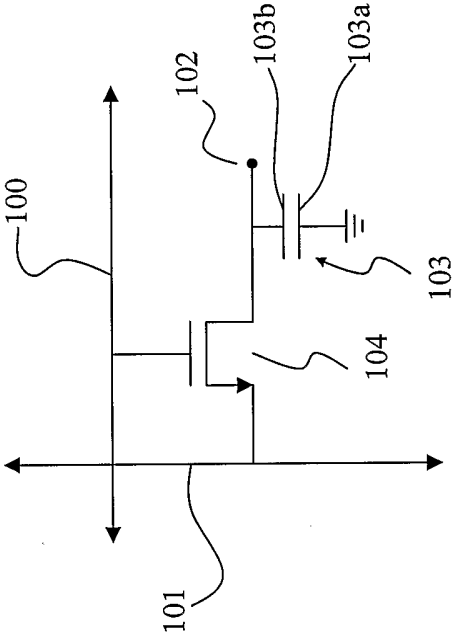


FIG. 1

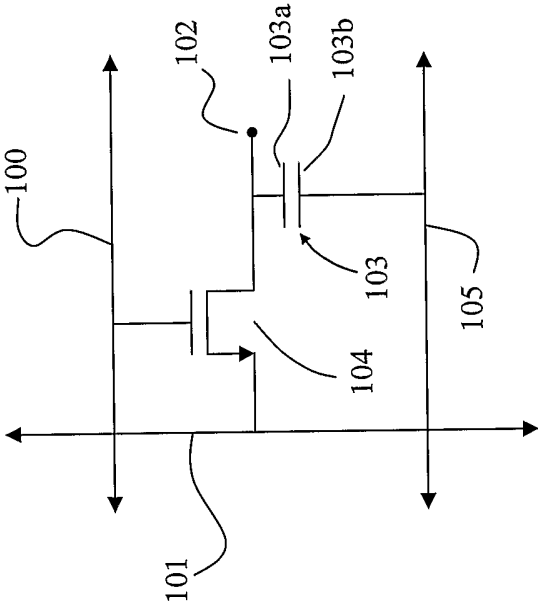
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FIG. 2 (Prior Art)



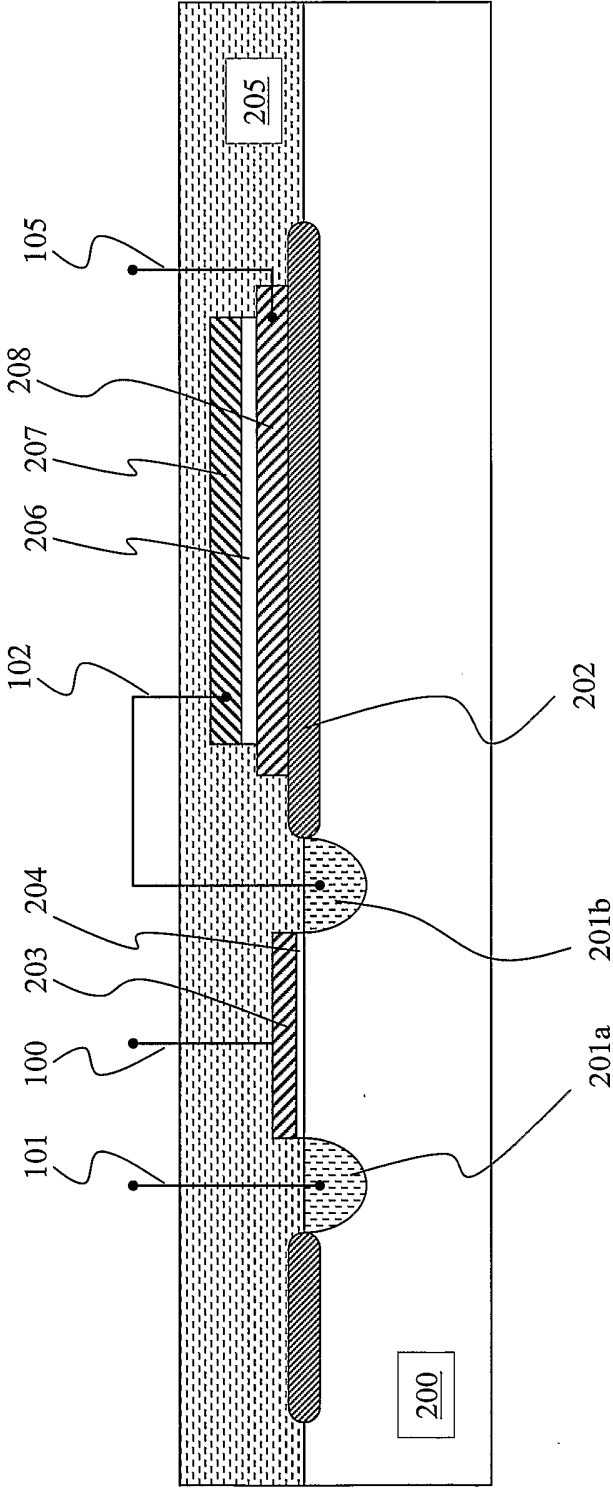
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FIG. 3



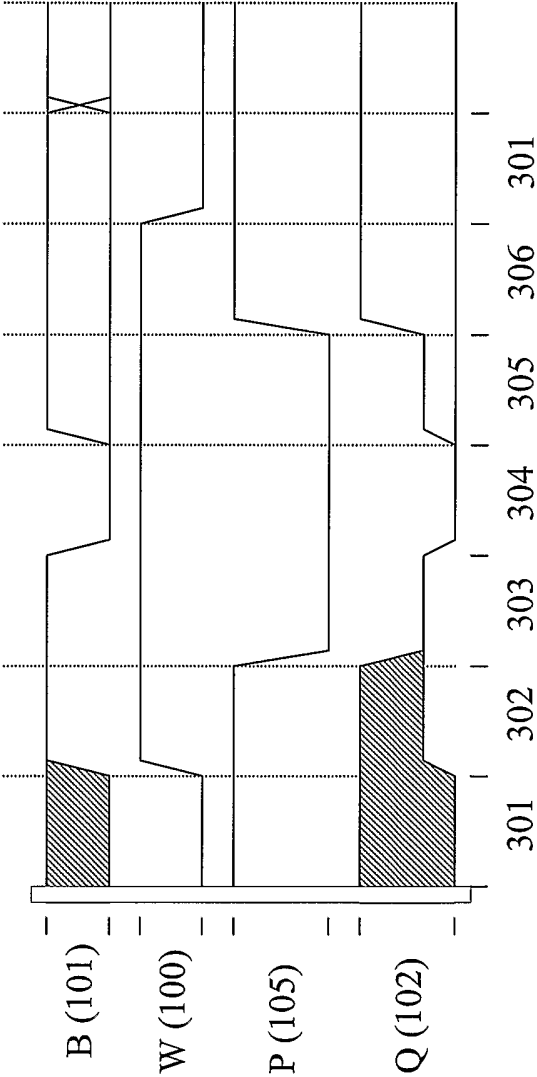
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FIG. 4



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FIG. 5



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US03/00600

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G11C 11/24

US CL : 365/149, 185.25, 64; 359/296, 248

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/149, 185.25, 64; 359/296, 248

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|--|---------------------------|
| A,P | US 6,421,285 B2 (Matsuzaki et al) 16 July 2002 (16.07.2002), Fig. 4 | 1-24, 26-32, 49-63, 68-85 |
| A,P | US 6,344,672 B2 (Huffman) 05 February 2002 (05.02.2002), fig. 2, 6; Col. 2, line 36-59; col. 6, line 25-col. 7, line 3 and line 25; col. 7, line 25-48, fig. 3; col. 8, lines 14-18. | 1-24, 26-85 |
| A,P | US 6,466,358 B2 (Tew) 15 October 2002 (15.10.2002) Fig. 1, 2; col. 5, line 32-col. 6, line 17 | 1-24, 26-85 |
| A,E | US 6,535,187 B1 (Wood) 18 March 2003 (18.03.2003), fig. 1, col. 2, lines 46-67. | 1-24, 26-85 |



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

22 April 2003 (22.04.2003)

Date of mailing of the international search report

07 MAY 2003

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