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(54) Title: DUAL-PORT SRAM MEMORY USING SINGLE-PORT MEMORY CELL

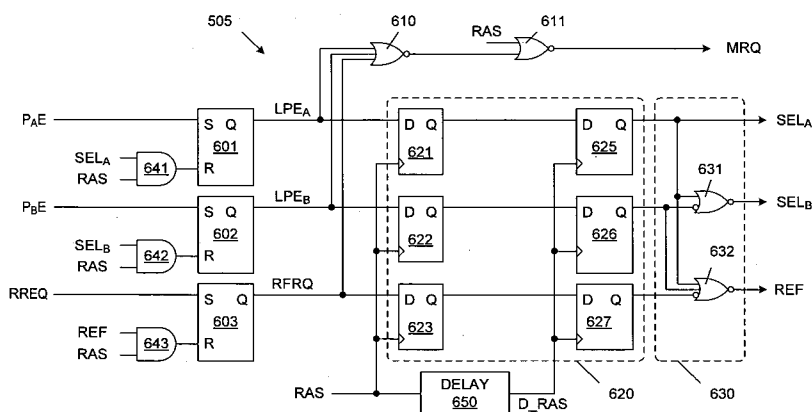


FIG. 6

(57) Abstract: A dual-port memory system is implemented using single-port memory cells. An access arbiter having a synchronization circuit is used to prioritize and synchronize the access requests associated with the two ports. The access arbiter can also prioritize and synchronize refresh requests, in the case where the single-port memory cells require refresh. Access requests on the two ports and the refresh requests can be asynchronous. The access arbiter synchronizes the various requests by latching the requests into first-stage registers when a row access signal (RAS) is activated, and subsequently latching the contents of the first-stage registers into second-stage registers after a selected delay.

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 07/0204

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 12/00 (2008.04)

USPC - 711/149

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 711/149

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
USPC: 711/147-149

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO WEST (PGPUB,USPAT,EPAB,JPAB); GOOGLE Scholars; Arbitrate, request, port, read-only, read/write, memory, cell, array, store, deactivate, activate, synchronization, prioritizing, semiconductor, control signal, data, sequencer

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2003/0135699 A1 (MATSUZAKI et al.) 17 July 2003 (17.07.2003) entire document	1-5, 7, 10-16, and 18
--	(especially Fig 10, para [0004], [0008], [0019], [0172]-[0173], [0182]-[0184], [0187]-[0188],	-----
Y	[0198], [0214]-[0215], [0302], [0316], [0318]-[0319], [0495], [0552]-[0556])	6, 8-9, 17, 19-21
Y	US 2003/0067830 A1 (LEUNG et al.) 10 April 2003 (10.04.2003) entire document (especially para [0069]-[0071])	6, 17
Y	US 2002/0146025 A1 (OKINA) 10 October 2002 (10.10.2002) entire document (especially para [0019], [0021], [0039])	8-9 and 19-21
A	US 5,197,035 A (ITO) 23 March 1993 (23.03.1993) entire document	1-21
A	US 2005/0005069 A1 (AU et al.) 06 January 2005 (06.01.2005) entire document	1-21
A	US 6,070,256 A (WU et al.) 30 May 2000 (30.05.2000) entire document	1-21

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