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(54) **Title**: TRENCH GATE TRENCH FIELD PLATE SEMI-VERTICAL SEMI-LATERAL MOSFET

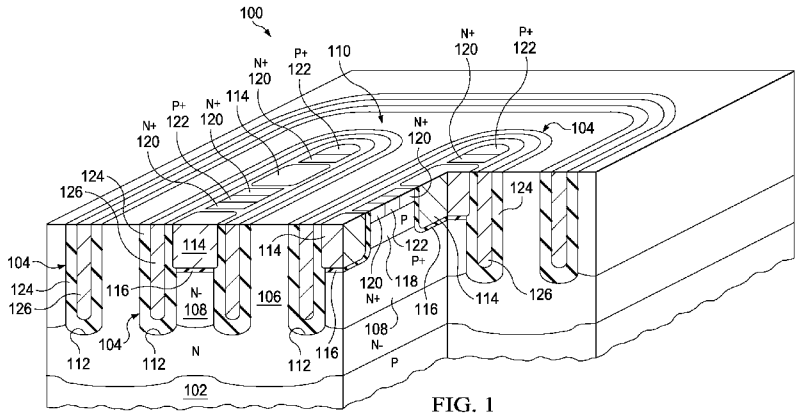

FIG. 1

(57) **Abstract**: In described examples, a semiconductor device (100) has a vertical drain extended MOS transistor (110) with deep trench structures (104) to define a vertical drift region (108) and at least one vertical drain contact region (106), separated from the vertical drift region (108) by at least one instance of the deep trench structures (104). Dopants are implanted into the vertical drain contact regions (106), and the semiconductor device (100) is annealed, so that the implanted dopants diffuse proximate to a bottom of the deep trench structures (104). The vertical drain contact regions (106) make electrical contact to the proximate vertical drift region (108) at the bottom of the intervening deep trench structure (104). At least one gate (114), body region (118) and source region (120) are formed above the drift region (108) at, or proximate to, a top surface of a substrate (102) of the semiconductor device (100). The deep trench structures (104) are spaced to form RESURF regions for the drift region (108).

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TRENCH GATE TRENCH FIELD PLATE SEMI-VERTICAL SEMI-LATERAL MOSFET

[0001] This relates in general to semiconductor devices, and in particular to drain extended transistors in semiconductor devices.

BACKGROUND

[0002] An extended drain metal oxide semiconductor (MOS) transistor may be characterized by the resistance of the transistor in the on state, the lateral area that the transistor occupies at the top surface of the substrate containing the transistor, and the breakdown potential between the drain node and the source node of the transistor that limits the maximum operating potential of the transistor. It may be desirable to reduce the area of the transistor for given values of the on-state resistance and the breakdown potential. One technique to reduce the area is to configure the drift region in the extended drain in a vertical orientation, so that drain current in the drift region flows perpendicularly to the top surface of the substrate. Integrating a vertically oriented drift region in a semiconductor device using planar processing while limiting fabrication cost and complexity to desired levels may be problematic.

SUMMARY

[0003] In described examples, a semiconductor device having a vertical drain extended MOS transistor may be formed by forming deep trench structures to define a vertical drift region of the transistor and to define at least one vertical drain contact region proximate to the drift region, separated from the vertical drift region by at least one instance of the deep trench structures. Dopants are implanted into the vertical drain contact regions, and the semiconductor device is annealed, so that the implanted dopants diffuse proximate to a bottom of the deep trench structures. The vertical drain contact regions make electrical contact to the proximate vertical drift region at the bottom of the intervening deep trench structure. At least one gate, body region and source region are formed above the drift region at, or proximate to, a top surface of a substrate of the semiconductor device. The deep trench structures are spaced to form RESURF regions for the drift region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a cross-sectional view of a semiconductor device having a vertical drain extended MOS transistor.

[0005] FIG. 2 is a cross-sectional view of another semiconductor device having a vertical drain extended MOS transistor.

[0006] FIG. 3 is a cross-sectional view of a further semiconductor device having a vertical drain extended MOS transistor.

[0007] FIG. 4 is a cross-sectional view of another semiconductor device having a vertical drain extended MOS transistor.

[0008] FIG. 5 is a cross-sectional view of a further semiconductor device having a vertical drain extended MOS transistor.

[0009] FIG. 6A through FIG. 6E are cross-sectional views of a semiconductor device in successive stages of fabrication.

[0010] FIG. 7 and FIG. 8 are top views of semiconductor devices having vertical drain extended MOS transistors.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0011] The following co-pending patent applications are hereby incorporated by reference: Application No. US 14/044,915; and Application No. US 14/044,926.

[0012] In at least one example, a semiconductor device may be an integrated circuit containing the vertical drain extended MOS transistor and at least one other transistor. The semiconductor device may be, in another example, a discrete device in which the vertical drain extended MOS transistor is the only transistor.

[0013] For the purposes of this description, the term "specific resistivity" with respect to a transistor is a product of an area the transistor occupies at a top surface of a substrate in which the transistor is formed times a resistance of the transistor when the transistor is fully turned on.

[0014] For the purposes of this description, the term "RESURF" refers to a material that reduces an electric field in an adjacent semiconductor region. For example, a RESURF region may be a semiconductor region with an opposite conductivity type from the adjacent semiconductor region. RESURF structures are described in Appels, et al., "Thin Layer High Voltage Devices" Philips J, Res. 35 1-13, 1980.

[0015] The examples described in this disclosure describe n-channel devices. Corresponding p-channel devices may be formed by appropriate changes in doping polarities. FIG. 1 is a cross-sectional view of a semiconductor device having a vertical drain extended MOS transistor. The semiconductor device 100 is formed in and on a p-type semiconductor substrate 102. Deep trench structures 104 are disposed in the substrate 102 to define at least one n-type vertical drain contact region 106 and at least one n-type vertically oriented drift region 108 of the vertical drain extended MOS transistor 110. The vertical drain contact region 106 is bounded on at least two opposite sides by the deep trench structures 104. The vertical drain contact region 106 is n-type and extends below bottoms 112 of the deep trench structures 104 in this example. The vertical drain contact region 106 may extend laterally under the bottoms 112 of the deep trench structures 104 to separate the vertically oriented drift region 108 from a p-type bottom region of the substrate 102 as shown in FIG. 1. In other examples, the vertical drain contact region 106 may have a more limited lateral extent. The vertically oriented drift regions 108 are n-type and make electrical connection to the vertical drain contact region 106 proximate to the bottoms of the deep trench structures 104. In this example, electrical connection to the vertical drain contact region 106 is made at a top surface of the substrate 102.

[0016] At least one gate 114 and corresponding gate dielectric layer 116 are disposed over the vertically oriented drift regions 108. In this example, the gates 114 are disposed in trenches in the substrate 102 and extend between adjacent instances of the deep trench structures 104. At least one p-type body region 118 is disposed in the substrate 102 adjacent to the gates 114 and the vertically oriented drift regions 108. At least one n-type source region 120 is disposed in the substrate adjacent to the gates 114. One or more optional p-type body contact regions 122 may be disposed in the substrate 102 abutting the body regions 118. In this example, electrical connection to the source regions 120 and the body contact regions 122 are made at a top surface of the substrate 102. Other configurations of gates may be used in the vertical drain extended MOS transistor 110 with the configuration of deep trench structures 104, vertical drain contact region 106 and vertically oriented drift region 108 shown in FIG. 1.

[0017] The deep trench structures 104 may be 1 to 5 microns deep, and 0.5 to 1.5 microns wide. For example, deep trench structures 104 that are 2.5 microns deep may provide 30 volt operation for the vertical drain extended MOS transistor 110. Deep trench structures 104 that are 4 microns deep may provide 50 volt operation for the vertical drain extended MOS transistor

110. The deep trench structures 104 have dielectric liners 124 and may have optional electrically conductive central members 126. Instances of the deep trench structures 104 abutting the vertically oriented drift regions 108 may be spaced 0.5 to 2 microns apart to provide RESURF regions for the vertically oriented drift regions 108. Instances of the deep trench structures 104 abutting the vertical drain contact region 106 may be spaced 0.5 to 2.5 microns apart. During operation of the vertical drain extended MOS transistor 110, the electrically conductive central members 126, if any, may be electrically biased to reduce a peak electric field in the vertically oriented drift regions 108. For example, the electrically conductive central members 126 may be connected to source regions 120, to the gates 114 or to a bias source having a desired potential.

[0018] Instances of the vertically oriented drift regions 108 are disposed adjacent to the vertical drain contact region 106. For example, instances of the vertically oriented drift regions 108 may alternate with the vertical drain contact region 106, as shown in FIG. 1. The deep trench structures 104 may surround the vertically oriented drift regions 108, as shown in FIG. 1. The vertical drain contact region 106 may be contiguous, as shown in FIG. 1. Alternate configurations of the deep trench structures 104 are discussed below. Forming the vertical drain extended MOS transistor 110, so that the deep trench structures 104 provide RESURF regions for the vertically oriented drift regions 108, may provide a desired balance between operating voltage and specific resistivity for the vertical drain extended MOS transistor 110. Forming the vertical drain contact region 106 to isolate the vertically oriented drift regions 108 from the bottom region of the substrate 102 may desirably reduce a resistance of the vertical drain extended MOS transistor 110.

[0019] FIG. 2 is a cross-sectional view of another semiconductor device having a vertical drain extended MOS transistor. The semiconductor device 200 is formed in and on a p-type semiconductor substrate 202. Deep trench structures 204, as described in reference to FIG. 1, are disposed in the substrate 202 to define at least one n-type vertical drain contact region 206 and at least one n-type vertically oriented drift region 208 of the vertical drain extended MOS transistor 210. The vertical drain contact region 206 is bounded on at least two opposite sides by the deep trench structures 204. The vertical drain contact region 206 is n-type and extends below bottoms 212 of the deep trench structures 204 in this example. The vertical drain contact region 206 may extend laterally past the bottoms 212 of the deep trench structures 204, but not enough to isolate the vertically oriented drift region 208 from a bottom region of the substrate 202, as shown in

FIG. 2. In other examples, the vertical drain contact region 206 may have a more limited vertical and/or lateral extent. The vertically oriented drift regions 208 are n-type and make electrical connection to the vertical drain contact region 206 proximate to the bottoms of the deep trench structures 204. In this example, electrical connection to the vertical drain contact region 206 is made at a top surface of the substrate 202.

[0020] At least one gate 214 and corresponding gate dielectric layer 216 are disposed over the vertically oriented drift regions 208. In this example, the gates 214 are disposed in trenches in the substrate 202 and do not abut adjacent instances of the deep trench structures 204. At least one p-type body region 218 is disposed in the substrate 202 adjacent to the gates 214 and the vertically oriented drift regions 208. At least one n-type source region 220 is disposed in the substrate adjacent to the gates 214. One or more optional p-type body contact regions 222 may be disposed in the substrate 202 abutting the body regions 218. In this example, electrical connection to the source regions 220 and the body contact regions 222 are made at a top surface of the substrate 202. Other configurations of gates may be used in the vertical drain extended MOS transistor 210 with the configuration of deep trench structures 204, vertical drain contact region 206 and vertically oriented drift region 208 shown in FIG. 2.

[0021] Instances of the vertically oriented drift regions 208 are disposed adjacent to the vertical drain contact region 206. For example, instances of the vertically oriented drift regions 208 may alternate with the vertical drain contact region 206, as shown in FIG. 2. The deep trench structures 204 may surround the vertically oriented drift regions 108, as shown in FIG. 2. The vertical drain contact region 106 may be contiguous, as shown in FIG. 2. Forming the vertical drain extended MOS transistor 210, so that the deep trench structures 204 provide RESURF regions for the vertically oriented drift regions 208, may provide a desired balance between operating voltage and specific resistivity for the vertical drain extended MOS transistor 210. Forming the vertical drain contact region 206 to extend laterally past the bottoms 212 of the deep trench structures 204, but not enough to isolate the vertically oriented drift region 208 from a bottom region of the substrate 202, may allow depletion of the vertically oriented drift region 208 along a greater vertical distance, and desirably allow operation at a higher voltage.

[0022] FIG. 3 is a cross-sectional view of a further semiconductor device having a vertical drain extended MOS transistor. The semiconductor device 300 is formed in and on a p-type semiconductor substrate 302. Deep trench structures 304, as described in reference to FIG. 1, are

disposed in the substrate 302 to define at least one n-type vertical drain contact region 306 and at least one n-type vertically oriented drift region 308 of the vertical drain extended MOS transistor 310. The vertical drain contact region 306 is bounded on at least two opposite sides by the deep trench structures 304. The vertical drain contact region 306 is n-type and may extend below bottoms 312 of the deep trench structures 304 as shown in FIG. 3. In this example, the vertically oriented drift region 308 is laterally displaced from the vertical drain contact region 306 by at least two instances of the deep trench structures 304, providing a horizontal drift component to an extended drain of the vertical drain extended MOS transistor 310. In this example, electrical connection to the vertical drain contact region 306 is made at a top surface of the substrate 302.

[0023] At least one gate 314 and corresponding gate dielectric layer 316 are disposed over the vertically oriented drift regions 308. In this example, the gates 314 are disposed above the substrate 302 over a p-type body region 318 and n-type source region 320. One or more optional p-type body contact regions 322 may be disposed in the substrate 302 abutting the body regions 318. In this example, electrical connection to the source regions 320 and the body contact regions 322 are made at a top surface of the substrate 302. Other configurations of gates may be used in the vertical drain extended MOS transistor 310 with the configuration of deep trench structures 304, vertical drain contact region 306 and laterally displaced vertically oriented drift region 308 shown in FIG. 3. Forming the vertically oriented drift region 308 to be laterally displaced from the vertical drain contact region 306 may allow lateral depletion of the vertically oriented drift region 308, and may advantagously increase an operating voltage of the vertical drain extended MOS transistor 310 without requiring deeper instances of the deep trench structures 304.

[0024] FIG. 4 is a cross-sectional view of another semiconductor device having a vertical drain extended MOS transistor. The semiconductor device 400 is formed in and on a p-type semiconductor substrate 402. Deep trench structures 404 are disposed in the substrate 402 as described in reference to FIG. 1, to define at least one vertical drain contact region 406 and at least one vertically oriented drift region 408 of the vertical drain extended MOS transistor 410. The vertical drain contact region 406 is bounded on at least two opposite sides by the deep trench structures 404. The vertical drain contact region 406 is n-type and in this example extends proximate to, but not below, bottoms 412 of the deep trench structures 404. The vertically

oriented drift regions 408 are n-type and make electrical connection to the vertical drain contact region 406 proximate to the bottoms 412 of the deep trench structures 404.

[0025] At least one gate 414 and corresponding gate dielectric layer 416 is disposed over the vertically oriented drift regions 408. In this example, the gates 414 are disposed above the substrate 402 over a p-type body region 418 and n-type source region 420. One or more optional p-type body contact regions 422 may be disposed in the substrate 402 abutting the body regions 418. In this example, portions of the vertically oriented drift regions 408 directly under the gates 414 are laterally separated from nearest instances of the deep trench structures 404 by dielectric material 434, such as field oxide 434. Such a configuration may add a horizontal drift component to the vertical drain extended MOS transistor 410, and may advantagously increase an operating voltage of the vertical drain extended MOS transistor 410. The portion of the vertically oriented drift regions 408 directly under the gates 414 may also possibly be laterally separated from nearest instances of the vertical drain contact region 406 by at least two instances of the deep trench structures 404, as shown in FIG. 3. Other configurations of gates may be used in the vertical drain extended MOS transistor 410 with the configuration of deep trench structures 404, vertical drain contact region 406 and vertically oriented drift region 408 shown in FIG. 4. Forming the vertically oriented drift region 408 to be laterally displaced from the vertical drain contact region 406 may allow lateral depletion of the vertically oriented drift region 408, and may advantagously increase an operating voltage of the vertical drain extended MOS transistor 410 without requiring deeper instances or additional instances of the deep trench structures 404.

[0026] FIG. 5 is a cross-sectional view of a further semiconductor device having a vertical drain extended MOS transistor. The semiconductor device 500 is formed in and on a p-type semiconductor substrate 502 as described in reference to FIG. 1. Deep trench structures 504 are disposed in the substrate 502 as described in reference to FIG. 1 to define vertical portions of at least one vertical drain contact region 506 and at least one vertically oriented drift region 508 of the vertical drain extended MOS transistor 510. The vertical drain contact region 506 is bounded on at least two opposite sides by the deep trench structures 504. The vertical drain contact regions 506 are n-type and, in this example, extend proximate to, and possibly below, bottoms 512 of the deep trench structures 504. In this example, the vertically oriented drift region 508 extends below the bottoms 512 of the deep trench structures 504 and extends laterally to form a

continuous n-type region. The vertically oriented drift region 508 is n-type and makes electrical connection to the vertical drain contact regions 506. Such a configuration may advantageously reduce an on-state resistance of the vertical drain extended MOS transistor 510.

[0027] At least one gate 514 and corresponding gate dielectric layer 516 is disposed above the vertically oriented drift regions 508. In this example, the gates 514 are disposed in the dielectric liners 524 of the deep trench structures 504, adjacent to a p-type body region 518 and n-type source region 520. One or more optional p-type body contact regions 522 may be disposed in the substrate 502 abutting the body regions 518. Other configurations of gates may be used in the vertical drain extended MOS transistor 510 with the configuration of deep trench structures 504, vertical drain contact region 506 and vertically oriented drift region 508 shown in FIG. 5.

[0028] FIG. 6A through FIG. 6E are cross-sectional views of a semiconductor device in successive stages of fabrication. Referring to FIG. 6A, the semiconductor device 600 is formed in and on a p-type semiconductor substrate 602, such as a single crystal silicon wafer. A drift region ion implant process is performed, which implants n-type dopants such as phosphorus into the substrate 602 in an area defined for vertically oriented drift regions, to form a drift implanted region 630. For example, a dose of the drift region ion implant process may be 1×10^{12} cm^{-2} to 1×10^{13} cm^{-2}. In at least one version of this embodiment, the drift implanted region 630 may extend over areas defined for vertical drain contact region, as shown in FIG. 6A. In an alternate version, the drift implanted region 630 may be confined to an area of the substrate defined for the vertically oriented drift regions.

[0029] Referring to FIG. 6B, deep isolation trenches 628 are formed in the substrate 602, such as by a process stating with forming a layer of hard mask material over a top surface of the substrate 602. A hard mask may be formed by forming an etch mask by a photolithographic followed by removing the hard mask material over regions defined for the deep isolation trenches 628 using a reactive ion etch (RIE) process. After patterning the hard mask, material is removed from the substrate 602 in the deep isolation trenches 628 using an anisotropic etch process, such as a Bosch deep RIE process or a continuous deep RIE process.

[0030] Referring to FIG. 6C, dielectric liners 624 are formed in the deep isolation trenches 628, so that the dielectric liners 624 abut the substrate 602. For example, the dielectric liners 624 may include thermally grown silicon dioxide. The dielectric liners 624 may also include one or

more layers of dielectric material such as silicon dioxide, silicon nitride and/or silicon oxynitride, formed by a chemical vapor deposition (CVD) process.

[0031] Optional electrically conductive central members 626 may be formed on the dielectric liners 624. For example, the electrically conductive central members 626 may include polycrystalline silicon, commonly referred to as polysilicon, formed by thermally decomposing SiH_4 gas inside a low-pressure reactor at a temperature of 580 °C to 650 °C. The polysilicon may be doped during formation to provide a desired electrical conductivity. The deep isolation trenches 628 filled with the dielectric liners 624 and the electrically conductive central members 626, if any, form deep trench structures 604. Unwanted dielectric material over the top surface of the substrate 602 from formation of the dielectric liners 624 and unwanted conductive material over the top surface of the substrate 602 from formation of the electrically conductive central members 626 may be removed, such as by using an etchback and/or chemical mechanical polish (CMP) process.

[0032] Referring to FIG. 6D, a drain contact ion implant process is performed, which implants n-type dopants such as phosphorus into the substrate 602 in an area defined for the vertical drain contact region, to form a drain contact implanted region 632. A dose of the drift region ion implant process is at least ten times higher than the drift region ion implant dose, and may be 1×10^{16} cm^{-2} to 3×10^{16} cm^{-2} for example. The drain contact ion implant process may provide dopants to polysilicon versions of the electrically conductive central members 626, to attain a desired electrical conductivity.

[0033] Referring to FIG. 6E, a thermal drive operation is performed, which heats the substrate 602 to activate and diffuse the implanted dopants in the drift implanted regions 630 and the drain contact implanted region 632 and thereby form the vertically oriented drift regions 608 and the vertical drain contact region 606, respectively. Conditions of the thermal drive operation depend on a depth of the deep trench structures 604 and a desired lateral extent of the vertical drain contact region 606 at the bottoms of the deep trench structures 604. For example, a vertical drain extended MOS transistor with deep trench structures 604 that are 2.5 microns deep may have a thermal drive operation, which heats the substrate 602 at 1100 °C for 3.5 to 4 hours, or equivalent anneal conditions, such as 1125 °C for 2 hours, or 1050 °C for 12 hours.

[0034] FIG. 7 and FIG. 8 are top views of semiconductor devices having vertical drain extended MOS transistors. Gates shown in FIG. 7 and FIG. 8 are disposed in trenches as

discussed in reference to FIG. 2, but other configurations of gates may be used in these examples. Referring to FIG. 7, the semiconductor device 700 is formed in and on a semiconductor substrate 702 as described in reference to FIG. 6A. Deep trench structures 704 with closed loop configurations are disposed in the substrate 702. Instances of the deep trench structures 704 laterally surround vertical drain contact regions 706. Gates 714 and gate dielectric layer 716 of the vertical drain extended MOS transistor 710 are disposed between the deep trench structures 704 laterally surrounding the vertical drain contact regions 706. A vertical drift region 708 is disposed between the deep trench structures 704 surrounding the vertical drain contact regions 706. A body region, source regions and body contact regions of the vertical drain extended MOS transistor 710 are not shown in FIG. 7 to more clearly show the arrangement of the vertical drift region 708 and the vertical drain contact regions 706. An instance of the deep trench structures 704 laterally surrounds the vertical drain extended MOS transistor 710. Electrical connection to the vertical drain contact regions 706 are made at a top surface of the substrate 702. Surrounding the vertical drain contact regions 706 with the deep trench structures 704 may prevent a breakdown electric field between a drain contact and a body region of the vertical drain extended MOS transistor 710, and may advantageously allow the vertical drain extended MOS transistor 710 to operate at a higher voltage than otherwise.

[0035] Referring to FIG. 8, the semiconductor device 800 is formed in and on a semiconductor substrate 802 as described in reference to FIG. 6A. Deep trench structures 804 with linear configurations are disposed in the substrate 802. Vertical drain contact regions 806 are disposed between adjacent pairs of the linear deep trench structures 804. Gates 814 and gate dielectric layers 816 are disposed between adjacent pairs of the deep trench structures 804 alternating with the vertical drain contact regions 806. Vertical drift regions 808 are disposed between the alternate pairs of deep trench structures 804 with the gates 814. A body region 818 is disposed around the linear deep trench structures 804 and extends over the vertical drift regions 808 to abut the gates 814; the portion of the body region 818 extending over the vertical drift regions 808 and the source regions and body contact regions of the vertical drain extended MOS transistor 810 are not shown in FIG. 8 to more clearly show the arrangement of the vertical drift region 808 and the vertical drain contact regions 806. An instance of the deep trench structures 804 laterally surrounds the vertical drain extended MOS transistor 810. Electrical connection to the vertical drain contact regions 806 are made at a top surface of the substrate

802. Disposing the vertical drain contact regions 806 between linear deep trench structures 804 may advantageously reduce an area required for the vertical drain extended MOS transistor 810, thereby reducing a fabrication cost of the semiconductor device 800.

[0036] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate comprising a semiconductor having a first conductivity type; and

a vertical drain extended metal oxide semiconductor (MOS) transistor, including: a deep trench structure disposed in the substrate, at least one micron deep, having a dielectric liner abutting the substrate; a vertical drain contact region having a second conductivity type opposite from the first conductivity type disposed in the substrate, the vertical drain contact region abutting and being bounded on at least two opposite sides by the deep trench structure, the vertical drain contact region extending below a bottom of the deep trench structure; a vertically oriented drift region having the second conductivity type, disposed in the substrate, laterally separated from the vertical drain contact region by a portion of the deep trench structure, the vertically oriented drift region making electrical contact to the vertical drain contact region proximate to the bottom of the deep trench structure; and a body region having the first conductivity type disposed over the vertically oriented drift region.

2. The semiconductor device of claim 1, wherein the vertical drain contact region does not extend laterally past the deep trench structure abutting the vertical drain contact region.

3. The semiconductor device of claim 1, wherein the vertical drain contact region extends laterally past the deep trench structure abutting the vertical drain contact region.

4. The semiconductor device of claim 1, wherein the vertical drain contact region extends laterally under the vertically oriented drift region and abuts an adjacent portion of the vertical drain contact region.

5. The semiconductor device of claim 1, wherein the vertical drain contact region is laterally surrounded by the deep trench structure, the deep trench structure having a closed loop configuration.

6. The semiconductor device of claim 1, wherein the vertically oriented drift region is laterally surrounded by the deep trench structure, the deep trench structure having a closed loop configuration.

7. The semiconductor device of claim 1, wherein the body region abuts the portion of the deep trench structure that abuts the vertical drain contact region opposite from the body region.

8. The semiconductor device of claim 1, wherein the body region is laterally separated by

dielectric material from the portion of the deep trench structure that abuts the vertical drain contact region opposite from the body region.

9. The semiconductor device of claim 1, wherein the deep trench structure is 2.5 microns to 5 microns deep.

10. The semiconductor device of claim 1, wherein: the first conductivity type is p-type; and the second conductivity type is n-type.

11. A method of forming a semiconductor device, the method comprising:

providing a substrate comprising a semiconductor having a first conductivity type; and

forming a vertical drain extended MOS transistor, by a process including: implanting dopants of a second conductivity type opposite from the first conductivity type into the substrate in an area defined for a vertically oriented drift region; forming a deep isolation trench at least one micron deep in the substrate, the deep isolation trench abutting the area defined for the vertically oriented drift region; forming a dielectric liner in the deep isolation trench, the dielectric liner contacting the substrate, to form at least one deep trench structure; implanting dopants of the second conductivity type into the substrate in an area defined for a vertical drain contact region bounded on at least two opposite sides by the deep trench structure, such that a dose of the dopants in the vertical drain contact region is at least ten times higher than a dose of the dopants in the vertically oriented drift region, wherein the vertically oriented drift region is laterally separated from the vertical drain contact region by a portion of the deep trench structure; and performing a thermal drive operation that heats the substrate to activate and diffuse the implanted dopants in the area defined for the vertically oriented drift region and the area defined for the drain contact region to form the vertically oriented drift region and the vertical drain contact region, respectively, so that the vertical drain contact region extends below a bottom of the deep trench structure, and so that the vertically oriented drift region makes electrical contact to the vertical drain contact region proximate to the bottom of the deep trench structure; and forming a body region having the first conductivity type disposed over the vertically oriented drift region.

12. The method of claim 11, further including forming an electrically conductive central member on the dielectric liner in the deep isolation trench.

13. The method of claim 12, wherein the electrically conductive central member comprises polysilicon, and wherein implanting dopants in the vertical drain contact region provides dopants

to the electrically conductive central member.

14. The method of claim 11, wherein the vertical drain contact region extends laterally under the vertically oriented drift region and abuts an adjacent portion of the vertical drain contact region.

15. The method of claim 11, wherein the vertical drain contact region is laterally surrounded by the deep trench structure, the deep trench structure having a closed loop configuration.

16. The method of claim 11, wherein the vertically oriented drift region is laterally surrounded by the deep trench structure, the deep trench structure having a closed loop configuration.

17. The method of claim 11, wherein the body region abuts the portion of the deep trench structure that abuts the vertical drain contact region opposite from the body region.

18. The method of claim 11, wherein the body region is laterally separated by dielectric material from the portion of the deep trench structure that abuts the vertical drain contact region opposite from the body region.

19. The method of claim 11, wherein the deep trench structure is 2.5 microns to 5 microns deep.

20. The method of claim 11, wherein: the first conductivity type is p-type; and the second conductivity type is n-type.

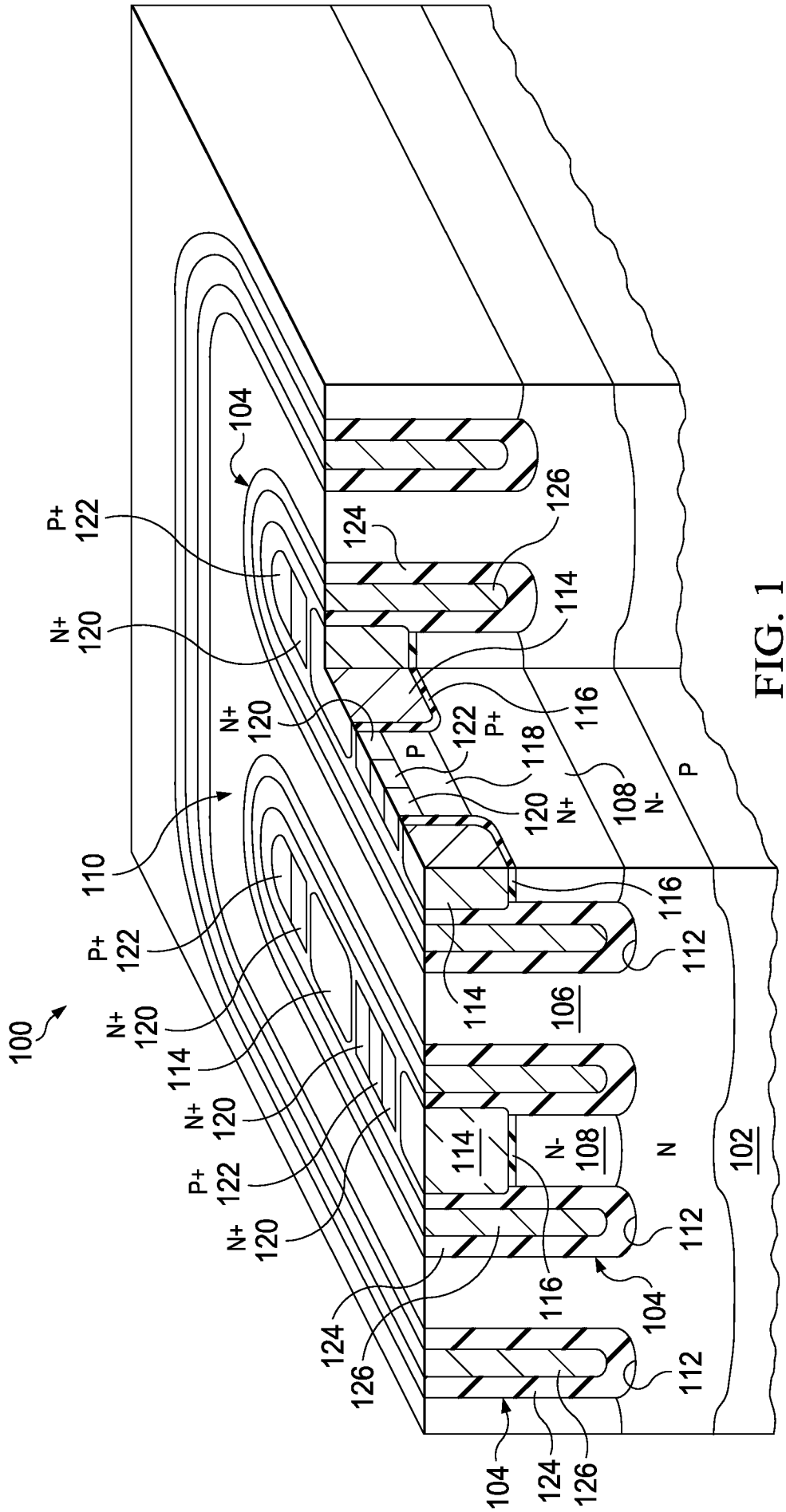

FIG. 1

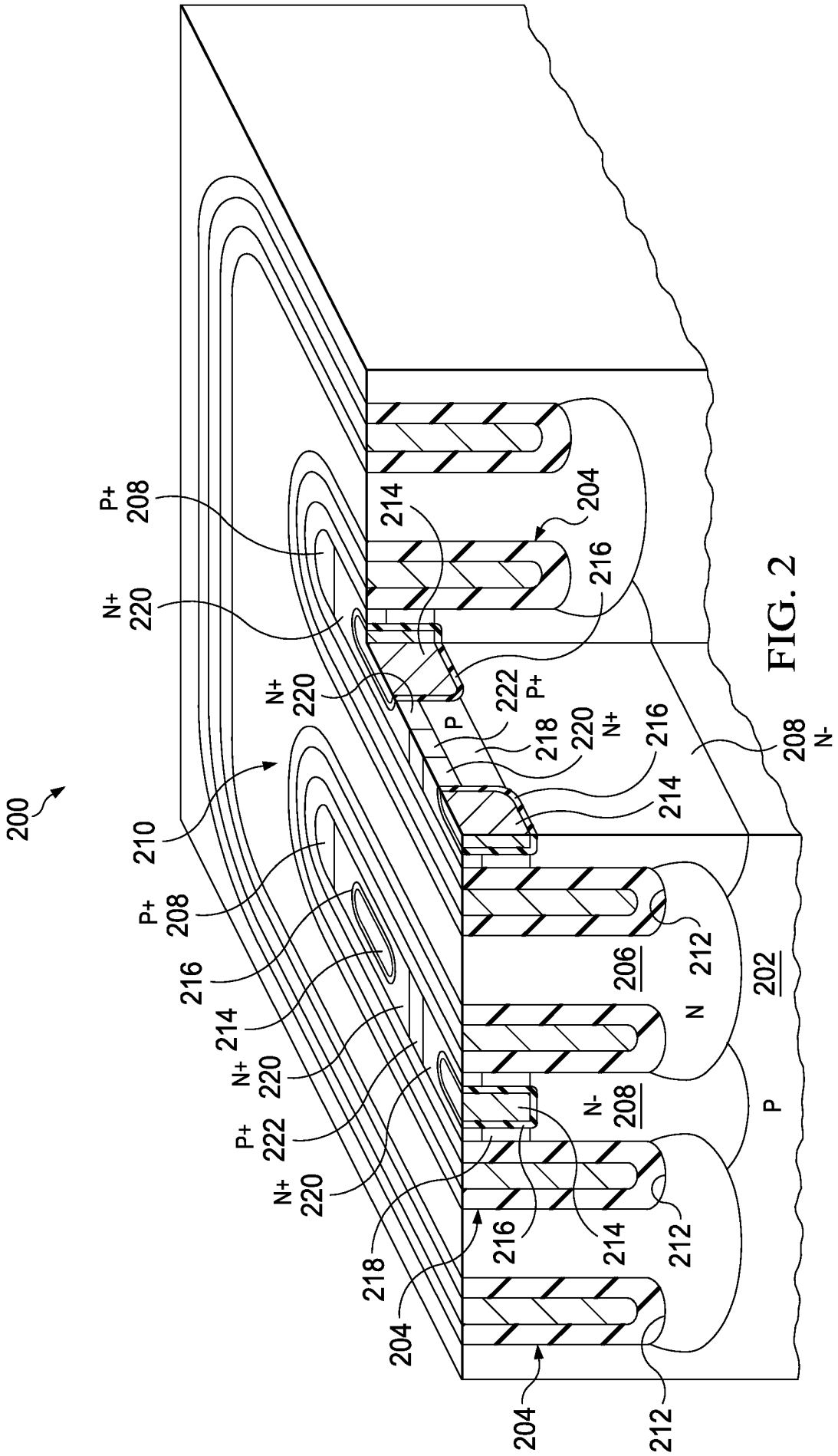
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FIG. 2

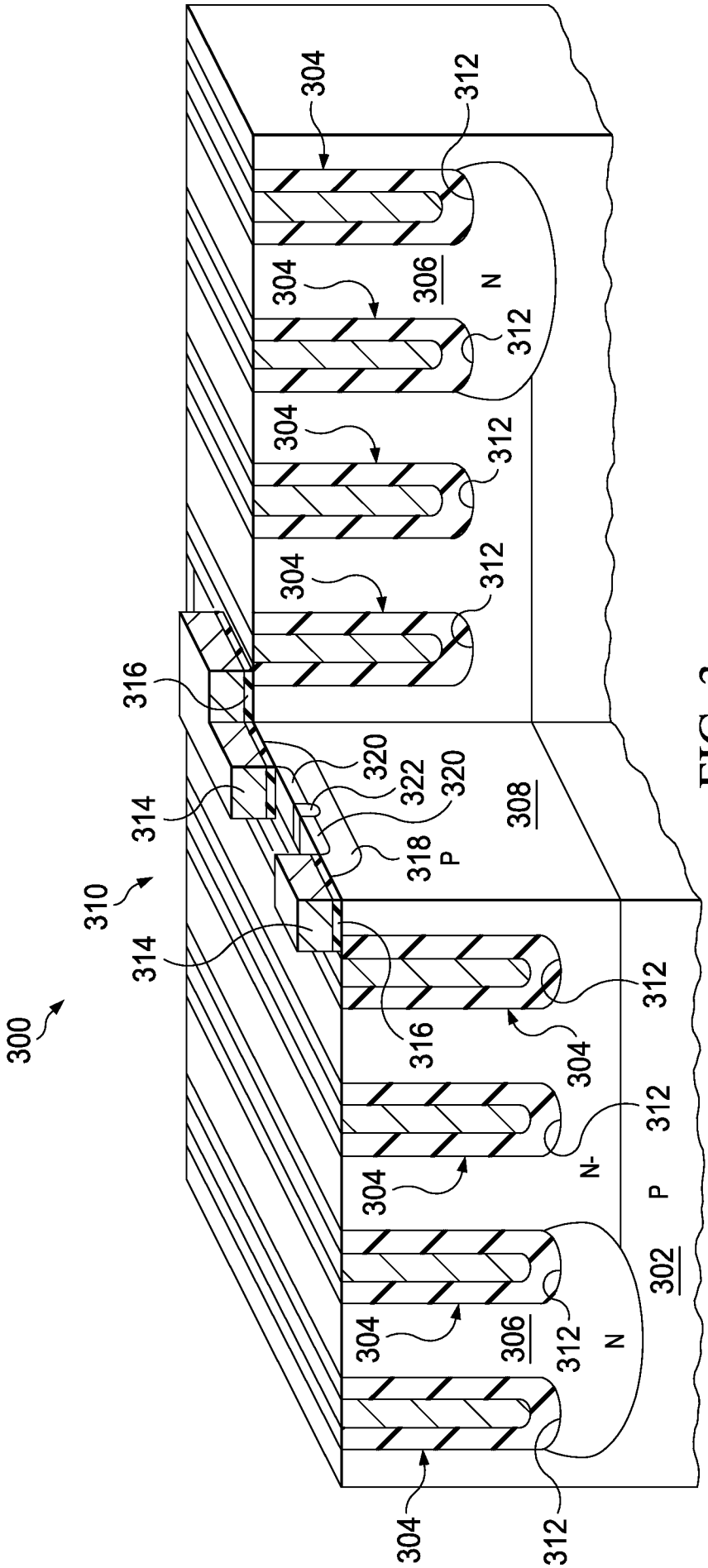


FIG. 3

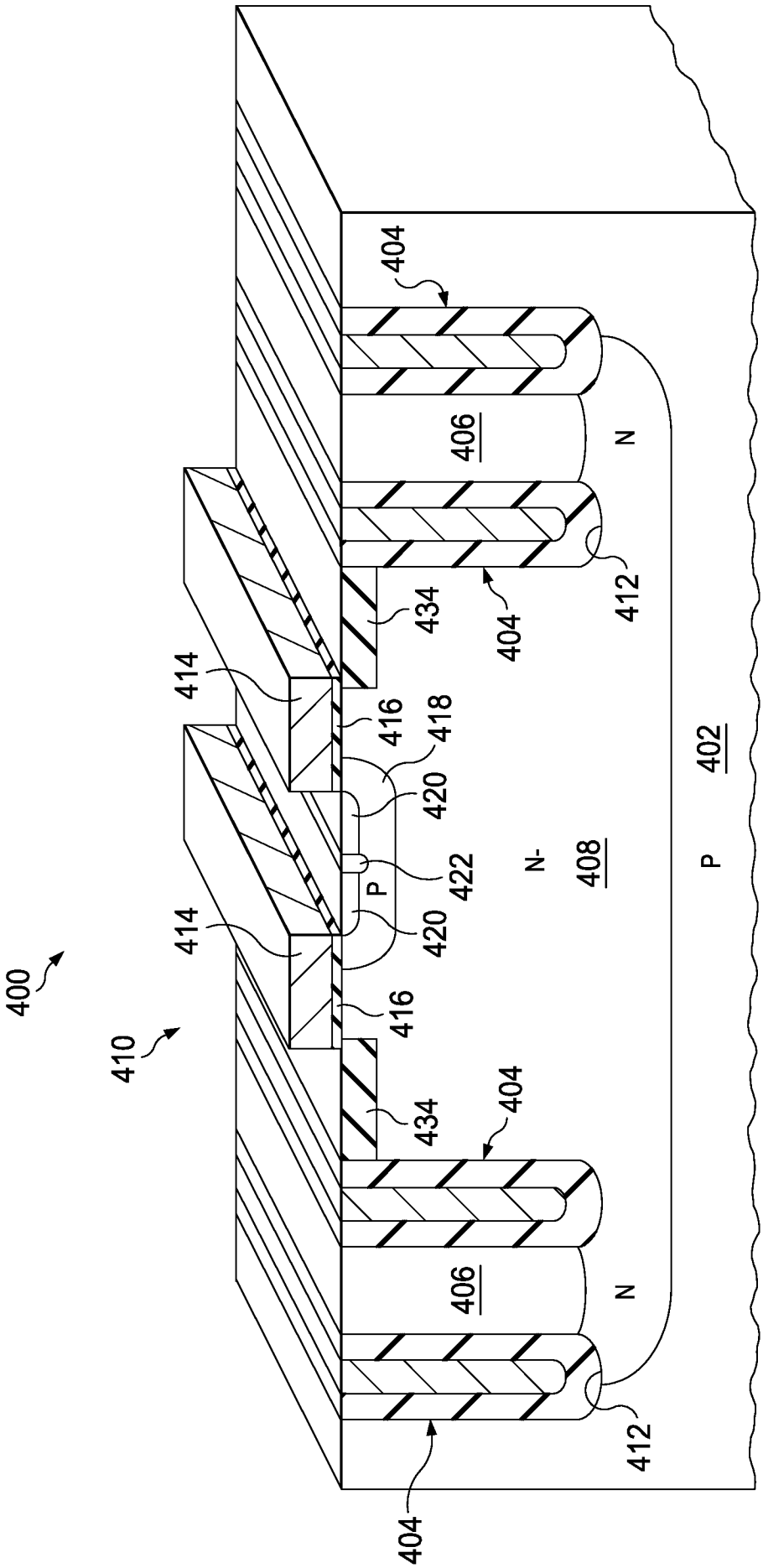


FIG. 4

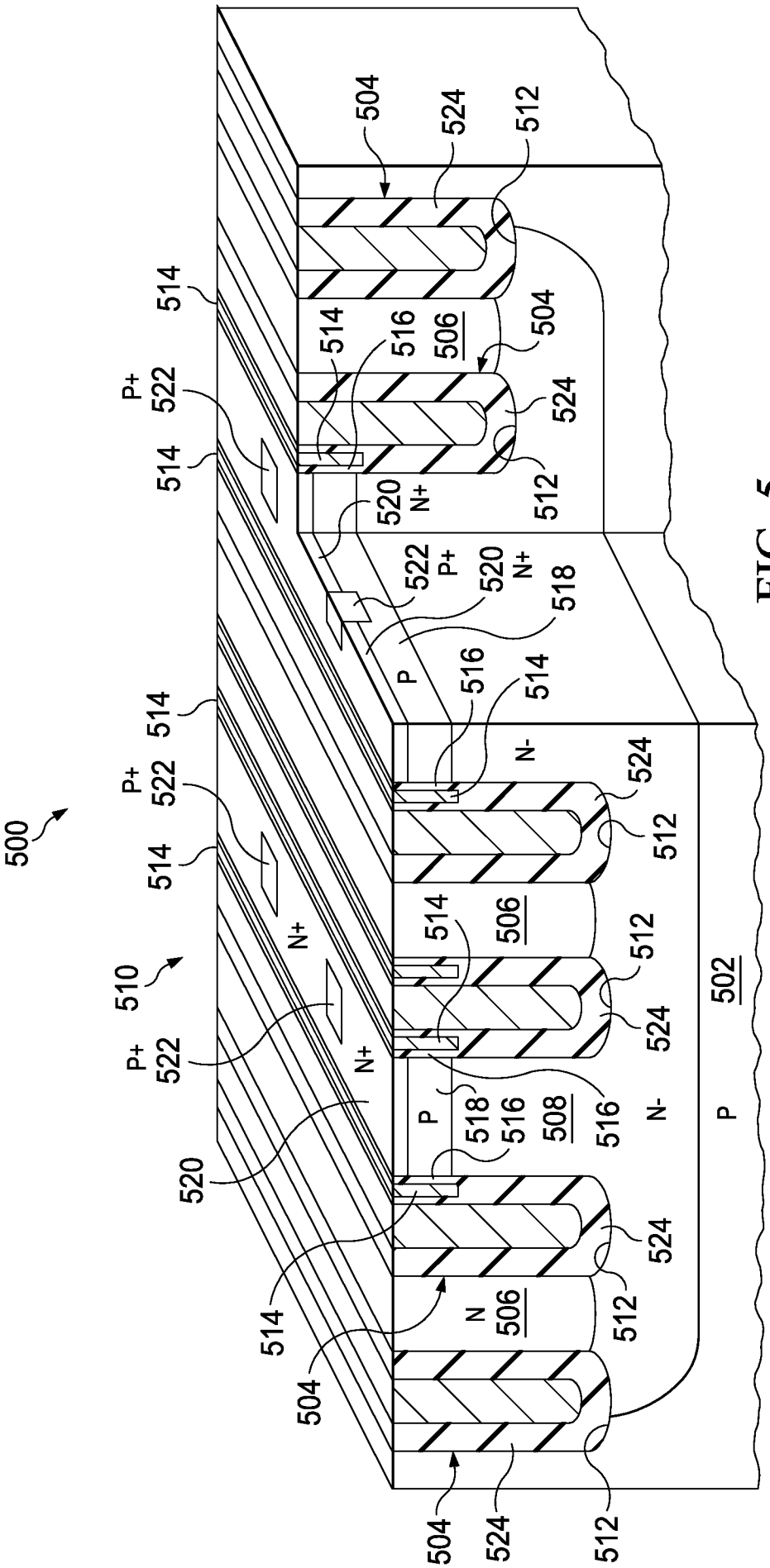


FIG. 5

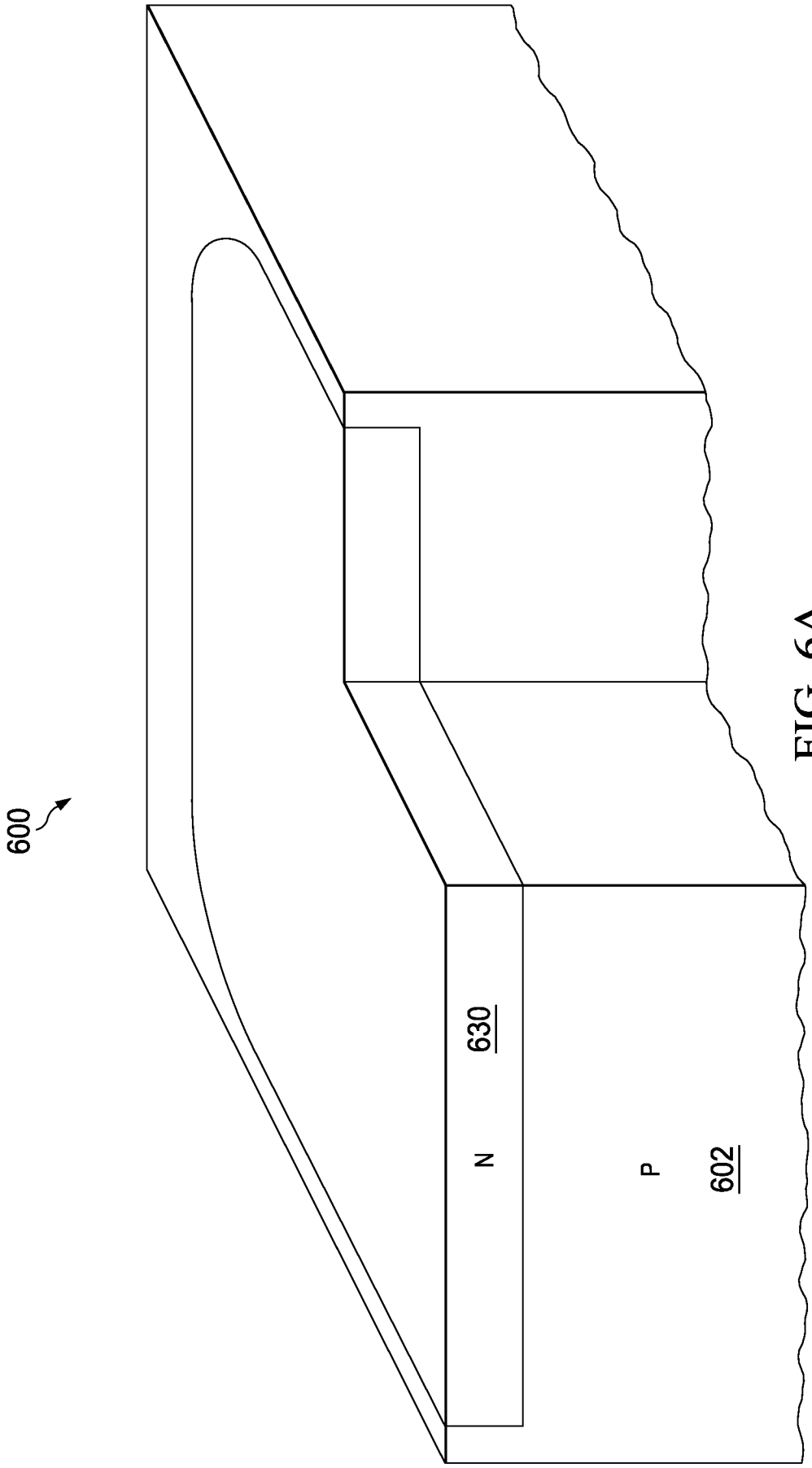


FIG. 6A

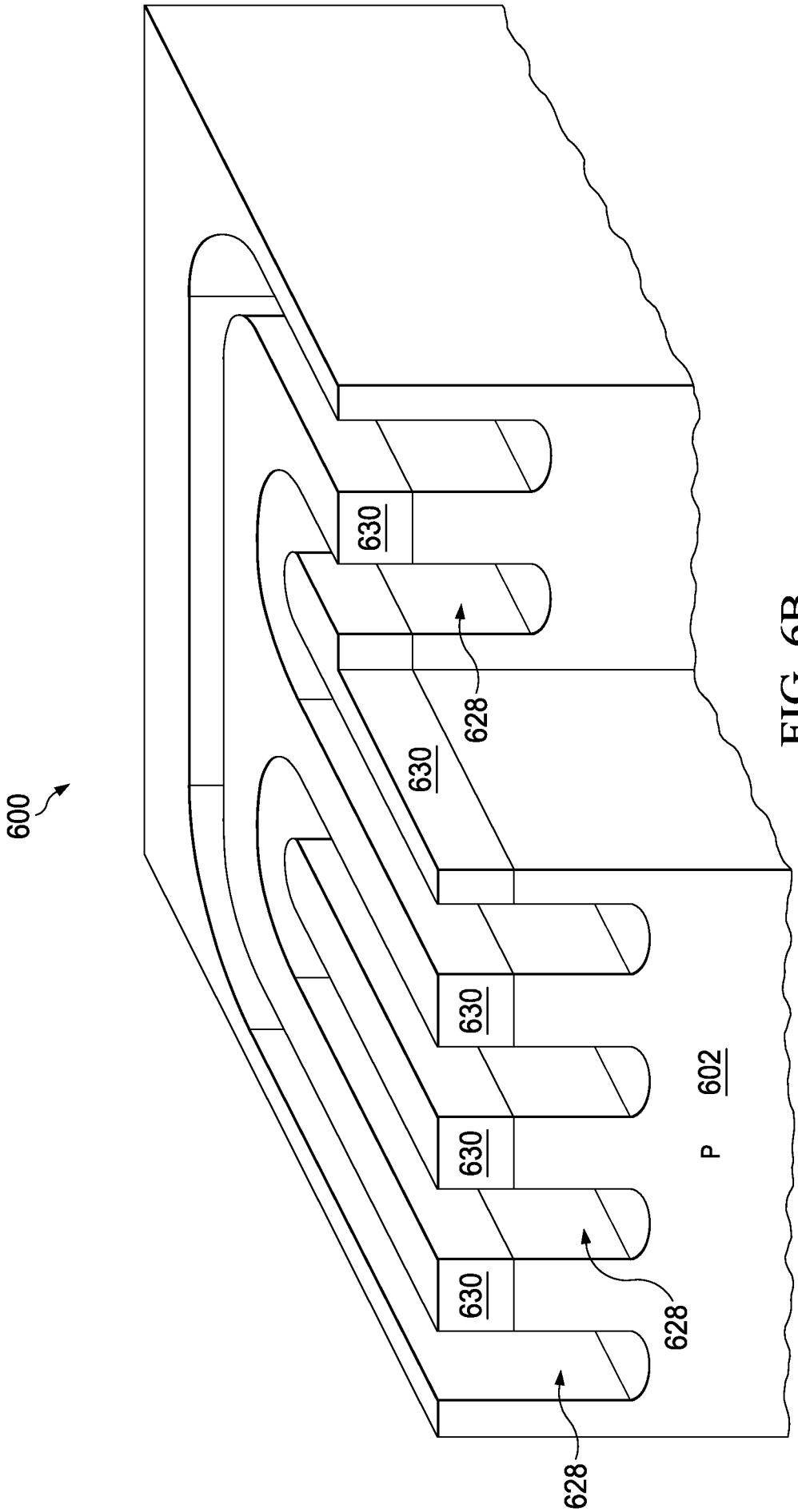
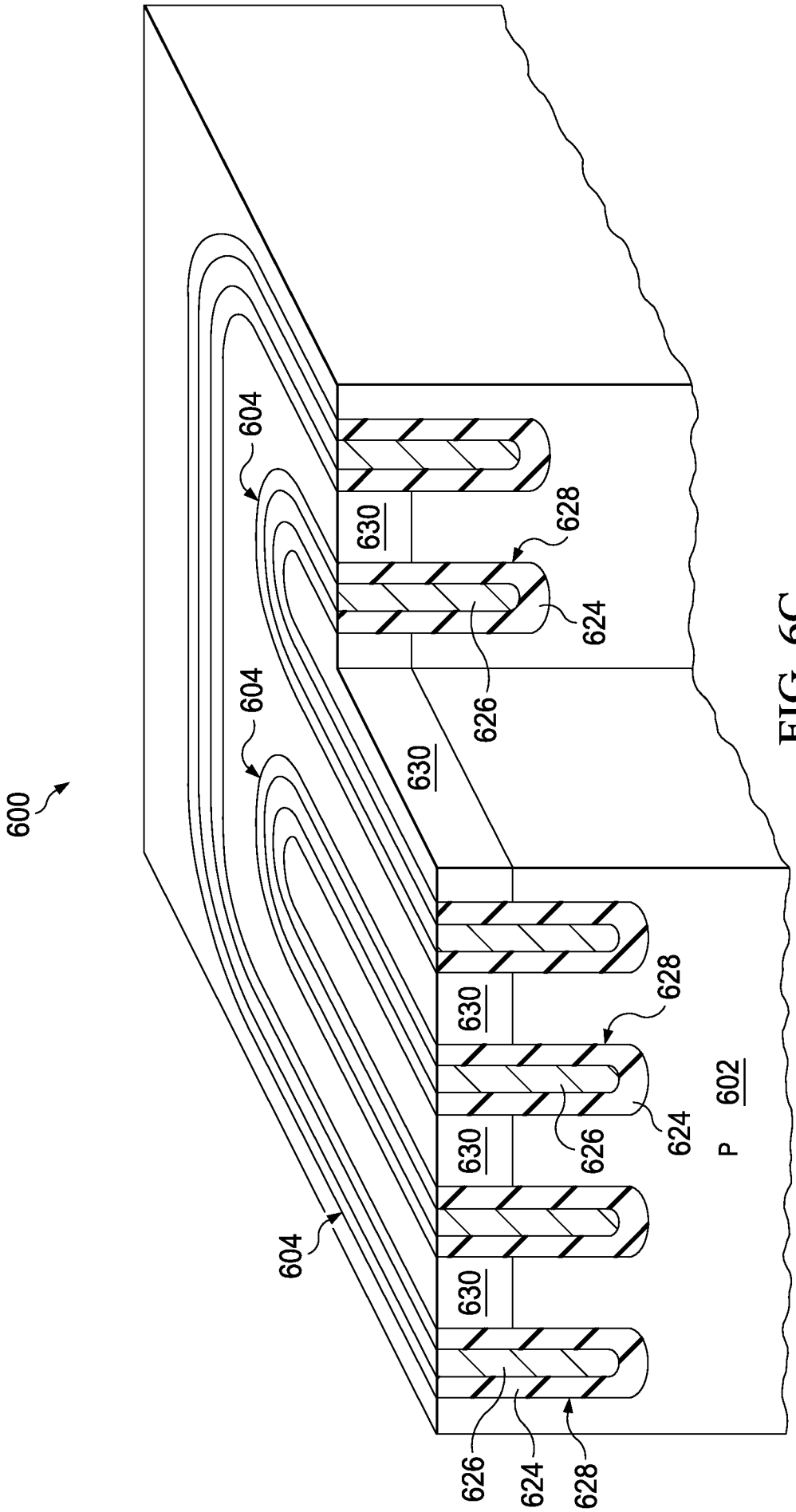


FIG. 6B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P 602

FIG. 6C

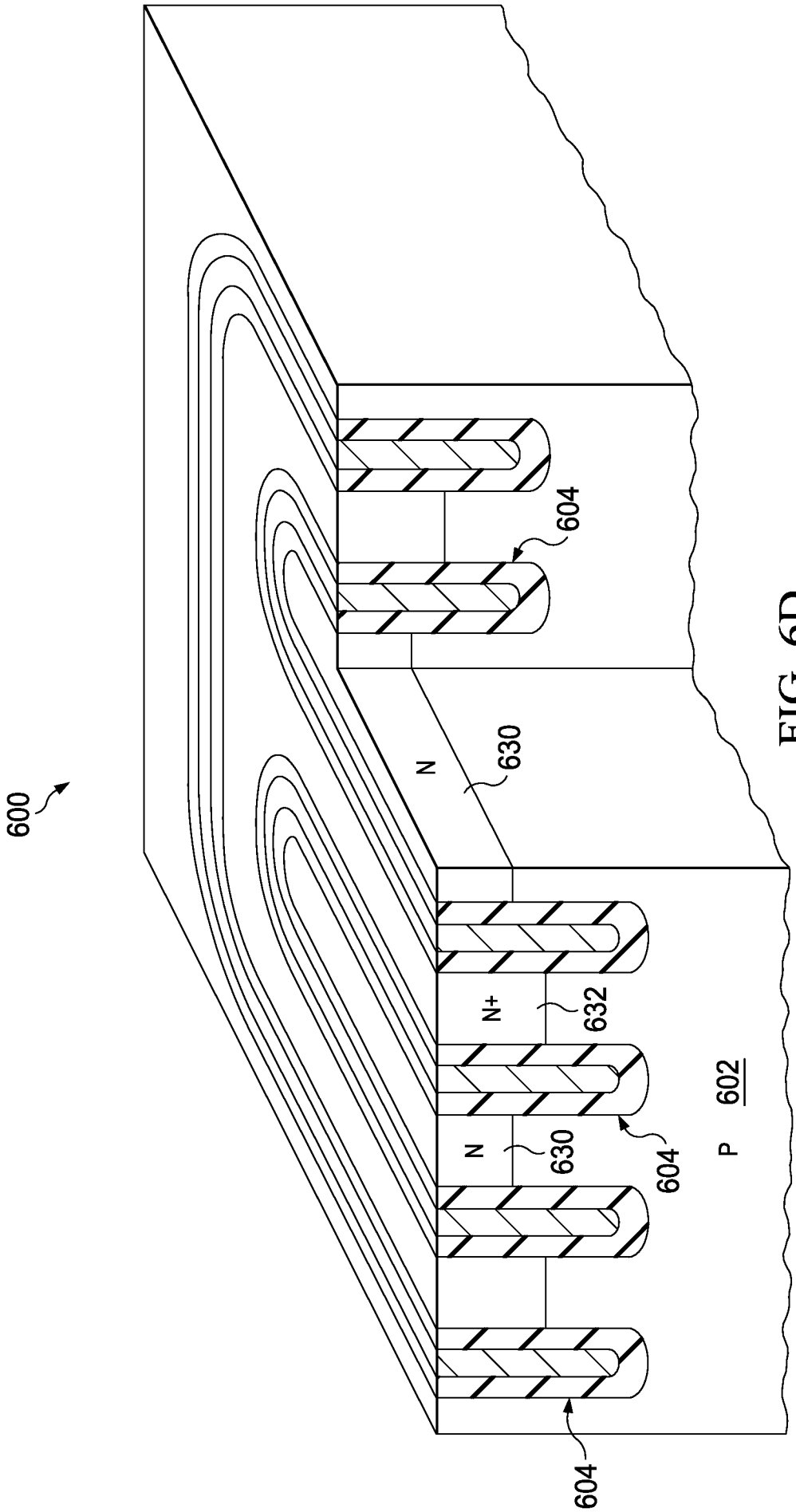

FIG. 6D

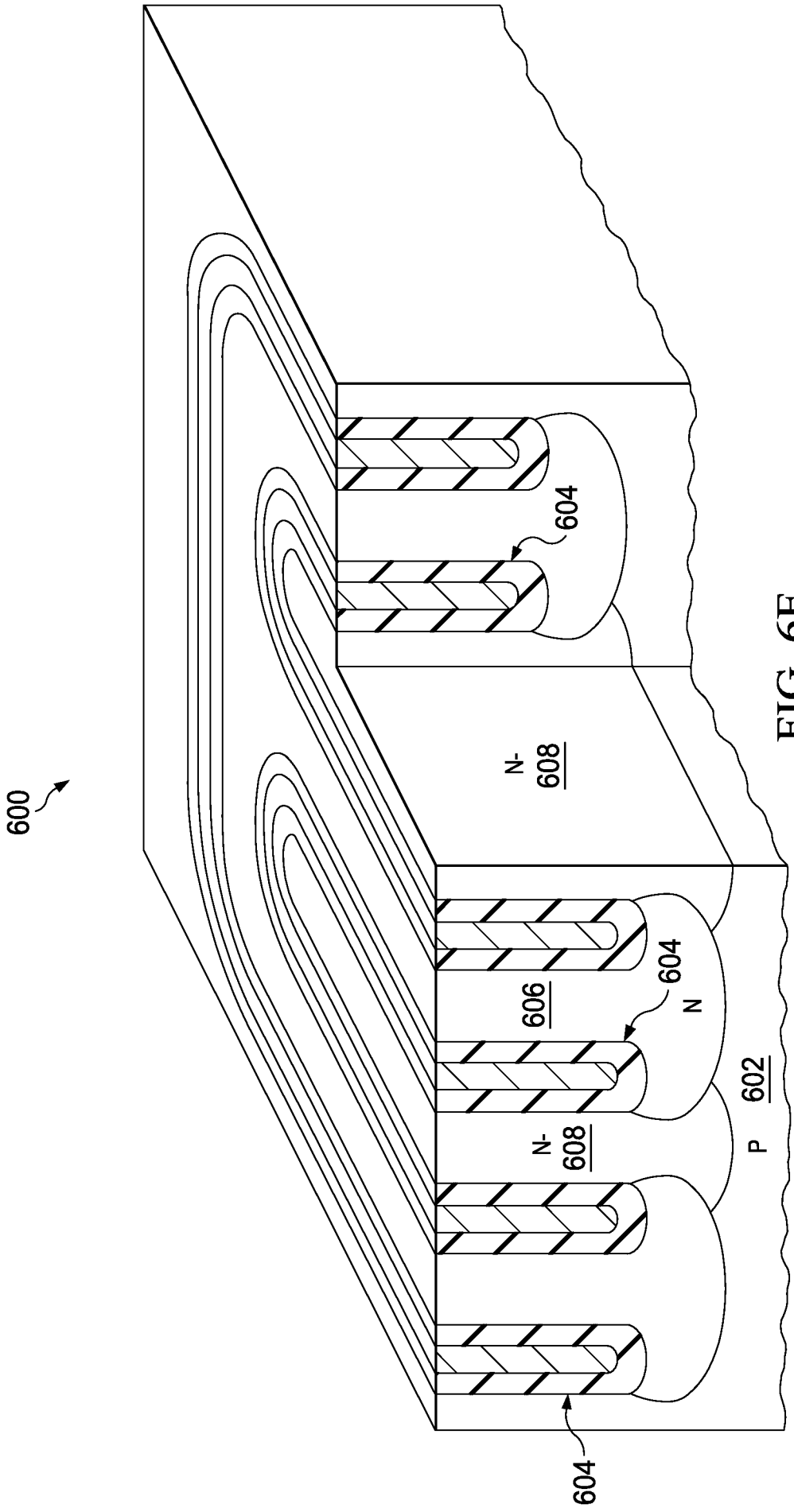

FIG. 6E

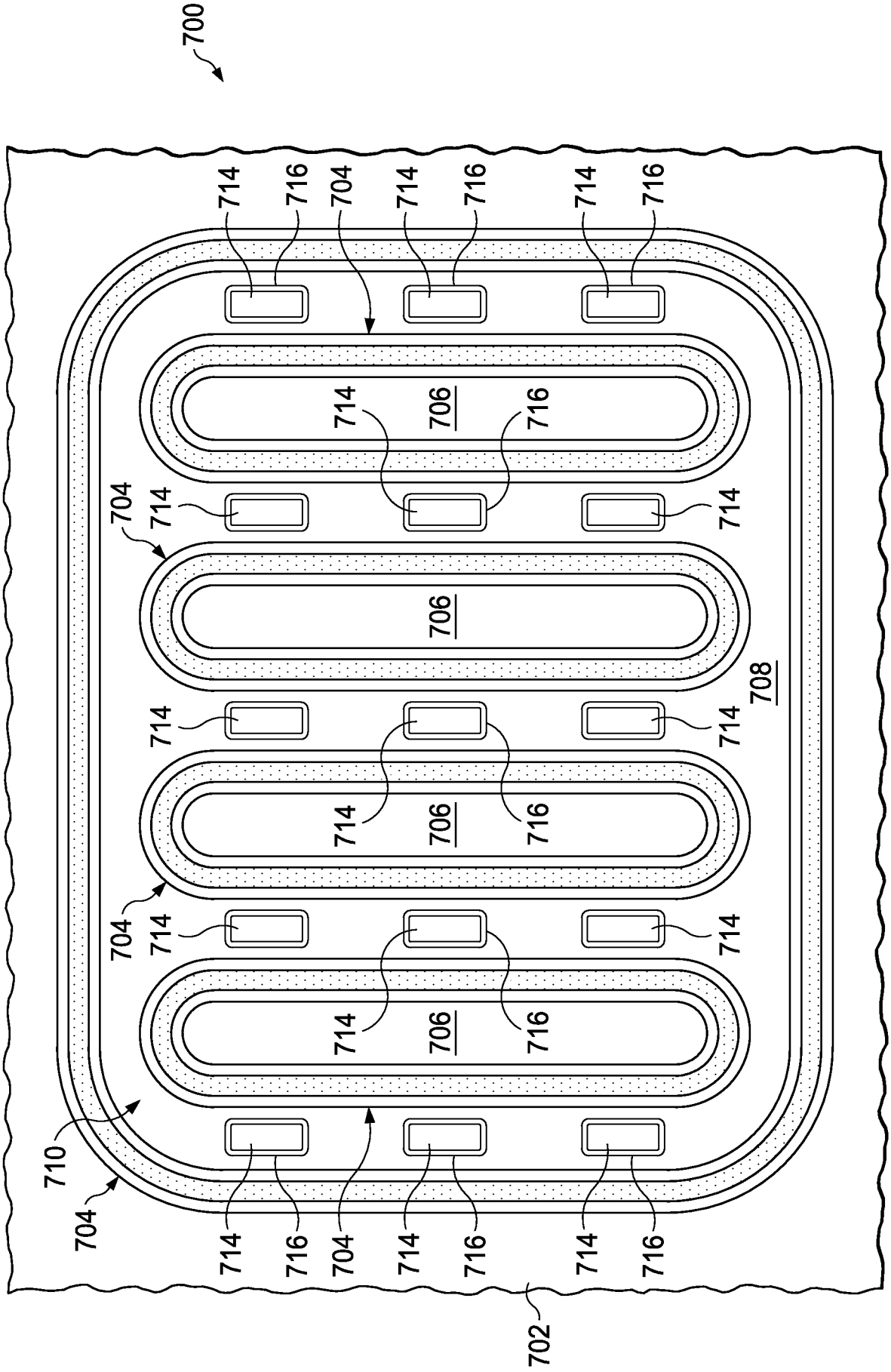

FIG. 7

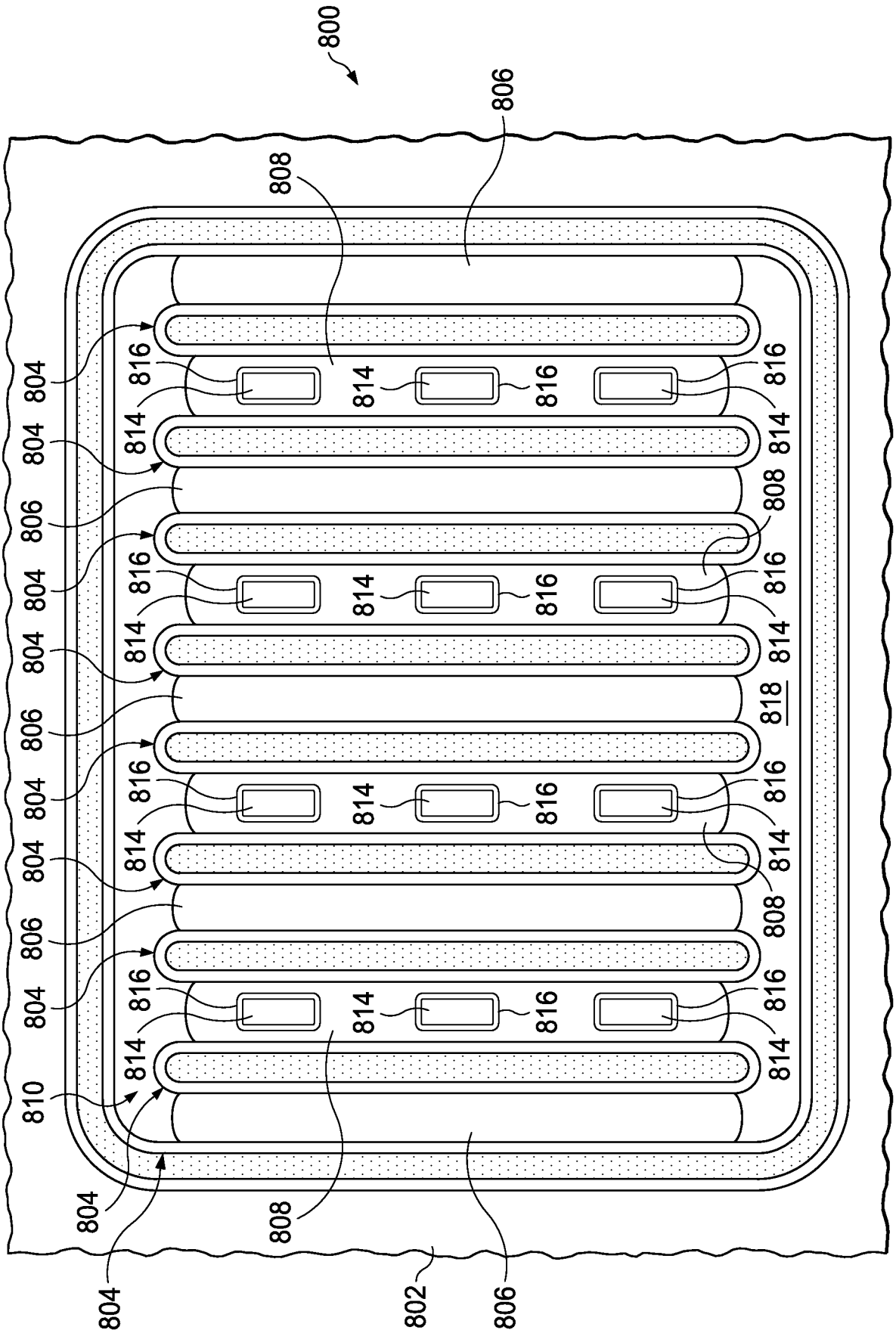

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2014/057790

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/088 *(2006.01)*
H01L 29/78 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/085, 27/088, 27/092, 27/098, 29/772, 29/775, 29/778, 29/78, 29/286, 29/792, 29/80, 29/808

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/0193502 A1 (TEXAS INSTRUMENTS INCORPORATED) 01.08.2013, abstract, par. [0018]-[0020], [0034], fig. 1A-1P	1-20
A	US 6593620 B1 (GENERAL SEMICONDUCTOR, INC.) 15.07.2003	1-20
A	RU 2230394 C1 (OAO "OKB "ISKRA") 10.06.2004	1-20
A	US 5365102 A (NORTH CAROLINA STATE UNIVERSITY) 15.11.1994	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 December 2014 (23.12.2014)	15 January 2015 (15.01.2015)

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