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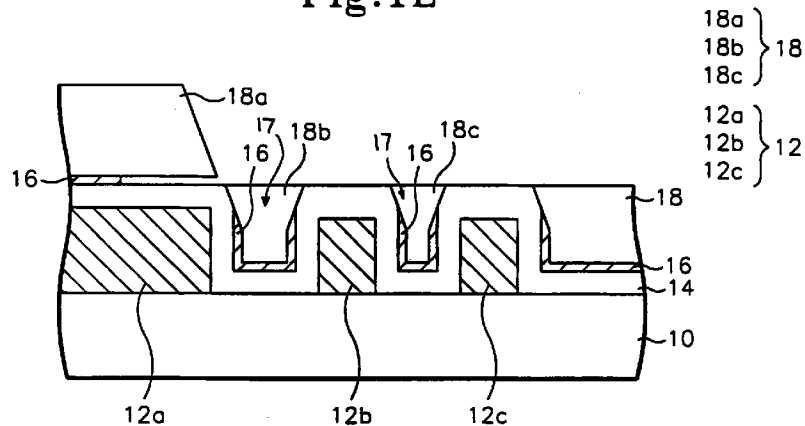
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(54) Planarising a semiconductor substrate

(57) A method for planarising a substrate 10, such as a semiconductor substrate, having an uneven topography uses different etch rates of insulating layers. First 14 and second 16 insulating layers are formed on an elevated region and a recessed region. Portions of the second insulating layer at an interface between the elevated region and the recessed region are removed, to isolate a portion of the second insulating layer within the recessed region from a portion of second insulating

layer overlying the elevated region. A third insulating layer 18 is formed on the resultant surface, and is partially removed from its upper surface until a part of the portion of second insulating layer overlying the elevated region is exposed. The portion of second insulating layer overlying the elevated region is removed, causing lift-off of corresponding portions 18a of the third insulating layer.

Fig.1E





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EUROPEAN SEARCH REPORT

Application Number  
EP 98 30 3917

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
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Place of search	Date of completion of the search	Examiner	
THE HAGUE	23 July 1999	Königstein, C	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		& : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT  
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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on  
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