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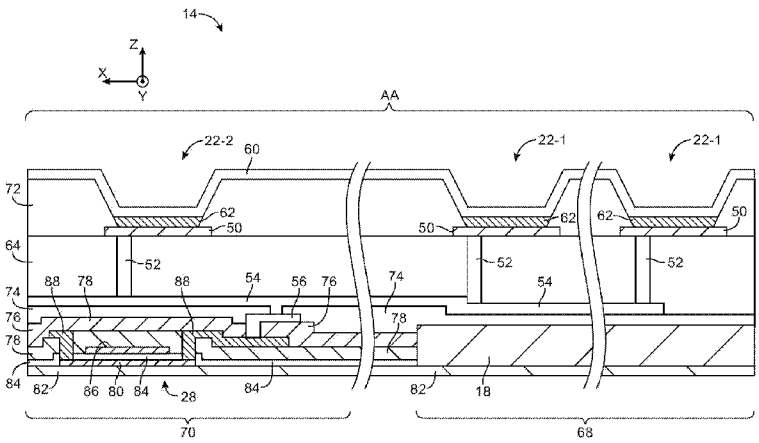

FIG. 7

(57) Abstract: An electronic device may be provided with a display. The display may be formed from an array of organic light-emitting diode display pixels (22-1, 22-2). Each display pixel may have an organic light-emitting diode having an anode (50) and a cathode (60) and may have an associated pixel circuit (70) for controlling the light-emitting diode. The anodes may be formed from patches of metal arranged in an array on the display. The display pixels may be controlled using data lines and gate lines. The gate lines may control thin-film transistors in the pixel circuits. Gate driver circuitry (18) along the left and right edges of the display may supply signals to the gate lines. The pixel circuits may be located in the center of the display between the gate driver circuitry. Some of the anodes (50 of pixel 22-2) may overlap the pixel circuits and some of the anodes (50 of pixels 22-1) may overlap the gate driver circuitry (18).

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Displays With Overlapping Light-Emitting Diodes and Gate Drivers

This application claims priority to U.S. Patent Application No. 14/262,363 filed on April 25, 2014, which is hereby incorporated by reference herein in its entirety.

Background

[0001] This relates generally to electronic devices and, more particularly, to electronic devices with displays that have thin-film transistor circuits and light-emitting diodes.

[0002] Electronic devices often include displays. For example, cellular telephones and portable computers include displays for presenting information to users.

[0003] Displays such as organic light-emitting diode displays have arrays of display pixels based on light-emitting diodes. In this type of display, each display pixel includes a light-emitting diode and thin-film transistors for controlling application of a signal to the light-emitting diode. The array of display pixels is used to present images to a user. Gate driver circuitry is located around the periphery of the display. The presence of the gate driver circuitry along the edges of the display can create undesirable inactive border regions in which no image light is emitted.

[0004] It would therefore be desirable to be able to provide improved electronic device displays such as displays with minimized border regions.

Summary

[0005] An electronic device may be provided with a display. The display may be formed from an array of organic light-emitting diode display pixels. Each display pixel may have an organic light-emitting diode having an anode and a cathode. An associated pixel circuit in each display pixel may be used to control the light-emitting diode of that display pixel.

[0006] The anodes may be formed from patches of metal arranged in an array on the display. A shared cathode may overlap the anodes. Patterned emissive layer material may be interposed between the anode and cathode of each light-emitting diode. When current flows between the anode and cathode of a light-emitting diode, light is produced for the display pixel contain the light-emitting diode.

[0007] The display pixels may be controlled using data lines and gate lines (scan lines). The gate lines may control thin-film transistors in the pixel circuits of the display pixels. Gate driver circuitry along the left and right edges of the display may supply signals to the gate lines. The gate driver circuitry may include a chain of shift register circuits and buffers that drive gate line signals from the shift register circuits onto corresponding gate lines.

[0008] The pixel circuits may be located in the center of the display and may be flanked on either side by gate driver circuitry running along opposing edges of the display. Some of the anodes in the display may overlap the pixel circuits in the center of the display and some of the anodes may overlap the gate driver circuitry. The use of anodes that overlap the gate driver circuitry allows display pixel structures near the edge of the display to emit light for forming display images, thereby reducing or eliminating inactive border regions in the display.

Brief Description of the Drawings

[0009] FIG. 1 is a perspective view of an illustrative electronic device in accordance with an embodiment.

[0010] FIG. 2 is a diagram of an illustrative display such as an organic light-emitting diode display having an array of organic light-emitting diode display pixels in accordance with an embodiment.

[0011] FIG. 3 is a diagram of an illustrative organic light-emitting diode display pixel in accordance with an embodiment.

[0012] FIG. 4 is a circuit diagram of illustrative gate driver circuitry for a display in accordance with an embodiment.

[0013] FIG. 5 is a diagram of an illustrative organic light-emitting diode display having display pixel structures that overlap gate driver circuitry to minimize inactive display borders in accordance with an embodiment.

[0014] FIG. 6 is a cross-sectional side view of an illustrative display showing how display pixel anodes may overlap gate driver circuitry in accordance with an embodiment.

[0015] FIG. 7 is a cross-sectional side view of an illustrative display showing how illustrative thin-film transistor circuitry and display pixel circuitry that may be used in a display in which display pixel anodes overlap gate driver circuitry in accordance with an embodiment.

[0016] FIG. 8 is a top view of an illustrative display showing how illustrative thin-film transistor circuitry and display pixel circuitry that may be used in a display in which display pixel anodes overlap gate driver circuitry in accordance with an embodiment.

Detailed Description

[0017] Electronic devices may be provided with displays having minimized inactive border regions. FIG. 1 is a perspective view of an illustrative electronic device of the type that may have a display with a minimized border. An electronic device such as electronic device 10 of FIG. 1 may be a computing device such as a laptop computer, a computer monitor containing an embedded computer, a tablet computer, a cellular telephone, a media player, or other handheld or portable electronic device, a smaller device such as a wrist-watch device, a pendant device, a headphone or earpiece device, or other wearable or miniature device, a television, a computer display that does not contain an embedded computer, a gaming device, a navigation device, an embedded system such as a system in which electronic equipment with a display is mounted in a kiosk or automobile, equipment that implements the functionality of two or more of these devices, or other electronic equipment. In the illustrative configuration of FIG. 1, device 10 is a portable device such as a cellular telephone, media player, tablet computer, or other portable computing device. Other configurations may be used for device 10 if desired. The example of FIG. 1 is merely illustrative.

[0018] In the example of FIG. 1, device 10 includes a display such as display 14. Display 14 has been mounted in a housing such as housing 12. Housing 12, which may sometimes be referred to as an enclosure or case, may be formed of plastic, glass, ceramics, fiber composites, metal (e.g., stainless steel, aluminum, etc.), other suitable materials, or a combination of any two or more of these materials. Housing 12 may be formed using a unibody configuration in which some or all of housing 12 is machined or molded as a single structure or may be formed using multiple structures (e.g., an internal frame structure, one or more structures that form exterior housing surfaces, etc.).

[0019] Display 14 may be a touch screen display that incorporates a layer of conductive capacitive touch sensor electrodes or other touch sensor components (e.g., resistive touch sensor components, acoustic touch sensor components, force-based touch sensor components, light-based touch sensor components, etc.) or may be a display that is not touch-sensitive. Capacitive touch screen electrodes may be formed from an array of indium tin oxide pads or other transparent conductive structures.

[0020] Display 14 may include an array of display pixels formed from an array of organic

light-emitting diode display pixels or display pixels based on other display technologies.

[0021] Display 14 may be protected using a display cover layer such as a layer of transparent glass or clear plastic. Openings may be formed in the display cover layer. For example, an opening may be formed in the display cover layer to accommodate a button such as button 13. An opening may also be formed in the display cover layer to accommodate ports such as speaker port 15.

[0022] Display 14 may contain an array of display pixels that display images for a user. The region of display 14 that contains the display pixels and that displays the images is sometimes referred to as the active area of the display. Active area AA of display 14 may be surrounded by a region such as inactive area IA that is free of display pixels and that does not emit light for displaying images. As shown in FIG. 1, active area AA may have a rectangular shape. At the upper and lower ends of device 10 of FIG. 1, inactive area IA may each have a dimension W2 that is sufficient to accommodate openings for speaker 15 and button 13 or other components. One the opposing left and right edges of display 14 and device 10, inactive area IA has a border width of W1. To improve device aesthetics and provide maximized area for displaying images for a user in a compact device, it may be desirable to minimize the magnitude of W1 (i.e., to make W1 equal to zero or to otherwise reduce the size of W1). This may be done by stacking display pixel structures such as display pixel anodes over display driver circuitry such as gate driver circuits running along the opposing left and right edges of display 14.

[0023] A circuit diagram of an illustrative display that may be configured to have minimized inactive borders is shown in FIG. 2. Display 14 may be formed from layers of material that have been deposited and patterned on a substrate. The substrate may be a rectangular layer such as a layer of glass, plastic, metal, or other materials.

[0024] Display 14 may have an array of display pixels 22 for displaying images for a user. The array of display pixels 22 may be formed from rows and columns of display pixel structures. There may be any suitable number of rows and columns in the array of display pixels 22 (e.g., ten or more, one hundred or more, or one thousand or more).

[0025] Display driver circuitry such as display driver integrated circuit 16 may be coupled to conductive paths such as metal traces on the display substrate using solder or conductive adhesive. Display driver integrated circuit 16 (sometimes referred to as a timing controller

chip) may contain communications circuitry for communicating with system control circuitry over path 25. Path 25 may be formed from traces on a flexible printed circuit or other cable. The control circuitry may be located on a main logic board in an electronic device such as a cellular telephone, computer, set-top box, media player, portable electronic device, or other electronic equipment in which display 14 is being used. During operation, the control circuitry may supply display driver integrated circuit 16 with information on images to be displayed on display 14. To display the images on display pixels 22, display driver integrated circuit 16 may supply corresponding image data to data lines D while issuing clock signals and other control signals to supporting thin-film transistor display driver circuitry such as gate driver circuitry 18 and demultiplexing circuitry 20.

[0026] Display driver circuitry such as demultiplexer circuitry 20 and gate line driver circuitry 18 may be formed from thin-film transistors on the display substrate. Thin-film transistors may also be used in forming pixel circuits in display pixels 22. The thin-film transistor circuitry in display 14 may, in general, be formed using any suitable type of thin-film transistors (e.g., silicon-based transistors such as low-temperature polysilicon thin-film transistors, semiconducting-oxide-based transistors such as amorphous indium gallium zinc oxide thin-film transistors, etc.).

[0027] Gate driver circuitry 18 may be formed on a display substrate (e.g., on the left and right edges of display 14, on only a single edge of display 14, or elsewhere in display 14). Demultiplexer circuitry 20 may be used to demultiplex data signals from display driver integrated circuit 16 onto a plurality of corresponding data lines D. With this illustrative arrangement of FIG. 1, data lines D run vertically through display 14. Each data line D is associated with a respective column of display pixels 22. Gate lines G run horizontally through display 14. Each gate line G is associated with a respective row of display pixels 22. Gate driver circuitry 18 may be located on the left side of display 14, on the right side of display 14, or on both the right and left sides of display 14, as shown in FIG. 2.

[0028] Gate driver circuitry 18 may assert gate signals (sometimes referred to as scan signals or transistor control signals) on the gate lines G in display 14. For example, gate driver circuitry 18 may receive clock signals and other control signals from display driver integrated circuit 16 and may, in response to the received signals, assert a gate signal on gate lines G in sequence, starting with the gate line signal G in the first row of display pixels 22.

As each gate line is asserted, the corresponding display pixels in the row in which the gate line is asserted will display the display data appearing on the data lines D. In display configurations with multiple scan lines per row, the control signals on the scan lines can be coordinated so that the transistors and other circuitry in the pixel circuit of the display pixels being controlled by the scan lines can perform threshold voltage compensation functions and other functions associated with operating display pixels 22. Other global and/or local control signals may be supplied to display pixels 22, if desired.

[0029] Each display pixel 22 in display 14 contains a respective organic light-emitting diode. A schematic diagram of an illustrative organic light-emitting diode display pixel 22 is shown in FIG. 3. As shown in FIG. 3, display pixel 22 may include light-emitting diode 26 controlled by a thin-film transistor-based pixel circuit PC. A positive power supply voltage ELVDD may be supplied to positive power supply terminal 34 and a ground power supply voltage ELVSS may be supplied to ground power supply terminal 36. Diode 26 may have an anode coupled to drive transistor 28 and a cathode coupled to ground power supply terminal 36. The state of drive transistor 28 in pixel circuit PC controls the amount of current flowing through diode 26 and therefore the amount of emitted light 40 from display pixel 22.

[0030] To ensure that transistor 28 is held in a desired state between successive frames of data, display pixel 22 may include a storage capacitor such as storage capacitor Cst. The voltage on storage capacitor Cst is applied to the gate of transistor 28 at node A to control transistor 28. Data can be loaded into storage capacitor Cst using one or more switching transistors such as switching transistor 30. When switching transistor 30 is off, data line D is isolated from storage capacitor Cst and the gate voltage on terminal A is equal to the data value stored in storage capacitor Cst (i.e., the data value from the previous frame of display data being displayed on display 14). When gate line G (sometimes referred to as a scan line) in the row associated with display pixel 22 is asserted, switching transistor 30 will be turned on and a new data signal on data line D will be loaded into storage capacitor Cst. The new signal on capacitor Cst is applied to the gate of transistor 28 at node A, thereby adjusting the state of transistor 28 and adjusting the corresponding amount of light 40 that is emitted by light-emitting diode 26.

[0031] If desired, display pixel circuits for display pixels 22 of display 14 may be implemented using different numbers of switching transistors, different numbers of storage

capacitors, different numbers of control lines, and other different types of display pixel circuit architectures. The circuitry of illustrative display pixel circuit PC of display pixel 22 in FIG. 3 is merely an example.

[0032] Illustrative gate driver circuitry 18 for display 14 is shown in FIG. 4. As shown in FIG. 4, gate driver circuitry 18 may include a chain of shift register circuits 42. At the output of each shift register circuit, a respective gate line buffer 44 may be used to drive a corresponding gate line signal (scan line signal) onto a corresponding gate line G. In displays having multiple scan lines per row of display pixels 22, there may be multiple gate lines (scan lines) G and corresponding buffers 44 at the output of each shift register circuitry in each row. The example of FIG. 4 is merely illustrative.

[0033] To minimize the sizes of the left and right borders of display 14, some of structures in display pixels 22 of active area AA may overlap gate driver circuitry 18. As shown in FIG. 5, for example, gate driver circuitry 18 may be arranged along the left edge of display 14 (as an example). Gate driver circuitry 18 of FIG. 5 may contain shift register circuits 42 and buffers 44 of the type shown in FIG. 4. Active area AA of display 14 may include an array of display pixels 22. Display pixels 22 may be organized in a rectangular array having rows and columns. Some display pixel structures such as the anodes and pixel circuits in display pixels 22-2 may lie in the center of display 14 and may not overlap any of gate driver circuitry 18. Other display pixel structures such as the anodes of display pixels 22-1 may fully or partly overlap gate driver circuitry 18. Because the anodes of display pixels 22-1 form part of light-emitting diodes 26 for display pixels 22-1, the anodes of display pixels 22-1 that overlap gate driver circuitry 18 can emit light for forming part of an image. There may therefore be little or no inactive area IA along the left (or right) edges of display 14.

[0034] FIG. 6 is a cross-sectional side view of display 14 showing illustrative layers of metal and metal via structures that may be used in forming a display having a layout of the type shown in FIG. 5. As shown in FIG. 6, a portion of display (e.g., the portion extending from X=0 to X=X1 in FIG. 6) may contain gate driver circuitry 18. Another portion of the display (e.g., the portion extending from X=X1 to X=X2) may contain display pixel circuits PC. Display pixel circuits PC may contain thin-film transistors, capacitor structures for storage capacitor Cst, and other circuitry for display pixels 22 (see, e.g., display pixel circuit PC of FIG. 3). Pixel circuits PC may be coupled to respective light-emitting diodes 26. Each

light-emitting diode may have a respective anode 50. A shared cathode may be used for the light-emitting diodes of display 14. Light 40 (FIG. 3) is emitted by emissive material that is sandwiched between anodes 50 and the cathode.

[0035] Anodes 50 that are near the edge of display 14 (i.e., anodes running along the left and/or right edge of display 14 that are associated with display pixels 22-1) overlap gate driver circuitry 18. Anodes 50 that are located nearer the center of display 14 (i.e., anodes associated with display pixels 22-2 of FIG. 6) do not overlap any of gate driver circuitry 18, but rather only overlap pixel circuits PC.

[0036] As shown in FIG. 6, display 14 may be formed from patterned metal and vias layers. In addition to the layers used in forming gate driver circuitry 18 and pixel circuits PC (e.g., metal layers such as a first metal layer M1 that forms thin-film transistor gates and a second metal layer M2 that forms thin-film transistor source-drain electrodes), these layers of display 14 may include a third metal layer M3 for forming conductive paths 56, a fourth metal layer M4 for forming conductive paths 54, a via layer VIA for forming vias 52, and a metal layer for forming anodes 50. Paths 56 are used to couple pixel circuits PC to respective horizontal lines 54. Vias 52 are used in coupling respective anodes 50 to lines 54.

[0037] Pixel circuits PC may be arranged in a rectangular area in the center of display 14 and may be flanked by gate driver circuits 18 on opposing edges of display 14. The spacing between pixel circuits PC is preferably constant (fixed) across the surface of display 14. As shown in FIG. 6, for example, pixel circuits PC may have a fixed pitch (pixel-circuit-to-pixel-circuit spacing) of P. Anodes 50 likewise have a fixed pitch (anode-to-anode spacing) as shown by fixed anode separation PB. Anodes 50 are spread out across the entire width (or nearly the entire width) of display 14 to minimize inactive border IA, whereas pixel circuits PC are inset slightly from the edges of display 14 to accommodate gate driver circuitry 18 along the left and right edges of the display substrate. Anode pitch PB is therefore greater than pixel circuit pitch P.

[0038] Because anodes 50 are spaced apart by a value PB that is greater than the spacing P between pixel circuits PC, the lengths of horizontal lines 54 in metal layer M4 vary across as a function of lateral distance X across the width of display 14. As shown in FIG. 6, for example, the leftmost line segment 54 has a length D1, the next-to-leftmost line segment 54 has a length D2 that is less than D1, and successive line segments 54 have progressively

decreasing lengths at locations approaching the center of display 14 (see, e.g., line segment length D3, which is less than line segment length D2). By continuously varying the lengths of the horizontal connecting lines between pixel circuits PC and respective anodes 50, an array of pixel circuits PC in the center of display 14 that have a smaller pitch P can be coupled to an array of anodes 50 that cover the entire display 14 with a larger pitch PB. There may be a small inactive peripheral area IA of gate driver circuitry 18 that is not covered by display pixel anodes 50 or all of gate driver circuitry 18 may be covered with display pixel anodes 50. In either case, inactive border width W1 is minimized due to the overlap of anodes 50 and gate driver circuitry 18.

[0039] FIG. 7 is a cross-sectional side view of illustrative structures that may be used in forming a display with gate driver circuitry that is overlapped by anodes 50 of active area AA. The right edge portion of display 14 is shown in FIG. 7. The left edge of display 14 may be formed using the same structures.

[0040] As shown in FIG. 7, display pixels 22-1 and 22-2 may have respective anodes 50 each of which is overlapped by a respective emissive layer structure 62. Each display pixel may include a portion of a shared cathode (layer 60) and a respective anode 50. The emissive material 62 of each display pixel emits light when current is passed between cathode 60 and the anode 50 in that display pixel. Display pixels 22-2 have anodes 50 that do not overlap gate driver circuitry 18. Display pixels 22-1 are formed from anodes 50 that overlap gate driver circuitry 18.

[0041] Vias 52 may be formed from a metal or other conductive material that passes through dielectric layer 64. Dielectric layer 64 may be an organic planarization layer (e.g., a polymer layer). Pixel definition layer 66 may define the positions of emissive material areas 62 and may be formed from a dielectric such as polyimide or other polymer. Cathode layer 60 may be formed from a conductive layer such as a layer of transparent conductive material (e.g., indium tin oxide and a thin layer of metal such as a 100 angstrom silver layer).

[0042] A metal layer (e.g., a fourth metal layer) may be used to form lines 54, as described in connection with FIG. 6. The metal layer for forming paths 54 may be formed on top of passivation layers 74 and 76 (e.g., layers of silicon oxide and/or silicon nitride). Interlayer dielectric layers (e.g., silicon oxide and/or nitride layers) such as layer 78 may be formed under passivation layer 76.

[0043] Gate driver circuitry 18 may be formed from thin-film transistor circuitry on substrate 82. Pixel circuits PC (see, e.g., circuitry 70) may be also be formed on substrate 82. Pixel circuits PC may include transistors such as thin-film transistor 28. Transistor 28 may be a drive transistor for driving a light-emitting diode 26 that is formed from a respective anode 50, emissive layer 62, and portion of cathode 60). As shown in FIG. 7, transistor 28 includes a semiconducting channel formed from semiconductor layer 80. Layers such as layer 80 may be formed from silicon (e.g., polysilicon), may be formed from a semiconducting oxide such as indium gallium zinc oxide, or may be formed from other semiconductors.

[0044] Layer 80 and the other thin-film transistor circuitry of FIG. 7 may be formed on substrate 82. Substrate 82 may include one or more layers of glass, polymer (e.g., polyimide), metal, ceramic, or other materials.

[0045] Gate insulator layer 84 may be formed from silicon oxide or other dielectric material and may cover semiconductor channel layers such as channel layer 86 in thin-film transistors such as transistor 28. A patterned metal layer (e.g., a second metal layer sometimes referred to as M2 or a source-drain metal layer) may be used in forming source-drain electrodes 88 for transistors such as transistor 28. Each thin-film transistor may have a gate electrode such as gate electrode 86 of transistor 28. Gate electrode 86 may be formed from metal (e.g., a first metal layer) on gate insulator layer 84. As shown in FIG. 7, each gate 86 overlaps a respective channel region 80 and lies between respective source-drain electrodes 88. During operation, the drive transistor 28 of each pixel circuit PC supplies drive current to a corresponding anode 50 and the associated light-emitting diode 26 that is formed from that anode. This causes the display pixel 22 that includes that light-emitting diode to emit light 40 (FIG. 3). Paths such as horizontal paths 54 may be used to distribute the drive current from thin-film transistors such as transistor 28 of FIG. 7 to associated anodes 50 (e.g., anodes 50 overlapping display driver circuitry 18 and anodes 50 that overlap pixel circuits PC).

[0046] FIG. 8 is a top view of an illustrative scheme in which pixel circuits PC have been laterally interconnected with display pixels using horizontal paths 54. Pixels 22 may include subpixels with differently colored emissive layers 64 (e.g., red layers R, blue layers B, and green layers G). Layers 64 may overlap respective anodes 50. The anodes 50 of pixels 22 may be laterally spaced from the pixel circuits PC that are controlling pixels 22 (e.g., to allow

some anodes 50 to be stacked above gate driver circuitry 18). Horizontal paths 54 may convey signals between pixel circuits PC (e.g., pixel circuits for respectively controlling blue, red, and green subpixels) and associated anodes 50 in display pixels 22.

[0047] In accordance with an embodiment, an organic light-emitting diode display is provided that includes a substrate, pixel circuits on the substrate, gate driver circuitry along at least one edge of the substrate, and an array of display pixels, the display pixels include anodes that overlap the gate driver circuitry and anodes that overlap the pixel circuits.

[0048] In accordance with another embodiment, the organic light-emitting diode display includes a shared cathode layer that overlaps all of the anodes.

[0049] In accordance with another embodiment, the organic light-emitting diode display includes emissive material between the shared cathode layer and each anode.

[0050] In accordance with another embodiment, the pixel circuits have a pixel-circuit-to-pixel-circuit spacing and the anodes have an anode-to-anode spacing that is larger than the pixel-circuit-to-pixel-circuit spacing.

[0051] In accordance with another embodiment, the organic light-emitting diode display includes horizontal lines that couple some of the pixel circuits to the anodes that overlap the gate driver circuitry.

[0052] In accordance with another embodiment, the organic light-emitting diode display includes a first metal layer, a third metal layer, and a second metal layer between the first and third metal layers, the horizontal lines are formed from the third metal layer.

[0053] In accordance with another embodiment, the gate driver circuitry includes shift register circuits.

[0054] In accordance with another embodiment, the organic light-emitting diode display includes an organic planarization layer interposed between the gate driver circuitry the anodes that overlap the gate driver circuitry.

[0055] In accordance with another embodiment, the pixel circuits and gate driver circuitry include thin-film transistors formed from a semiconductor layer selected from the group consisting of: a silicon layer and semiconducting oxide layer.

[0056] In accordance with another embodiment, the thin-film transistors include gates that overlap the semiconductor layer.

[0057] In accordance with another embodiment, the organic light-emitting diode display

include a first metal layer that forms the gates, a second metal layer that forms source-drain electrodes for the thin-film transistors, a fourth metal layer that forms lateral signal paths between the pixel circuits and the anodes that overlap the gate driver circuitry, and a third metal layer between the second metal layer and the fourth metal layer.

[0058] In accordance with another embodiment, the organic light-emitting diode display includes horizontal metal lines that couple the pixel circuits to the anodes that overlap the gate driver circuitry.

[0059] In accordance with another embodiment, the gate driver circuitry includes shift register circuitry and buffer circuits.

[0060] In accordance with another embodiment, the organic light-emitting diode display includes data lines and gate lines, each buffer circuit provides a signal to a respective one of the gate lines.

[0061] In accordance with an embodiment, an organic light-emitting diode display is provided that includes a rectangular substrate having four edges including left and right edges, a left-hand gate driver circuit located along the left edge, a right-hand gate driver circuit located along the right edge, and an array of display pixels each having a light-emitting diode with an anode and a cathode and each having a pixel circuit that controls current through the light-emitting diode of that display pixel, some of the anodes are located between the left-hand gate driver circuit and the right-hand gate driver circuit overlapping the pixel circuits, some of the anodes overlap the left-hand gate driver circuit, and some of the anodes overlap the right-hand gate driver circuit.

[0062] In accordance with another embodiment, the left-hand gate driver circuit and the right-hand gate driver circuit include shift register circuits and buffers.

[0063] In accordance with another embodiment, the buffers provide control signals to horizontal lines extending across the rectangular substrate between the left to the right edges.

[0064] In accordance with another embodiment, the organic light-emitting diode display includes emissive material on each anode, the cathodes are formed from a shared cathode layer that overlaps the anodes that overlap the left-hand gate driver circuit, the anodes that overlap the right-hand gate driver circuit, and the anodes overlapping the pixel circuits between the left-hand gate driver circuit and the right-hand gate driver circuit.

[0065] In accordance with an embodiment, an organic light-emitting diode display is

provided that includes gate driver circuitry formed from a chain of shift register circuits, and an array of display pixels to display images, each display pixel includes a light-emitting diode having a cathode, an anode, and emissive material that emits light, each display pixel receives a signal from the gate driver circuitry, and some of the anodes overlap the chain of shift register circuits.

[0066] In accordance with another embodiment, each of the display pixels has a pixel circuit that controls emission of the light from the light-emitting diode of that display pixel, some of the anodes overlap the pixel circuits, the pixel circuits are located between a first portion of the gate driver circuitry on a first edge of the display and a second portion of the gate driver circuitry on an opposing second edge of the display, and the pixel circuit of each display pixel includes a thin-film drive transistor having a source-drain terminal coupled to the anode of the light-emitting diode for that display pixel.

[0067] The foregoing is merely illustrative and various modifications can be made by those skilled in the art without departing from the scope and spirit of the described embodiments. The foregoing embodiments may be implemented individually or in any combination.

Claims

What is claimed is:

1. An organic light-emitting diode display, comprising:
a substrate;
pixel circuits on the substrate;
gate driver circuitry along at least one edge of the substrate; and
an array of display pixels, wherein the display pixels include anodes that overlap the gate driver circuitry and anodes that overlap the pixel circuits.

2. The organic light-emitting diode display defined in claim 1 further comprising a shared cathode layer that overlaps all of the anodes.

3. The organic light-emitting diode display defined in claim 2 further comprising emissive material between the shared cathode layer and each anode.

4. The organic light-emitting diode display defined in claim 3 wherein the pixel circuits have a pixel-circuit-to-pixel-circuit spacing and wherein the anodes have an anode-to-anode spacing that is larger than the pixel-circuit-to-pixel-circuit spacing.

5. The organic light-emitting diode display defined in claim 4 further comprising horizontal lines that couple some of the pixel circuits to the anodes that overlap the gate driver circuitry.

6. The organic light-emitting diode display defined in claim 5 further comprising a first metal layer, a third metal layer, and a second metal layer between the first and third metal layers, wherein the horizontal lines are formed from the third metal layer.

7. The organic light-emitting diode display defined in claim 5 wherein the gate driver circuitry includes shift register circuits.

8. The organic light-emitting diode display defined in claim 7 further

comprising an organic planarization layer interposed between the gate driver circuitry the anodes that overlap the gate driver circuitry.

9. The organic light-emitting diode display defined in claim 1 wherein the pixel circuits and gate driver circuitry include thin-film transistors formed from a semiconductor layer selected from the group consisting of: a silicon layer and semiconducting oxide layer.

10. The organic light-emitting diode display defined in claim 9 wherein the thin-film transistors include gates that overlap the semiconductor layer.

11. The organic light-emitting diode display defined in claim 9 further comprising a first metal layer that forms the gates, a second metal layer that forms source-drain electrodes for the thin-film transistors, a fourth metal layer that forms lateral signal paths between the pixel circuits and the anodes that overlap the gate driver circuitry, and a third metal layer between the second metal layer and the fourth metal layer.

12. The organic light-emitting diode display defined in claim 1 further comprising horizontal metal lines that couple the pixel circuits to the anodes that overlap the gate driver circuitry.

13. The organic light-emitting diode display defined in claim 12 wherein the gate driver circuitry includes shift register circuitry and buffer circuits.

14. The organic light-emitting diode display defined in claim 13 further comprising data lines and gate lines, wherein each buffer circuit provides a signal to a respective one of the gate lines.

15. An organic light-emitting diode display, comprising:

a rectangular substrate having four edges including left and right edges;

a left-hand gate driver circuit located along the left edge;

a right-hand gate driver circuit located along the right edge; and

an array of display pixels each having a light-emitting diode with an anode and a cathode and each having a pixel circuit that controls current through the light-emitting diode of that display pixel, wherein some of the anodes are located between the left-hand gate driver circuit and the right-hand gate driver circuit overlapping the pixel circuits, wherein some of the anodes overlap the left-hand gate driver circuit, and wherein some of the anodes overlap the right-hand gate driver circuit.

16. The organic light-emitting diode display defined in claim 15 wherein the left-hand gate driver circuit and the right-hand gate driver circuit include shift register circuits and buffers.

17. The organic light-emitting diode display defined in claim 15 wherein the buffers provide control signals to horizontal lines extending across the rectangular substrate between the left to the right edges.

18. The organic light-emitting diode display defined in claim 17 further comprising emissive material on each anode, wherein the cathodes are formed from a shared cathode layer that overlaps the anodes that overlap the left-hand gate driver circuit, the anodes that overlap the right-hand gate driver circuit, and the anodes overlapping the pixel circuits between the left-hand gate driver circuit and the right-hand gate driver circuit.

19. An organic light-emitting diode display, comprising:

gate driver circuitry formed from a chain of shift register circuits; and

an array of display pixels to display images, wherein each display pixel includes a light-emitting diode having a cathode, an anode, and emissive material that emits light, wherein each display pixel receives a signal from the gate driver circuitry, and wherein some of the anodes overlap the chain of shift register circuits.

20. The organic light-emitting diode display defined in claim 19 wherein

each of the display pixels has a pixel circuit that controls emission of the light from the light-emitting diode of that display pixel, wherein some of the anodes overlap the pixel circuits, wherein the pixel circuits are located between a first portion of the gate driver circuitry on a first edge of the display and a second portion of the gate driver circuitry on an opposing second edge of the display, and wherein the pixel circuit of each display pixel includes a thin-film drive transistor having a source-drain terminal coupled to the anode of the light-emitting diode for that display pixel.

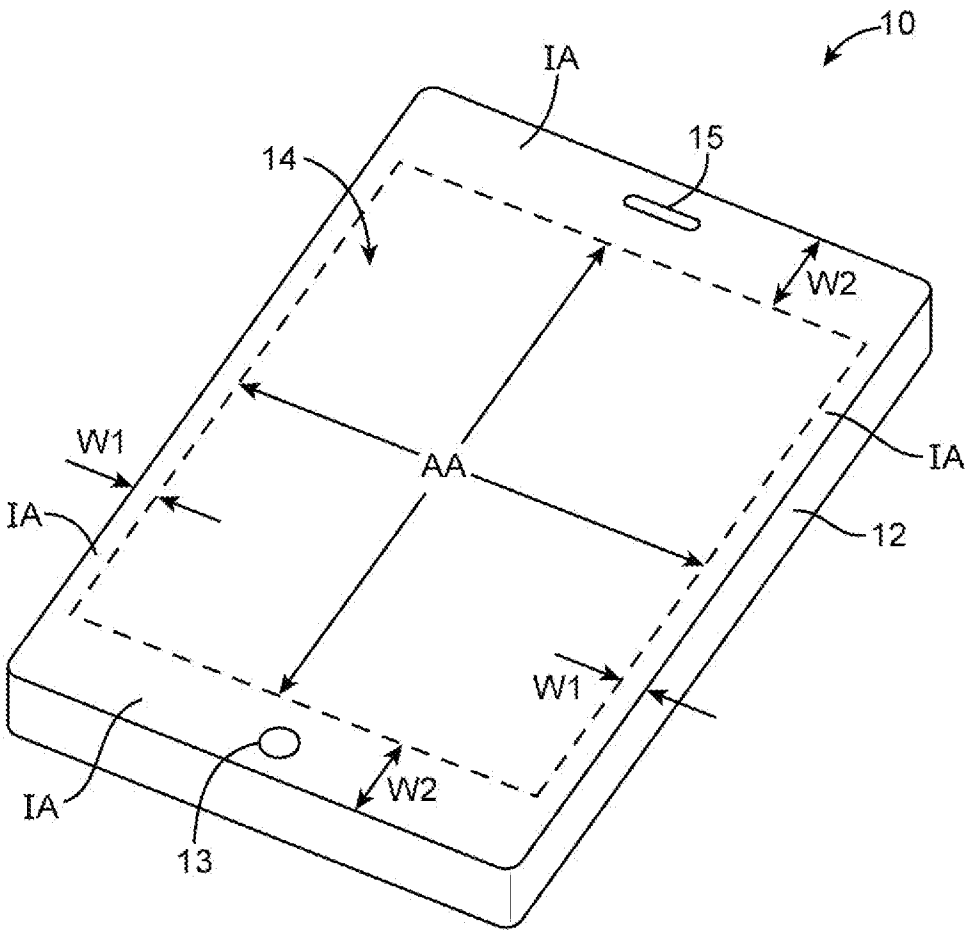

FIG. 1

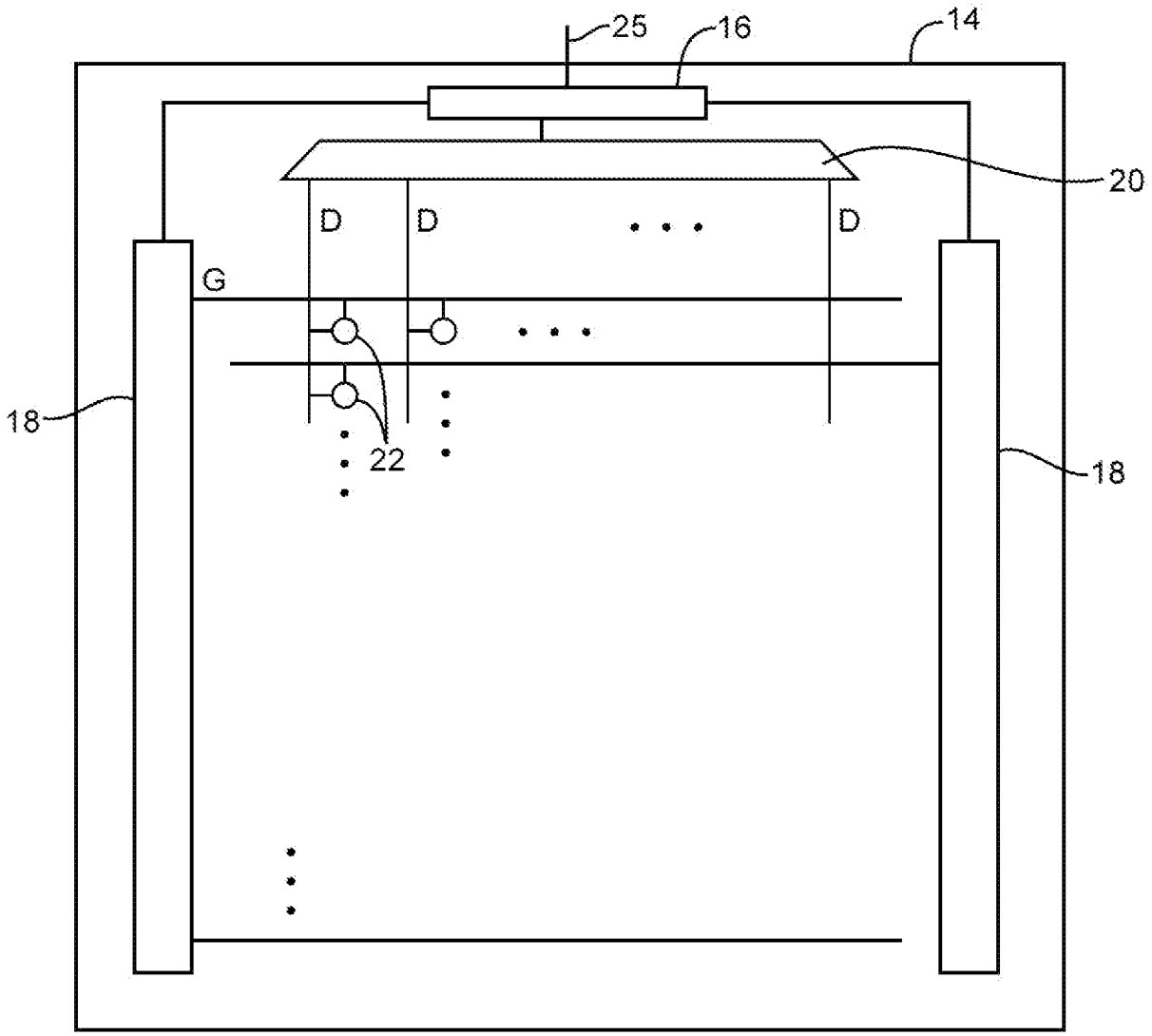

FIG. 2

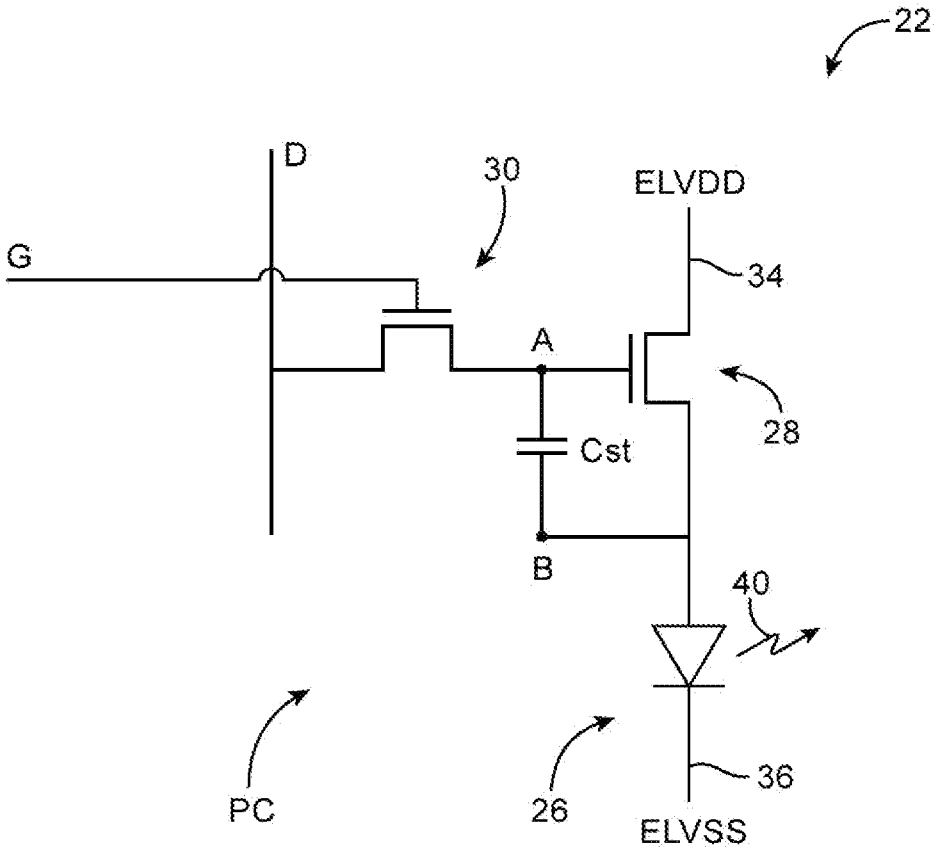

FIG. 3

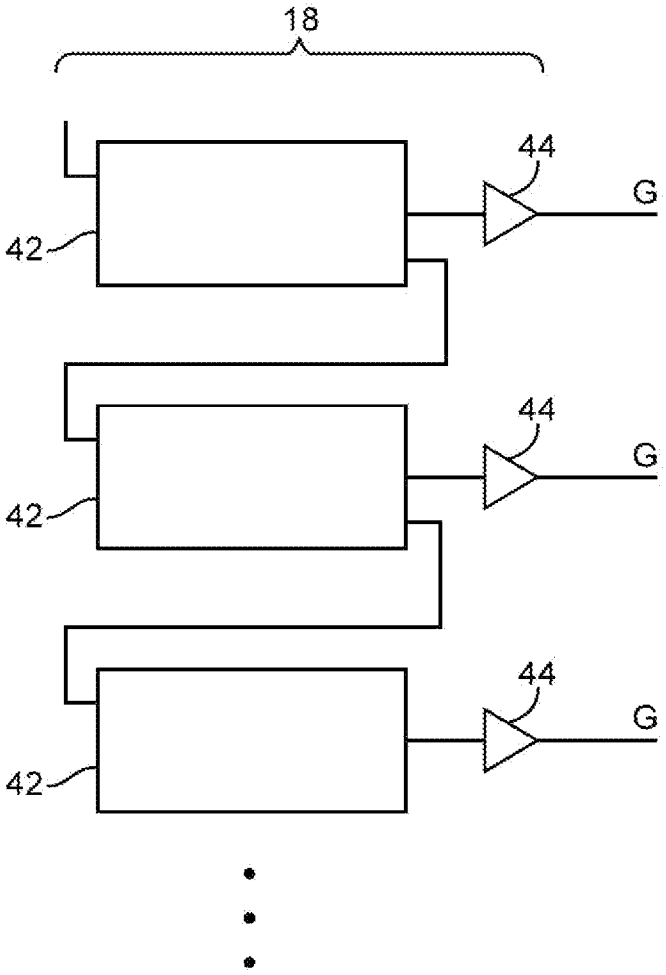

FIG. 4

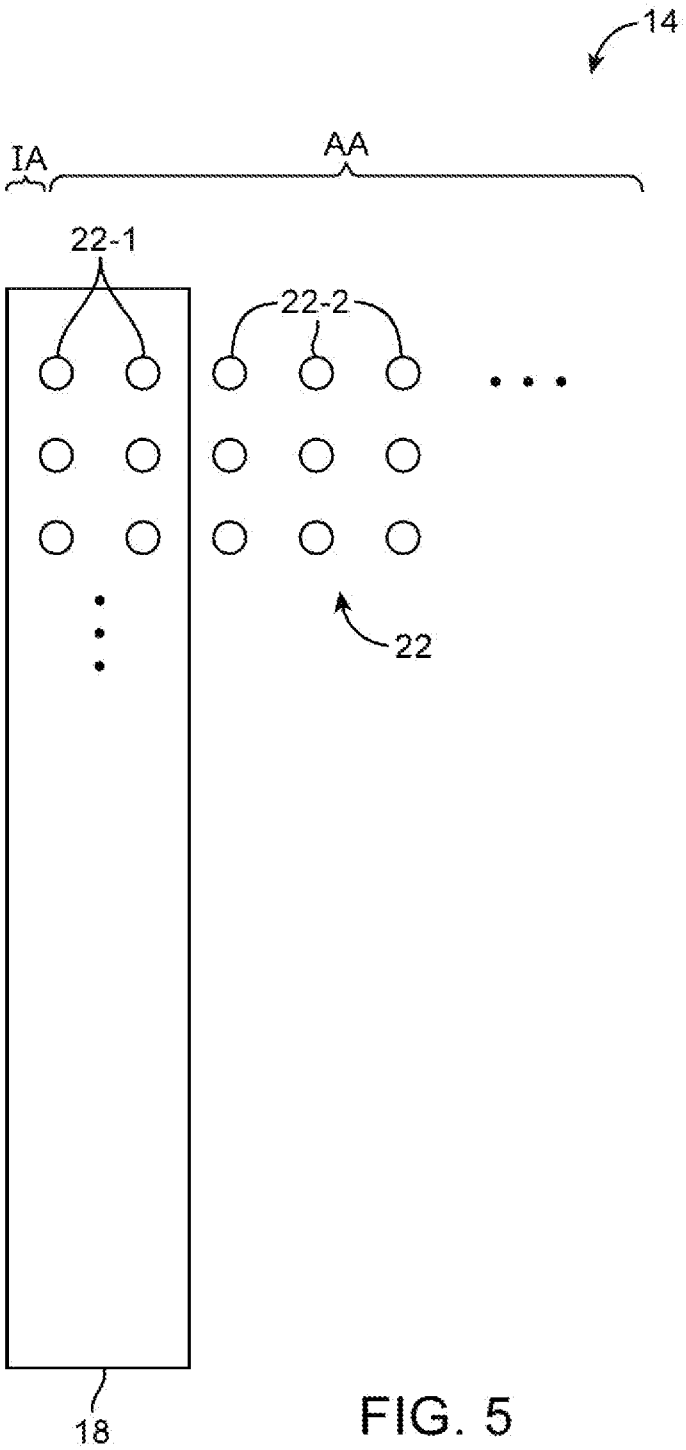

FIG. 5

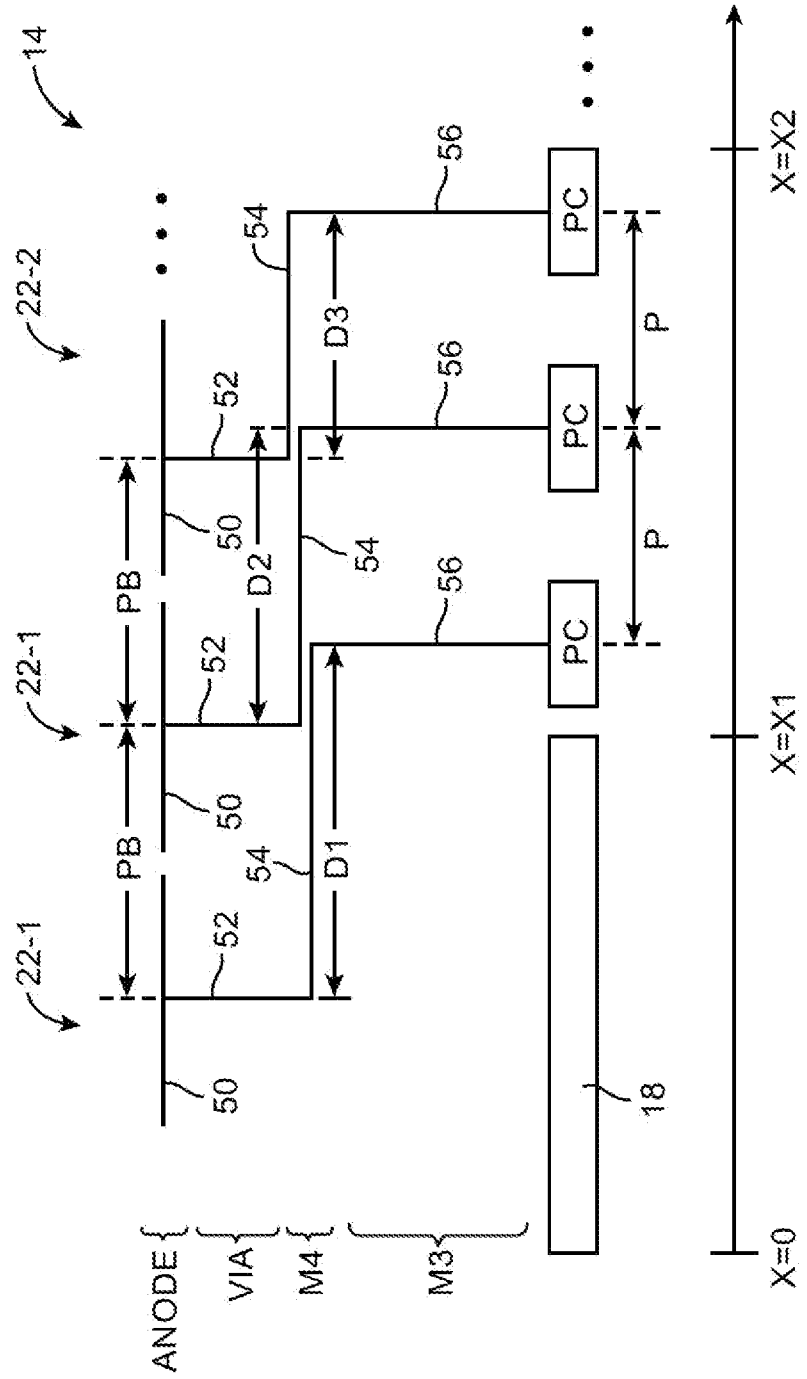
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FIG. 6

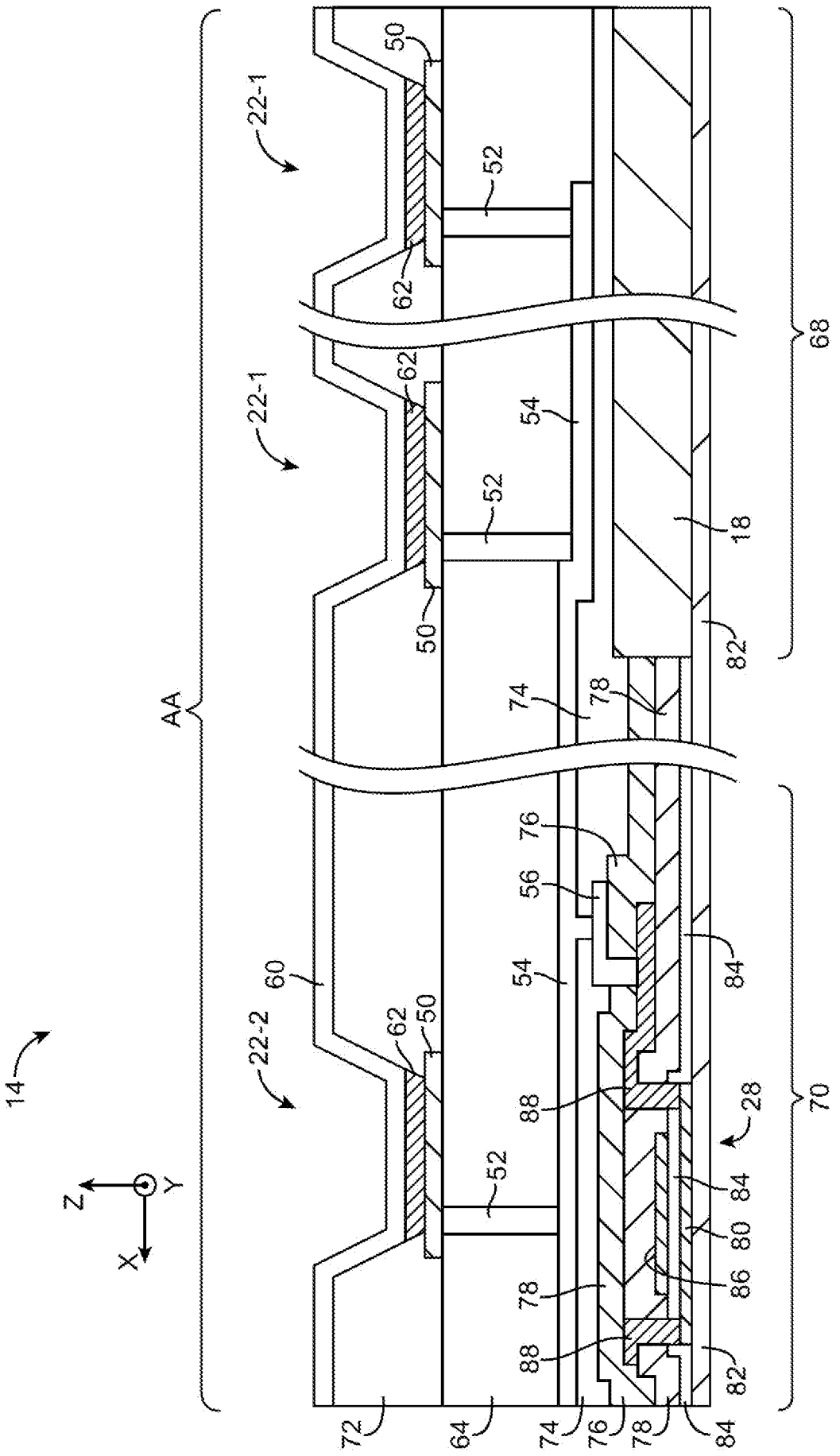
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FIG. 7

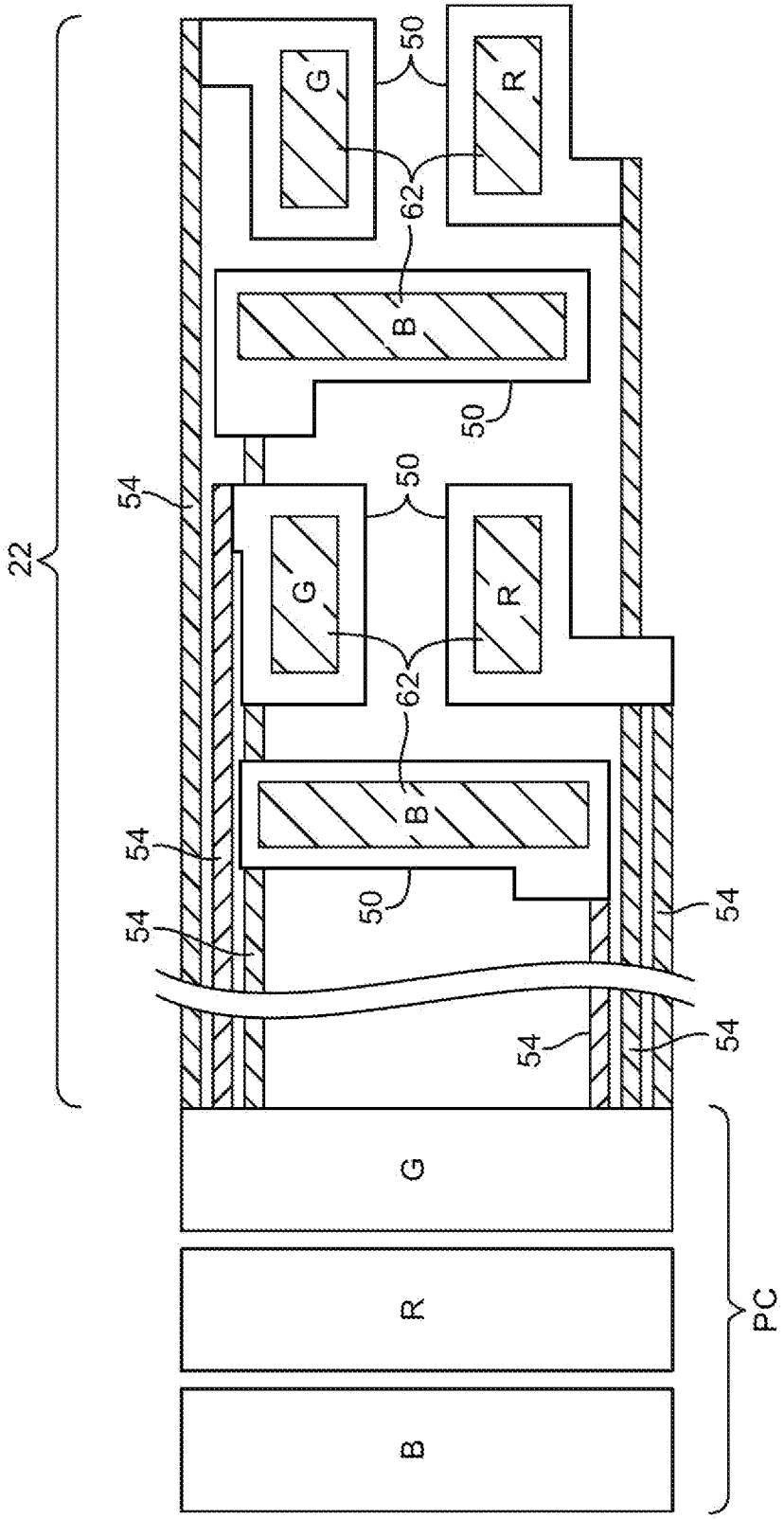

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/027375

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2011/248968 A1 (SUH MI-SOOK [KR]) 13 October 2011 (2011-10-13) paragraph [0062] - paragraph [0086]; figures 3-5 paragraphs [0031], [0059], [0075], [0080] -----	1-12 13-18
X Y	US 2012/146886 A1 (MINAMI TETSUO [JP] ET AL) 14 June 2012 (2012-06-14) paragraphs [0074], [0076], [0077], [0148], [0158]; figures 1,2B,6,10 paragraph [0086] - paragraph [0098]; figure 9 ----- -/--	1-3,9, 12-14 1,13-18

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 July 2015	09/10/2015

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Pusch, Catharina

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2015/027375

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2013/334543 A1 (KIM YOUNG GU [KR] ET AL) 19 December 2013 (2013-12-19) paragraphs [0005], [0022], [0043], [0044], [0052], [0096], [0097], [0119]; figure 1	1,15
Y	US 2003/030381 A1 (YAMAZAKI SHUNPEI [JP] ET AL) 13 February 2003 (2003-02-13) paragraph [0106] - paragraph [0109]; figure 4	1,15-18

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/027375

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-18

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-18

   organic light emitting diode display comprising gate driver circuit and a substrate

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2. claims: 19, 20

   organic light emitting diode display comprising gate driver circuit formed from a chain of shift register circuits

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2015/027375

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		US 2013334543 A1	19-12-2013
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		CN 101666951 A	10-03-2010
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