United States Patent

Berger

[15] **3,660,685**

[45] **May 2, 1972**

[54] PULSE GENERATING TRANSFORMER CIRCUIT

[72] Inventor: **James K. Berger,** Sherman Oaks, Calif.

[73] Assignee: **Pioneer Magnetics, Inc.,** Santa Monica, Calif.

[22] Filed: **Feb. 25, 1971**

[21] Appl. No.: **118,704**

[52] **U.S. Cl.** **307/260,** 307/254

[51] **Int. Cl.** **H03k 5/00**

[58] **Field of Search** 307/260, 261, 254; 328/113; 331/117, 95

[56] **References Cited**

UNITED STATES PATENTS

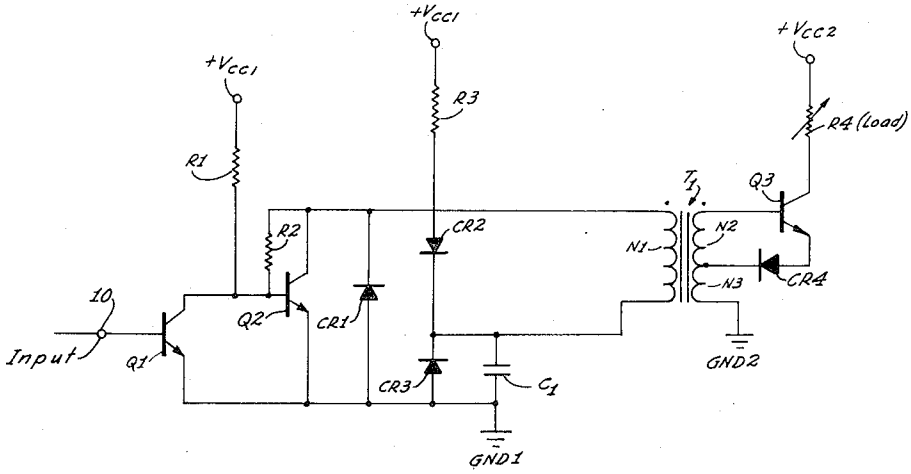
3,291,110 12/1966 Peters ..... 307/260 X

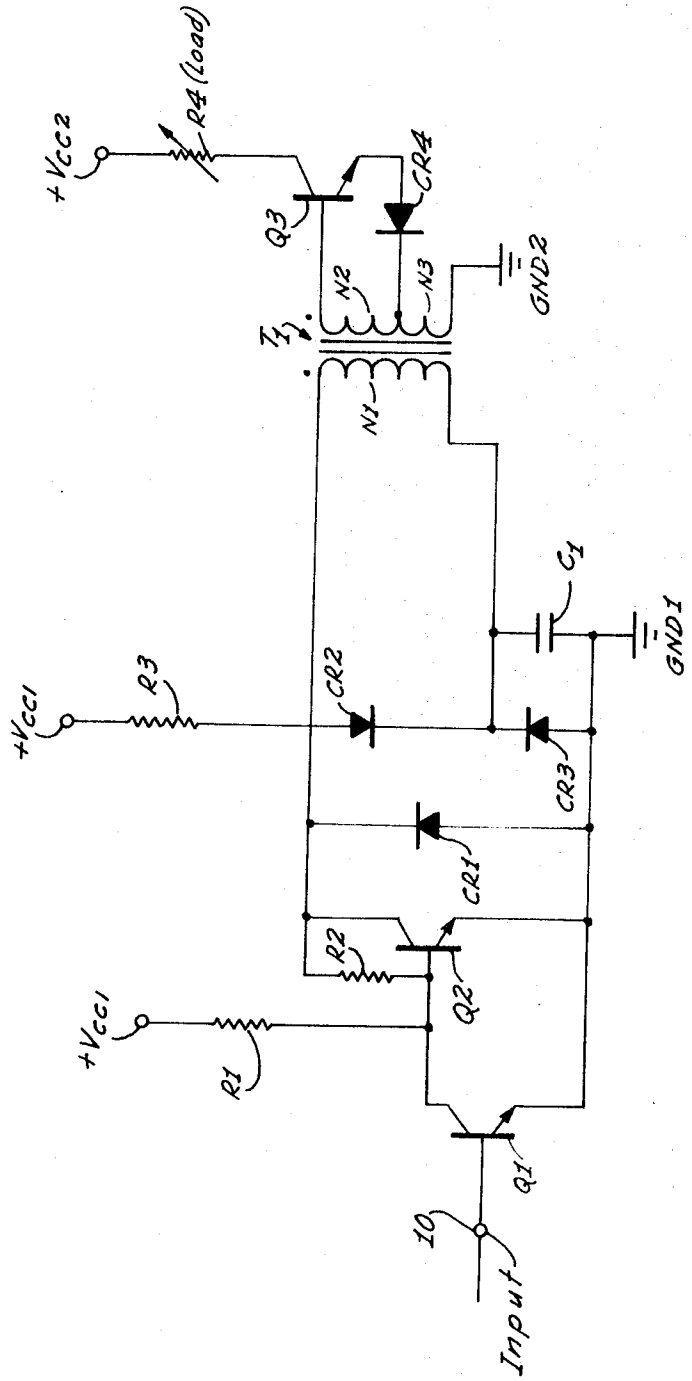
Primary Examiner—Donald D. Forrer
Assistant Examiner—B. P. Davis
Attorney—Jessup & Beecher

[57] **ABSTRACT**

A pulse generating transformer circuit is provided for producing a series of uni-polar pulses of variable amplitude and duration, and in which the transformer is reset between successive pulses within a time independent of the product of the amplitude and duration of the individual pulses produced by the circuit. In this way, there is no limitation of the rapidity with which the successive pulses produced by the circuit may follow one another. The circuit of the invention achieves its desired purpose by connecting a winding of the transformer in parallel with a capacitor to form a resonant circuit which is effective for one half-cycle.

6 Claims, 1 Drawing Figure





INVENTOR:
James K. Berger
Kemp and Beecher
By Keith D. Beecher
ATTORNEYS

PULSE GENERATING TRANSFORMER CIRCUIT

BACKGROUND OF THE INVENTION

Copending application Ser. No. 58,042, which was filed July 24, 1970, in the name of the present inventor, is concerned with an improved power supply which is intended to replace the usual relatively heavy, costly and inefficient power supply of the prior art. The power supply described in the copending application is a fly-back regulated type, in which electric energy from an appropriate source is alternately stored in a transformer, and then released into the load.

The circuit of the present invention may be incorporated into the power supply of the copending application, and it has general utility in the design of electronic equipment in which it is desired to use a transformer to provide a train of uni-polar pulses individually having variable amplitude and duration. In the usual prior art transformer pulse generating circuit, a time proportional to the volt-second area of each pulse generated thereby is required to reset the transformer. Since it is essential for the transformer to be fully recovered between each successive pulse generated by the circuit, a limitation is established in the prior art circuit on the repetition frequency of the pulses generated thereby. In the case of large-area pulses, for example, the transformer reset or recovery time may be unacceptably long.

The circuit of the present invention overcomes the aforesaid difficulty by providing a transformer reset time which is essentially independent of the area of the individual pulses. An advantage of the circuit of the invention is that it accomplishes the desired result without the need for a transistor capable of withstanding the high reset voltage required to make the reset time relatively short.

BRIEF DESCRIPTION OF THE DRAWING

The single FIGURE is a circuit diagram of a transformer pulse generating circuit incorporating the concepts and principles of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

The circuit shown in the accompanying figure includes an input terminal **10** which is connected to the base of an NPN transistor Q1 which may be of the type designated 2N5172. The emitter of the transistor Q1 is connected to a first ground point GND1 associated with a source of unidirectional potential V_{cc1}, which may be of the order of 15 volts, the negative terminal of that source being connected to the ground point GND1. The collector of the transistor Q1 is connected to the base of a transistor Q2 and to a pair of resistors R1 and R2. The resistor R1 is connected to the positive terminal of the source $+V_{cc1}$, and has a value, for example, of 1.5 kilo-ohms. The resistor R2 is a damping resistor. It is interconnected between the base and collector of the transistor Q2, and it has a value, for example, of 4.7 kilo-ohms. The transistor Q2 is an NPN transistor, and may be of the type designated 2N4400. The emitter of the transistor Q2 is connected to the GND1 point, and its collector is connected to one side of the primary winding N1 of a transformer T1. A diode CR1 is connected across the collector and emitter of the transistor Q2. The diode CR1 may be of the type designated 1N4148.

The other side of the primary winding N1 of the transformer T1 is connected to a pair of diodes CR2 and CR3, and to a capacitor C1. The diode CR3 and the capacitor C1 are both connected to the ground point GND1. The diode CR2 is connected through a resistor R3 to the positive terminal of the source V_{cc1}. The resistor R3 may have a resistance of 2.2 kilo-ohms, and the diodes CR2 and CR3 may both be of the type designated 1N4148. The capacitor C1 may have a capacity of 0.0047 microfarads.

The secondary N2 of the transformer T1 has one side connected to a ground point GND2, and a source of unidirectional potential V_{cc2} has its negative terminal connected to that ground point. The other side of the secondary winding N2 is connected to the base of a transistor Q3. The transistor Q3 is a power transistor, and it may be of the type designated DTS411. The transistor Q3 has its collector connected through a variable load designated R4 to the positive terminal of the source $+V_{cc2}$. The emitter of the transistor Q3 is connected back through a diode CR4 to a tap on the secondary winding N2 to establish a third winding N3. The diode CR4 may be of the type designated 1N4721.

In the circuit of the single figure, the transformer T1 provides pulses which drive the power transistor Q3 which, in turn, controls the load R4. The amplitude of the pulses generated by the transformer T1 may vary because the base-emitter voltage of Q3, and the forward conduction voltage of the diode CR4 vary with load current and temperature. The pulse width is variable, and it is controlled by the input applied to the terminal **10**, and which is introduced to the base of the transistor Q1. The illustrated circuit has the property of resetting the transformer T1 after each pulse in a time which is essentially constant, and independent of the width or amplitude of the pulses generated by the transformer T1.

Prior to each output pulse, the input transistor Q1 is rendered non-conductive, and the transistor Q2 is conductive due to the current flow through the resistor R1. A small current flows from the positive terminal V_{cc1} through the resistor R3, through the diode CR2, through the primary winding N1 of the transformer T1, and through the conductive transistor Q2 to the ground point GND1. At this time, there is no voltage across the secondary winding N2, so that the output transistor Q3 is non-conductive.

To initiate a pulse, the transistor Q1 is rendered conductive by the input signal. Current then flows through the resistor R1 to ground through the conductive transistor Q1 instead of flowing into the base of the transistor Q2, so that the transistor Q2 becomes non-conductive. The current which was flowing in the primary winding N1 must continue, due to the inductance of that winding. This current now flows through the damping resistor R2 and through the transistor Q1 to the ground point GND1. The value of R2 is selected so that the voltage across the primary winding N1 necessary to cause the aforesaid current in the resistor R2 is sufficient so that the voltage across the secondary N2, related by the ratio N2/N1, is great enough to cause the transistor Q3 to become conductive. When the transistor Q3 becomes conductive, load current flows from the positive terminal V_{cc2} through the load resistance R4, and through the conductive transistor Q3 and diode CR4, and through the winding N3 to the ground point GND2. This current in the winding N3 produces a current in the winding N2 these currents are mutually related by approximately the ratio N3/N2.

The foregoing regenerative action provides the transistor Q3 with a base current proportional to its emitter current, and the transistor Q3 remains conductive for the duration of the pulse. When the pulse is to be terminated, the input signal applied to the base of the transistor Q1 causes that transistor to become non-conductive. Current through the resistors R1 and R2 then flow into the base of the transistor Q2, causing the transistor Q2 to become conductive. Current then flows in the loop formed by the diode CR3, the primary winding N1, and the transistor Q2 back to the diode CR3. The drive to the transistor Q2 is sufficient so that this current exceeds the emitter current of the transistor Q3 multiplied by the ratio N3/N1, so that the current in the winding N2 and in the base of the transistor Q3 must reverse. This provides a turn-off drive to Q3, and Q3 becomes non-conductive. The conduction of the transistor Q2 now rises to a saturation point, and at that instant, the voltage across the winding N1 is nearly zero. The reset of the transformer now begins.

Since the transistor Q2 is saturated and effectively connects the winding N1 in parallel with the capacitor C, a resonant circuit is formed consisting of the capacitor C1 and the primary inductance L_p of the transformer T1. At that time, the capacitor C1 is essentially discharged and stores negligible energy.

The transformer T1 has energy proportional to the pulse area stored in the primary inductance L_p. Due to this stored energy, the circuit will oscillate at a frequency determined by

$$f=\frac{1}{2\pi\sqrt{L_pC1}}$$

or $f = 1/(2\pi\sqrt{L_pC1})$. The initial polarity of the oscillation will be such that the cathode of the diode CR3 goes positive with respect to the ground point GND1 to reverse bias the diode, so that the diode CR3 has no effect. Also, the transistor Q3 and the diode CR4 are reverse biased and have no effect. Current through the resistor R3 and the diode CR2 aids the oscillation until the voltage on the capacitor C1 equals V_{cc1}, at which time the diode CR2 will become reverse biased and have no further effect. The effect of the resistor R3 is nearly negligible, due to the large value of the resistor R3.

The oscillation will continue for one half-cycle, at the end of which the capacitor C1 will again be discharged, and the energy stored in the transformer T1 will have been transferred to the capacitor C1 and then taken back to the transformer T1, but of opposite polarity. At that time, the residual current in the winding N1 will be of nearly the same amplitude as it was at the end of the pulse, but of opposite polarity. The transformer now is reset, and is ready for a new pulse.

It will be appreciated that the voltage across the capacitor C1 during the reset time was a half sine wave, whose area is proportional to the pulse area, but whose frequency is independent of the area. The reset time was $\tau = \frac{1}{2}(2\pi\sqrt{L_pC1})$, or $\tau = \sqrt{L_pC1}$. The amplitude of the half sine wave varies to provide the necessary area, but none of the transistors are exposed to this voltage, so the voltage may be large to make the reset time short.

It will be observed that the energy stored in the transformer T1 at the end of each reset period is always of the correct polarity to initiate a new cycle, but is not always of the same magnitude. This is not of any importance, since the transformer is always reset at least to the condition which prevails for the initial pulse. That is, the current in the primary winding N1 is equal to the current provided by the resistor R3. If the transformer is further reset, it does not have any significance.

It should be pointed out that the resistor R2 is provided to protect the transistor Q2 from voltage spikes due to the leakage reactance in the transformer T1, and which would otherwise occur each time the transistor Q2 is rendered non-conductive. The diode CR1 is provided to prevent the collector of the transistor Q2 from going negative at the start of the reset period, since the reset current at this time may exceed the current capability of the transistor Q2 in the inverted mode. The diode CR2 serves to disconnect the resistor R3 from the resonant circuit during most of the reset period, so as to avoid damping the circuit and diminishing its quality factor "Q." The diode CR4 protects the transistor Q3 from the possibility of excessive reverse base-emitter voltage if the reset amplitude is high, and it provides an additional turn-off bias to enable the transistor Q3 rapidly to achieve its non-conductive state.

It is evident, of course, that the circuit of the invention is not limited to the particular output circuit illustrated in the drawing, but is generally applicable to all transformer circuits which provide unipolar output pulses.

Therefore, although a particular embodiment of the invention has been shown and described, modifications may be made. It is intended in the following claims to cover the modifications which come within the spirit and scope of the invention.

What is claimed is:

1. A pulse producing circuit including: a transformer having a primary winding and a secondary winding; a load circuit connected to said secondary winding; an input circuit connected to said primary winding and including a first switching transistor responsive to an input signal for cyclically connecting said primary winding across a unidirectional potential source for a predetermined time interval for each cycle as determined by said input signals, and including capacitor means and a second switching transistor for connecting said capacitor means into a resonant circuit relationship with said primary winding at the end of each of said predetermined intervals, so as to create an oscillation across said resonant circuit; each of said first and second transistors including base, emitter and collector electrodes; a damping resistor connected between the collector electrode and base electrode of said second transistor; a diode connected across the emitter electrode and collector electrode of said second transistor; and said input circuit further including diode means connected across said capacitor means to limit said oscillation to one-half cycle and thereby reset said transformer.

2. The circuit defined in claim 1 in which the collector electrode of said second transistor is connected to one side of the primary winding of said transformer, and the emitter electrode of said second transistor is connected to a point of reference potential, and in which said capacitor means is connected to the other side of said primary winding and to said point of reference potential.

3. The circuit defined in claim 2 and which includes a resistor and diode means series connected with one another and connecting said capacitor means to one terminal of said unidirectional potential source.

4. The pulse producing circuit defined in claim 1 in which said output circuit includes a power transistor having a base connected to one side of said secondary winding, and having a collector and an emitter, and which includes diode means connecting said emitter to a tap on said secondary winding, the other side of said secondary winding being connected to a point of reference potential.

5. The circuit defined in claim 4 and which includes a load connected to the collector of said transistor and to the positive terminal of a second unidirectional potential source, the negative terminal of said second source being connected to said point of reference potential.

6. The circuit defined in claim 5 and in which the said load is connected between the said point of reference potential and the said secondary winding, and the collector of said power transistor is connected to the positive terminal of said second unidirectional potential source.

* * * * *